- **General-Purpose Signal-Processing Analog Front End (AFE)**
- **Single 5-V Power Supply**
- **Power Dissipation . . . 100 mW Typ**
- **Signal-to-Distortion Ratio . . . 70 dB Typ**
- **Serial-Port Interface**
- **Differential Outputs Drive 3-V Peak into a 600-Ω Differential Load**
- **Differential Architecture Throughout**
- **1-μm Advanced LinEPIC™ Process**
- **14-Bit Dynamic Range ADC and DAC**
- **2s-Complement Data Format**

description

The TLC320V343 analog interface circuit (AIC) is an audio-band processor that provides an analog-to-digital and digital-to-analog input/output interface system on a single monolithic CMOS chip. This device integrates a band-pass switched-capacitor antialiasing input filter, a 14-bit-resolution analog-to-digital converter (ADC), a 14-bit-resolution digital-to-analog converter (DAC), a low-pass switched-capacitor output-reconstruction filter, (sin x)/x compensation, and a serial port for data and control transfers.

The internal circuit configuration and performance parameters are determined by reading control information into the eight available data registers. The register data sets up the device for a given mode of operation and application.

The major functions of the TLC320V343 are:

- To convert audio-signal data to digital format by the ADC channel
- To provide the interface and control logic to transfer data between its serial input and output terminals and a DSP or microprocessor
- To convert received digital data back to an audio signal through the DAC channel

The antialiasing input low-pass filter is a switched-capacitor filter with a sixth-order elliptic characteristic. The high-pass filter is a single-pole filter to preserve low-frequency response as the low-pass filter cutoff is adjusted. There is a 3-pole continuous time filter that precedes this filter to eliminate any aliasing caused by the filter clock signal.

The output-reconstruction switched-capacitor filter is a sixth-order elliptic transitional low-pass filter followed by a second-order (sin x)/x correction filter. This filter is followed by a 3-pole continuous time filter to eliminate images of the filter clock signal.

The AIC consists of two signal processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously; data reception at the DAC channel and data transmission from the ADC channel occur during the same time interval. The data transfer is in 2s-complement format.

Typical applications for this device include modems, speech processing, analog interface for digital-signal processors (DSPs), industrial process control, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders.

The TLC320V343 is characterized for operation from 0°C to 70°C.

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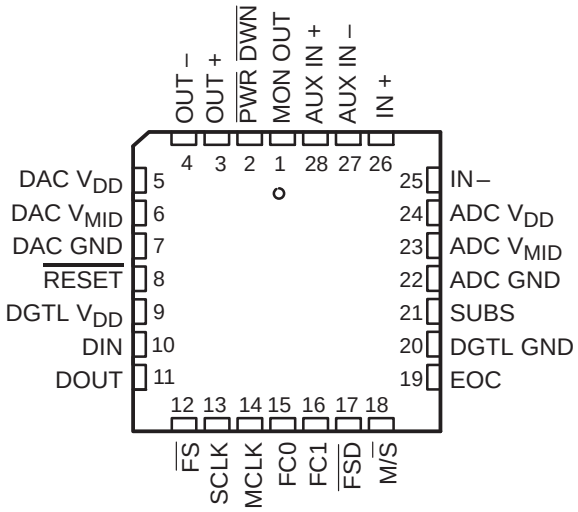
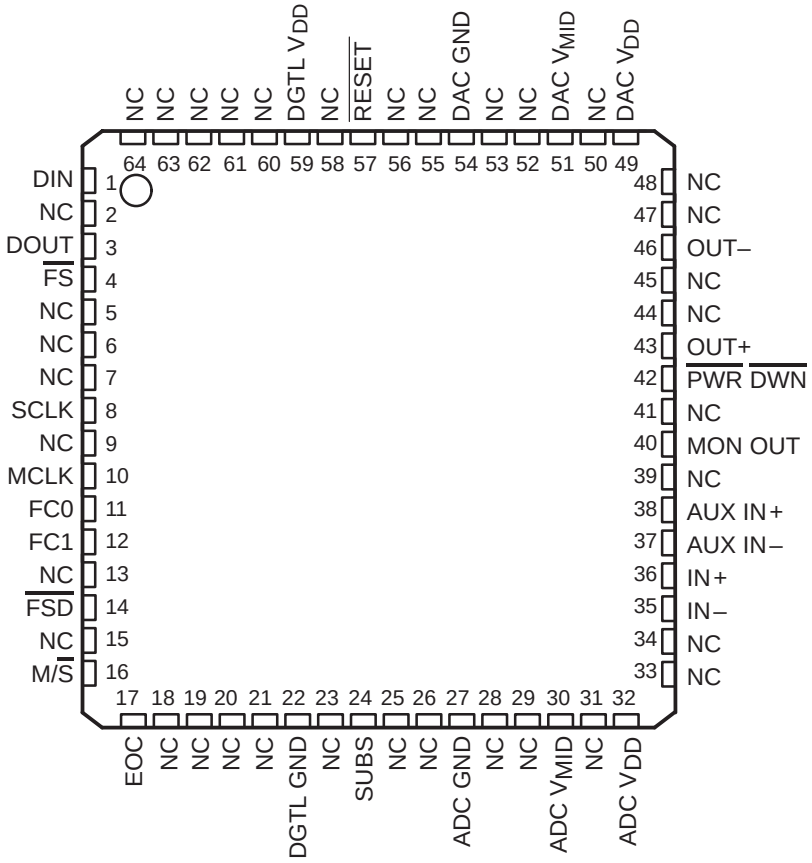
FN PACKAGE
(TOP VIEW)

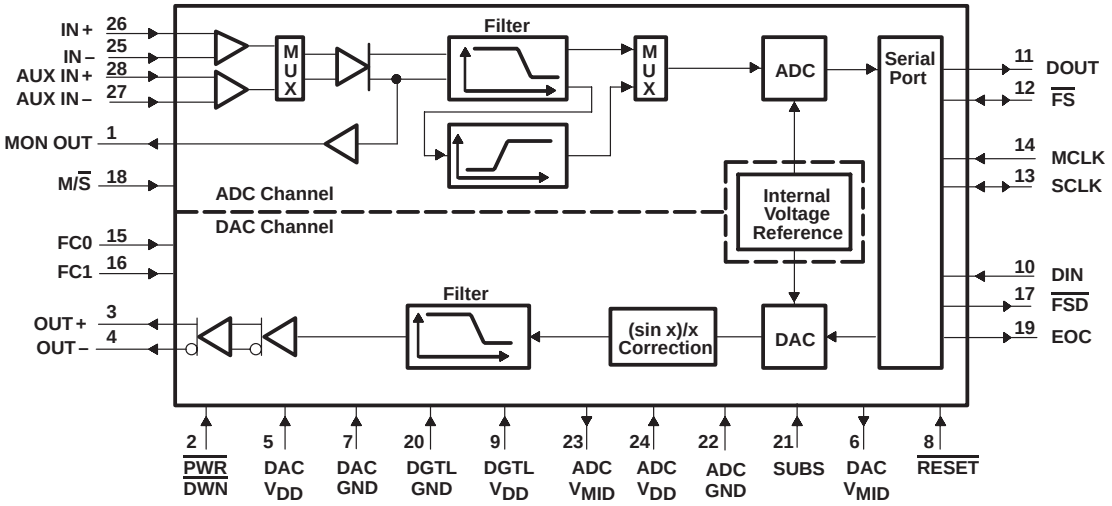


PM PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



NOTE A: Terminal numbers shown are for the FN package.

Terminal Functions

TERMINAL NAME	NO.†	NO.‡	I/O	DESCRIPTION
ADC V_{DD}	24	32	I	Analog supply voltage for the ADC channel
ADC V_{MID}	23	30	O	Midsupply for the ADC channel (requires a bypass capacitor). ADC V_{MID} must be buffered when used as an external reference.
ADC GND	22	27	I	Analog ground for the ADC channel
AUX IN+	28	38	I	Noninverting input to auxiliary analog input amplifier
AUX IN–	27	37	I	Inverting input to auxiliary analog input amplifier
DAC V_{DD}	5	49	I	Digital supply voltage for the DAC channel
DAC V_{MID}	6	51	O	Midsupply for the DAC channel (requires a bypass capacitor). DAC V_{MID} must be buffered when used as an external reference.
DAC GND	7	54	I	Analog ground for the DAC channel
DIN	10	1	I	Data input. DIN receives the DAC input data and command information and is synchronized with SCLK.
DOUT	11	3	O	Data output. DOUT outputs the ADC data results and register read contents. DOUT is synchronized with SCLK.
DGTL V_{DD}	9	59	I	Digital supply voltage for control logic
DGTL GND	20	22	I	Digital ground for control logic
EOC	19	17	O	End-of-conversion output. EOC goes high at the start of the ADC conversion period and low when conversion is complete. EOC remains low until the next ADC conversion period begins and indicates the internal device conversion period.
FC0	15	11	I	Hardware control input. FC0 is used in conjunction with FC1 to request secondary communication and phase adjustments. FC0 must be tied low when it is not used.
FC1	16	12	I	Hardware control input. FC1 is used in conjunction with FC0 to request secondary communication and phase adjustments. FC1 must be tied low when it is not used.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION
$\overline{FS}$	12	4	I/O	Frame synchronization. When $\overline{FS}$ goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, $\overline{FS}$ is low during the simultaneous 16-bit transmission to DIN and from DOUT. In slave mode, $\overline{FS}$ is externally generated and must be low for one shift-clock period minimum to initiate the data transfer.
$\overline{FSD}$	17	14	O	Frame synchronization delayed output. This $\overline{FSD}$ active-low output synchronizes a slave device to the frame synchronization timing of the master device. $\overline{FSD}$ is applied to the slave $\overline{FS}$ input and is the same duration as the master $\overline{FS}$ signal but delayed in time by the number of shift clocks programmed in the $\overline{FSD}$ register.
IN+	26	36	I	Noninverting input to analog input amplifier
IN–	25	35	I	Inverting input to analog input amplifier
MCLK	14	10	I	The master clock input drives all of the key logic signals of the AIC.
MON OUT	1	40	O	The monitor output allows monitoring of analog input and is a high-impedance output.
M/$\overline{S}$	18	16	I	Master/slave select input. When M/$\overline{S}$ is high, the device is the master and when low, it is a slave.
OUT+	3	43	O	Noninverting output of analog output power amplifier. OUT+ can drive transformer hybrids or high-impedance loads directly in a differential connection or a single-ended configuration with a buffered V_{MID}.
OUT–	4	46	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
$\overline{PWR}$ $\overline{DWN}$	2	42	I	Power-down input. When $\overline{PWR}$ $\overline{DWN}$ is taken low, the device is powered down so that the existing internally programmed state is maintained. When $\overline{PWR}$ $\overline{DWN}$ is brought high, full operation resumes.
$\overline{RESET}$	8	57	I	Reset input that initializes the internal counters and control registers. $\overline{RESET}$ initiates the serial data communications, initializes all of the registers to their default values, and puts the device in a preprogrammed state. After a low-going pulse on $\overline{RESET}$, the device registers are initialized to provide a 16-kHz data conversion rate and 7.2-kHz filter bandwidth for a 10.368-MHz master clock input signal.
SCLK	13	8	I/O	Shift clock. SCLK clocks the digital data into DIN and out of DOUT during the frame synchronization interval. When configured as an output (M/$\overline{S}$ high), SCLK is generated internally by dividing the master clock signal frequency by four. When configured as an input (M/$\overline{S}$ low), SCLK is generated externally and synchronously to the master clock. This signal clocks the serial data into and out of the device.
SUBS	21	24	I	Substrate connection. SUBS should be tied to ADC GND.

† Terminal numbers shown are for the FN package.
‡ Terminal numbers shown are for the PM package.

detailed description

definitions and terminology

ADC channel	All signal processing circuits between the analog input and the digital conversion results at DOUT
d	Valid programmed or default data in the control register format (see secondary serial communications definition) when discussing other data-bit portions of the register
Dxx	Bit position in the primary data word (xx is the bit number)
DAC channel	All signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUT+ and OUT–
Data transfer interval	The time during which data is transferred from DOUT and to DIN. This interval is 16 shift clocks regardless of whether the shift clock is internally or externally generated. The data transfer is initiated by the falling edge of the frame-sync signal.
DSxx	Bit position in the secondary data word (xx is the bit number)
f_i	The analog input frequency of interest
Frame sync	The falling edge of the signal that initiates the data-transfer interval. The primary frame sync starts the primary communications, and the secondary frame sync starts the secondary communications.
Frame sync and sampling period	The time between falling edges of successive primary frame-sync signals
Frame-sync interval	The time period occupied by 16 shift clocks. Regardless of the mode of operation, there is always an internal frame-sync interval signal that goes low on the rising edge of SCLK and remains low for 16 shift clocks. It is used for synchronization of the serial-port internal signals. It goes high on the seventeenth rising edge of SCLK.
f_s	The sampling frequency that is the reciprocal of the sampling period
Host	Any processing system that interfaces to DIN, DOUT, SCLK, or $\overline{FS}$
Primary (serial) communications	The digital data-transfer interval. Since the device is synchronous, the signal data words from the ADC channel and to the DAC channel occur simultaneously.
Secondary (serial) communications	The digital control and configuration data-transfer interval into DIN, and the register read-data cycle out DOUT. The data-transfer interval occurs when requested by hardware or software.
Signal data	The input signal and all of the converted representations through the ADC channel which returns through the DAC channel to the analog output. This is contrasted with the purely digital software control data.

ADC signal channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. The signal is amplified by the input amplifier at one of three software-selectable gains (typically 0 dB, 6 dB, or 12 dB). A squelch mode can also be programmed for the input amplifier.

The amplifier output is filtered and applied to the ADC input. The ADC converts the signal into discrete digital words in 2s-complement format corresponding to the analog-signal value at the sampling time. These 16-bit digital words, representing sampled values of the analog input signal, are clocked out of the serial port, (DOUT), one word for each primary communication interval. During secondary communications, the data previously programmed into the registers can be read out with the appropriate register address and with the read bit set to 1. When no register read is requested, all 16 bits are 0.

DAC signal channel

DIN receives the 16-bit serial data word (2s-complement) from the host during the primary communications interval and latches the data on the seventeenth rising edge of SCLK. The data are converted to an analog voltage by the DAC with a sample-and-hold circuit and then sent through a (sin x)/x correction circuit and a smoothing filter. An output buffer with three software-programmable gains (0 dB, –6 dB, and –12 dB), as shown in register four, drives the differential outputs OUT+ and OUT–. A squelch mode can also be programmed for the output buffer. During secondary communications, the configuration program data are read into the device control registers.

serial interface

The digital serial interface consists of the shift clock, the frame-synchronization signal, the ADC-channel data output, and the DAC-channel data input. During the primary 16-bit frame-synchronization interval, the SCLK transfers the ADC channel results from DOUT and transfers 16-bit DAC data into DIN.

During the secondary frame-synchronization interval, the SCLK transfers the register read data from DOUT when the read bit is set to a 1. In addition, the SCLK transfers control and device parameter information into DIN. The functional sequence is shown in Figure 1.

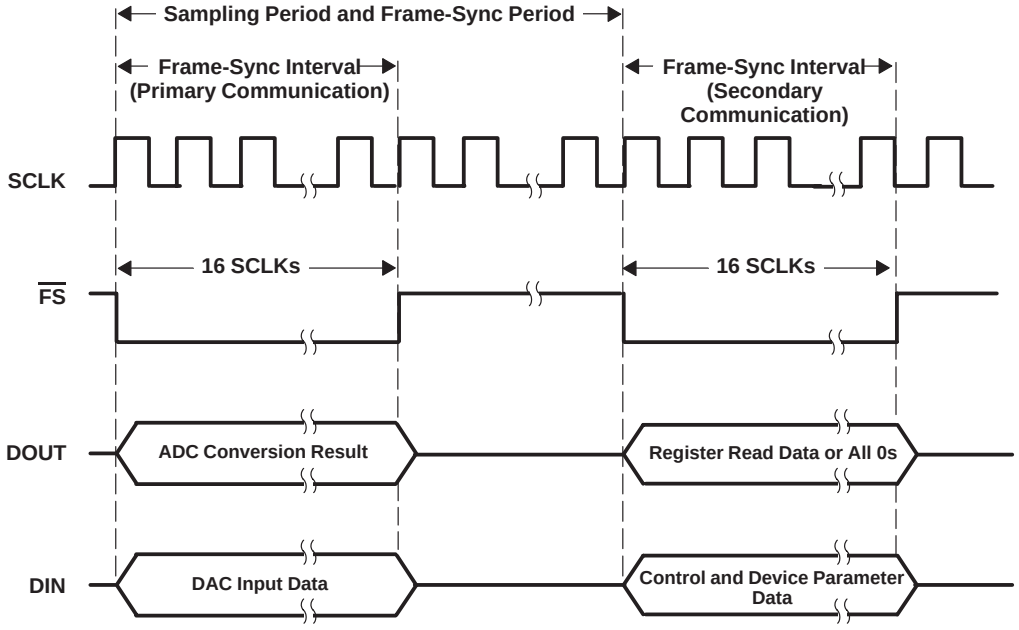


Figure 1. Functional Sequence for Primary and Secondary Communication

required minimum number of MCLK periods

The number of MCLKs necessary for proper operation when only the primary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 4 MCLKs per SCLK
= 72 MCLKs minimum

The number of MCLKs necessary for proper operation when the primary and secondary communications are used is:

Total number of MCLKs = (16 + 2) SCLKs × 2 × 4 MCLKs per SCLK
= 144 MCLKs minimum

Even though the TLC320V343 can perform with this number of MCLKs, the host may need more time to execute the required software instructions between primary and secondary communication intervals.

terminal functions

frame-sync function

The frame-sync signal indicates that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal.

frame sync ($\overline{FS}$)

The frame sync is generated internally. $\overline{FS}$ goes low on the rising edge of SCLK and remains low for the 16-bit data transfer. In addition to generating its own frame-sync interval, the master also outputs a frame sync for each slave that is being used.

midpoint voltages (ADC V_{MID} and DAC V_{MID})

Since the device operates at a single supply voltage, two midpoint voltages are generated for internal signal processing. ADC V_{MID} is used for the ADC channel reference, and DAC V_{MID} is used for the DAC channel reference. The two references minimize channel-to-channel noise and crosstalk. ADC V_{MID} and DAC V_{MID} must be buffered when used as a reference for external signal processing.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, DGTL V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Supply voltage range, DAC V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Supply voltage range, ADC V_{DD} (see Notes 1 and 2)	–0.3 V to 6.5 V
Differential supply voltage range, DGTL V_{DD} to DAC V_{DD}	–0.3 V to 6.5 V
Differential supply voltage range, all positive supply voltages to ADC GND, DAC GND, DGTL GND, SUBS	–0.3 V to 6.5 V
Output voltage range, DOUT	–0.3 V to DGTL V_{DD} + 0.3 V
Input voltage range, DIN	–0.3 V to DGTL V_{DD} + 0.3 V
Ground voltage range, ADC GND, DAC GND, DGTL GND, SUBS	–0.3 V to DGTL V_{DD} + 0.3 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–40°C to 25°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. Voltage values for DGTL V_{DD} are with respect to DGTL GND, voltage values for DAC V_{DD} are with respect to DAC GND, and voltage values for ADC V_{DD} are with respect to ADC GND. For the subsequent electrical, operating, and timing specifications, the symbol V_{DD} denotes all positive supplies. DAC GND, ADC GND, DGTL GND, and SUBS are at 0 V unless otherwise specified.
2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below must be followed when applying power:
   (1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
   (2) Connect voltages ADC V_{DD} and DAC V_{DD}.
   (3) Connect voltage DGTL V_{DD}.
   (4) Connect the input signals.

   The sequence below must be followed when removing power.
   (1) Disconnect the input signals.
   (2) Disconnect voltage DGTL V_{DD}.
   (3) Disconnect voltages ADC V_{DD} and DAC V_{DD}.
   (4) Disconnect SUBS, DGTL GND, ADC GND, and DAC GND from ground.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{DD}	4.5	5	5.5	V
Steady-state differential voltage between any two supplies			0.1	V
High-level digital input voltage, V_{IH}	2.2			V
Low-level digital input voltage, V_{IL}			0.8	V
Load current from ADC V_{MID} and DAC, I_O			100	µA
Conversion time for the ADC and DAC channels		10 FCLK periods		
Master clock frequency, f_{MCLK}		10.368	15	MHz
Analog input voltage (differential, peak to peak), $V_{ID(PP)}$		6		V
Differential output load resistance, R_L	600			Ω
Single ended to buffered DAC V_{MID} voltage load resistance, R_L	300			Ω
Operating free-air temperature, T_A	0		70	°C

NOTE: 2. To avoid possible damage to these CMOS devices and associated operating parameters, the sequence below must be followed when applying power:
(1) Connect SUBS, DGTL GND, ADC GND, and DAC GND to ground.
(2) Connect voltages ADC V_{DD} and DAC V_{DD}.
(3) Connect voltage DGTL V_{DD}.
(4) Connect the input signals.
The sequence below must be followed when removing power.
(1) Disconnect the input signals.
(2) Disconnect voltage DGTL V_{DD}.
(3) Disconnect voltages ADC V_{DD} and DAC V_{DD}.
(4) Disconnect SUBS, DGTL GND, ADC GND, and DAC GND from ground.

electrical characteristics over recommended range of operating free-air temperature, MCLK = 5.184 MHz, V_{DD} = 5 V, outputs unloaded, for total device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{DD}	Supply current	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		20	22	mA
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 µs and clock signals present		1	2	mA
P_D	Power dissipation	$\overline{PWR}$ $\overline{DWN}$ = 1 and clock signals present		100		mW
		$\overline{PWR}$ $\overline{DWN}$ = 0 after 500 µs and clock signals present		5		mW
		Software power down, (bit D00, register 6 set to 1)		15	20	mW
ADC V_{MID}		No load	ADC $V_{DD}/2$ −0.1		ADC $V_{DD}/2$ +0.1	V
DAC V_{MID}		No load	DAC $V_{DD}/2$ −0.1		DAC $V_{DD}/2$ +0.1	V

† All typical values are at V_{DD} = 5 V and T_A = 25°C.

electrical characteristics over recommended range of operating free-air temperature, V_{DD} = 5 V, digital I/O terminals (DIN, DOUT, EOC, FC0, FC1, $\overline{FS}$, $\overline{FSD}$, MCLK, M/$\overline{S}$, SCLK)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1.6 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to DGTL V_{DD}			10	µA
I_{IL}	Low-level input current, any digital input	V_I = 0 V to 0.8 V			10	µA
C_i	Input capacitance			5		pF
C_o	Output capacitance			5		pF

electrical characteristics over recommended range of operating free-air temperature, V_{DD} = 5 V, ADC and DAC channels

ADC channel filter transfer function, FCLK = 144 kHz, f_s = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 3)	f_i = 50 Hz		–2	dB
	f_i = 200 Hz	–1.8	–0.2	
	f_i = 300 Hz to 3 kHz	–0.2	0.2	
	f_i = 3.3 kHz	–0.35	0.03	
	f_i = 3.4 kHz	–1	–0.1	
	f_i = 4 kHz		–14	
	$f_i \geq$ 4.6 kHz		–32	

NOTE 3: The differential analog input signals are sine waves at 6 V peak-to-peak. The reference gain is at 1020 Hz.

ADC channel input, V_{DD} = 5 V, input amplifier gain = 0 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage (see Note 4)	Single ended		3		V
		Differential		6		V
	ADC converter offset error	Band-pass filter selected		10	30	mV
CMRR	Common-mode rejection ratio at IN+, IN–, AUX IN+, AUX IN– (see Note 5)			55		dB
r_i	Input resistance at IN+, IN–, AUX IN+, AUX IN–			100		kΩ
	Squelch	DS03, DS02 = 0 in register 4		60		dB

NOTES: 4. The differential range corresponds to the full-scale digital output.
5. Common-mode rejection ratio is the ratio of the ADC converter offset error with no signal and the ADC converter offset error with a common-mode nonzero signal applied to either IN+ and IN– together or AUX IN+ and AUX IN– together.

ADC channel signal-to-distortion ratio, V_{DD} = 5 V, f_s = 8 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = 6 dB		A_V = 12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
ADC channel signal-to distortion ratio (see Note 6)	V_I = –6 dB to –1 dB	68		—		—		dB
	V_I = –12 dB to –6 dB	63		68		—		
	V_I = –18 dB to –12 dB	57		63		68		
	V_I = –24 dB to –18 dB	51		57		63		
	V_I = –30 dB to –24 dB	45		51		57		
	V_I = –36 dB to –30 dB	39		45		51		
	V_I = –42 dB to –36 dB	33		39		45		
	V_I = –48 dB to –42 dB	27		33		39		

NOTE 6: The analog input test signal is a 1020-Hz sine wave with 0 dB = 6 V peak to peak as the reference level for the analog input signal.

DAC channel filter transfer function, FCLK = 144 kHz, f_s = 9.6 kHz, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain relative to gain at f_i = 1020 Hz (see Note 7)	f_i < 200 Hz		0.15	dB
	f_i = 200 Hz	–0.5	0.2	
	f_i = 300 Hz to 3 kHz	–0.2	0.2	
	f_i = 3.3 kHz	–0.35	0.03	
	f_i = 3.4 kHz	–1	–0.1	
	f_i = 4 kHz		–14	
	$f_i \geq$ 4.6 kHz		–32	

NOTE 7: The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak.

DAC channel signal-to-distortion ratio, V_{DD} = 5 V, f_s = 8 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	A_V = 0 dB		A_V = –6 dB		A_V = –12 dB		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
DAC channel signal-to-distortion ratio (see Note 8)	V_O = –6 dB to 0 dB	68		—		—		dB
	V_O = –12 dB to –6 dB	63		68		—		
	V_O = –18 dB to –12 dB	57		63		68		
	V_O = –24 dB to –18 dB	51		57		63		
	V_O = –30 dB to –24 dB	45		51		57		
	V_O = –36 dB to –30 dB	39		45		51		
	V_O = –42 dB to –36 dB	33		39		45		
	V_O = –48 dB to –42 dB	27		33		39		

NOTE 8: The input signal, V_I, is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at full-scale digital input = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

system distortion, V_{DD} = 5 V, f_s = 8 kHz, FCLK = 144 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC channel attenuation	Second harmonic	Single-ended input (see Note 9)				dB
		Differential input (see Note 9)	70			
	Third harmonic and higher harmonics	Single-ended input (see Note 9)				
		Differential input (see Note 9)	70			
DAC channel attenuation	Second harmonic	Single-ended output (buffered DAC V_{MID}) (see Note 10)				
		Differential output (see Note 10)	70			
	Third harmonic and higher harmonics	Single-ended output (see Note 10)				
		Differential output (see Note 10)	70			

NOTES: 9. The input signal is a 1020-Hz sine wave for the ADC channel. Harmonic distortion is defined for an input level of –1 dB.
10. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–. Harmonic distortion is specified for a signal input level of 0 dB.

noise, low-pass and band-pass switched-capacitor filters included, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC idle channel noise		Inputs tied to ADC V_{MID} f_s = 8 kHz, FCLK = 144 kHz, (see Note 11)		180	300	µVrms
DAC idle channel noise	Broad-band noise	DIN INPUT = 00000000000000 f_s = 8 kHz, FCLK = 144 kHz, (see Note 12)		180	300	
	Noise (0 to 7.2 kHz)			180	300	
	Noise (0 to 3.6 kHz)			180	300	

NOTES: 11. The ADC channel noise is calculated by taking the RMS value of the digital output codes of the ADC channel and converting it to microvolts.
12. The DAC channel noise is measured differentially from OUT+ to OUT– across 600 Ω.

absolute gain error, V_{DD} = 5 V, f_s = 8 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
ADC channel absolute gain error (see Note 13)	–1-dB input signal	T_A = –40 to 85°C		±1	dB
DAC channel absolute gain error (see Note 14)	0-dB input signal, R_L = 600 Ω	T_A = –40 to 85°C		±1	

NOTES: 13. ADC absolute gain error is the variation in gain from the ideal gain over the specified input signal levels. The gain is measured with a –1-dB, 1020-Hz sine wave. The –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB input signal levels.
14. The DAC input signal is the digital equivalent of a 1020-Hz sine wave (full-scale analog output at digital full-scale input = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

relative gain and dynamic range, V_{DD} = 5 V, f_s = 8 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ADC channel relative gain tracking error (see Note 15)	–48-dB to –1-dB input signal range		±0.2	dB
DAC channel relative gain tracking error (see Note 16)	–48-dB to 0-dB input signal range $R_{L(diff)}$ = 600 Ω		±0.2	

NOTES: 15. ADC gain tracking is the ratio of the measured gain at one ADC channel input level to the gain measured at any other input level. The ADC channel input is a –1-dB 1020-Hz sine wave input signal. A –1-dB input signal allows for any positive gain or offset error that may affect gain measurements at or close to 0-dB ADC input signal levels.
16. DAC gain tracking is the ratio of the measured gain at one DAC channel digital input level to the gain measured at any other input level. The DAC channel input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output voltage with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

power-supply rejection, V_{DD} = 5 V (unless otherwise noted)(see Note 17)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC V_{DD} Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		dB
	f_i = 30 to 50 kHz		55		
DAC V_{DD} Supply-voltage rejection ratio, DAC channel	f_i = 0 to 30 kHz		40		
	f_i = 30 to 50 kHz		45		
DGTL V_{DD} Supply-voltage rejection ratio, ADC channel	f_i = 0 to 30 kHz		50		
	f_i = 30 to 50 kHz		55		
DGTL V_{DD} Supply-voltage rejection ratio, DAC channel	Single ended, f_i = 0 to 30 kHz		40		
	f_i = 30 to 50 kHz		45		
	Differential, f_i = 0 to 30 kHz		40		
	f_i = 30 to 50 kHz		45		

NOTE 17: Power-supply rejection measurements are made with both the ADC and the DAC channels idle and a 200-mV peak-to-peak signal applied to the appropriate supply.

crosstalk attenuation, V_{DD} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC channel crosstalk attenuation	DAC channel idle with DIN = 00000000000000, ADC input = 0 dB, 1020-Hz sine wave, Gain = 0 dB (see Note 18)		80		dB
DAC channel crosstalk attenuation	ADC channel idle with INP, INM, AUX IN+, and AUX IN– at ADC V_{MID}		80		dB
	DAC channel input = digital equivalent of a 1020-Hz sine wave (see Note 19)		80		

NOTES: 18. The test signal is a 1020-Hz sine wave with a 0 dB = 6-V peak-to-peak reference level for the analog input signal.
19. The input signal is the digital equivalent of a 1020-Hz sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 6 V peak to peak. The load impedance for the DAC output buffer is 600 Ω from OUT+ to OUT–.

monitor output characteristics, V_{DD} = 5 V (unless otherwise noted) (see Note 20)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage	Quiescent level = ADC V_{MID} Z_L = 10 kΩ and 60 pF	1.3	1.5		V
V_{OO}	Output offset voltage	No load, single ended relative to ADC V_{MID}		5	10	mV
r_o	DC output resistance			50		Ω
V_{OC}	Output common-mode voltage	No load	0.4 ADC V_{DD}	0.5 ADC V_{DD}	0.6 ADC V_{DD}	V
G	Voltage gain (see Note 21)	Gain = 0 dB	–0.2	0	0.2	dB
		Gain 2 = –8 dB	–8.2	–8	–7.8	
		Gain 3 = –18 dB	–18.4	–18	–17.6	
		Squelch (see Note 22)			–60	

NOTES: 20. All monitor output tests are performed with a 10-kΩ load resistance.
21. Monitor gains are measured with a 1020-Hz, 6-V peak-to-peak sine wave applied differentially between IN+ and IN–.The monitor output gains are nominally 0 dB, –8 dB, and –18 dB relative to its input; however, the output gains are –6 dB relative to IN+ and IN– or AUX IN+ and AUX IN–.
22. Squelch is measured differentially with respect to ADC V_{MID}.

timing requirements and specifications in master mode

recommended input timing requirements for master mode, V_{DD} = 5 V

		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{RESET}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 3)	25			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 3)			20	ns

operating characteristics over recommended range of operating free-air temperature, V_{DD} = 5 V (unless otherwise noted) (see Note 23)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{f(SCLK)}$	Shift clock fall time (see Figure 3)		13	18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 3)		13	18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FL)}$	Delay time from SCLK high to $\overline{FS}$ low (see Figure 3, Figure 5, and Note 24)		5	15	ns
$t_{d(CH-FH)}$	Delay time from SCLK high to $\overline{FS}$ high (see Figure 3)		5	20	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figure 3 and Figure 8)			20	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 9)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 10)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 10)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 10)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 10)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns
$t_{d(MH-FL)}$	Delay time from MCLK high to $\overline{FS}$ low			53	ns

NOTES: 23. All timing specifications are valid with C_L = 20 pF.
24. $\overline{FSD}$ occurs 1/2 shift-clock cycle ahead of $\overline{FS}$ when the device is operating in the master mode.

timing requirements and specifications in slave mode and codec emulation mode

recommended input timing requirements for slave mode, V_{DD} = 5 V

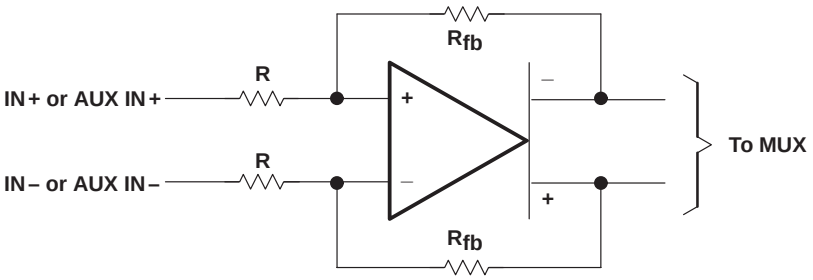
		MIN	NOM	MAX	UNIT
$t_{r(MCLK)}$	Master clock rise time		5		ns
$t_{f(MCLK)}$	Master clock fall time		5		ns
	Master clock duty cycle	40%		60%	
$t_{w(RESET)}$	$\overline{RESET}$ pulse duration	1 MCLK			
$t_{su(DIN)}$	DIN setup time before SCLK low (see Figure 4)	20			ns
$t_{h(DIN)}$	DIN hold time after SCLK high (see Figure 4)			20	ns
$t_{su(FL-CH)}$	Setup time from $\overline{FS}$ low to SCLK high			±SCLK/4	ns

operating characteristics over recommended range of operating free-air temperature, V_{DD} = 5 V (unless otherwise noted) (see Note 23)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(SCLK)}$	Shift clock cycle time (see Figure 4)	125			ns
$t_{f(SCLK)}$	Shift clock fall time (see Figure 4)			18	ns
$t_{r(SCLK)}$	Shift clock rise time (see Figure 4)			18	ns
	Shift clock duty cycle	45%		55%	
$t_{d(CH-FDL)}$	Delay time from SCLK high to $\overline{FSD}$ low (see Figure 7)			50	ns
$t_{d(CH-FDH)}$	Delay time from SCLK high to $\overline{FSD}$ high			40	ns
$t_{d(FL-FDL)}$	Delay time from $\overline{FS}$ low to $\overline{FSD}$ low (slave to slave) (see Figure 6)			40	ns
$t_{d(CH-DOUT)}$	Delay time from SCLK high to DOUT valid (see Figure 4 and Figure 8)			40	ns
$t_{d(CH-DOUTZ)}$	Delay time from SCLK↑ to DOUT in high-impedance state (see Figure 9)		20		ns
$t_{d(ML-EL)}$	Delay time from MCLK low to EOC low (see Figure 10)		40		ns
$t_{d(ML-EH)}$	Delay time from MCLK low to EOC high (see Figure 10)		40		ns
$t_{f(EL)}$	EOC fall time (see Figure 10)		13		ns
$t_{r(EH)}$	EOC rise time (see Figure 10)		13		ns
$t_{d(MH-CH)}$	Delay time from MCLK high to SCLK high			50	ns
$t_{d(MH-CL)}$	Delay time from MCLK high to SCLK low			50	ns

NOTE 23: All timing specifications are valid with C_L = 20 pF.

PARAMETER MEASUREMENT INFORMATION



R_{fb} = R for DS03 = 0 and DS02 = 1
R_{fb} = 2R for DS03 = 1 and DS02 = 0
R_{fb} = 4R for DS03 = 1 and DS02 = 1
R = 100 kΩ nominal

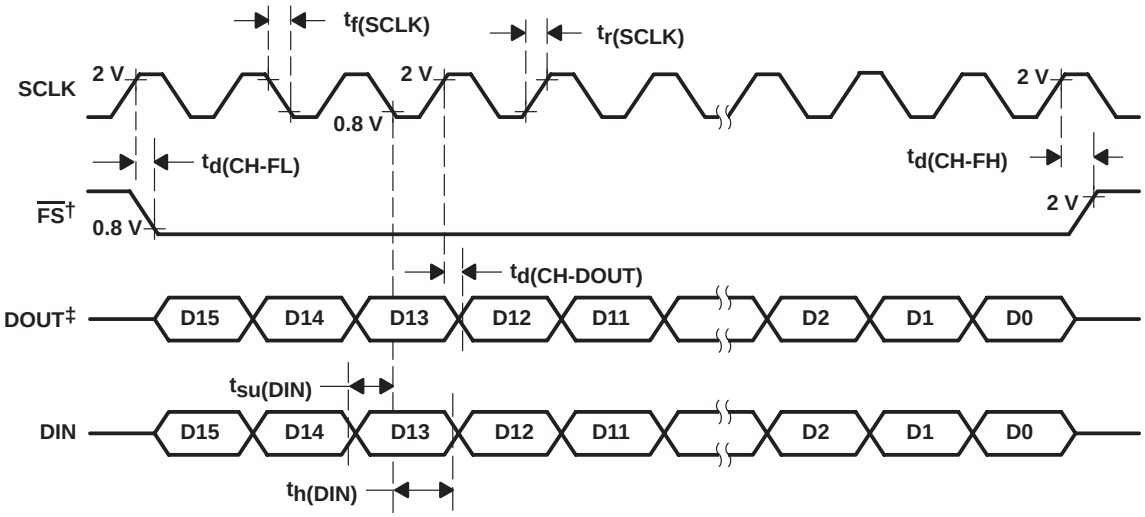
Figure 2. IN+ and IN– Gain-Control Circuitry

Table 1. Gain Control (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion 2s Complement)†

INPUT CONFIGURATION	CONTROL REGISTER 4		ANALOG INPUT‡	A/D CONVERSION RESULT
	DS03	DS02		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	0	0	All	Squelch
	0	1	V_{ID} = ±3 V	±Full scale
	1	0	V_{ID} = ±1.5 V	±Full scale
	1	1	V_{ID} = ±0.75 V	±Full scale
Single-ended configuration§ Analog input = IN+ – V_{MID} = AUX IN+ – V_{MID}	0	0	All	Squelch
	0	1	V_I = ±1.5 V	±Half scale
	1	0	V_I = ±1.5 V	±Full scale
	1	1	V_I = ±0.75 V	±Full scale

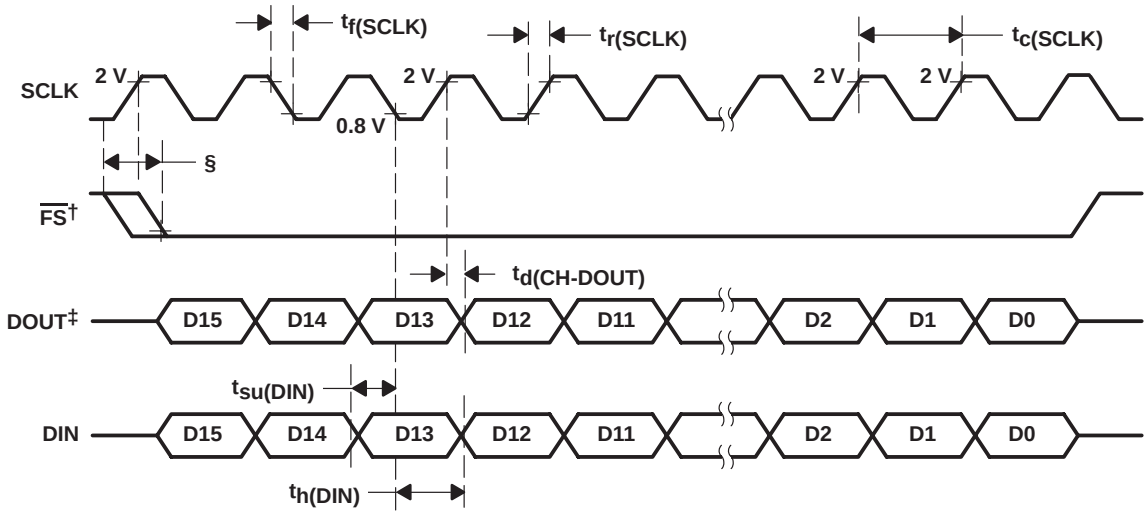
† V_{DD} = 5 V
‡ V_{ID} = differential input voltage, V_I = input voltage referenced to ADC V_{MID} with IN– or AUX IN– connected to ADC V_{MID}. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.
§ For single-ended inputs, the analog input voltage must not exceed the supply rails. All single-ended inputs must be referenced to the internal reference voltage, ADC V_{MID}, for best common-mode performance.

PARAMETER MEASUREMENT INFORMATION



† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.

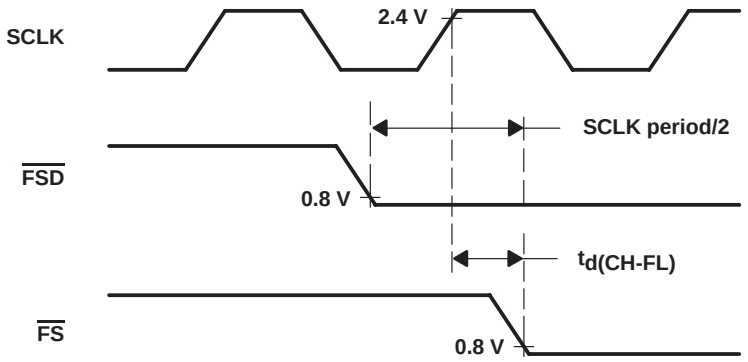
Figure 3. AIC Stand-Alone and Master-Mode Timing



† The time between falling edges of two primary $\overline{FS}$ signals is the conversion period.
‡ The data on DOUT are shifted out on the rising edge of the shift clock, and the data on DIN are shifted in on the falling edge of the shift clock.
§ The high-to-low transition of $\overline{FS}$ must must occur within ±1/4 of a shift-clock period around the 2-V level of the shift clock.

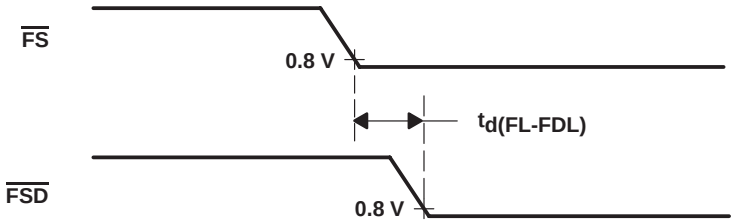
Figure 4. AIC Slave and Codec Emulation Mode

PARAMETER MEASUREMENT INFORMATION



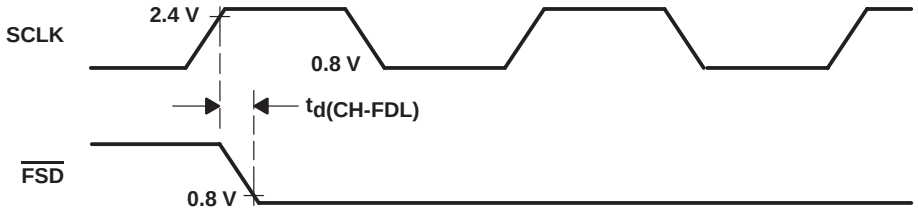
NOTE A: Timing shown is for the TLC320V343 operating as the master or as a stand-alone device.

Figure 5. Master or Stand-Alone $\overline{FS}$ and $\overline{FSD}$ Timing



NOTE A: Timing shown is for the TLC320V343 operating in the slave mode ($\overline{FS}$ and SCLK signals generated externally). The programmed data value in the $\overline{FSD}$ register is 0.

Figure 6. Slave $\overline{FS}$ to $\overline{FSD}$ Timing



NOTE A: Timing shown is for the TLC320V343 operating in the slave mode ($\overline{FS}$ and SCLK signals generated externally). There is a data value in the $\overline{FSD}$ register greater than 18 decimal.

Figure 7. Slave SCLK to $\overline{FSD}$ Timing

PARAMETER MEASUREMENT INFORMATION

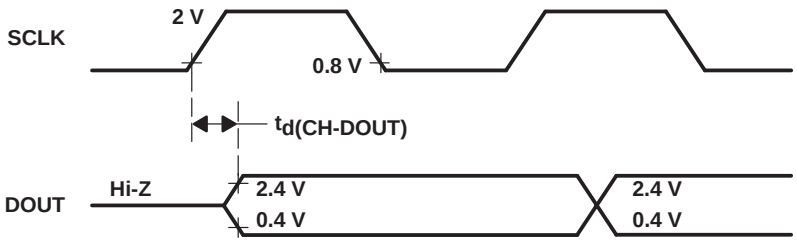


Figure 8. DOUT Enable Timing from Hi-Z

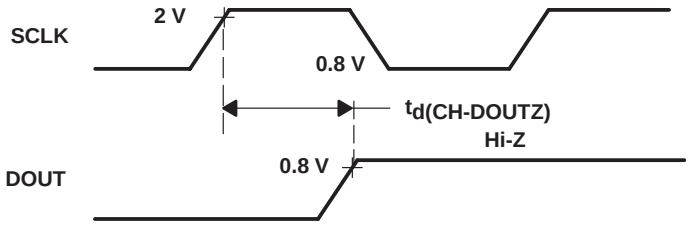


Figure 9. DOUT Delay Timing to Hi-Z

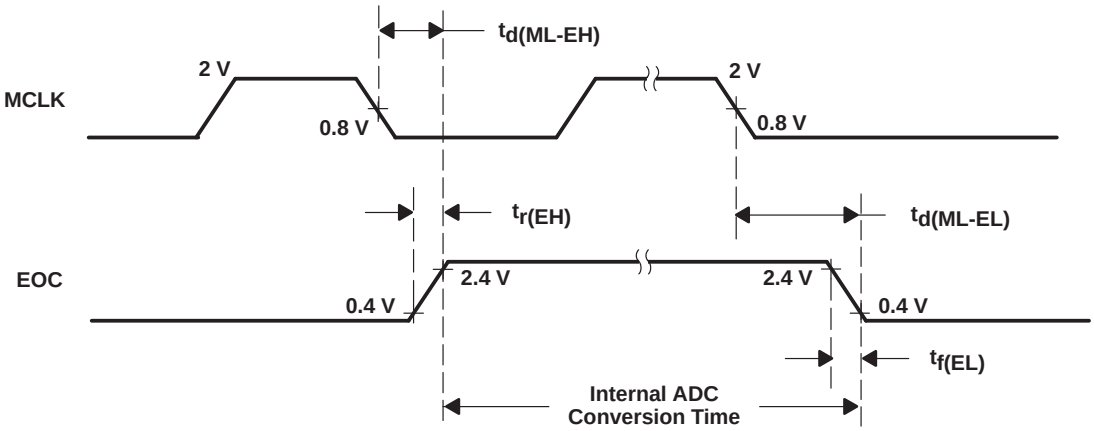
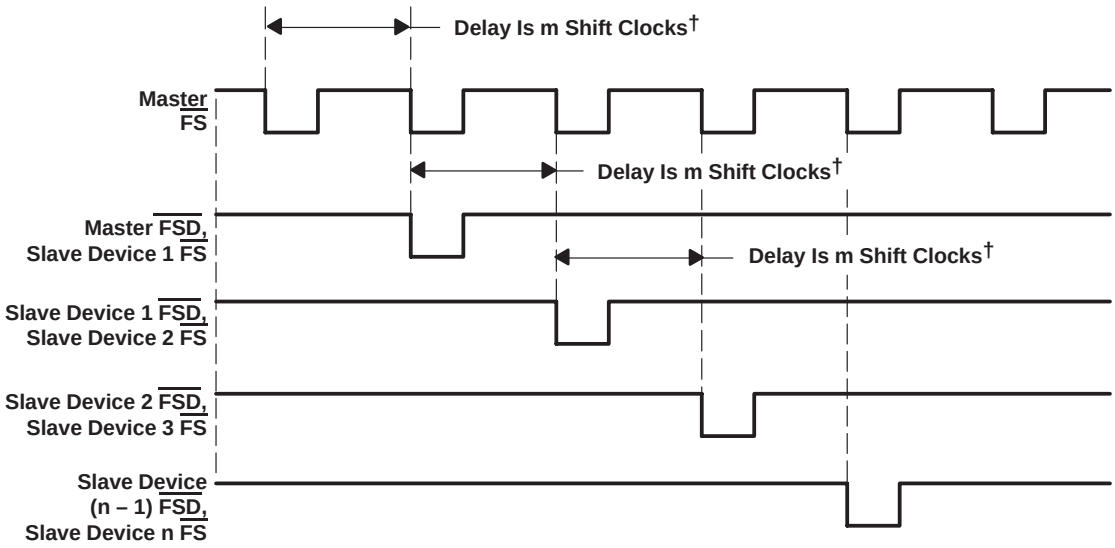


Figure 10. EOC Frame Timing

PARAMETER MEASUREMENT INFORMATION



† The delay time from any $\overline{FS}$ signals to the corresponding $\overline{FSD}$ signals is m shift clocks with the value of m being the numerical value of the data programmed into the $\overline{FSD}$ register. In the master mode with slave devices, the same data word programs the master and all slave devices; therefore, master to slave 1, slave 1 to slave 2, slave 2 to slave 3, etc., have the same delay time.

Figure 11. Master-Slave Frame-Sync Timing After a Delay Has Been Programmed into the $\overline{FSD}$ Registers

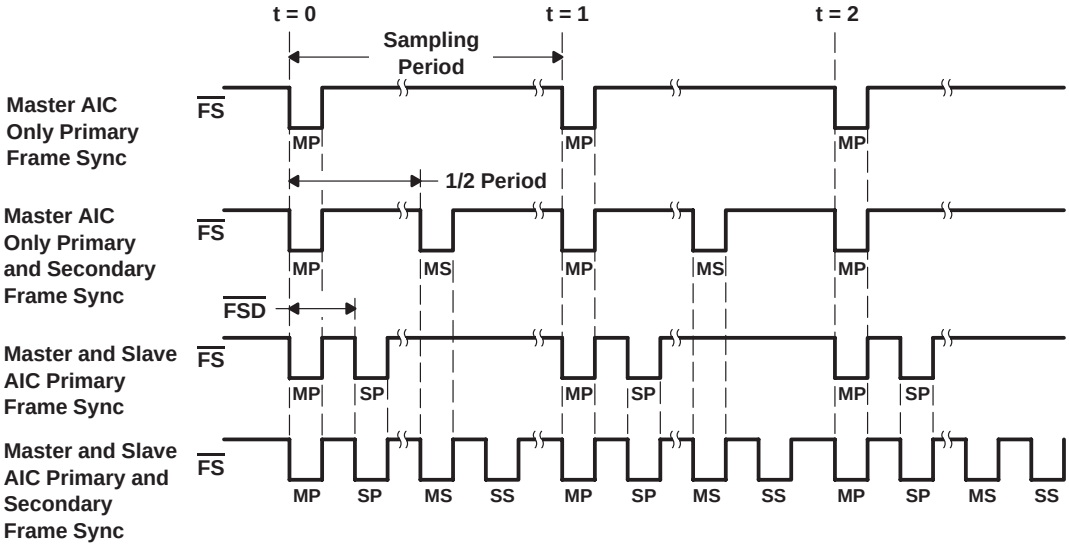


Figure 12. Master and Slave Frame-Sync Sequence with One Slave

TYPICAL CHARACTERISTICS

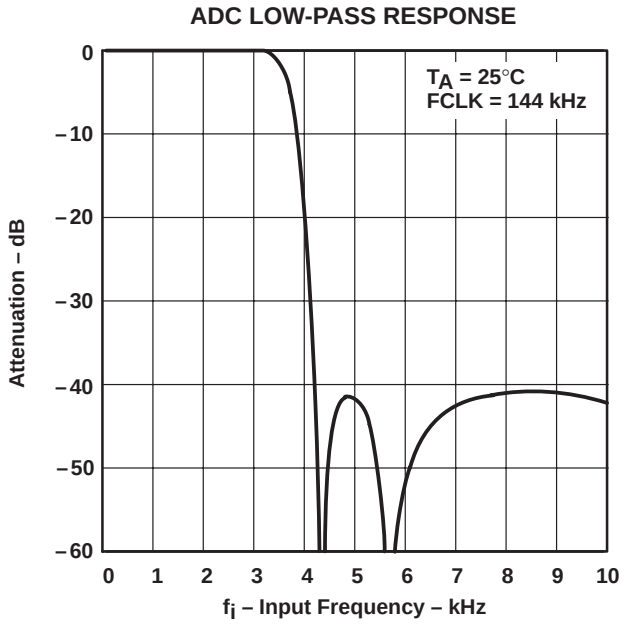


Figure 13.

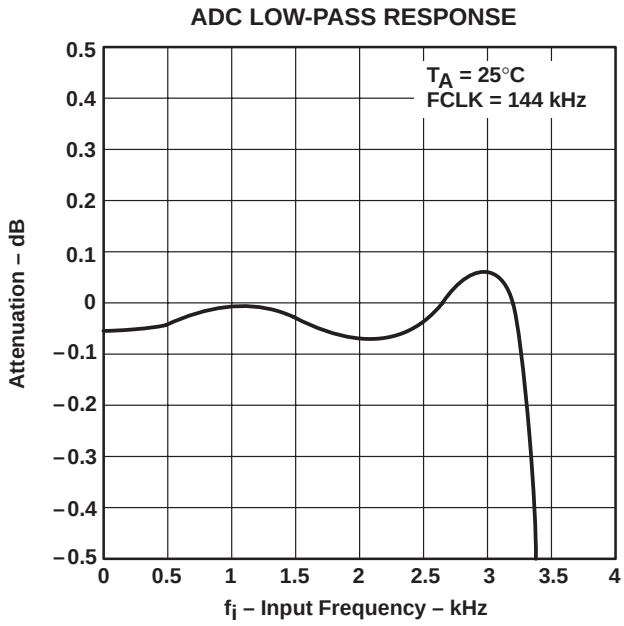


Figure 14.

TYPICAL CHARACTERISTICS

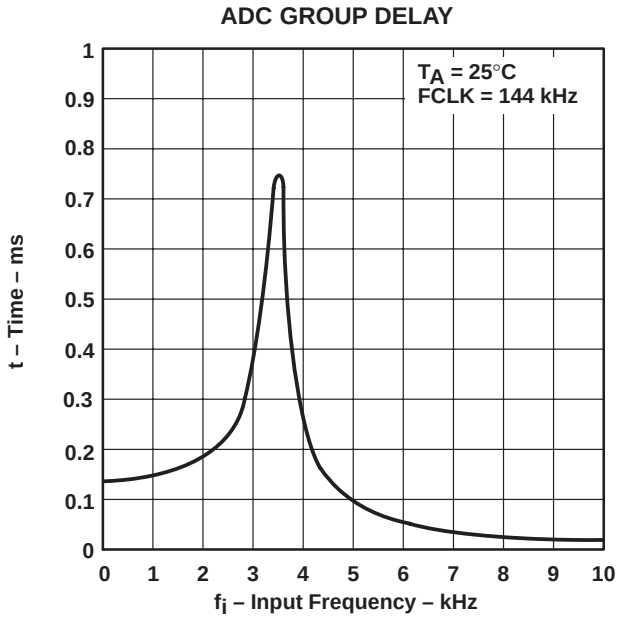


Figure 15.

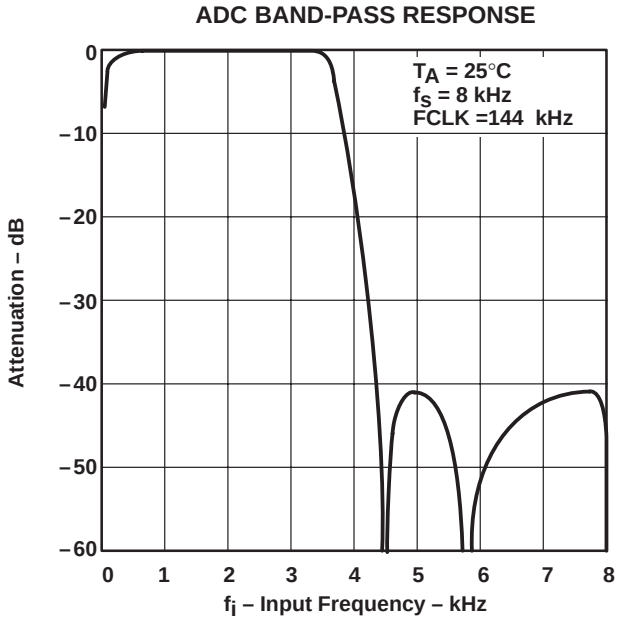


Figure 16.

TYPICAL CHARACTERISTICS

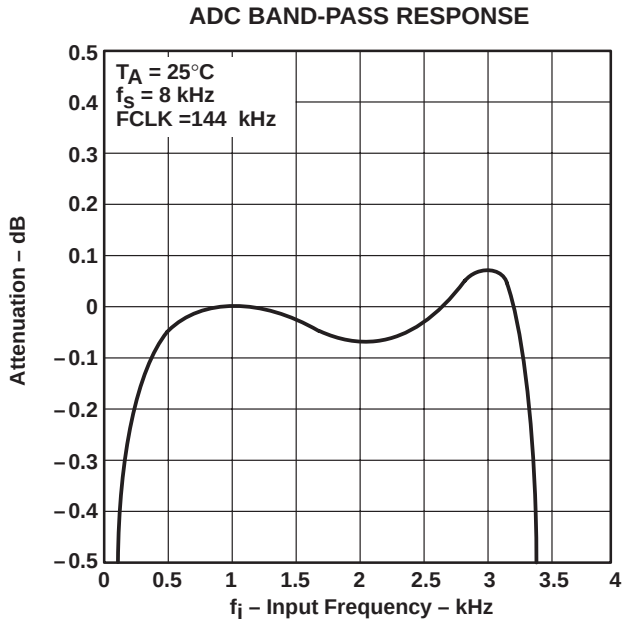


Figure 17.

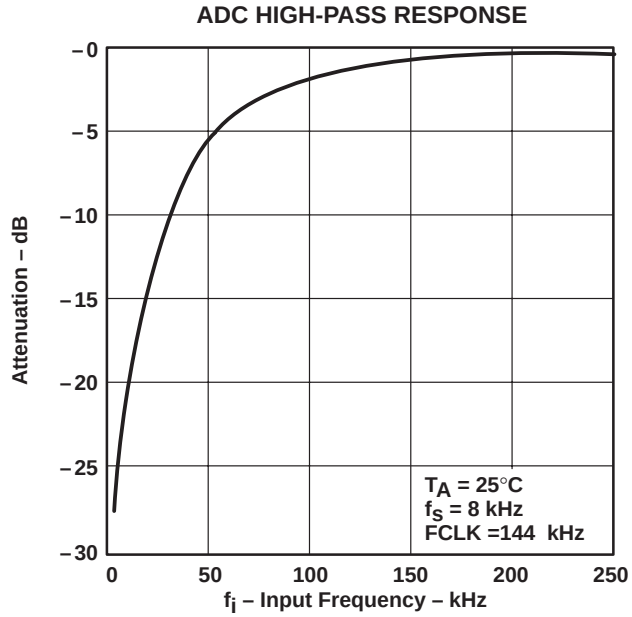


Figure 18.

TYPICAL CHARACTERISTICS

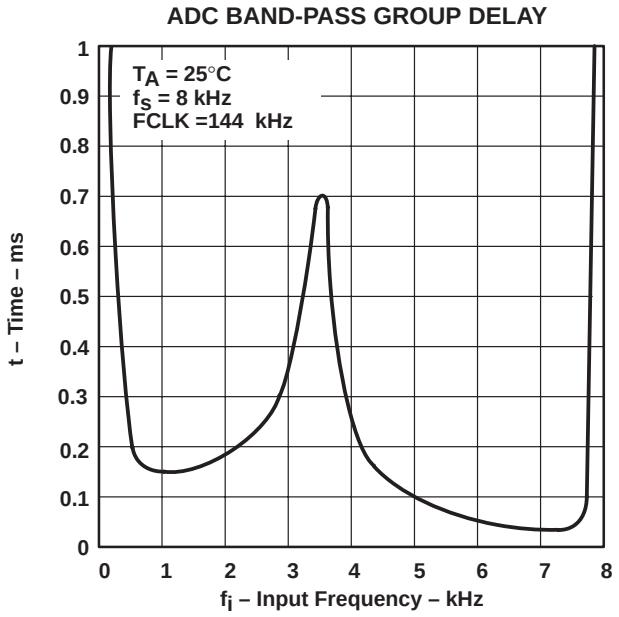


Figure 19.

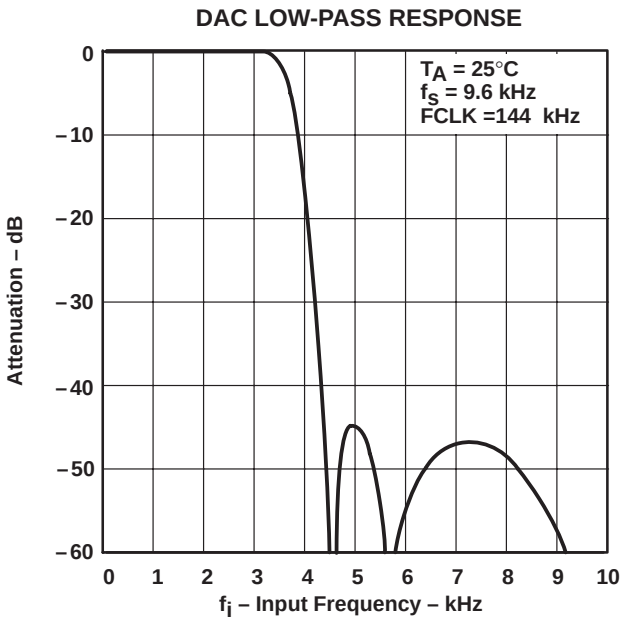


Figure 20.

TYPICAL CHARACTERISTICS

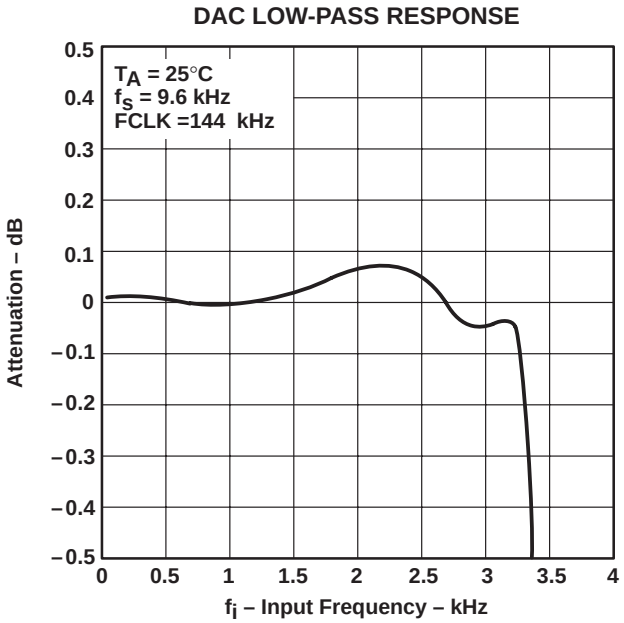


Figure 21.

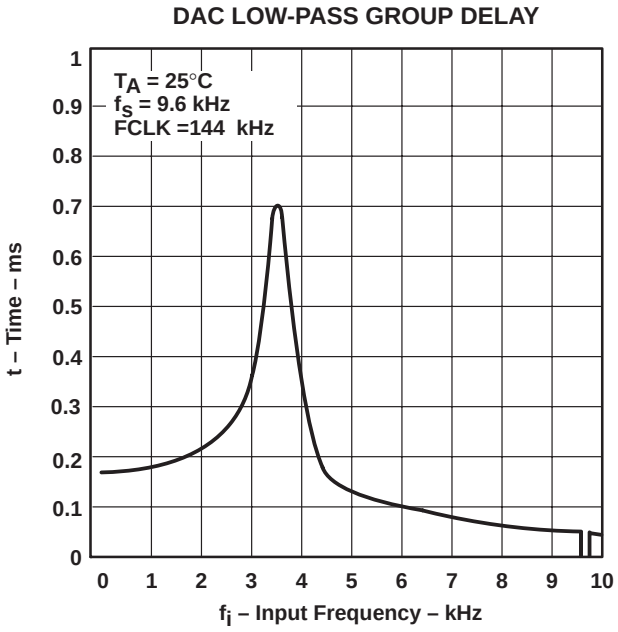


Figure 22.

TYPICAL CHARACTERISTICS

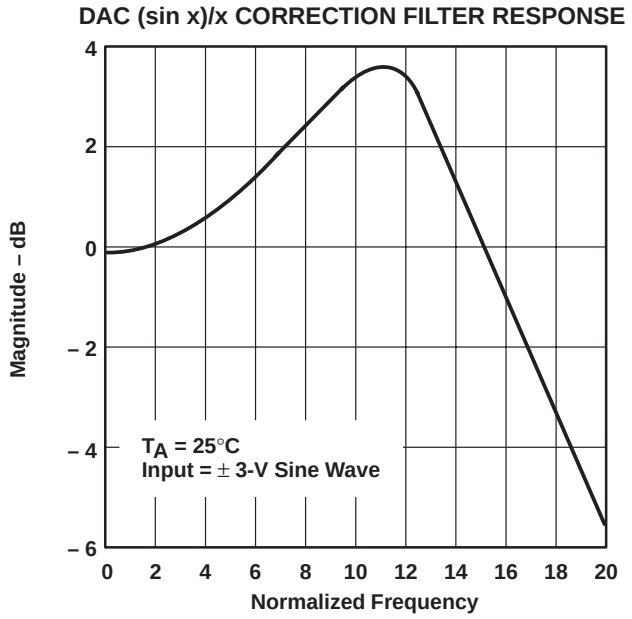


Figure 23.

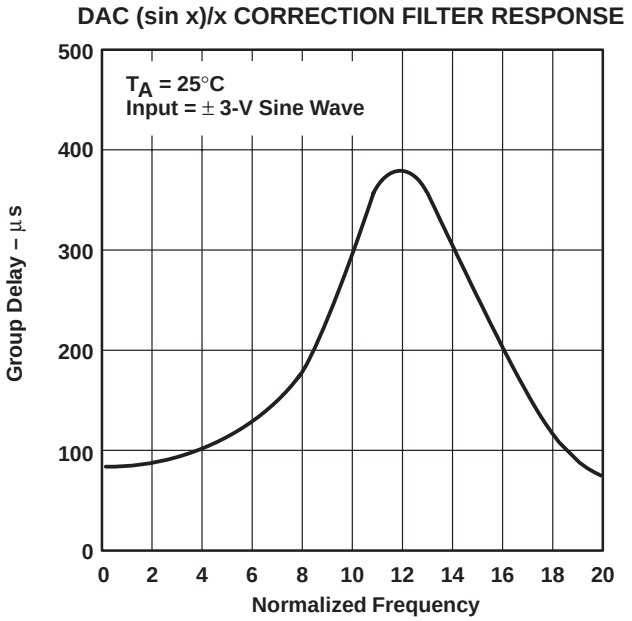


Figure 24.

TYPICAL CHARACTERISTICS

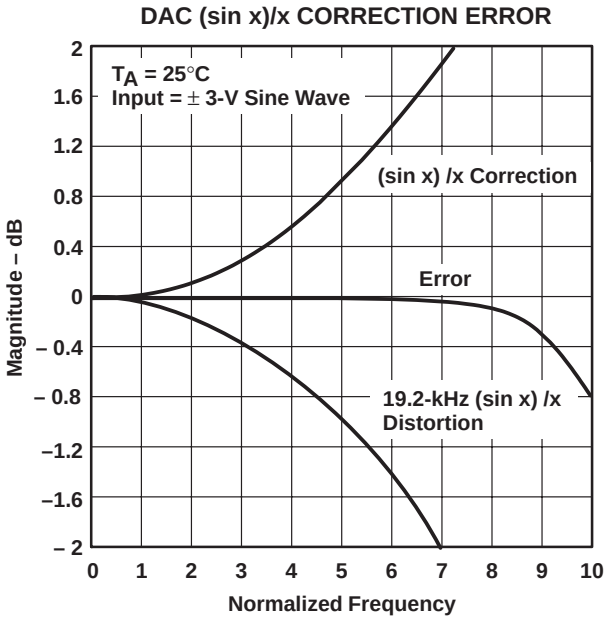


Figure 25.

APPLICATION INFORMATION

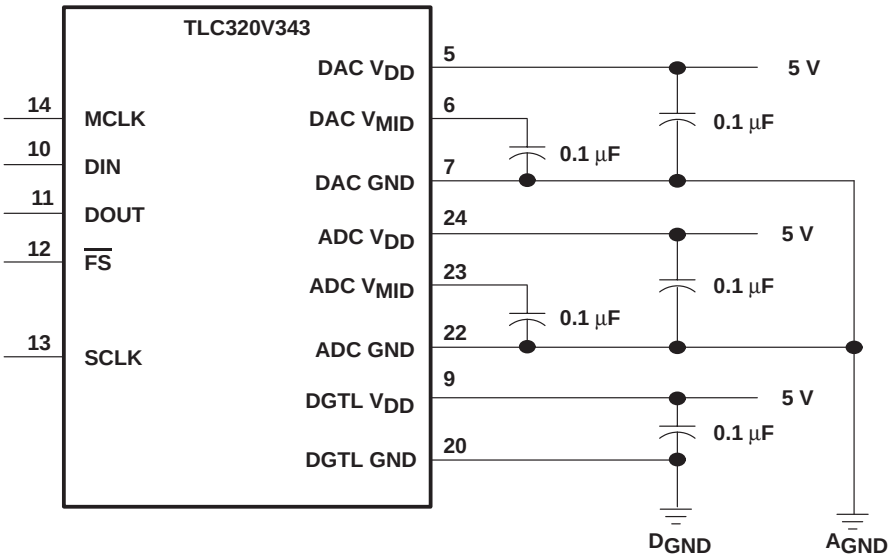


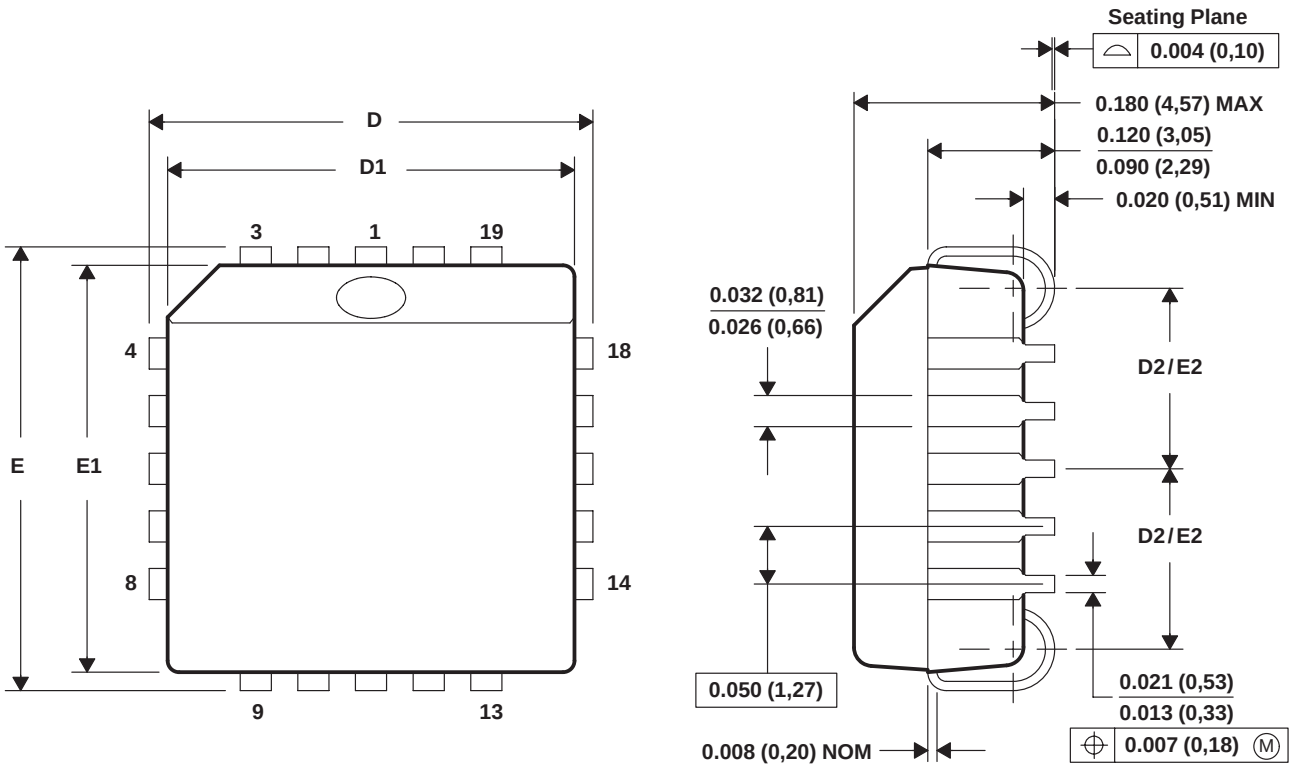
Figure 26. Stand-Alone Mode (to DSP Interface)

NOTE A: Terminal numbers shown are for the FN package.

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



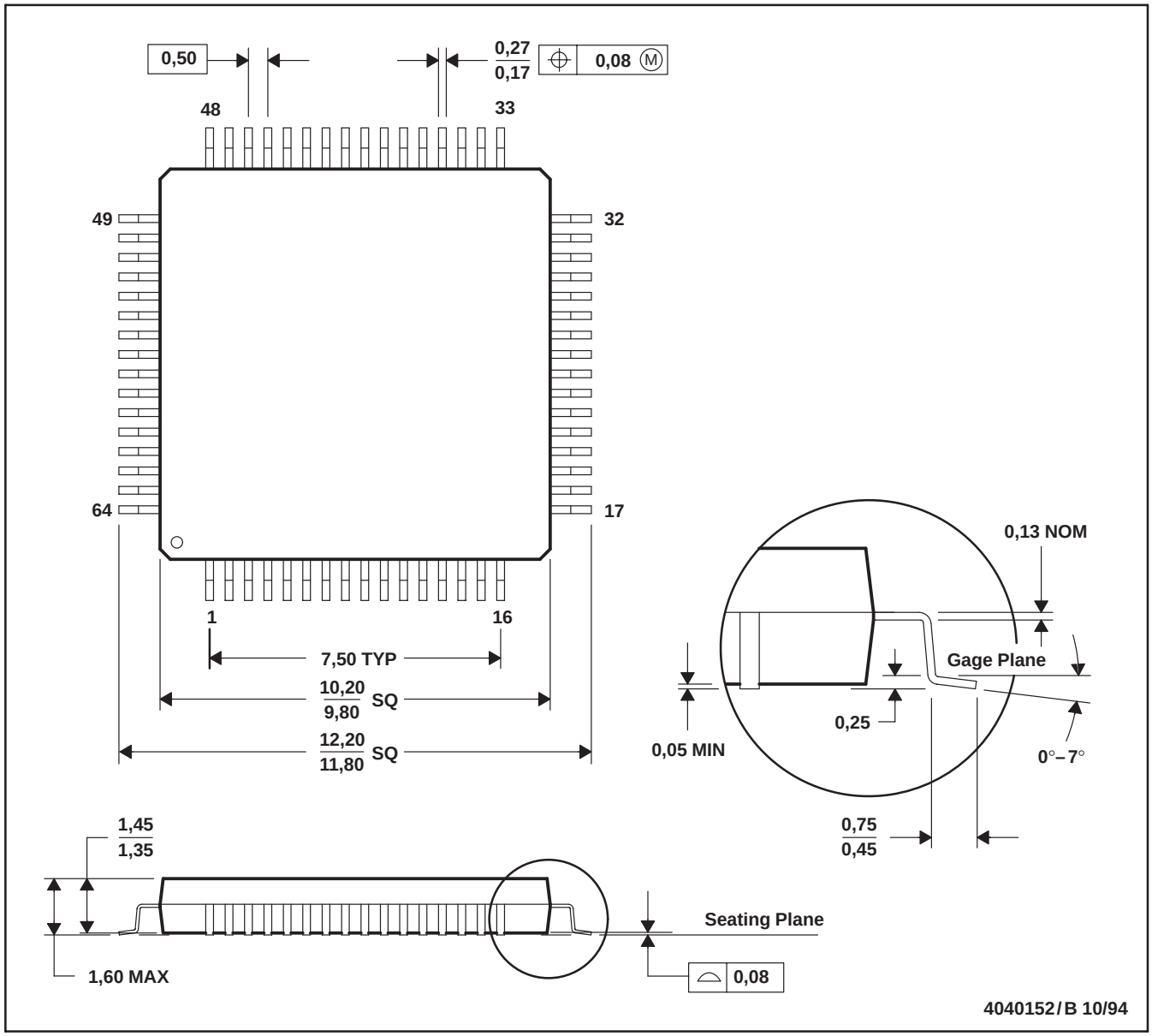
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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