



QUAD, 10-BIT, LOW-POWER, VOLTAGE OUTPUT, I²C INTERFACE DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Micropower Operation:** 500 μ A at 3 V V_{DD}
- **Fast Update Rate:** 188 kSPS
- **Per-channel Power-down Capability**
- **Power-On Reset to Zero**
- **2.7-V to 5.5-V Analog Power Supply**
- **10-Bit Monotonic**
- **I²C™ Interface Up to 3.4 Mbps**
- **Data Transmit Capability**
- **On-Chip Output Buffer Amplifier, Rail-to-Rail Operation**
- **Double-Buffered Input Register**
- **Address Support for up to Four DAC6574s**
- **Synchronous Update Support for up to 16 Channels**
- **Operation From -40° C to 105° C**
- **Small 10 Lead MSOP Package**

APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

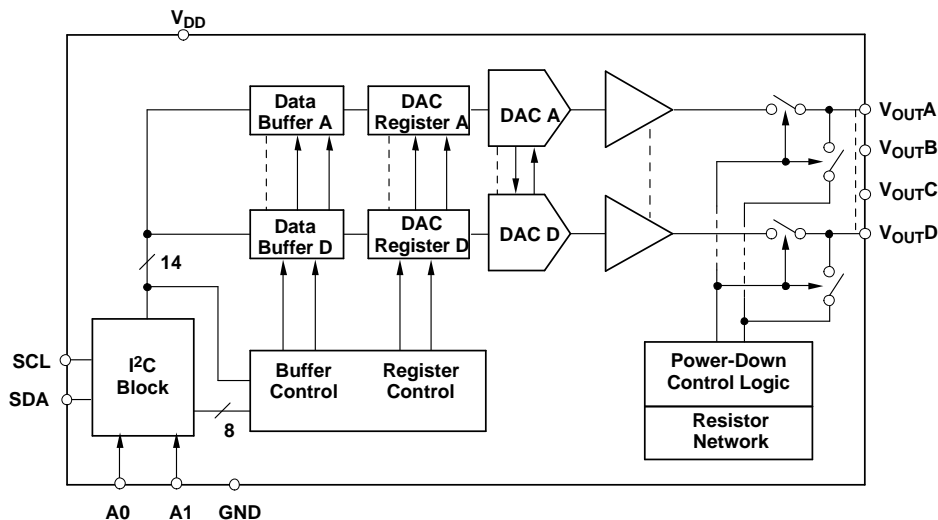
DESCRIPTION

The DAC6574 is a low-power, quad channel, 10-bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC6574 utilizes an I²C compatible two wire serial interface supporting high-speed interface mode with address support of up to four DAC6574s for a total of 16 channels on the bus.

The DAC6574 uses V_{DD} and GND to set the output range of the DAC. The DAC6574 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write takes place to the device. The DAC6574 contains a per-channel power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 200 nA at 5 V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is less than 3mW at $V_{DD} = 5$ V reducing to 1 μ W in power-down mode.

TI offers a variety of data converters with I²C interface. See DACx57x family of 16/12/10/8 bit, single and quad channel DACs. Also see ADS7823 and ADS1100, 12-bit octal channel and 16-bit single channel ADCs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I²C is a trademark of Philips Corporation.



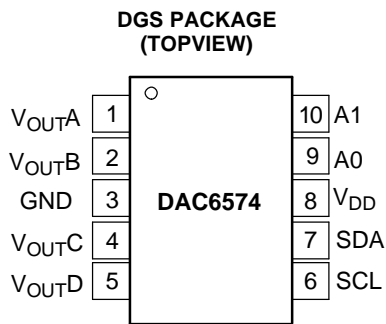
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---------|---------|------------------------|---------------------------------|-----------------|-----------------|--------------------------|
| DAC6574 | 10-MSOP | DGS | –40°C TO +105°C | D674 | DAC6574IDGS | 80 Piece Tube |
| | | | | | DAC6574IDGSR | 2500 Piece Tape and Reel |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|-----|-------------------|--|
| 1 | V _{OUTA} | Analog output voltage from DAC A |
| 2 | V _{OUTB} | Analog output voltage from DAC B |
| 3 | GND | Ground reference point for all circuitry on the part |
| 4 | V _{OUTC} | Analog output voltage from DAC C |
| 5 | V _{OUTD} | Analog output voltage from DAC D |
| 6 | SCL | Serial clock input |
| 7 | SDA | Serial data input and output |
| 8 | V _{DD} | Analog voltage supply input |
| 9 | A0 | Device address select - I ² C |
| 10 | A1 | Device address select - I ² C |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | |
|---|--------------------------------------|---------|
| V _{DD} to GND | –0.3 V to +6 V | |
| Digital input voltage to GND | –0.3 V to V _{DD} + 0.3 V | |
| V _{OUT} to GND | –0.3 V to V _{DD} + 0.3 V | |
| Operating temperature range | –40°C to +105°C | |
| Storage temperature range | –65°C to +150°C | |
| Junction temperature range (T _J max) | +150°C | |
| Power dissipation: | Thermal impedance (Θ _{JA}) | 270°C/W |
| | Thermal impedance (Θ _{JC}) | 77°C/W |
| Lead temperature, soldering: | Vapor phase (60s) | 215°C |
| | Infrared (15s) | 220°C |

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
 $V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications -40°C to $+105^\circ\text{C}$, unless otherwise specified.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---|-----------|---------------------|------------------------------|
| STATIC PERFORMANCE⁽¹⁾ | | | | | |
| Resolution | | 10 | | | Bits |
| Relative accuracy | | | ± 0.5 | ± 2 | LSB |
| Differential nonlinearity | Specified monotonic by design | | ± 0.1 | ± 0.5 | LSB |
| Zero-scale error | | | 5 | 20 | mV |
| Full-scale error | | | -0.15 | ± 1.0 | % of FSR |
| Gain error | | | | ± 1.0 | % of FSR |
| Zero code error drift | | | ± 7 | | $\mu\text{V}/^\circ\text{C}$ |
| Gain temperature coefficient | | | ± 3 | | ppm of FSR/ $^\circ\text{C}$ |
| OUTPUT CHARACTERISTICS⁽²⁾ | | | | | |
| Output voltage range | | 0 | | V_{DD} | V |
| Output voltage settling time (full scale) | $R_L = \infty$; $0\text{ pF} < C_L < 200\text{ pF}$ | | 7 | 9 | μs |
| | $R_L = \infty$; $C_L = 500\text{ pF}$ | | 12 | | μs |
| Slew rate | | | 1 | | V/ μs |
| dc crosstalk (channel-to-channel) | | | 0.01 | | LSB |
| ac crosstalk (channel-to-channel) | 1 kHz Sine Wave | | -100 | | dB |
| Capacitive load stability | $R_L = \infty$ | | 470 | | pF |
| | $R_L = 2\text{ k}\Omega$ | | 1000 | | pF |
| Digital-to-analog glitch impulse | 1 LSB change around major carry | | 12 | | nV-s |
| Digital feedthrough | | | 0.3 | | nV-s |
| DC output impedance | | | 1 | | Ω |
| Short-circuit current | $V_{DD} = 5\text{ V}$ | | 50 | | mA |
| | $V_{DD} = 3\text{ V}$ | | 20 | | mA |
| Power-up time | Coming out of power-down mode, $V_{DD} = +5\text{ V}$ | | 2.5 | | μs |
| | Coming out of power-down mode, $V_{DD} = +3\text{ V}$ | | 5 | | μs |
| LOGIC INPUTS⁽²⁾ | | | | | |
| Input current | | | | ± 1 | μA |
| V_{IN_L} , Input low voltage | | | | $0.3 \times V_{DD}$ | V |
| V_{IN_H} , Input high voltage | $V_{DD} = 3\text{ V}$ | $0.7 \times V_{DD}$ | | | V |
| Pin Capacitance | | | | 3 | pF |
| POWER REQUIREMENTS | | | | | |
| V_{DD} | | 2.7 | | 5.5 | V |
| I_{DD} (normal operation), including reference current | Excluding load current | | | | |
| | I_{DD} @ $V_{DD} = +3.6\text{ V to }+5.5\text{ V}$ | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ | 600 | 900 | μA |
| I_{DD} @ $V_{DD} = +2.7\text{ V to }+3.6\text{ V}$ | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ | 500 | 750 | μA | |
| I_{DD} (all power-down modes) | I_{DD} @ $V_{DD} = +3.6\text{ V to }+5.5\text{ V}$ | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ | 0.2 | 1 | μA |
| | I_{DD} @ $V_{DD} = +2.7\text{ V to }+3.6\text{ V}$ | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ | 0.05 | 1 | μA |
| POWER EFFICIENCY | | | | | |
| I_{OUT}/I_{DD} | $I_{LOAD} = 2\text{ mA}$, $V_{DD} = +5\text{ V}$ | | 93% | | |
| TEMPERATURE RANGE | | | | | |
| Specified performance | | -40 | | +105 | $^\circ\text{C}$ |

(1) Linearity tested using a reduced code range of 12 to 1012; output unloaded.

(2) Specified by design and characterization, not production tested.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND; all specifications -40°C to +105°C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|---|--|------------------------|-----|------|-------|
| f _{SCL} | SCL clock frequency | Standard mode | | | 100 | kHz |
| | | Fast mode | | | 400 | kHz |
| | | High-Speed Mode, C _B = 100 pF max | | | 3.4 | MHz |
| | | High-speed mode, C _B = 400 pF max | | | 1.7 | MHz |
| t _{BUF} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | μs |
| t _{HD} ; t _{STA} | Hold time (repeated) START condition | Standard mode | 4.0 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | High-speed mode | 160 | | | ns |
| t _{LOW} | LOW period of the SCL clock | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | μs |
| | | High-speed mode, C _B = 100 pF max | 160 | | | ns |
| | | High-speed mode, C _B = 400 pF max | 320 | | | ns |
| t _{HIGH} | HIGH period of the SCL clock | Standard mode | 4.0 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | High-Speed Mode, C _B = 100 pF max | 60 | | | ns |
| | | High-speed mode, C _B = 400 pF max | 120 | | | ns |
| t _{SU} ; t _{STA} | Setup time for a repeated START condition | Standard mode | 4.7 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | High-speed mode | 160 | | | ns |
| t _{SU} ; t _{DAT} | Data setup time | Standard mode | 250 | | | ns |
| | | Fast mode | 100 | | | ns |
| | | High-speed mode | 10 | | | ns |
| t _{HD} ; t _{DAT} | Data hold time | Standard mode | 0 | | 3.45 | μs |
| | | Fast mode | 0 | | 0.9 | μs |
| | | High-speed mode, C _B = 100 pF max | 0 | | 70 | ns |
| | | High-speed mode, C _B = 400 pF max | 0 | | 150 | ns |
| t _{RCL} | Rise time of SCL signal | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 + 0.1C _B | | 300 | ns |
| | | High-speed mode, C _B = 100 pF max | 10 | | 40 | ns |
| | | High-speed mode, C _B = 400 pF max | 20 | | 80 | ns |
| t _{RCL1} | Rise time of SCL signal after a repeated START condition and after an acknowledge BIT | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 + 0.1C _B | | 300 | ns |
| | | High-speed mode, C _B = 100 pF max | 10 | | 80 | ns |
| | | High-speed mode, C _B = 400 pF max | 20 | | 160 | ns |
| t _{FCL} | Fall time of SCL signal | Standard mode | | | 300 | ns |
| | | Fast mode | 20 + 0.1C _B | | 300 | ns |
| | | High-speed mode, C _B = 100 pF max | 10 | | 40 | ns |
| | | High-speed mode, C _B = 400 pF max | 20 | | 80 | ns |
| t _{RDA} | Rise time of SDA signal | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 + 0.1C _B | | 300 | ns |
| | | High-speed mode, C _B = 100 pF max | 10 | | 80 | ns |
| | | High-speed mode, C _B = 400 pF max | 20 | | 160 | ns |

TIMING CHARACTERISTICS (continued)

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND; all specifications $-40^\circ\text{C to }+105^\circ\text{C}$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------|---|--|---------------|-----|-----|---------------|
| t_{FDA} | Fall time of SDA signal | Standard mode | | | 300 | ns |
| | | Fast mode | $20 + 0.1C_B$ | | 300 | ns |
| | | High-speed mode, $C_B = 100\text{ pF max}$ | 10 | | 80 | ns |
| | | High-speed mode, $C_B = 400\text{ pF max}$ | 20 | | 160 | ns |
| $t_{SU}; t_{STO}$ | Setup time for STOP condition | Standard mode | 4.0 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | High-speed mode | 160 | | | ns |
| C_B | Capacitive load for SDA and SCL | | | 400 | | pF |
| t_{SP} | Pulse width of spike suppressed | Fast mode | | | 50 | ns |
| | | High-speed mode | | | 10 | ns |
| V_{NH} | Noise margin at the HIGH level for each connected device (including hysteresis) | Standard mode | $0.2 V_{DD}$ | | | V |
| | | Fast mode | | | | |
| | | High-speed mode | | | | |
| V_{NL} | Noise margin at the LOW level for each connected device (including hysteresis) | Standard mode | $0.1 V_{DD}$ | | | V |
| | | Fast mode | | | | |
| | | High-speed mode | | | | |

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

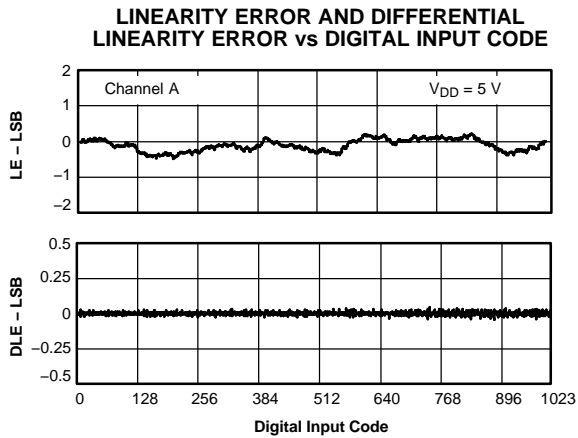


Figure 1.

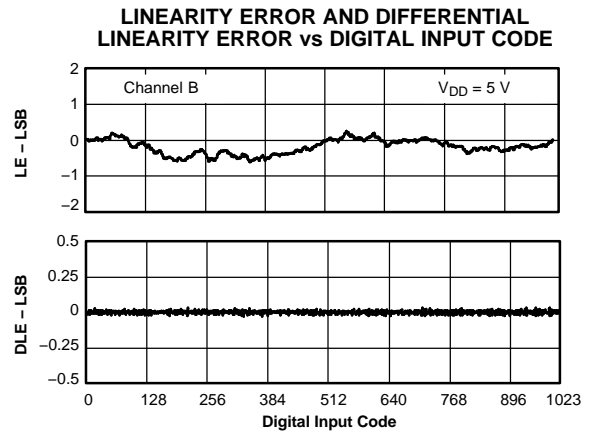


Figure 2.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

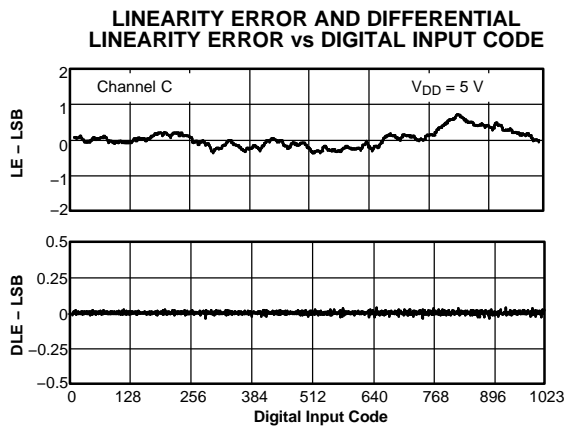


Figure 3.

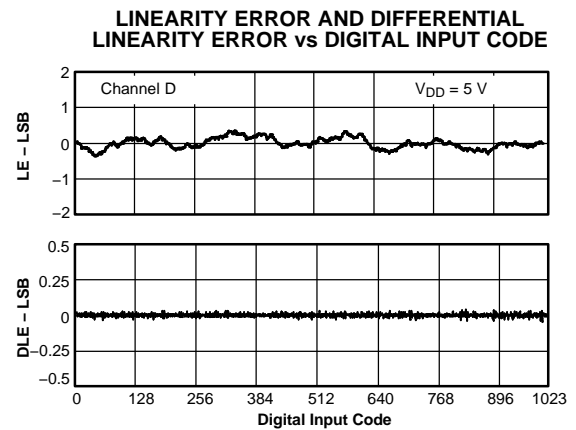


Figure 4.

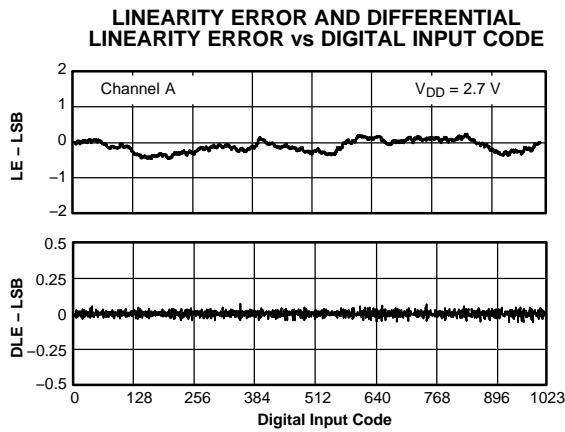


Figure 5.

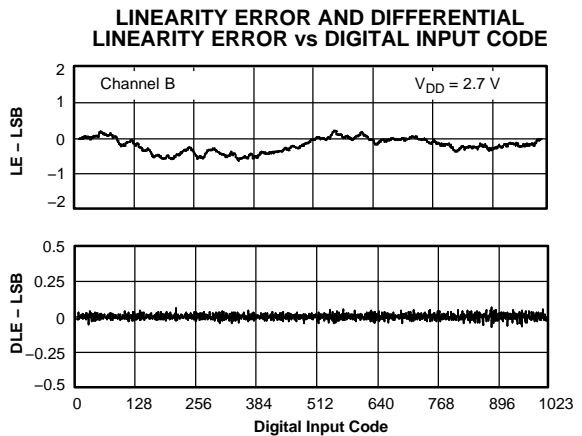


Figure 6.

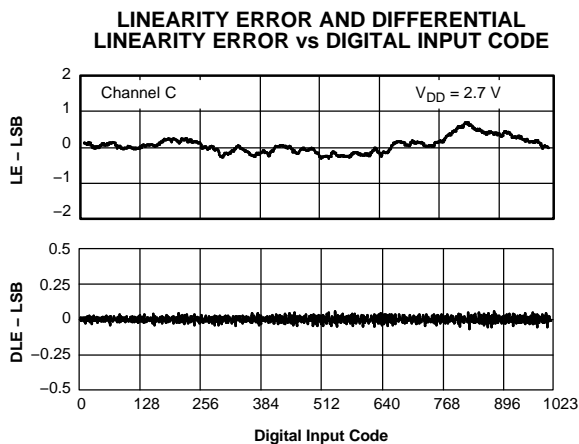


Figure 7.

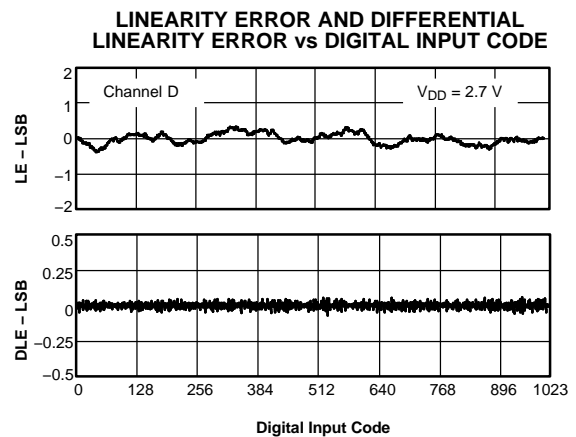


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

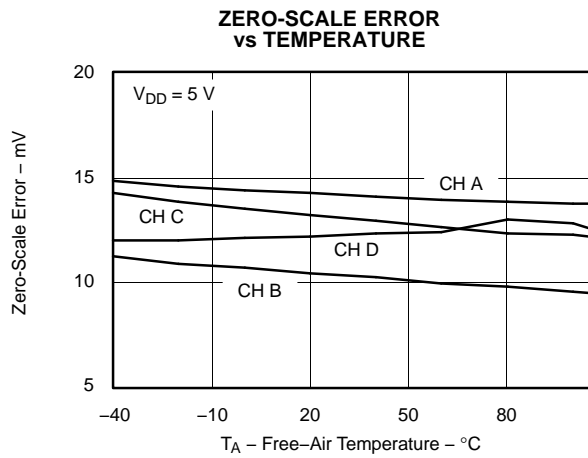


Figure 9.

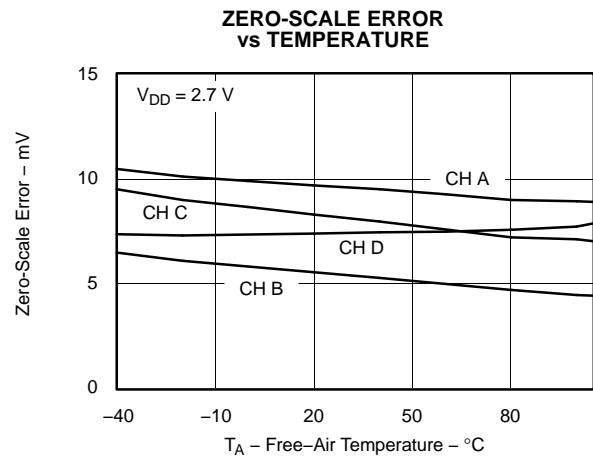


Figure 10.

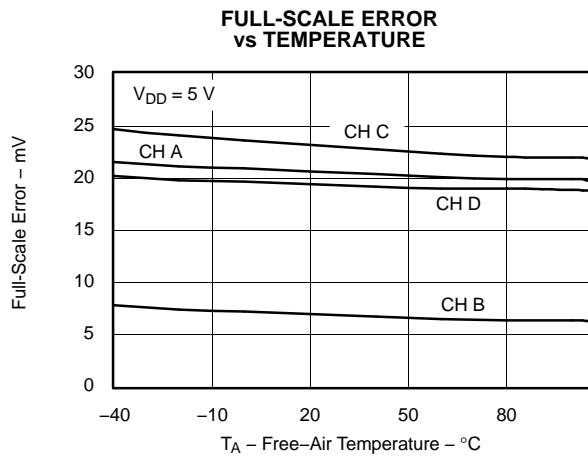


Figure 11.

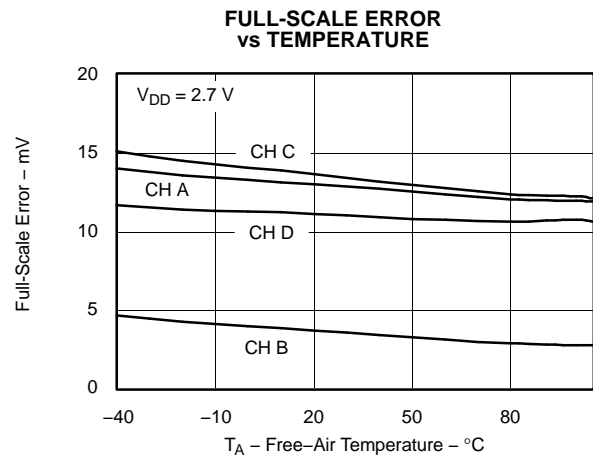


Figure 12.

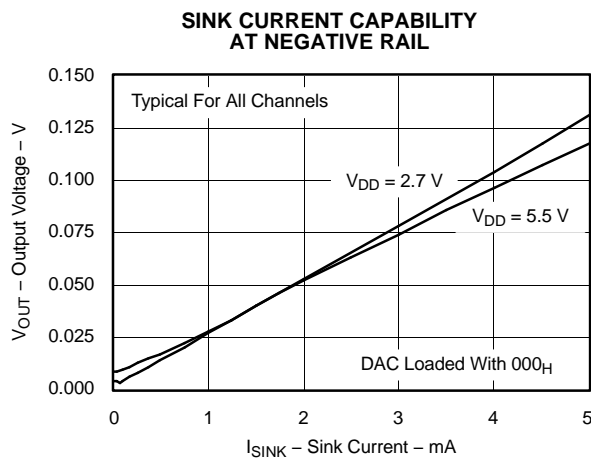


Figure 13.

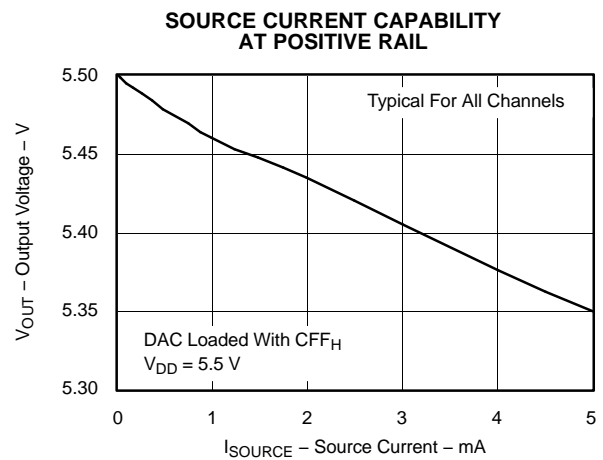


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

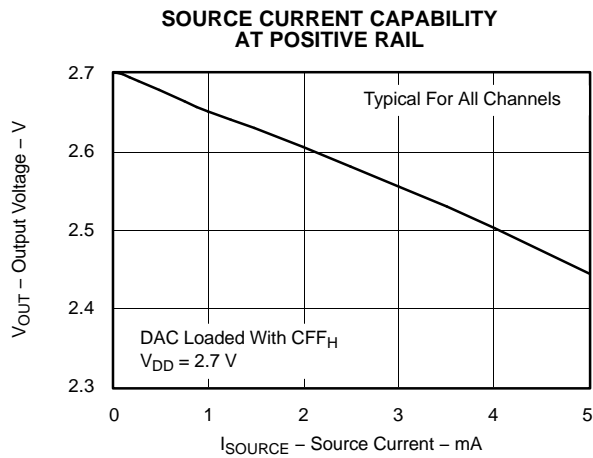


Figure 15.

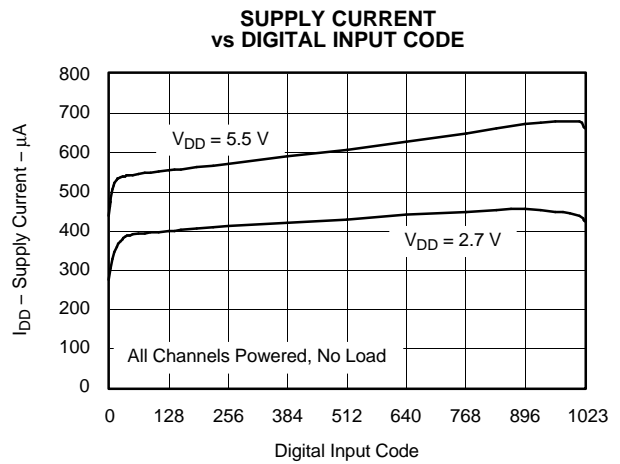


Figure 16.

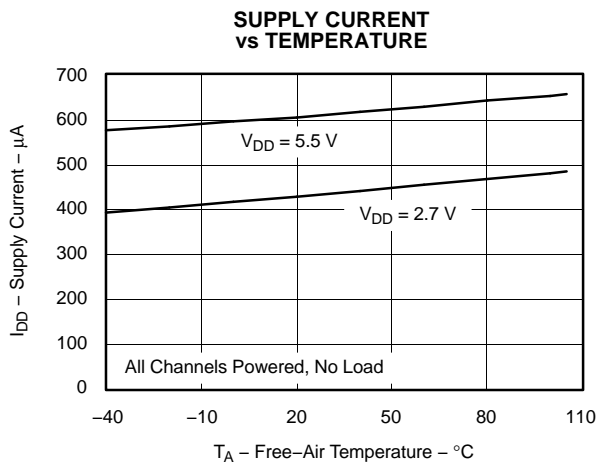


Figure 17.

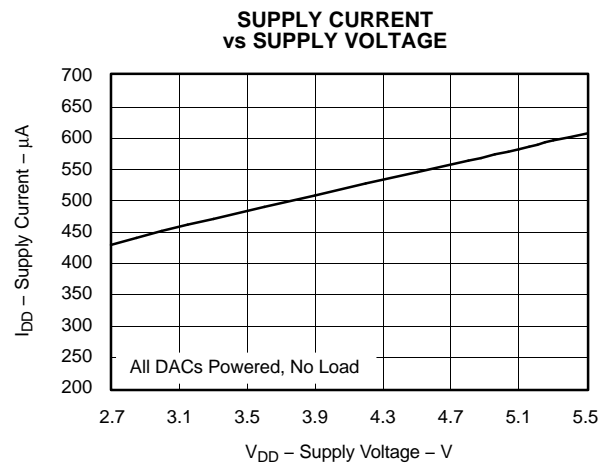


Figure 18.

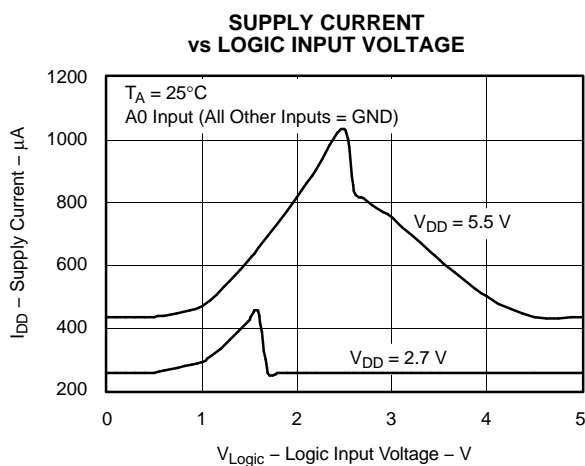


Figure 19.

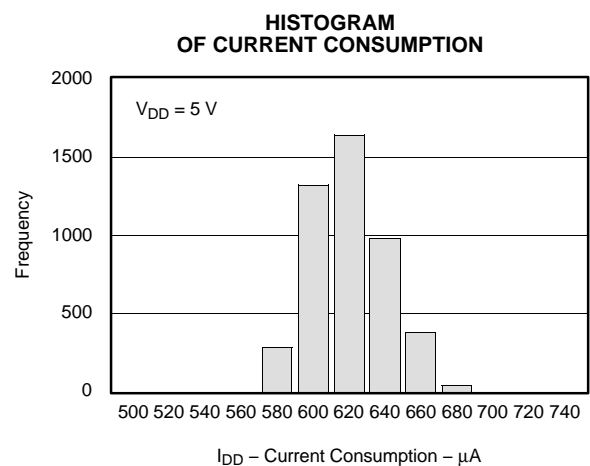


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

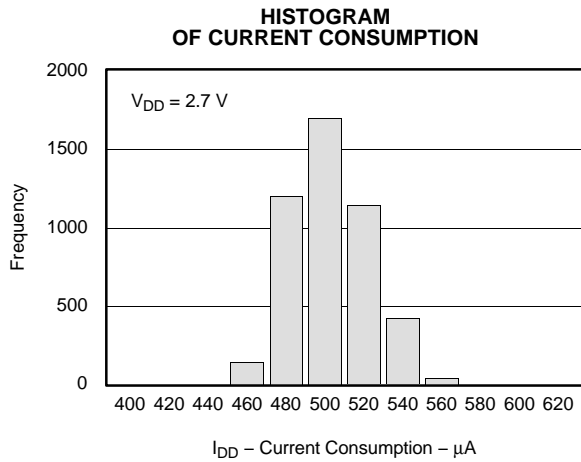


Figure 21.

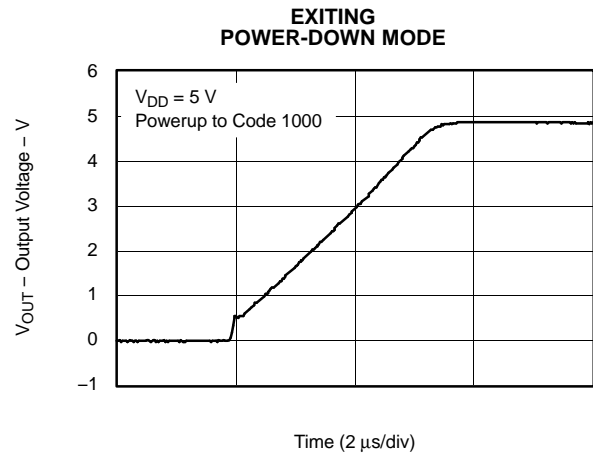


Figure 22.

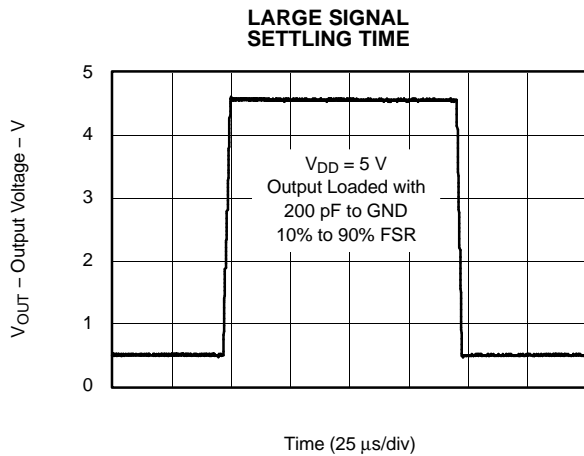


Figure 23.

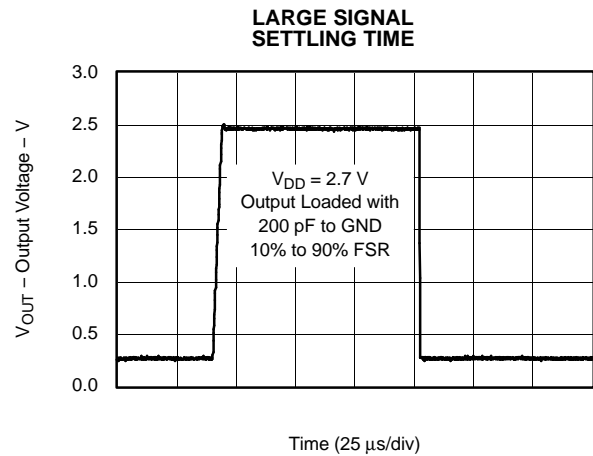


Figure 24.

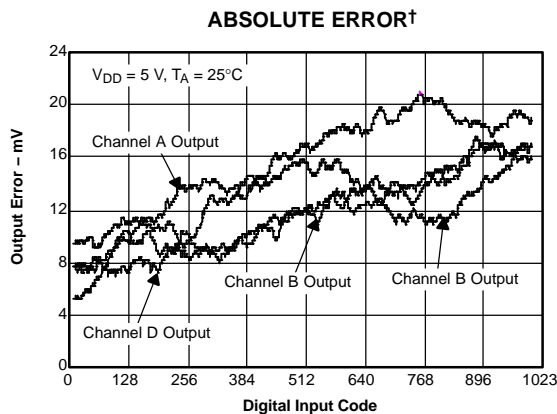


Figure 25.

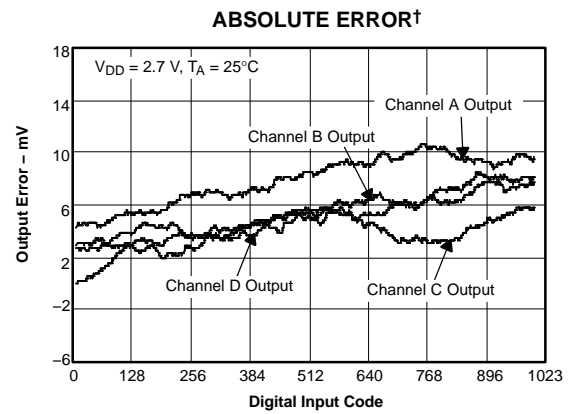


Figure 26.

†Absolute error is the deviation from ideal DAC characteristics. It includes affects of offset, gain, and integral linearity.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC6574 consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a generalized block diagram of the DAC architecture.

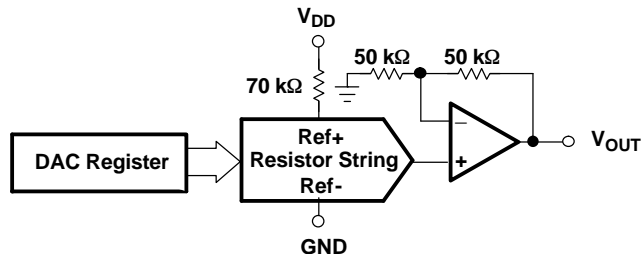


Figure 27. R-String DAC Architecture

The input coding to the DAC6574 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = V_{DD} \times \frac{D}{1024}$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 1023.

RESISTOR STRING

The resistor string section is shown in Figure 28. It is basically a divide-by-2 resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because the architecture consists of a string of resistors, it is specified monotonic.

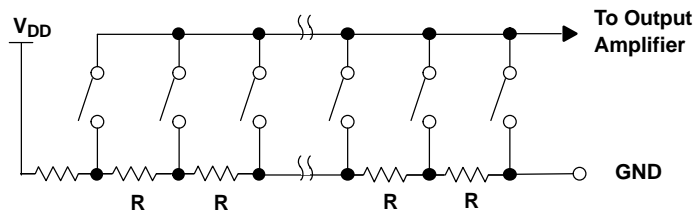


Figure 28. Typical Resistor String

Output Amplifier

The output buffer is a gain-of-2 noninverting amplifiers, capable of generating rail-to-rail voltages on its output, which gives an output range of 0V to V_{DD} . It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/μs with a half-scale settling time of 7 μs with the output unloaded.

I²C Interface

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

THEORY OF OPERATION (continued)

The DAC6574 works as a slave and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode. The DAC6574 supports 7-bit addressing; 10-bit addressing and general call address are *not* supported.

F/S-Mode Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 29. All I²C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses, and transmits the 7-bit address and the *read/write direction bit* R/\overline{W} on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data condition* requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 30). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 31) by pulling the SDA line low during the entire high period of the 9th SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/\overline{W} bit 1) or *receive* data from the slave (R/\overline{W} bit 0). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 29). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

H/S-Mode Protocol

- When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.
- The master generates a start condition followed by a valid serial byte containing H/S master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the H/S master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.
- The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the H/S-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in H/S-mode.

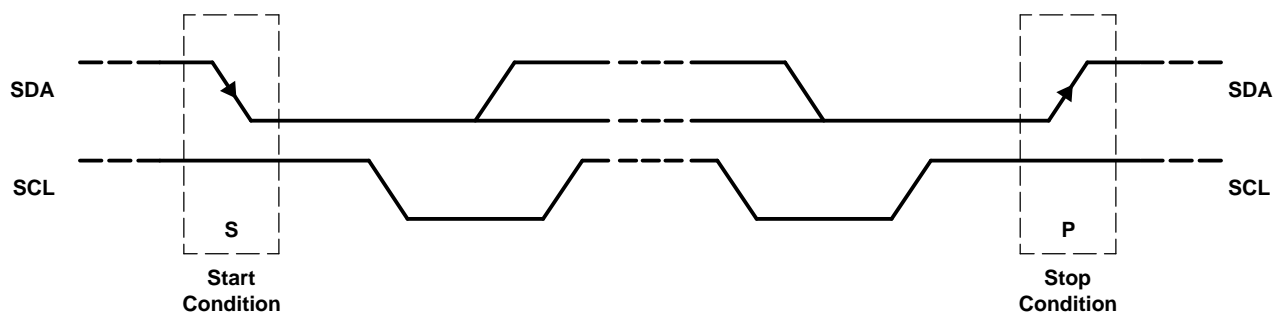


Figure 29. START and STOP Conditions

THEORY OF OPERATION (continued)

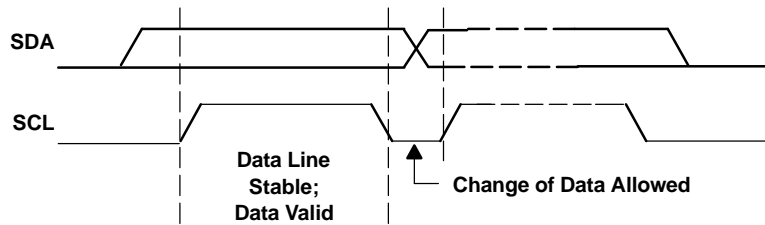


Figure 30. Bit Transfer on the I²C Bus

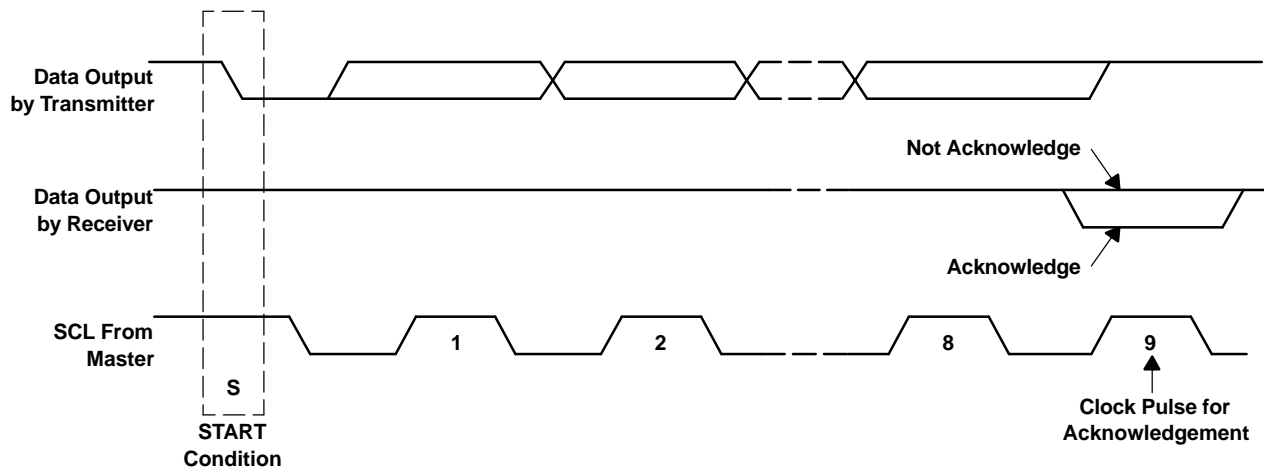


Figure 31. Acknowledge on the I²C Bus

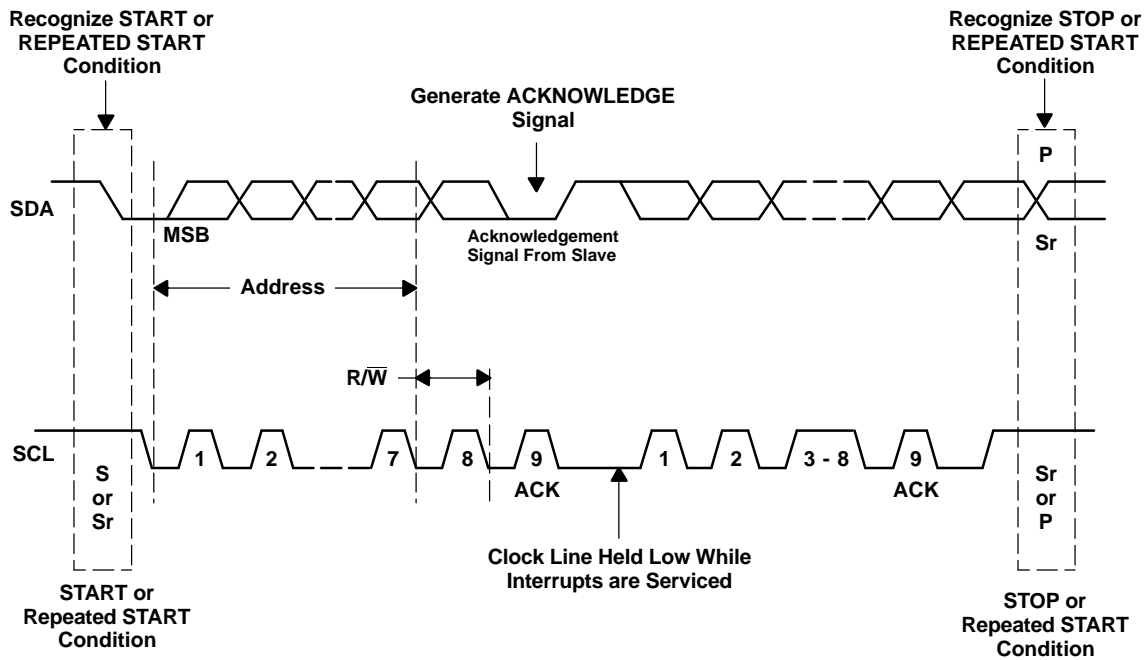


Figure 32. Bus Protocol

DAC6574 I²C Update Sequence

The DAC6574 requires a start condition, a valid I²C address, a control byte, an MSB byte, and an LSB byte for a single update. After the receipt of each byte, DAC6574 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the DAC6574. The control byte sets the operational mode of the selected DAC6574. Once the operational mode is selected by the control byte, DAC6574 expects an MSB byte followed by an LSB byte for data update to occur. DAC6574 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

Control byte needs not to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, DAC6574 requires a start condition, a valid I²C address, a control byte, an MSB byte and an LSB byte. For all consecutive updates, DAC6574 needs an MSB byte and an LSB byte as long as the control command remains the same.

Using the I²C high-speed mode ($f_{\text{scI}} = 3.4 \text{ MHz}$), the clock running at 3.4 MHz, each 10-bit DAC update other than the first update can be done within 18 clock cycles (MSB byte, acknowledge signal, LSB byte, acknowledge signal), at 188.88 KSPS. Using the fast mode ($f_{\text{scI}} = 400 \text{ kHz}$), clock running at 400 kHz, maximum DAC update rate is limited to 22.22 KSPS. Once a stop condition is received DAC6574 releases the I²C bus and awaits a new start condition.

Address Byte

| MSB | | | | | | | LSB |
|-----|---|---|---|---|----|----|-----|
| 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/W |

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory preset to 10011. The next two bits of the address are the device select bits A1 and A0. The A1, A0 address inputs can be connected to V_{DD} or digital GND, or can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins during the power-up sequence of the DAC6574. Up to 4 devices (DAC6574) can still be connected to the same I²C-Bus.

Broadcast Address Byte

| MSB | | | | | | | LSB |
|-----|---|---|---|---|---|---|-----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Broadcast addressing is also supported by DAC6574. Broadcast addressing can be used for synchronously updating or powering down multiple DAC6574 devices. DAC6574 is designed to work with other members of the DAC857x and DAC757x families to support multichannel synchronous update. Using the broadcast address, DAC6574 responds regardless of the states of the address pins. Broadcast is supported only in write mode (Master writes to DAC6574).

Control Byte

| MSB | | | | | | LSB | |
|-----|---|----|----|---|------|------|-----|
| 0 | 0 | L1 | L0 | X | Sel1 | Sel0 | PD0 |

Table 1. Control Register Bit Descriptions

| Bit Name | Bit Number/Description | |
|----------|---|---|
| L1 | Load1 (Mode Select) Bit | |
| L2 | Load0 (Mode Select) Bit | |
| | Are used for selecting the update mode. | |
| | 00 | Store I ² C data. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register of a selected channel. This mode does not change the DAC output of the selected channel. |
| | 01 | Update selected DAC with I ² C data. Most commonly utilized mode. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. This mode changes the DAC output of the selected channel with the new data. |
| | 10 | 4-channel synchronous update. The contents of MS-BYTE and LS-BYTE (or power down information) are stored in the temporary register and in the DAC register of the selected channel. Simultaneously, the other three channels get updated with previously stored data from the temporary register. This mode updates all four channels together. |
| | 11 | Broadcast update mode. This mode has two functions. In broadcast mode, DAC6574 responds regardless of local address matching, and channel selection becomes irrelevant as all channels update. This mode is intended to enable up to 16 channels simultaneous update, if used with the I ² C broadcast address (1001 0000). |
| | | If Sel1=0 |
| | | All four channels are updated with the contents of their temporary register data. |
| | | If Sel1=1 |
| | | All four channels are updated with the MS-BYTE and LS-BYTE data or powerdown. |
| Sel1 | Buff Sel1 Bit | |
| Sel0 | Buff Sel0 Bit | |
| | Channel Select Bits | |
| | 00 | Channel A |
| | 01 | Channel B |
| | 10 | Channel C |
| | 11 | Channel D |
| PD0 | Power Down Flag | |
| | 0 | Normal operation |
| | 1 | Power-down flag (MSB7 and MSB6 indicate a power-down operation, as shown in Table 2). |

Table 2. Control Byte

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | MSB7 | MSB6 | MSB5... | DESCRIPTION |
|--|----|-------|-------|------------|---------------------|----------|-----|-------------|-------------|--------------|--|
| 0 | 0 | Load1 | Load0 | Don't Care | Ch Sel 1 | Ch Sel 0 | PD0 | MSB (PD1) | MSB-1 (PD2) | MSB-2 ...LSB | |
| (Address Select) | | | | | | | | | | | |
| | | 0 | 0 | X | 0 | 0 | 0 | Data | | | Write to temporary register A (TRA) with data |
| | | 0 | 0 | X | 0 | 1 | 0 | Data | | | Write to temporary register B (TRB) with data |
| | | 0 | 0 | X | 1 | 0 | 0 | Data | | | Write to temporary register C (TRC) with data |
| | | 0 | 0 | X | 1 | 1 | 0 | Data | | | Write to temporary register D (TRD) with data |
| | | 0 | 0 | X | (00, 01, 10, or 11) | | 1 | see Table 8 | 0 | | Write to TRx (selected by C2 & C1 w/Powerdown Command) |
| | | 0 | 1 | X | (00, 01, 10, or 11) | | 0 | Data | | | Write to TRx (selected by C2 & C1 and load DACx w/data) |
| | | 0 | 1 | X | (00, 01, 10, or 11) | | 1 | see Table 8 | 0 | | Power-down DACx (selected by C2 and C1) |
| | | 1 | 0 | X | (00, 01, 10, or 11) | | 0 | Data | | | Write to TRx (selected by C2 & C1 w/ data and load all DACs) |
| | | 1 | 0 | X | (00, 01, 10, or 11) | | 1 | see Table 8 | 0 | | Power-down DACx (selected by C2 and C1) & load all DACs |
| Broadcast Modes (controls up to 4 devices on a single serial bus) | | | | | | | | | | | |
| X | X | 1 | 1 | X | 0 | X | X | X | | | Update all DACs, all devices with previously stored TRx data |
| X | X | 1 | 1 | X | 1 | X | 0 | Data | | | Update all DACs, all devices with MSB[7:0] and LSB[7:0] data |
| X | X | 1 | 1 | X | 1 | X | 1 | see Table 8 | 0 | | Power-down all DACs, all devices |

Most Significant Byte

Most significant byte MSB[7:0] consists of eight most significant bits of 10-bit unsigned binary D/A conversion data. If C0=1, MSB[7], MSB[6] indicate a power-down operation as shown in Table 8.

Least Significant Byte

Least significant byte LSB[7:0] consists of the 2 least significant bits of 10-bit unsigned binary D/A conversion data, followed by 6 *don't care* bits. DAC6574 updates at the falling edge of the acknowledge signal that follows the LSB[0] bit.

Default Readback Condition

If the user initiates a readback of a specified channel without first writing data to that specified channel, the default readback is all zeros, since the readback register is initialized to 0 during the power on reset phase.

DAC6574 Registers

Table 3. DAC6574 Architecture Register Descriptions

| REGISTER | DESCRIPTION |
|--|--|
| CTRL[7:0] | Stores 8-Bit wide control byte sent by the master |
| MSB[7:0] | Stores the 8 most significant bits of unsigned binary data sent by the master. Can also store 2-bit power-down data. |
| LSB[7:0] | Stores the 2 least significant bits of unsigned binary data sent by the master (in LSB[7] and LSB[6]). |
| TRA[11:0], TRB[11:0], TRC[11:0], TRD[11:0] | 12-bit temporary storage registers assigned to each channel. Two MSBs store power-down information, 10 LSBs store data. |
| DRA[11:0], DRB[11:0], DRC[11:0], DRD[11:0] | 12-bit DAC registers for each channel. Two MSBs store power-down information, 10 LSBs store DAC data. An update of this register means a DAC update with data or power-down. |

DAC6574 as a Slave Receiver - Standard and Fast Mode

Figure 33 shows the standard and fast mode master transmitter addressing a DAC6574 *Slave Receiver* with a 7-bit address.

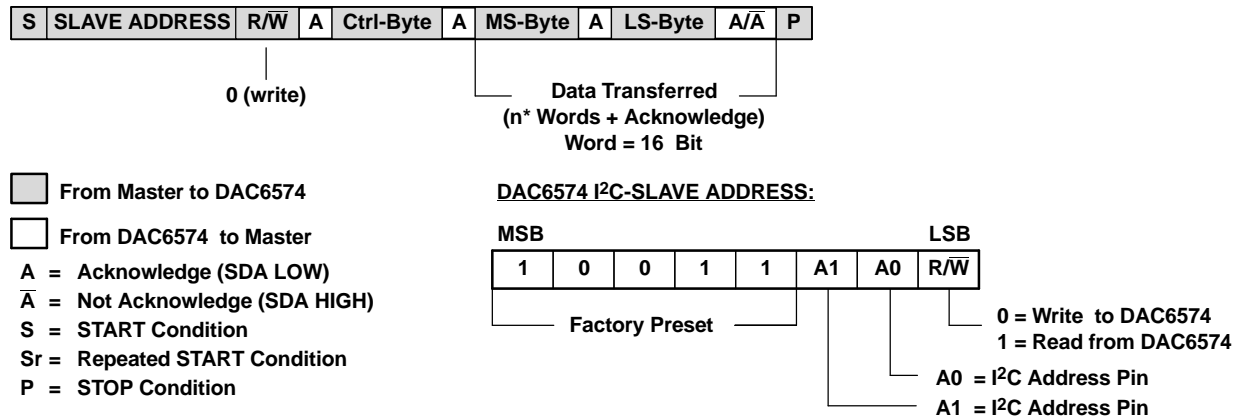


Figure 33. Standard and Fast Mode: Slave Receiver

DAC6574 as a Slave Receiver - High-Speed Mode

Figure 34 shows the high-speed mode master transmitter addressing a DAC6574 *Slave Receiver* with a 7-bit address.

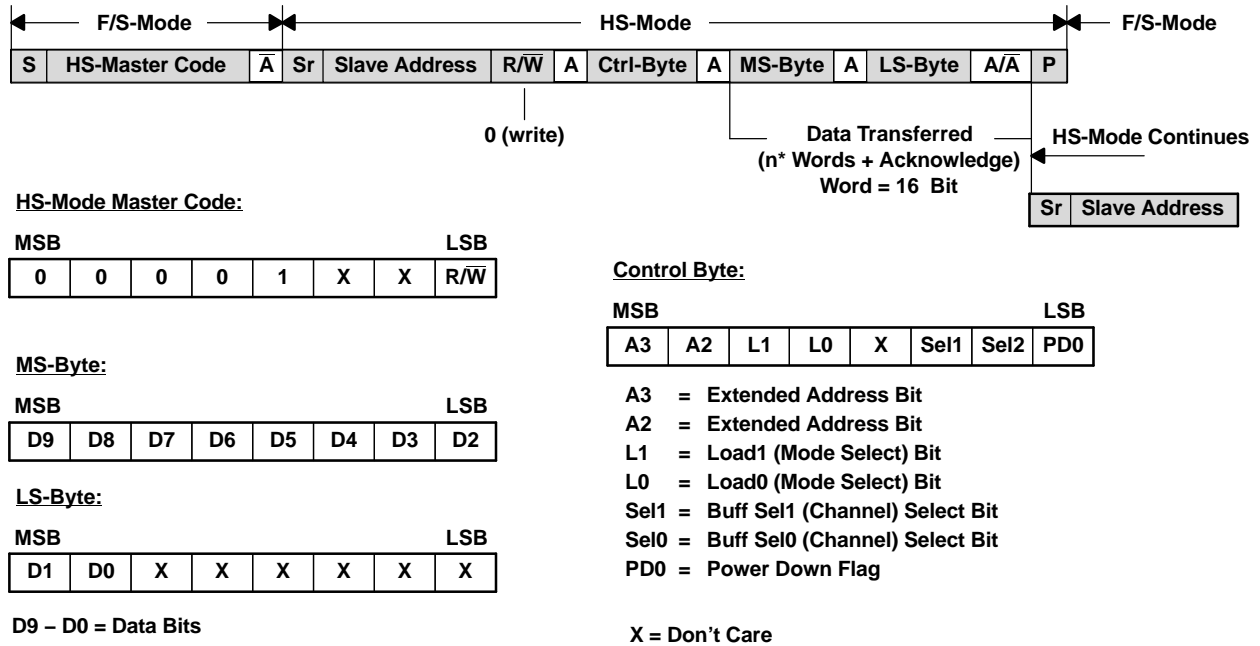


Figure 34. High-Speed Mode: Slave Receiver

Master Transmitter Writing to a Slave Receiver (DAC6574) in Standard/Fast Modes

All write access sequences begin with the device address (with $R/\overline{W} = 0$) followed by the control byte. This control byte specifies the operation mode of DAC6574 and determines which channel of DAC6574 is being accessed in the subsequent read/write operation. The LSB of the control byte (PD0-Bit) determines if the following data is power-down data or regular data.

With (PD0-Bit = 0) the DAC6574 expects to receive data in the following sequence *HIGH-BYTE –LOW-BYTE – HIGH-BYTE – LOW-BYTE...*, until a STOP Condition or REPEATED START Condition on the I²C-Bus is recognized (refer to the DATA INPUT MODE section of Table 4).

With (PD0-Bit = 1) the DAC6574 expects to receive 2 Bytes of power-down data (refer to the POWER DOWN MODE section of Table 4).

Table 4. Write Sequence in F/S Mode

| DATA INPUT MODE | | | | | | | | | |
|-----------------|---|-----|--------|--------|----|------------|------------|-------------------|---|
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/ \overline{W} | Write addressing (R/ \overline{W} =0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | x | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | Writing data word, high byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | D1 | D0 | x | x | x | x | x | x | Writing data word, low byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Data or Stop or Repeated Start ⁽¹⁾ | | | | | | | | Data or done ⁽²⁾ |
| POWER DOWN MODE | | | | | | | | | |
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/ \overline{W} | Write addressing (R/ \overline{W} =0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | x | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0 = 1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | PD1 | PD2 | 0 | 0 | 0 | 0 | 0 | 0 | Writing data word, high byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | x | x | x | x | x | x | Writing data word, low byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Stop or Repeated Start ⁽¹⁾ | | | | | | | | Done |

- (1) Use repeated START to secure bus operation and loop back to the stage of write addressing for next Write.
- (2) Once DAC6574 is properly addressed and control byte is sent, HIGH–BYTE–LOW–BYTE sequences can repeat until a STOP condition or repeated START condition is received.

Master Transmitter Writing to a Slave Receiver (DAC6574) in HS Mode

When writing data to the DAC6574 in HS-mode, the master begins to transmit what is called the *HS-Master Code* (0000 1XXX) in F/S-mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The master then *switches* to HS-mode and issues a *repeated start* condition, followed by the address byte (with R/W = 0) after which the DAC6574 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6574. The LSB of the control byte (PD0-Bit) determines if the following data is *power-down data* or regular data.

With (PD0-Bit = 0) the DAC6574 expects to receive data in the following sequence HIGH-BYTE – LOW-BYTE – HIGH-BYTE – LOW-BYTE..., until a STOP condition or *repeated start* condition on the I²C-Bus is recognized (refer to Table 5 HS-MODE WRITE SEQUENCE - DATA).

With (PD0-Bit = 1) the DAC6574 expects to receive 2 bytes of power-down data (refer to Table 5 HS-MODE WRITE SEQUENCE - POWER DOWN).

Table 5. Master Transmitter Writes to Slave Receiver (DAC6574) in HS-Mode

| HS MODE WRITE SEQUENCE - DATA | | | | | | | | | |
|-------------------------------------|---|-----|--------|--------|----|------------|------------|-----|--|
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 0 | 0 | 0 | 0 | 1 | X | X | X | HS Mode Master Code |
| NONE | Not Acknowledge | | | | | | | | No device may acknowledge HS master code |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/W | Write addressing (R/W=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | 0 | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | Writing data word, MSB |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | D1 | D0 | x | x | x | x | x | x | Writing data word, LSB |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Data or Stop or Repeated Start ⁽¹⁾ | | | | | | | | Data or done ⁽²⁾ |
| HS MODE WRITE SEQUENCE - POWER DOWN | | | | | | | | | |
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 0 | 0 | 0 | 0 | 1 | X | X | X | HS Mode Master Code |
| NONE | Not Acknowledge | | | | | | | | No device may acknowledge HS master code |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/W | Write addressing (R/W = 0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 2 | 0 | Buff Sel 1 | Buff Sel 0 | PD0 | Control Byte (PD0=1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | PD1 | PD2 | 0 | 0 | 0 | 0 | 0 | 0 | Writing data word, high byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | x | x | x | x | x | x | Writing data word, low byte |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Stop or repeated start ⁽¹⁾ | | | | | | | | Done |

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

(2) Once DAC6574 is properly addressed and control byte is sent, high-byte-low-byte sequences can repeat until a stop or repeated start condition is received.

DAC6574 as a Slave Transmitter—Standard and Fast Mode

Figure 35 shows the standard and fast mode master transmitter addressing a DAC6574 *Slave Transmitter* with a 7-bit address.

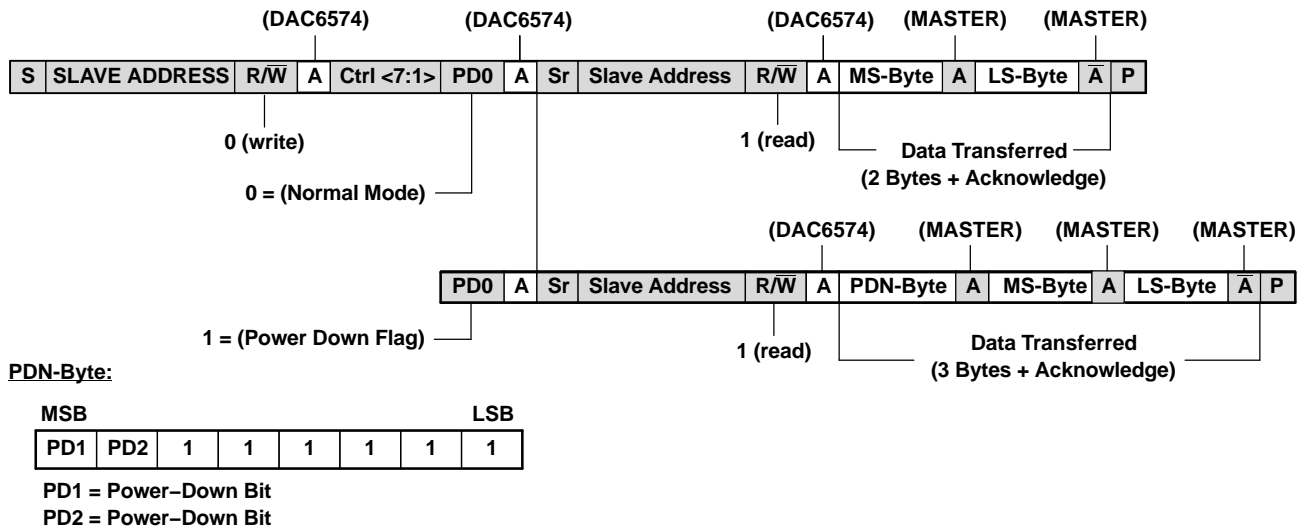


Figure 35. Standard and Fast Mode: Slave Transmitter

DAC6574 as a Slave Transmitter—High-Speed Mode

Figure 36 shows an I^2C -Master addressing DAC6574 in high-speed mode (with a 7-bit address), as a *Slave Transmitter*.

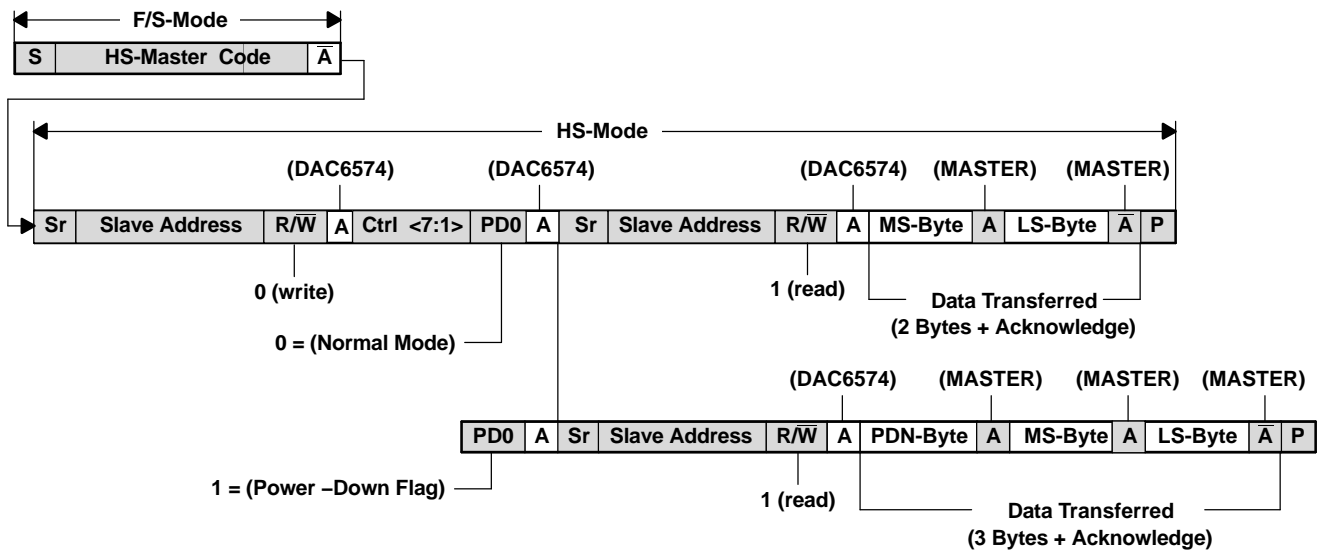


Figure 36. High-Speed Mode: Slave Transmitter

Master Receiver Reading From a Slave Transmitter (DAC6574) in Standard/Fast Modes

When reading data back from the DAC6574, the user begins with an address byte (with $R/\bar{W} = 0$) after which the DAC6574 will acknowledge by pulling SDA low. This address byte is usually followed by the Control Byte, which is also acknowledged by the DAC6574. Following this there is a REPEATED START condition by the Master and the address is resent with ($R/\bar{W} = 1$). This is acknowledged by the DAC6574, indicating that it is prepared to transmit data. Two or three bytes of data are then read back from the DAC6574, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP Condition follows.

With the (PD0-Bit = 0) the DAC6574 transmits 2 bytes of data, *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 2. Data Readback Mode - 2 bytes).

With the (PD0-Bit = 1) the DAC6574 transmits 3 bytes of data, *POWER-DOWN-BYTE* followed by the *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 2. Data Readback Mode - 3 bytes).

Table 6. Read Sequence in F/S Mode

| DATA READBACK MODE - 2 BYTES | | | | | | | | | |
|------------------------------|---------------------------------------|-----|--------|--------|----|------------|------------|-------------------------------|---|
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\bar{W} | Write addressing (R/\bar{W}=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | x | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\bar{W} | Read addressing (R/\bar{W} = 1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| DAC6574 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | Reading data word, high byte |
| Master | Master Acknowledges | | | | | | | | |
| DAC6574 | D1 | D0 | x | x | x | x | x | x | Reading data word, low byte |
| Master | Master Not Acknowledges | | | | | | | | Master signal end of read |
| Master | Stop or Repeated Start ⁽¹⁾ | | | | | | | | Done |
| DATA READBACK MODE - 3 BYTES | | | | | | | | | |
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\bar{W} | Write addressing (R/\bar{W}=0) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | x | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0=1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\bar{W} | Read addressing (R/\bar{W} = 1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| DAC6574 | PD1 | PD2 | 1 | 1 | 1 | 1 | 1 | 1 | Read power down byte |
| Master | Master Acknowledges | | | | | | | | |
| DAC6574 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | Reading data word, high byte |
| Master | Master Acknowledges | | | | | | | | |
| DAC6574 | D1 | D0 | x | x | x | x | x | x | Reading data word, low byte |
| Master | Master Not Acknowledges | | | | | | | | Master signal end of read |
| Master | Stop or Repeated Start ⁽¹⁾ | | | | | | | | Done |

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

Master Receiver Reading From a Slave Transmitter (DAC6574) in HS-Mode

When reading data to the DAC6574 in HS-MODE, the master begins to transmit, what is called the *HS-Master Code* (0000 1XXX) in F/S-mode. No device is allowed to acknowledge the *HS-Master Code*, so the *HS-Master Code* is followed by a NOT acknowledge.

The Master then *switches* to HS-mode and issues a REPEATED START condition, followed by the address byte (with $R/\overline{W} = 0$) after which the DAC6574 acknowledges by pulling SDA low. This address byte is usually followed by the control byte, which is also acknowledged by the DAC6574.

Then there is a REPEATED START condition initiated by the master and the address is resent with ($R/\overline{W} = 1$). This is acknowledged by the DAC6574, indicating that it is prepared to transmit data. Two or Three bytes of data are then read back from the DAC6574, depending on the (PD0-Bit). The value of *Buff-Sel1* and *Buff-Sel0* determines, which channel data is read back. A STOP condition follows.

With the (PD0-Bit = 0) the DAC6574 transmits 2 bytes of data, *HIGH-BYTE* followed by *LOW-BYTE* (refer to Table 7 HS-Mode Readback Sequence).

With the (PD0-Bit = 1) the DAC6574 transmits 3 bytes of data, *POWER-DOWN-BYTE* followed by the *HIGH-BYTE* followed by the *LOW-BYTE* (refer to Table 7 HS-Mode Readback Sequence).

Table 7. Master Receiver Reading Slave Transmitter (DAC6574) in HS-Mode

| HS MODE READBACK SEQUENCE | | | | | | | | | |
|---------------------------|-------------------------|-----|--------|--------|----|------------|------------|------------------|--|
| Transmitter | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | Comment |
| Master | Start | | | | | | | | Begin sequence |
| Master | 0 | 0 | 0 | 0 | 1 | X | X | X | HS Mode Master Code |
| NONE | Not Acknowledge | | | | | | | | No device may acknowledge HS master code |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\overline{W} | Write addressing ($R/\overline{W}=0$) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | 0 | 0 | Load 1 | Load 0 | X | Buff Sel 1 | Buff Sel 0 | PD0 | Control byte (PD0 = 1) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| Master | Repeated Start | | | | | | | | |
| Master | 1 | 0 | 0 | 1 | 1 | A1 | A0 | R/\overline{W} | Read addressing ($R/\overline{W}=1$) |
| DAC6574 | DAC6574 Acknowledges | | | | | | | | |
| DAC6574 | PD1 | PD2 | 1 | 1 | 1 | 1 | 1 | 1 | Power-down byte |
| Master | Master Acknowledges | | | | | | | | |
| DAC6574 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | Reading data word, high byte |
| Master | Master Acknowledges | | | | | | | | |
| DAC6574 | D1 | D0 | x | x | x | x | x | x | Reading data word, low byte |
| Master | Master Not Acknowledges | | | | | | | | Master signal end of read |
| Master | Stop or Repeated Start | | | | | | | | Done |

Power-On Reset

The DAC6574 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC register is filled with zeros and the output voltage is 0 V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. No device pin should be brought high before supply is applied.

Power-Down Modes

The DAC6574 contains four separate power-down modes of operation. The modes are programmable via two most significant bits of the MSB byte, while (CTRL[0] = PD0 = 1). Table 8 shows how the state of these bits correspond to the mode of operation of the device.

Table 8. Power-Down Modes of Operation for the DAC6574

| CTRL[0] | MSB[7] | MSB[6] | OPERATING MODE |
|---------|--------|--------|-----------------------|
| 1 | 0 | 0 | High Impedance Output |
| 1 | 0 | 1 | 1 kΩ to GND |
| 1 | 1 | 0 | 100 kΩ to GND |
| 1 | 1 | 1 | High Impedance |

When (CTRL[0] = PD0 = 0), the device works normally with its normal power consumption of 150 μA at 5 V per channel. However, for the power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but also the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or left open-circuit (high impedance). The output stage is illustrated in Figure 37.

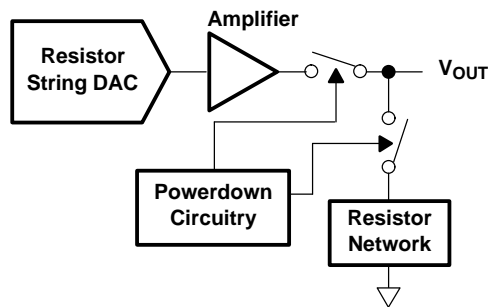


Figure 37. Output Stage During Power Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power down is typically 2.5 μs for $V_{DD} = 5$ V and 5 μs for $V_{DD} = 3$ V. (See the Typical Curves section for additional information.)

The DAC6574 offers a flexible power-down interface based on channel register operation. A channel consists of a single 10-bit DAC with power-down circuitry, a temporary storage register (TR) and a DAC register (DR). TR and DR are both 12 bits wide. Two MSBs represent the power-down condition and the 10 LSBs represent data for TR and DR. By using bits 11 and 10 of TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that MSB[7] and MSB[6] get transferred to TR[11] and TR[10] (DR[11] and DR[10]) when the power-down flag (CTRL[0] = PD0) is set. Therefore, DAC6574 treats power-down conditions like data and all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC6574s in the system, or it is possible to simultaneously power down a channel while updating data on other channels.

CURRENT CONSUMPTION

The DAC6574 typically consumes 150μA at $V_{DD} = 5$ V and 125μA at $V_{DD} = 3$ V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if $V_{IH} \ll V_{DD}$. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC6574 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC6574 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 kΩ can be driven by the DAC6574 while achieving a good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic.

CROSSTALK

The DAC6574 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.01 LSBs. The ac crosstalk measured (for a full-scale, 1 kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under -100 dB.

OUTPUT VOLTAGE STABILITY

The DAC6574 exhibits excellent temperature stability of ± 3 ppm/ $^{\circ}\text{C}$ typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ± 25 μV window for a $\pm 1^{\circ}\text{C}$ ambient temperature change. Combined with good dc noise performance and true 10-bit differential linearity, the DAC6574 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

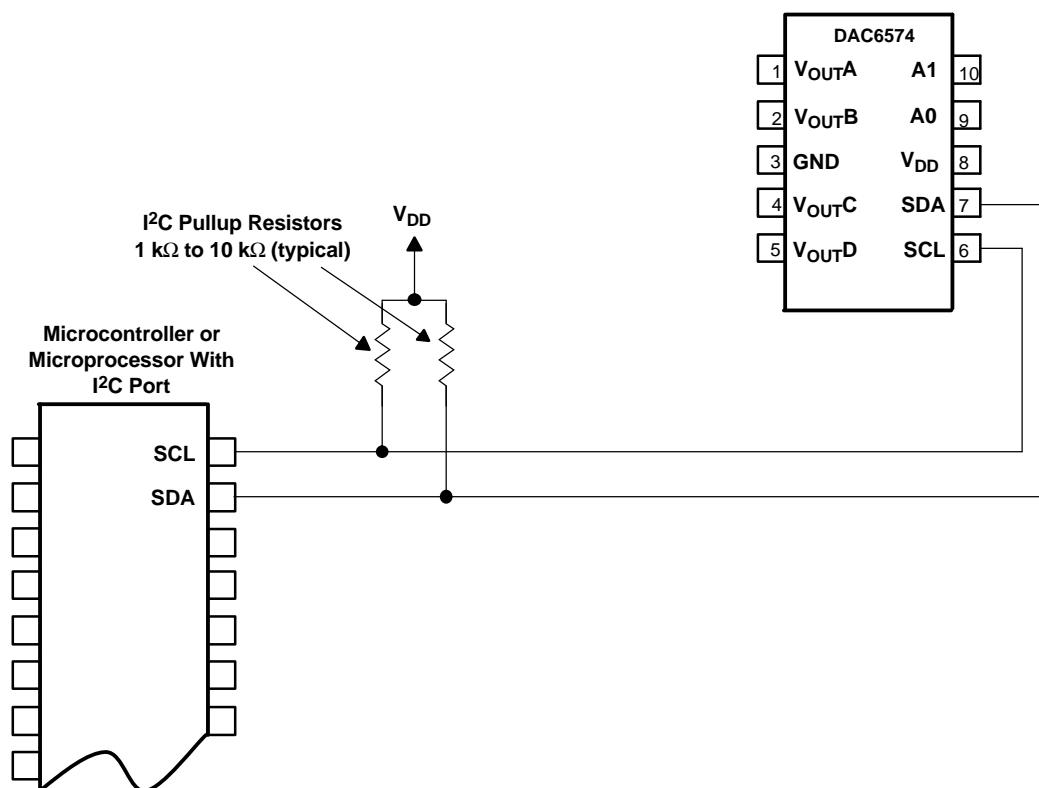
Settling time to within the 10-bit accurate range of the DAC6574 is achievable within 7 μs for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2 μs . The high-speed serial interface of the DAC6574 is designed in order to support up to 188 kSPS update rate. For full-scale output swings, the output stage of each DAC6574 channel typically exhibits less than 100 mV of overshoot and undershoot when driving a 200 pF capacitive load. Code-to-code change glitches are extremely low (~ 10 μV) given that the code-to-code transition does not cross an Nx64 code boundary. Due to internal segmentation of the DAC6574, code-to-code glitches occur at each crossing of an Nx64 code boundary. These glitches can approach 100 mVs for $N = 15$, but settle out within ~ 2 μs . Sufficient bypass capacitance is required to ensure 7 μs settling under capacitive loading. To observe the settling performance under resistive load conditions, the power supply (hence DAC6574 reference supply) must settle quicker than the DAC6574.

APPLICATION INFORMATION

The following sections give example circuits and tips for using the DAC6574 in various applications. For more information, contact your local TI representative, or visit the Texas Instruments website at <http://www.ti.com>.

BASIC CONNECTIONS

For many applications, connecting the DAC6574 is extremely simple. A basic connection diagram for the DAC6574 is shown in Figure 38. The 0.1 μF bypass capacitors help provide the momentary bursts of extra current needed from the supplies.



NOTE: DAC6574 power and input/output connections are omitted for clarity, except I²C Inputs.

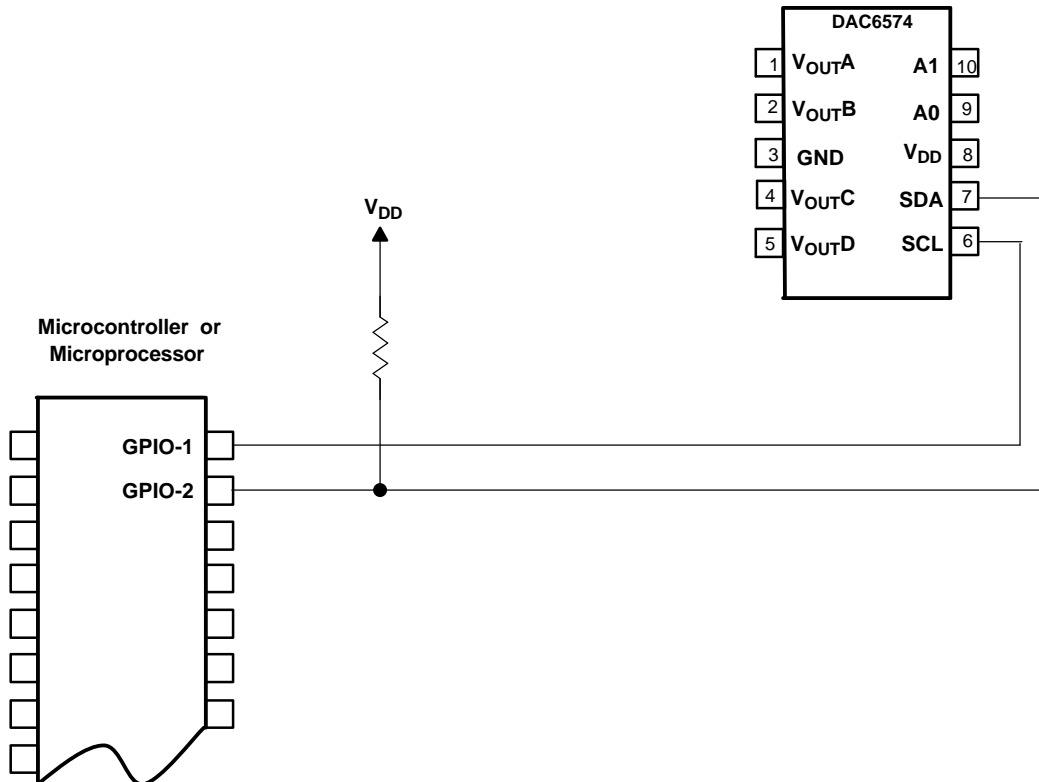
Figure 38. Typical DAC6574 Connections

The DAC6574 interfaces directly to standard mode, fast mode and high-speed mode I²C controllers. Any microcontroller's I²C peripheral, including master-only and non-multiple-master I²C peripherals, work with the DAC6574. The DAC6574 does not perform clock-stretching (i.e., it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I²C bus.

Pullup resistors are necessary on both the SDA and SCL lines because I²C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance on the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. If the pullup resistors are too small the bus drivers may not be able to pull the bus line low.

USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the DAC6574 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single DAC6574 is shown in Figure 39.

APPLICATION INFORMATION (continued)

NOTE: DAC6574 power and input/output connections are omitted for clarity, except I²C inputs.

Figure 39. Using GPIO With a Single DAC6574

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a zero; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this reads as a zero in the port's input register.

Note that no pullup resistor is shown on the SCL line. In this simple case the resistor is not needed. The microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the DAC6574 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pullup.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used. The SCL line should be high-Z or zero, and a pullup resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the DAC6574 drives the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pullup circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pullup resistor. Weak pullups are also provided on some microcontrollers, but usually these are too weak for I²C communication. Test any circuit before committing it to production.

POWER SUPPLY REJECTION

The positive reference voltage input of DAC6574 is internally tied to the power supply pin of the device. This increases I²C system flexibility, creating room for an extra I²C address pin in a low pin-count package. To eliminate the supply noise appearing at the DAC output, the user must pay close attention to how DAC6574 is powered. The supply to DAC6574 must be clean and well regulated. For best performance, use of a precision voltage reference is recommended to supply power to DAC6574. This is equivalent to providing a precision

APPLICATION INFORMATION (continued)

external reference to the device. Due to low power consumption of DAC6574, load regulation errors are negligible. In order to avoid excess power consumption at the Schmitt-triggered inputs of DAC6574, the precision reference voltage should be close to the I²C bus pullup voltage. For 3-V, 3.3-V and 5-V I²C bus pullup voltages, REF2930, REF2933 and REF02 precision voltage references are recommended respectively. These precision voltage references can be used to supply power for multiple devices on a system.

USING REF02 AS A POWER SUPPLY FOR DAC6574

Due to the extremely low supply current required by the DAC6574, a possible configuration is to use a REF02 +5 V precision voltage reference to supply the required voltage to the DAC6574 supply input as well as the reference input, as shown in Figure 40. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC6574. If the REF02 is used, the current it needs to supply to the DAC6574 is 600 μ A typical and 900 μ A max for $V_{DD} = 5$ V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5-k Ω load on a single DAC output) is:

$$600 \mu\text{A} + (5 \text{ V} / 5 \text{ k}\Omega) = 1.6 \text{ mA}$$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 400 μ V for 1.6 mA of current drawn from it. This corresponds to a 0.08 LSB error for a 0-V to 5-V output range.

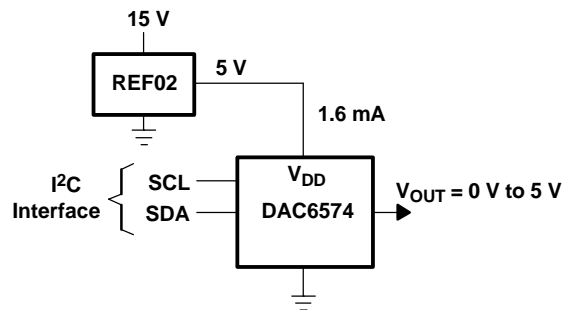


Figure 40. REF02 Power Supply

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

For best performance, the power applied to V_{DD} must be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} must be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1- μ F to 10- μ F capacitor in parallel with a 0.1- μ F bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5-V supply, removing the high-frequency noise.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| DAC6574IDGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | D674 | Samples |
| DAC6574IDGSG4 | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | D674 | Samples |
| DAC6574IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | D674 | Samples |
| DAC6574IDGSRG4 | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | D674 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC6574IDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

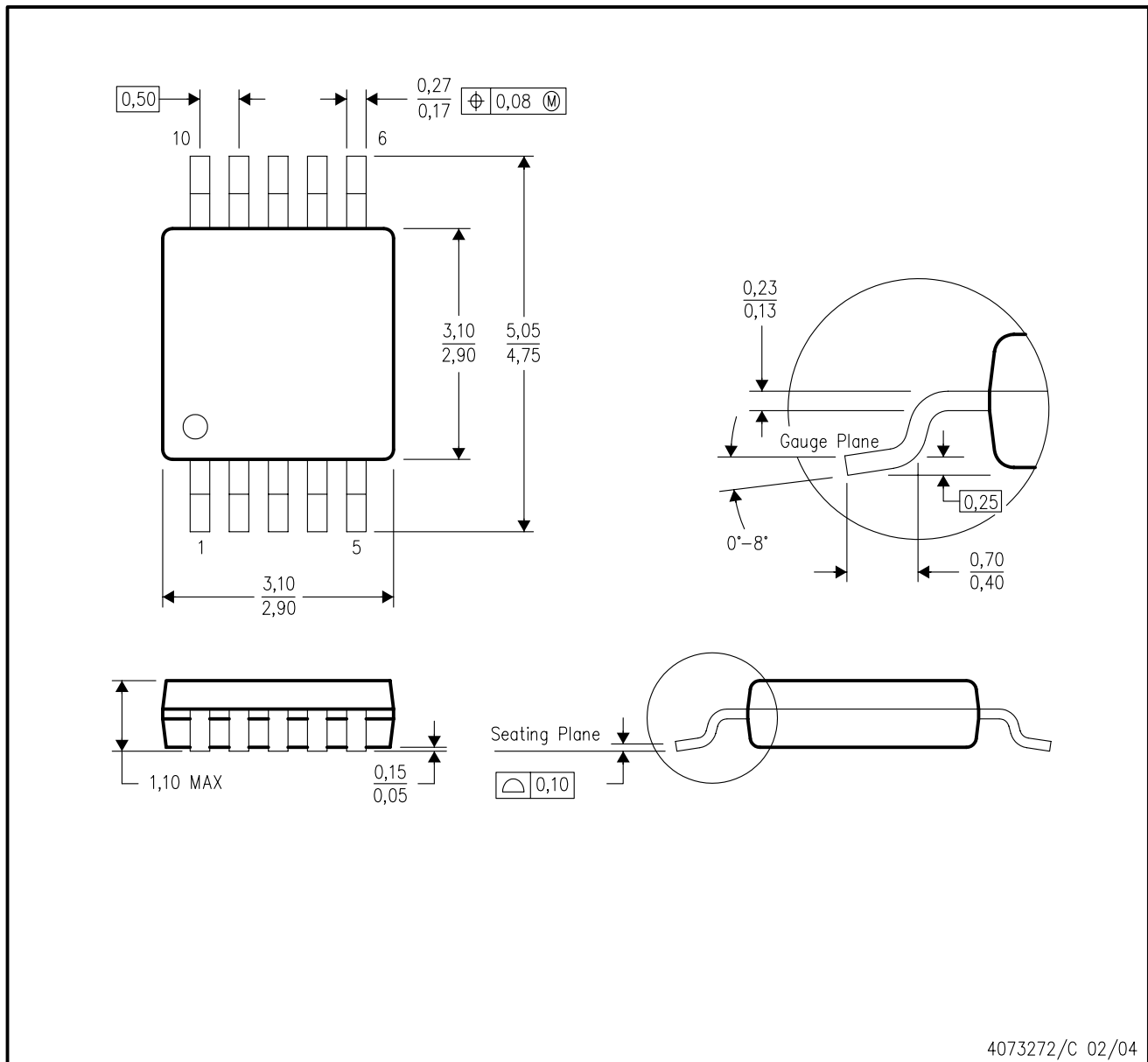


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC6574IDGSR | VSSOP | DGS | 10 | 2500 | 367.0 | 367.0 | 35.0 |

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com