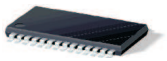


Typical Size
6.4 mm x 9.7 mm

34 V, Digital-Input Serializer for 5V Systems

FEATURES

- **Eight Digital Sensor Inputs**
  - **High Input Voltage up to 34 V**
  - **Selectable Debounce Filters From 0 ms to 3 ms**
  - **Flexible Input Current-Limited – 0.2 mA to 5.2 mA**
  - **Field Inputs Protected to 15-kV ESD**
- **Single 5V Supply**
- **Output Drivers for External Status LEDs**
- **Cascadable for More Inputs in Multiples of Eight**
- **SPI-Compatible Interface**
- **Over-Temperature Indicator**

APPLICATIONS

- **Industrial PCs**
- **Digital I/O Cards**
- **High Channel Count Digital Input Modules**
- **Decentralized I/O Modules**

DESCRIPTION

The SN65HVS885 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial and building automation. Operating from a 5V supply the device accepts field input voltages of up to 34V. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Inputs signals are current limited and then validated by internal debounce filters.

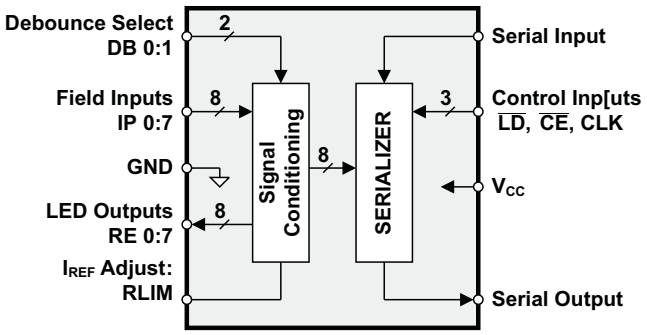
With the addition of few external components, the input switching characteristic can be configured in accordance with IEC61131-2 for Type 1, 2 and 3 sensor switches.

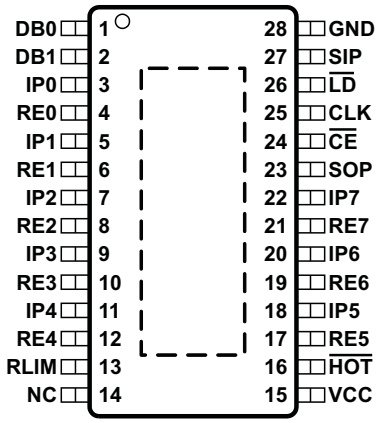
Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially.

Cascading of multiple devices is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Multiple devices can be cascaded through a single serial port, reducing both the isolation channels and controller inputs required.

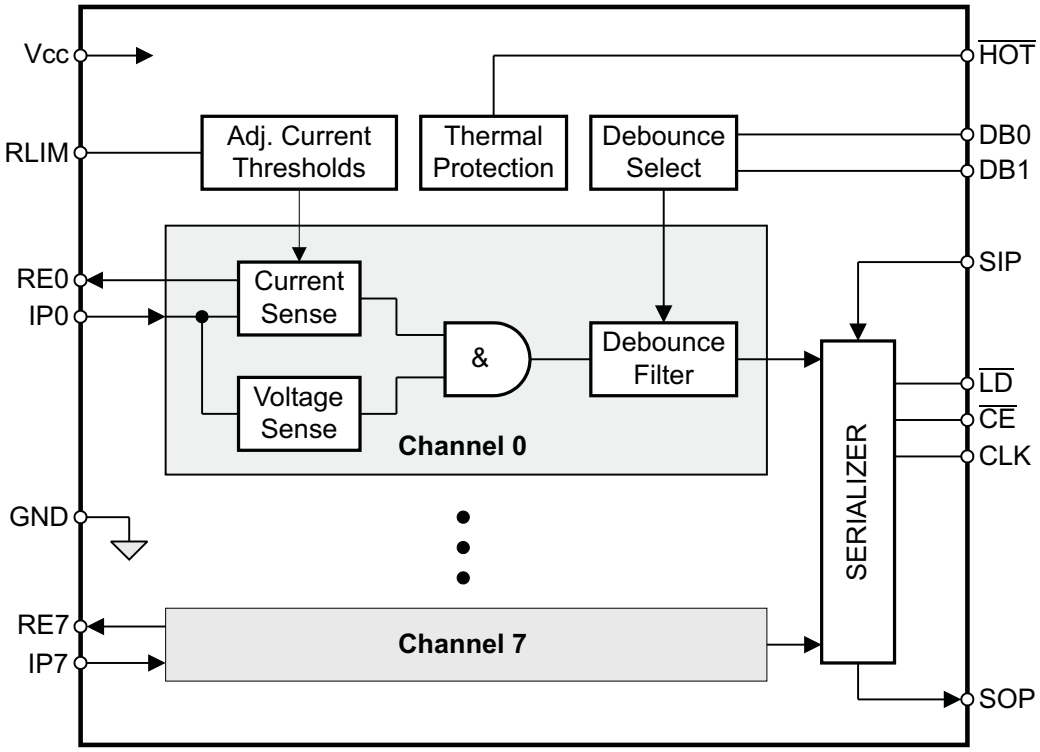
Input status can be visually indicated via constant current LED outputs. The current limit on the inputs is set by a single, external, precision resistor. An on-chip temperature sensor provides diagnostic information for graceful shutdown and system safety.

The SN65HVS885 is available in a 28-pin PWP PowerPAD™ package, allowing for efficient heat dissipation. The device is specified for operation at temperatures from –40°C to 125°C.





FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
PIN NO.	NAME	
1, 2	DB0, DB1	Debounce select inputs
3, 5, 7, 9, 11, 18, 20, 22	IPx	Input Channel x
4, 6, 8, 10, 12, 17, 19, 21	REx	Return Path x (LED drive)
13	RLIM	Current Limiting Resistor
14	NC	Not Connected
15	V_{CC}	5 V Device Supply
16	$\overline{HOT}$	Over-Temperature Flag
23	SOP	Serial Data Output
24	$\overline{CE}$	Clock Enable Input
25	CLK	Serial Clock Input
26	$\overline{LD}$	Load Pulse Input
27	SIP	Serial Data Input
28	GND	Device Ground

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

				VALUE	UNIT
V_{CC}	Device power input		V_{CC}	–0.5 to 6	V
V_{IPx}	Field digital inputs		IPx	–0.3 to 36	V
V_{ID}	Voltage at any logic input		DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$	–0.5 to 6	V
I_O	Output current		$\overline{HOT}$, SOP	±8	mA
V_{ESD}	Electrostatic discharge	Human-Body Model(2)	All pins	±4	kV
			IPx	±15	
		Charged-Device Model(3)	All pins	±1	kV
		Machine Model(4)	All pins	±100	V
P_{TOT}	Continuous total power dissipation		See Thermal Characteristics table		
T_J	Junction temperature			170	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) JEDEC Standard 22, Method A114-A.
(3) JEDEC Standard 22, Method C101
(4) JEDEC Standard 22, Method A115-A

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	High-K thermal resistance			35		°C/W
θ_{JB}	Junction-to-board thermal resistance				15		°C/W
θ_{JC}	Junction-to-case thermal resistance				4.27		°C/W
P_D	Device power dissipation	V_{CC} = 5 V, R_{IN} = 0Ω, R_{LIM} = 25 kΩ, RE0 – RE7 = GND, f_{CLK} = 100 MHz	IP0-IP7 = 34V			1100	mW
			IP0-IP7 = 30V				
			IP0-IP7 = 24V				
			IP0-IP7 = 12V				

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Device supply voltage	4.5	5	5.5	V
V_{IPL}	Field input low-state input voltage	0		4	V
V_{IPH}	Field input high-state input voltage	5.5		34	V
V_{IL}	Logic low-state input voltage	0		0.8	V
V_{IH}	Logic high-state input voltage	2.0		5.5	V
R_{LIM}	Current limiter resistor	17	25	500	kΩ
f_{IP}(1)	Input data rate	0		1	Mbps
T_A	Device	–40		125	°C
T_J				150	°C

(1) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = GND), and R_{IN} = 0 Ω

ELECTRICAL CHARACTERISTICS

over full-range of recommended operating conditions (unless otherwise noted)
all voltages measured against device ground, see Figure 9

PARAMETER		TERMINAL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FIELD INPUTS							
$V_{TH-(IP)}$	Low-level device input threshold voltage	IP0–IP7	R_{LIM} = 25 kΩ	4.0	4.3		V
$V_{TH+(IP)}$	High-level device input threshold voltage				5.2	5.5	V
$V_{HYS(IP)}$	Device input hysteresis				0.9		V
$V_{TH-(IN)}$	Low-level field input threshold voltage	measured at field side of R_{IN}	4.5 V < V_{CC} < 5.5 V, R_{IN} = 1.2 kΩ ± 5%, R_{LIM} = 25 kΩ, T_A ≤ 125°C	6	8.4		V
$V_{TH+(IN)}$	High-level field input threshold voltage				9.4	10	V
$V_{HYS(IN)}$	Field input hysteresis				1		V
R_{IP}	Input resistance	IP0–IP7	3 V < V_{IPx} < 6 V, R_{LIM} = 25 kΩ	0.2	0.63	1.1	kΩ
I_{IP-LIM}	Input current limit	IP0–IP7	R_{LIM} = 25 kΩ	3.15	3.6	4	mA
t_{DB}	Debounce times of input channels	IP0–IP7	DB0 = open, DB1 = GND		0		ms
			DB0 = GND, DB1 = open		1		
			DB0 = DB1 = open		3		
I_{RE-on}	RE on-state current	RE0–RE7	R_{LIM} = 25 kΩ, RE_X = GND	2.8	3.15	3.5	mA
DEVICE SUPPLY							
$I_{CC(VCC)}$	Supply current	V_{CC}	IP0 to IP7 = 24V, RE_X = GND, All logic inputs open		6.5	10	mA
LOGIC INPUTS AND OUTPUTS							
V_{OL}	Logic low-level output voltage	SOP, $\overline{HOT}$	I_{OL} = 20 µA			0.4	V
V_{OH}	Logic high-level output voltage		I_{OH} = –20 µA	4			V
I_{IL}	Logic input leakage current	DB0, DB1, SIP, $\overline{LD}$, $\overline{CE}$, CLK		–50		50	µA
T_{OVER}	Over-temperature indication				150		°C
T_{SHDN}	Shutdown temperature				170		°C

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{W1}	CLK pulse width	See Figure 6	4			ns
t_{W2}	$\overline{LD}$ pulse width	See Figure 4	6			ns
t_{SU1}	SIP to CLK setup time	See Figure 7	4			ns
t_{H1}	SIP to CLK hold time	See Figure 7	2			ns
t_{SU2}	Falling edge to rising edge ($\overline{CE}$ to CLK) setup time	See Figure 8	4			ns
t_{REC}	$\overline{LD}$ to CLK recovery time	See Figure 5	2			ns
f_{CLK}	Clock pulse frequency	See Figure 6	DC		100	MHz

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}, t_{PHL1}	CLK to SOP	C_L = 15 pF, see Figure 6			10	ns
t_{PLH2}, t_{PHL2}	$\overline{LD}$ to SOP	C_L = 15 pF, see Figure 4			14	ns
t_r, t_f	Rise and fall times	C_L = 15 pF, see Figure 6			6	ns

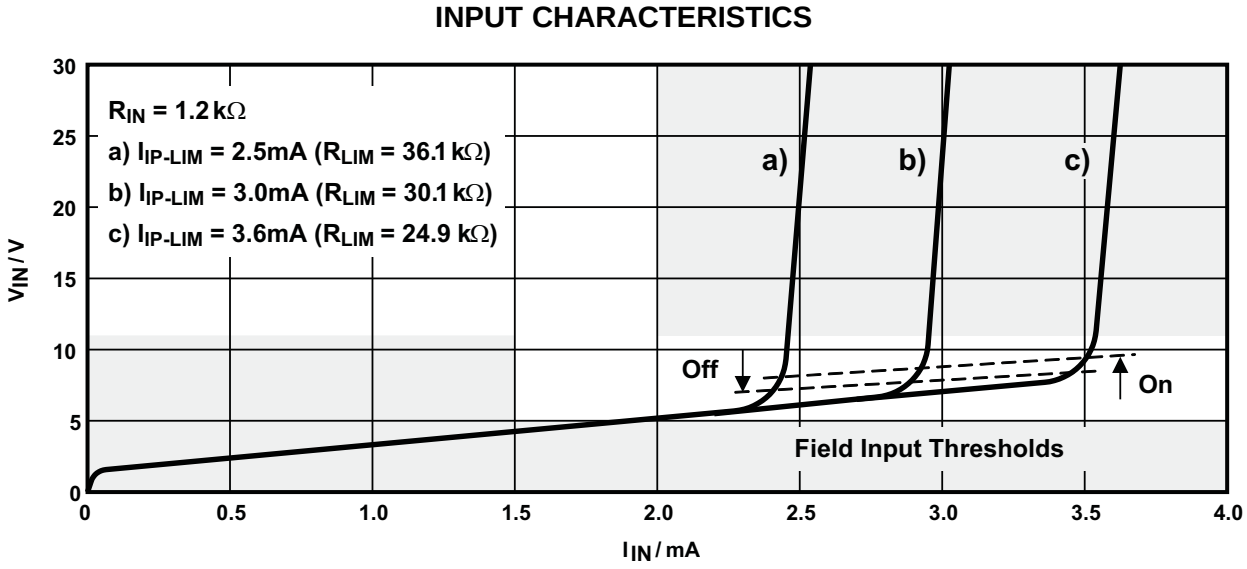


Figure 1. Typical Input Characteristics

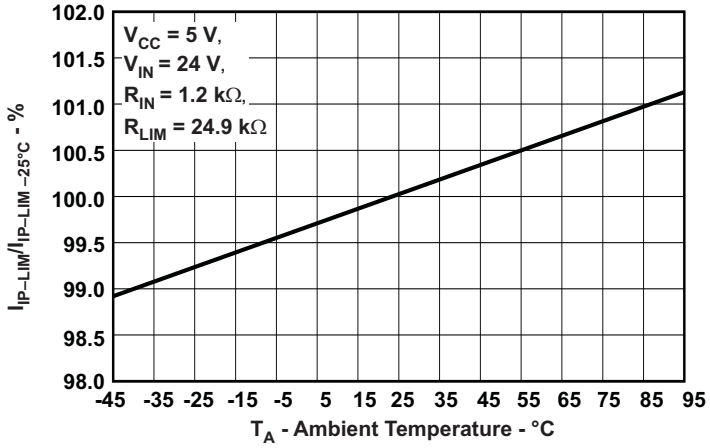


Figure 2. Typical Current Limiter Variation vs Ambient Temperature

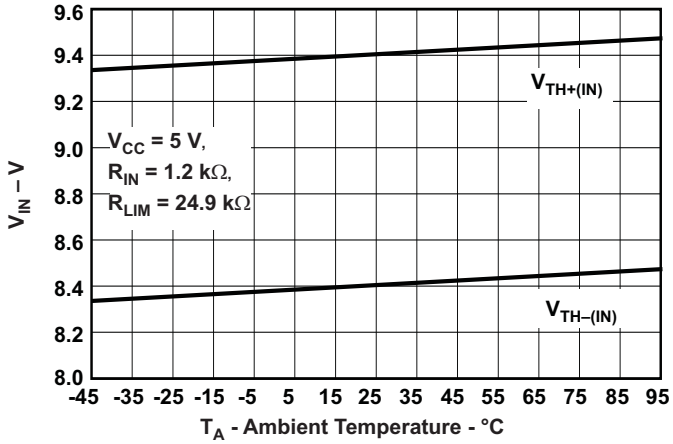


Figure 3. Typical Limiter Threshold Voltage Variation vs Ambient Temperature

PARAMETER MEASUREMENT INFORMATION

Waveforms

For the complete serial interface timing, refer to Figure 17.

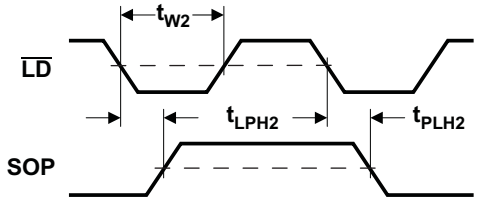


Figure 4. Parallel – Load Mode

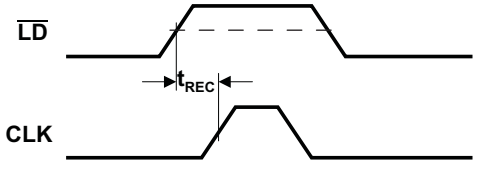


Figure 5. Serial – Shift Mode

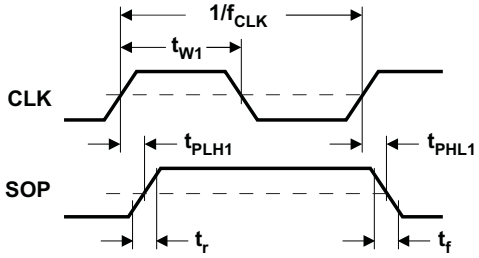


Figure 6. Serial – Shift Mode

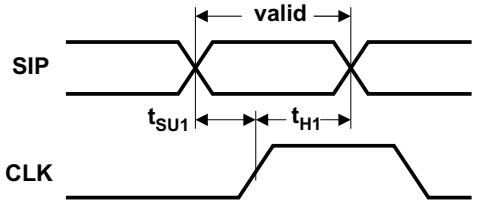


Figure 7. Serial – Shift Mode

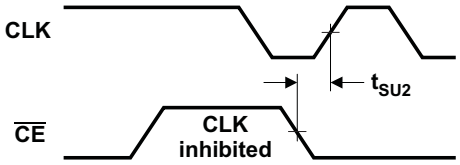


Figure 8. Serial – Shift Clock Inhibit Mode

Signal Conventions

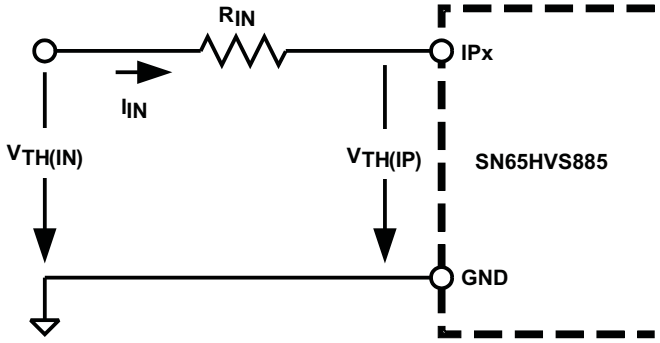


Figure 9. On/Off Threshold Voltage Measurements

DEVICE INFORMATION

Digital Inputs

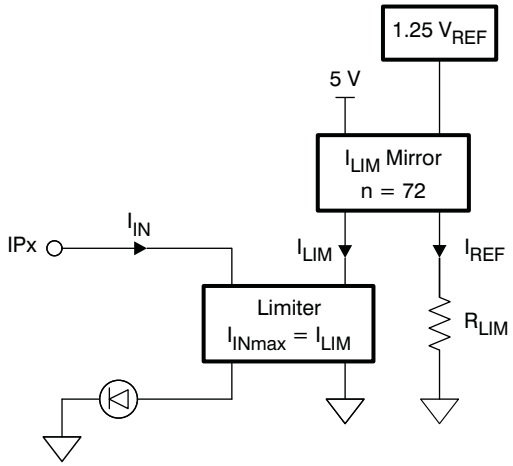


Figure 10. Digital Input Stage

Each digital input operates as a controlled current sink limiting the input current to a maximum value of I_{LIM}. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and I_{REF} is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of R_{LIM} to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

Inserting the actual values for n and V_{REF} gives: $R_{LIM} = 90\ V / I_{LIM}$.

While the device is specified for a current limit of **3.6 mA**, (via R_{LIM} = 25 kΩ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of **2.5 mA** simply calculate:

$$R_{LIM} = \frac{90\ V}{I_{LIM}} = \frac{90\ V}{2.5\ mA} = 36\ k\Omega$$

Debounce Filter

The HVS885 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

Table 1. Debounce Times

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (Filter bypassed)
GND	GND	Reserved

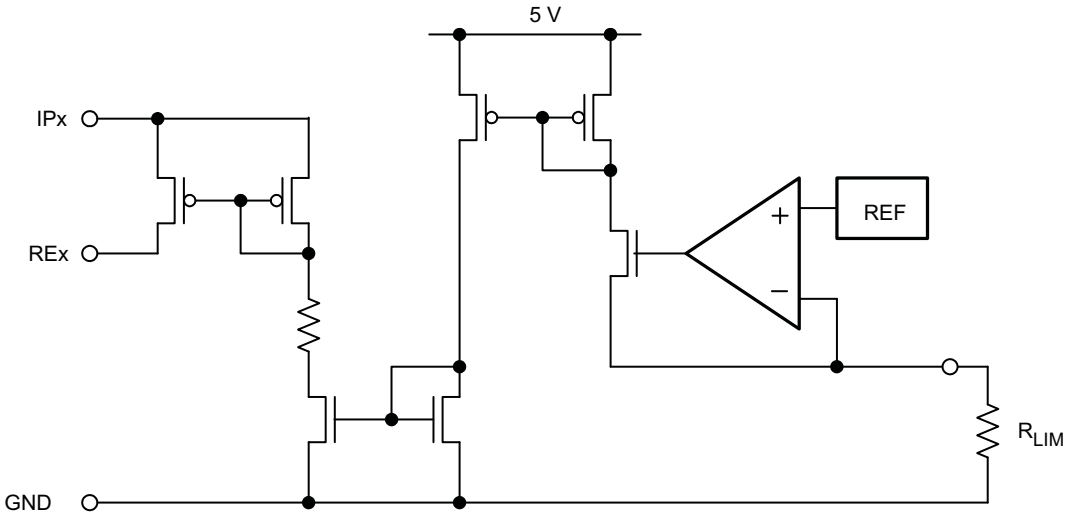


Figure 11. Equivalent Input Diagram

Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel, parallel-in serial-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low. Parallel loading is inhibited when $\overline{LD}$ is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

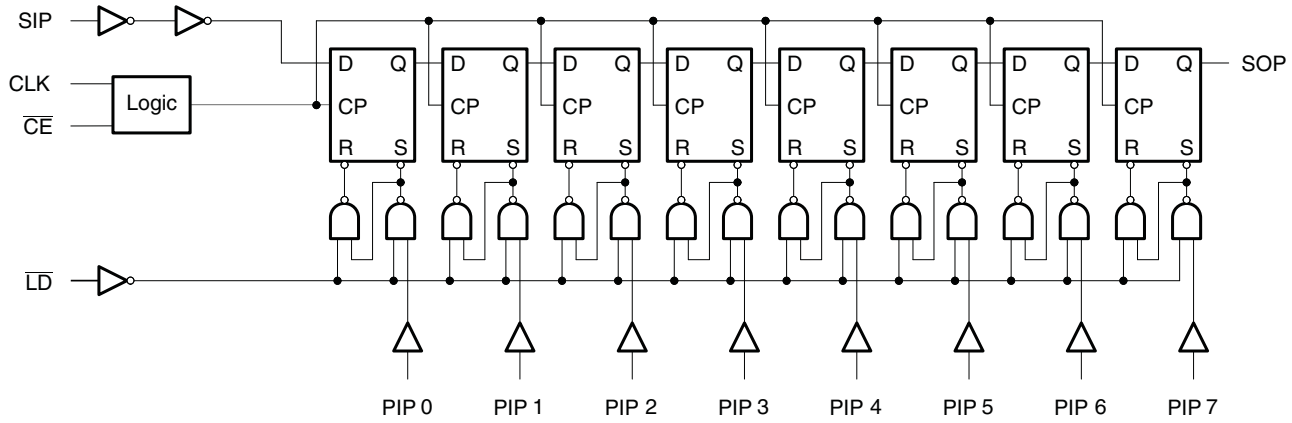


Figure 12. Shift Register Logic Structure

Table 2. Function Table

INPUTS			FUNCTION
$\overline{LD}$	CLK	$\overline{CE}$	
L	X	X	Parallel load
H	X	H	No change
H	↑	L	Shift (1)

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the temperature exceeds a first trip point at 150°C by pulling the $\overline{HOT}$ output low. If the junction temperature continues to rise, passing a second trip point at 170 °C, all device outputs assume high impedance state.

A special condition occurs when the chip temperature exceeds the second temperature trip point due to an output short; the $\overline{HOT}$ output buffer becomes high impedance, thus separating the buffer from the external circuitry. An internal 100-kΩ pulldown resistor, connecting the $\overline{HOT}$-pin to ground, is used as a "cooling down" resistor, which continues to provide a logic low level to the external circuitry.

APPLICATION INFORMATION

System-Level EMC

The SN65HVS885 is designed to operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards.

In addition to the device internal ESD structures, external protection circuitry shown in Figure 13, can be used to absorb as much energy from burst- and surge-transients as possible.

R_{IN}	1.2 kΩ, 1/4 W MELF Resistor
C_{IN}	220 nF, 60 V Ceramic Capacitor
C_S	4.7 nF, 2 kV Ceramic Capacitor

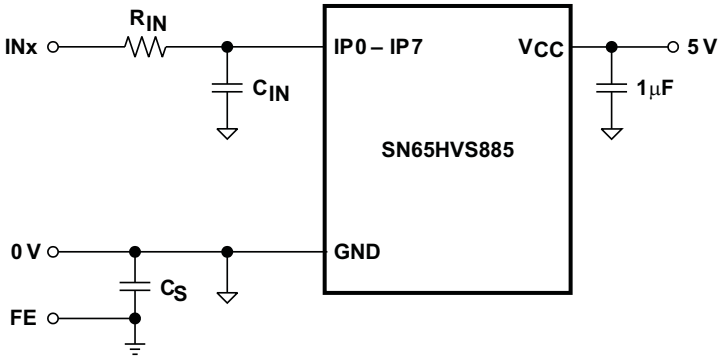


Figure 13. Typical EMC Protection Circuitry for Supply and Signal Inputs

Input Channel Switching Characteristics

The input stage of the HVS885 is so designed, that for an input resistor R_{IN} = 1.2 kΩ the trip point for signaling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 Type 1 and Type 3 switches.

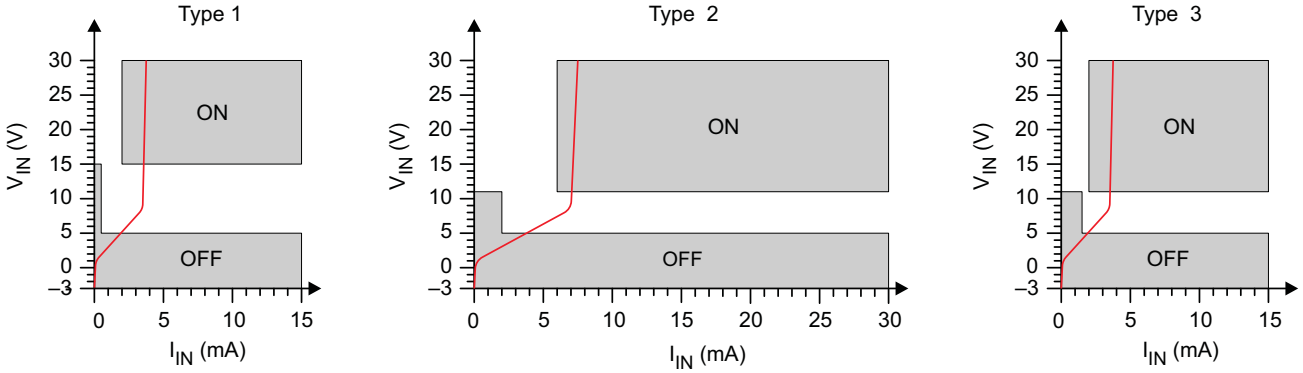


Figure 14. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches

For a Type 2 switch application, two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (GND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

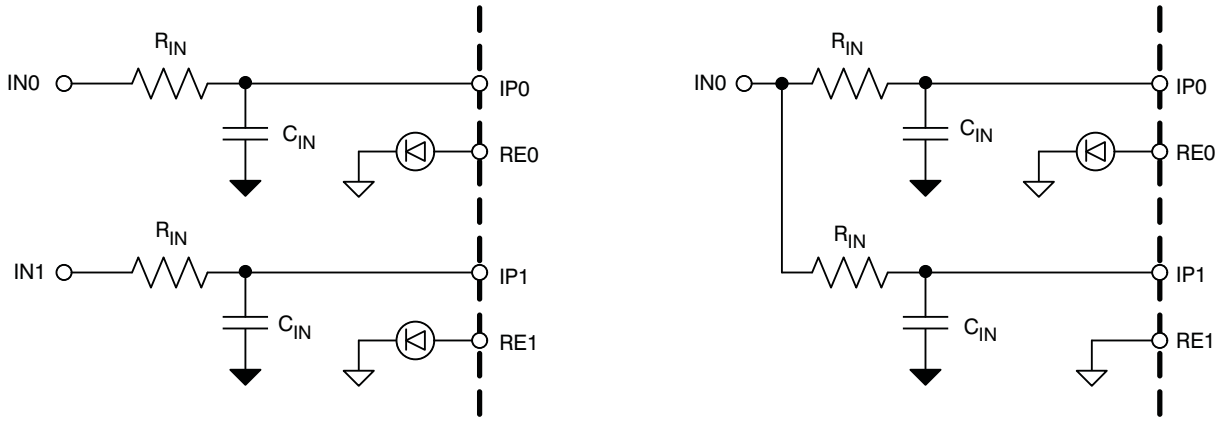


Figure 15. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input

Digital Interface Timing

The digital interface of the SN65HVS885 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard micro controllers.

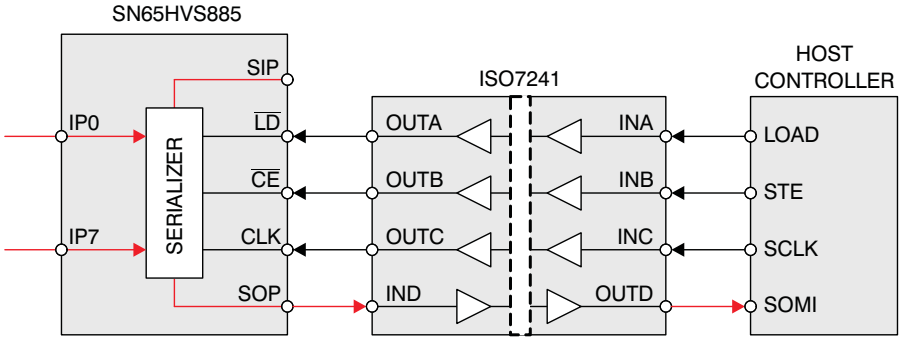


Figure 16. Simple Isolation of the Shift Register Interface

Upon a low-level at the load input, $\overline{LD}$, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking /LD high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

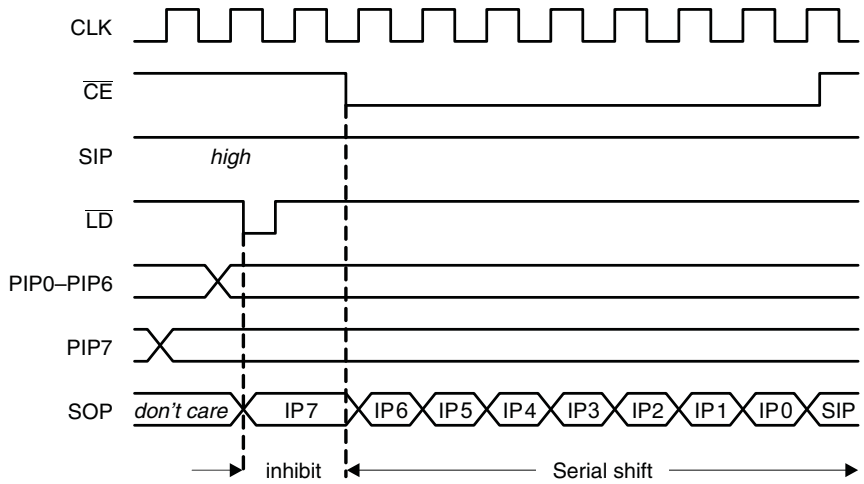


Figure 17. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register

Cascading for High Channel Count Input Modules

Designing high-channel count modules require cascading multiple SN65HVS885 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

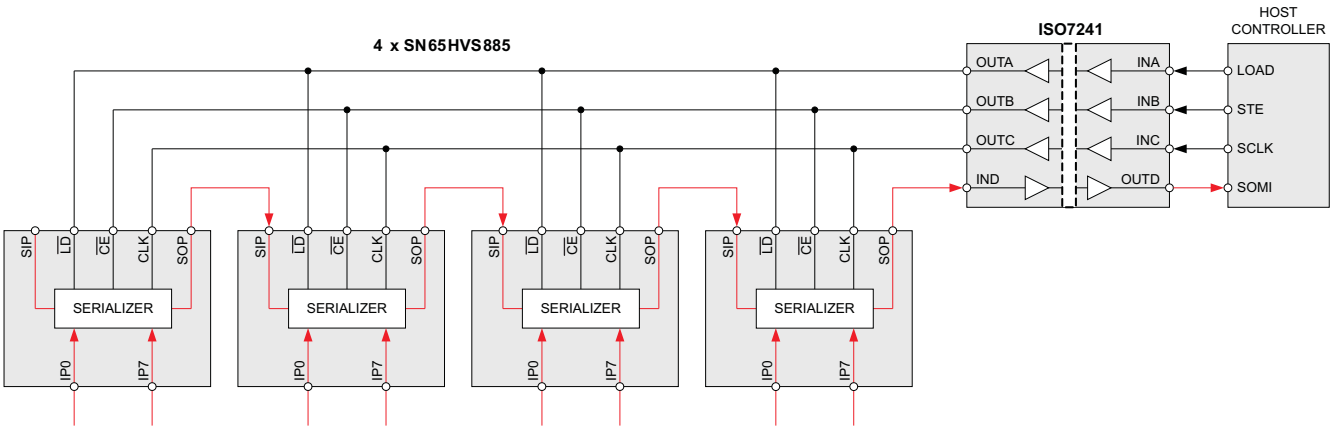


Figure 18. Cascading Four SN65HVS885 for a 32-Channel Input Module

Typical Digital Input Module Application

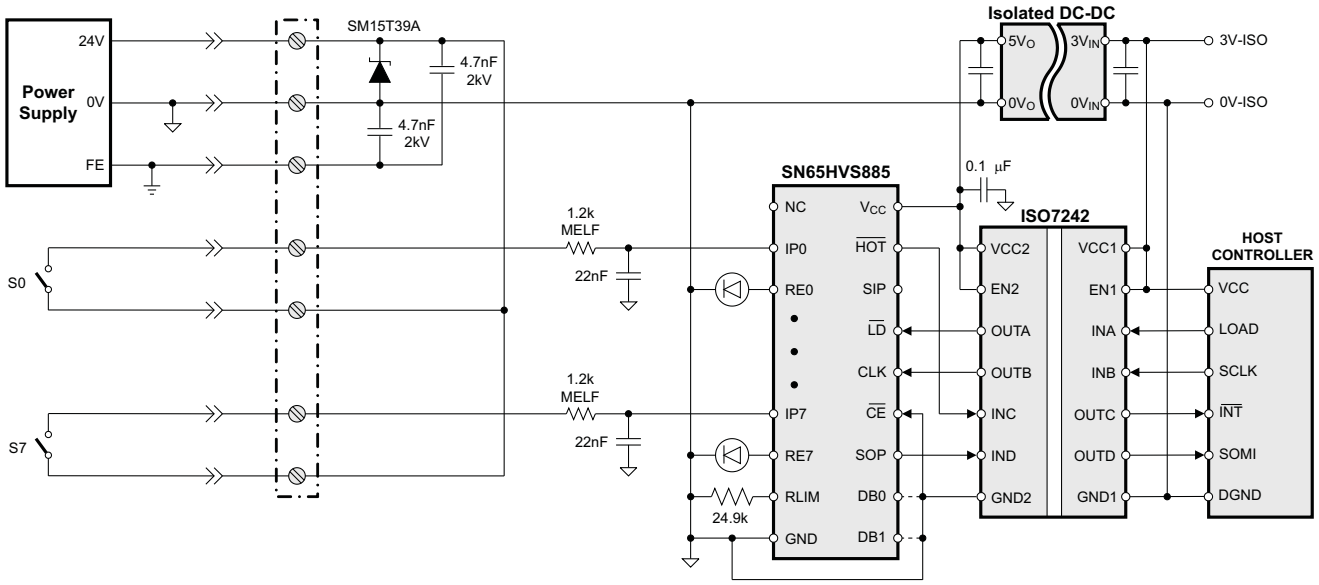


Figure 19. Typical Digital Input Module Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVS885PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS885	Samples
SN65HVS885PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS885	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

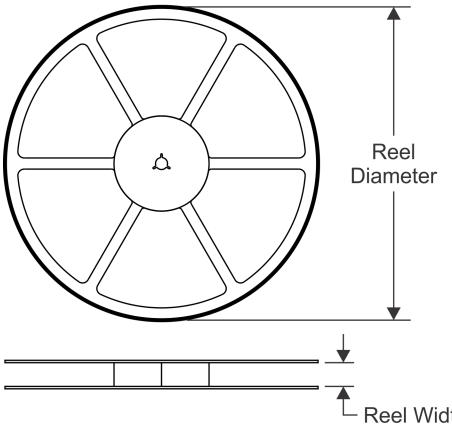
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

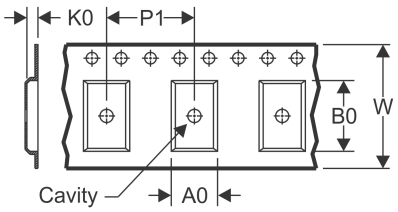
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

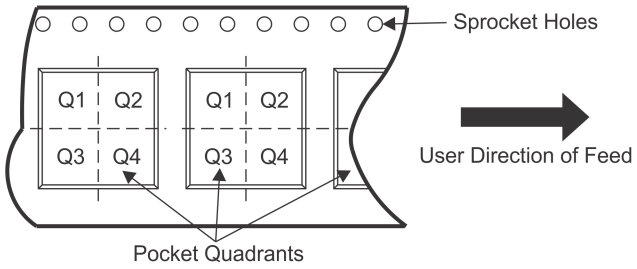


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

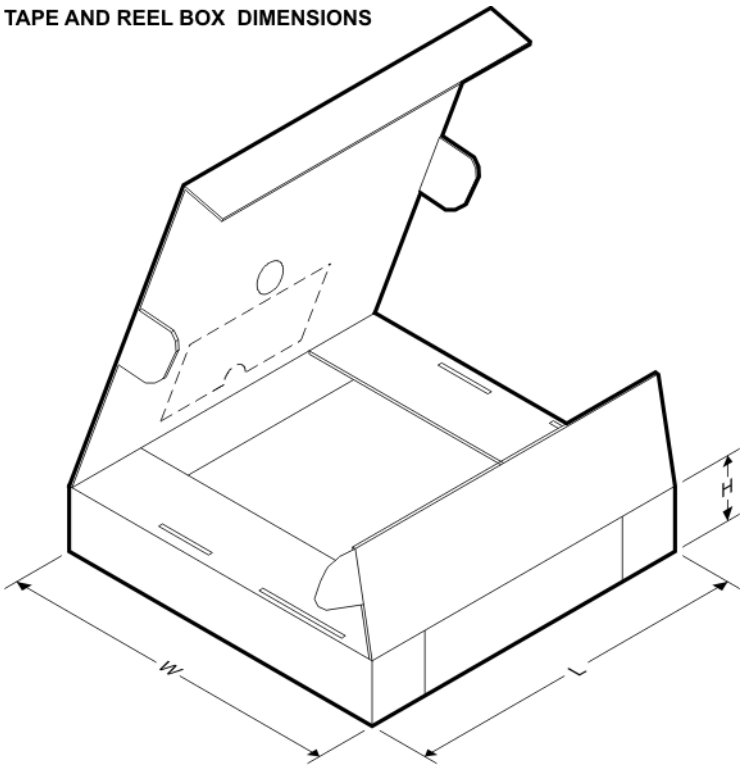
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVS885PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

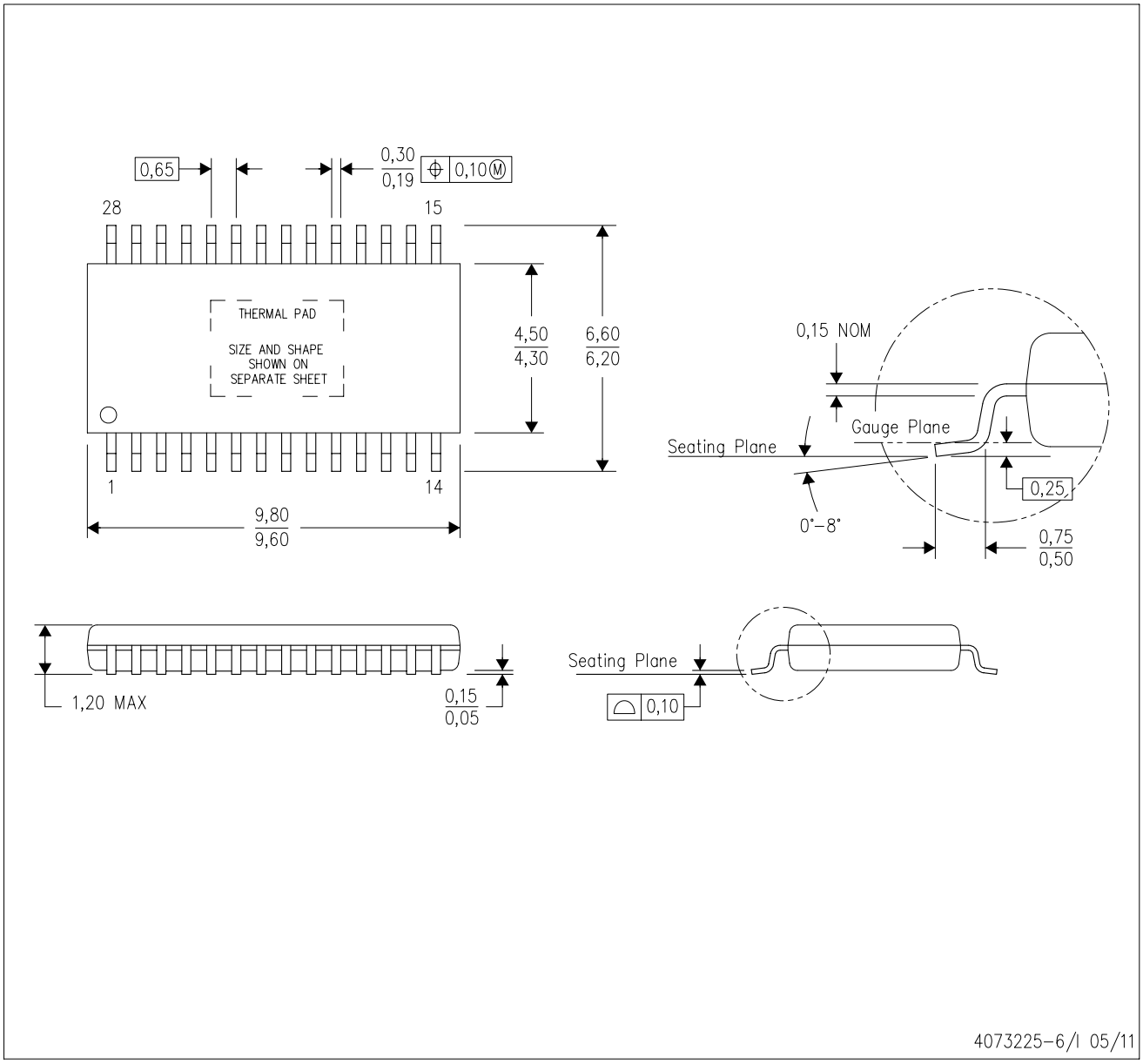
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVS885PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

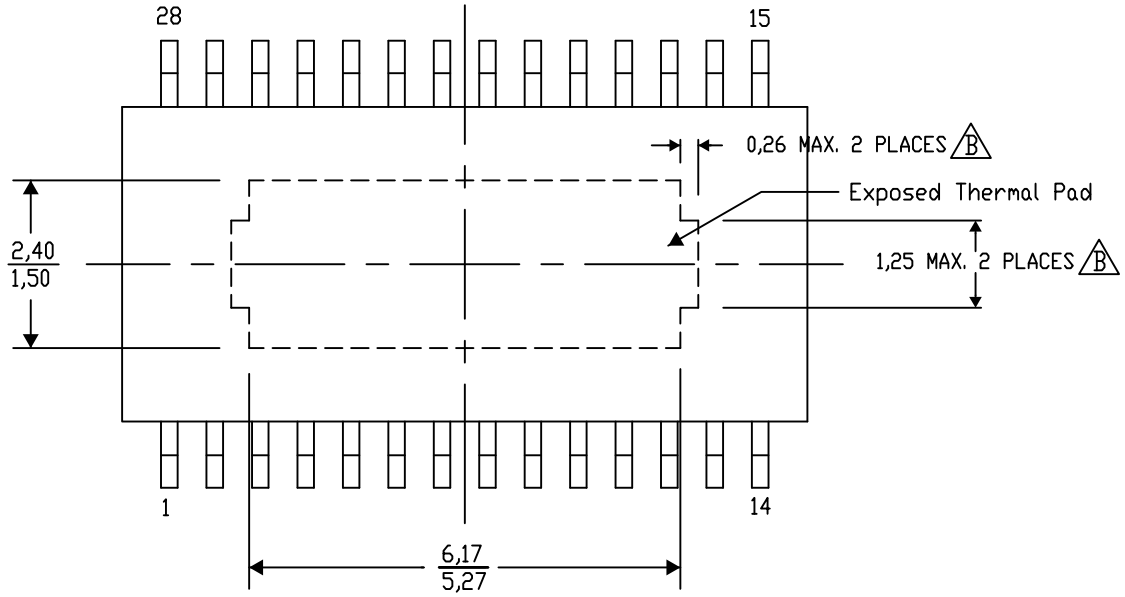
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

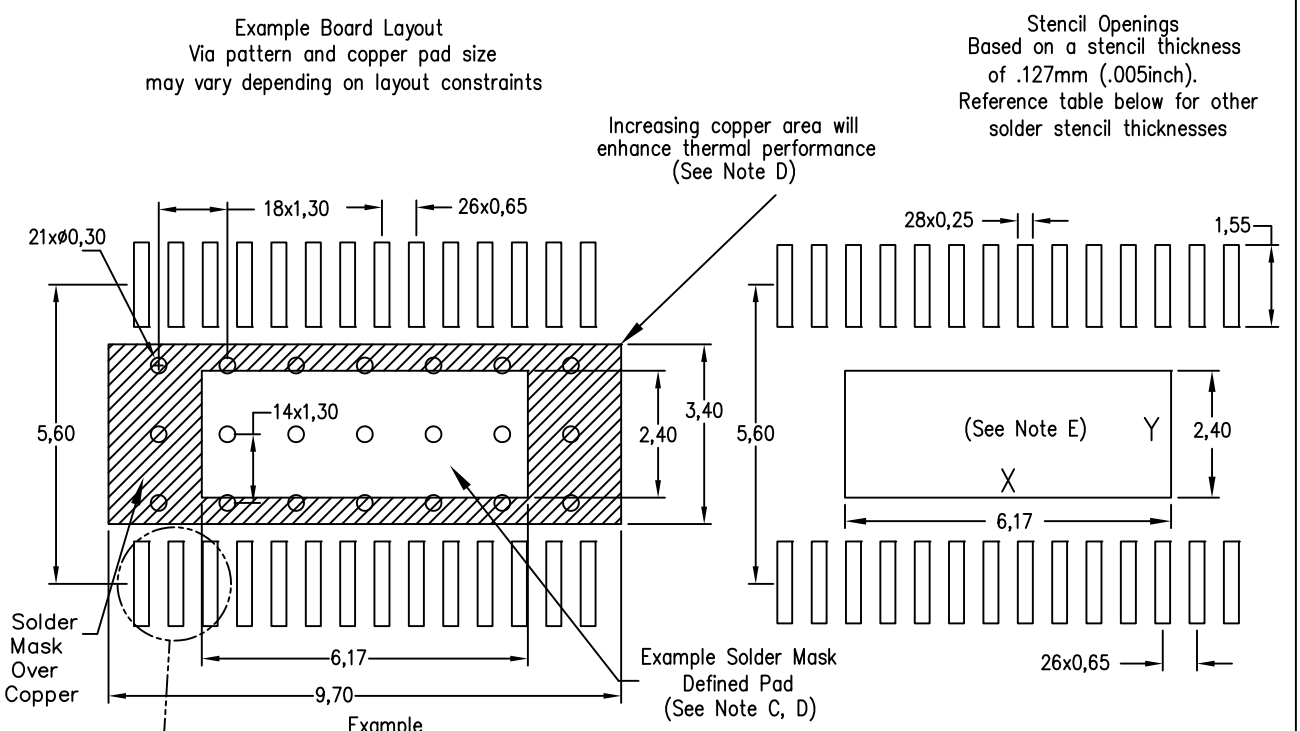
4206332–33/AD 01/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/S 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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