5.4Gbps DisplayPort 1.2 2-to-1 Differential Switch

Check for Samples: HD3SS212

FEATURES

- **Compatible with DisplayPort 1.2 Electrical Standard**
- **2:1 Switching Supporting Data Rates up to 5.4Gbps**
- **Supports HPD Switching**
- **Wide -3dB Differential BW of over 5.4 GHz**
- **Excellent Dynamic Characteristics (at 2.7GHz)**
  - **Crosstalk = –50dB**
  - **Isolation = –22dB**
  - **Insertion Loss = –1.4dB**
  - **Return Loss = –11 dB**
  - **Max Bit-Bit Skew = 4 ps**
- **VDD Operating Range 3.3 V ±10%**
- **Small 5 mm x 5 mm x 1 mm, 48-Ball u*BGA Package**
- **Output Enable ($\overline{OE}$) Pin Disables Switch to Save Power**
- **Power Consumption**
  - **HD3SS212 <10mW (Standby <30μW when $\overline{OE}$ = L)**

APPLICATIONS

- **Motherboard Applications Needing DP and PCI Express**
- **Desktop PCs**
- **Notebook PCs**
- **Docking**

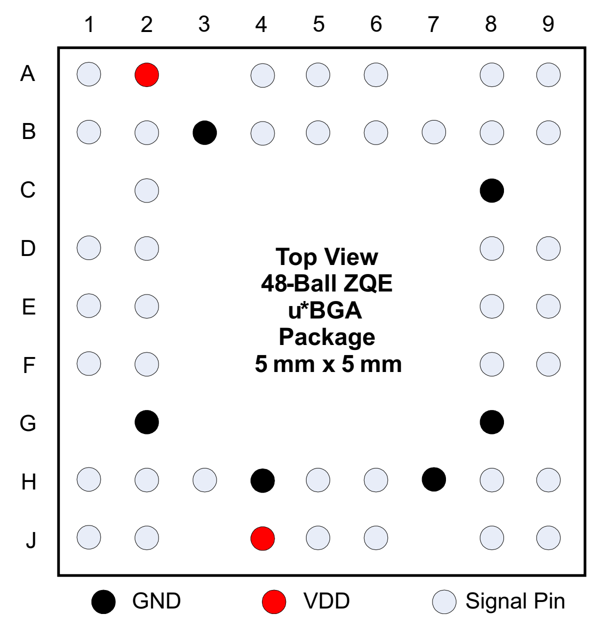


Figure 1. HD3SS212 Ball Map

DESCRIPTION

The HD3SS212 is a high-speed passive switch capable of switching two full DisplayPort 4 lane ports from one of two sources to one target location in an application. For DisplayPort Applications that HD3SS212 also supports switching of the Auxiliary (AUX) and Hot Plug Detect (HPD) signals. HPD path is a buffer which requires a 125kΩ pull-down resistor on the HPDC line.

A typical application would be a mother board that includes two GPUs that need to drive one DisplayPort sink. The GPU is selected by the Dx_SEL pin. The HD3SS212 is offered in a 48-ball BGA package and specified to operate from a single supply voltage of 3.3V over full industrial temperature range of –40°C to 105°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE
HD3SS212ZQER	HD3SS212	48-Ball u*BGA (ZQE)
HD3SS212ZQET		

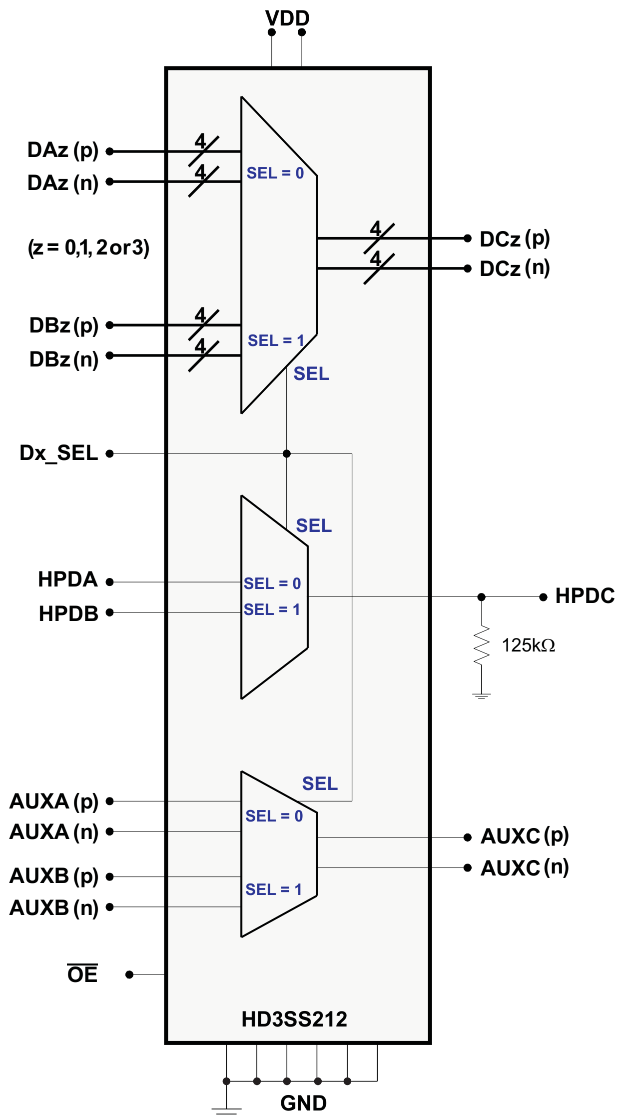


Figure 2. HD3SS212 Functional Block Diagram

	1	2	3	4	5	6	7	8	9
A	Dx_SEL	VDD		DA0(n)	DA1(n)	DA2(n)		DA3(p)	DA3(n)
B	DC0(n)	DC0(p)	GND	DA0(p)	DA1(p)	DA2(p)	OE#	DB0(p)	DB0(n)
C		NC						GND	
D	DC1(n)	DC1(p)						DB1(p)	DB1(n)
E	DC2(n)	DC2(p)						DB2(p)	DB2(n)
F	DC3(n)	DC3(p)						DB3(p)	DB3(n)
G		GND						GND	
H	AUXC(n)	AUXC(p)	HPDB	GND	NC	AUXB(p)	GND	NC	AUXA(p)
J	HPDC	HPDA		VDD	NC	AUXB(n)		NC	AUXA(n)

Figure 3. HD3SS212 Ball Map by Signal Name

PIN FUNCTIONS

PIN	PIN NAME	I/O	DESCRIPTION
A1	Dx_SEL	Control I	High Speed Port Selection Control Pins
B4 A4	DA0(p) DA0(n)	I/O	Port A, Channel 0, High Speed Positive Signal Port A, Channel 0, High Speed Negative Signal
B5 A5	DA1(p) DA1(n)	I/O	Port A, Channel 1, High Speed Positive Signal Port A, Channel 1, High Speed Negative Signal
B6 A6	DA2(p) DA2(n)	I/O	Port A, Channel 2, High Speed Positive Signal Port A, Channel 2, High Speed Negative Signal
A8 A9	DA3(p) DA3(n)	I/O	Port A, Channel 3, High Speed Positive Signal Port A, Channel 3, High Speed Negative Signal
B8 B9	DB0(p) DB0(n)	I/O	Port B, Channel 0, High Speed Positive Signal Port B, Channel 0, High Speed Negative Signal
D8 D9	DB1(p) DB1(n)	I/O	Port B, Channel 1, High Speed Positive Signal Port B, Channel 1, High Speed Negative Signal
E8 E9	DB2(p) DB2(n)	I/O	Port B, Channel 2, High Speed Positive Signal Port B, Channel 2, High Speed Negative Signal
F8 F9	DB3(p) DB3(n)	I/O	Port B, Channel 3, High Speed Positive Signal Port B, Channel 3, High Speed Negative Signal
B2 B1	DC0(p) DC0(n)	I/O	Port C, Channel 0, High Speed Positive Signal Port C, Channel 0, High Speed Negative Signal
D2 D1	DC1(p) DC1(n)	I/O	Port C, Channel 1, High Speed Positive Signal Port C, Channel 1, High Speed Negative Signal
E2 E1	DC2(p) DC2(n)	I/O	Port C, Channel 2, High Speed Positive Signal Port C, Channel 2, High Speed Negative Signal
F2 F1	DC3(p) DC3(n)	I/O	Port C, Channel 3, High Speed Positive Signal Port C, Channel 3, High Speed Negative Signal
H9 J9	AUXA(p) AUXA(n)	I/O	Port A AUX Positive Signal Port A AUX Negative Signal

PIN FUNCTIONS (continued)

PIN	PIN NAME	I/O	DESCRIPTION
H6 J6	AUXB(p) AUXB(n)	I/O	Port B AUX Positive Signal Port B AUX Negative Signal
H2 H1	AUXC(p) AUXC(n)	I/O	Port C AUX Positive Signal Port C AUX Negative Signal
J2, H3, J1	HPDA/B/C	I/O	Port A/B/C Hot Plug Detect
B7	$\overline{OE}$	I	Output Enable
A2, J4	VDD	Supply	3.3V Positive power supply voltage
B3, C8, G2, G8, H4, H7	GND	Supply	Negative power supply voltage
C2, H5, H8, J5, J8	NC		Electrically not connected

FUNCTIONAL DESCRIPTION

Refer to Figure 2.

The HD3SS212 behaves as a two to one using high bandwidth pass gates. The input port is selected using the Dx_SEL pin according to Table 1.

Table 1. Switch Control Logic

CONTROL LINES	SWITCHED I/O PINS(1)(2)				
Dx_SEL	DCz(p) PIN z = 0, 1, 2 or 3	DCz(n) PIN z = 0, 1, 2 or 3	HPDC PIN	AUXC(p) PIN	AUXC(n) PIN
L	DAz(p)	DAz(n)	HPDA	AUXA(p)	AUXA(n)
H	DBz(p)	DBz(n)	HPDB	AUXVB(p)	AUXVB(n)

(1) $\overline{OE}$ pin - For nomal operation, drive $\overline{OE}$ high. Driving the $\overline{OE}$ pin low will disable the switch to enable power savings.
(2) The ports which are not selected by the Control Lines will be in High Impedance State.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
Supply voltage range(3)	VDD	–0.5 V to 4 V
Voltage range	Differential I/O	–0.5 V to 4 V
	Control pin	–0.5 V to VCC +0.5V
Electrostatic discharge	Human body model(4)	±4,000V
	Charged-device model(5)	±1000V
Operating free-air temperature		–40°C to 105°C
Continuous power dissipation		See The Thermal Information Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) 5. Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC(1)		HD3SS212	UNITS
		48-Ball u*BGHA (ZQE)	
θ_{JA}	Junction-to-ambient thermal resistance	90.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.9	
θ_{JB}	Junction-to-board thermal resistance	53.9	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	53.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

typical values for all parameters are at V_{CC} = 3.3V and T_A = 25°C, all temperature limits are specified by design

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, $\overline{OE}$) (HPDC, 5V Tolerant)	2.0		VDD	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, $\overline{OE}$, HPDC)	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{I/O_CM}	Common voltage (Dx, AUXx)	Switch I/O common mode voltage	0		2.0	V
	Operating free-air temperature		–40		105	°C

ELECTRICAL CHARACTERISTICS

under recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input high current (Dx_SEL)	VDD = 3.6 V, VIN = VDD		3	10	µA
I_{IL}	Input low current (Dx_SEL)	VDD = 3.6 V, VIN = GND		0.01	1	µA
I_{LK}	Leakage current (Dx_SEL)	VDD = 3.3 V, Vi = 2V, $\overline{OE}$ = 3.3V		2	5	µA
		VDD = 0 V, Vi = 2 V, $\overline{OE}$ = 3.3 V		6	10	
	Leakage current (HPDA)	VDD = 3.3 V, Vi = 2 V, $\overline{OE}$ = 3.3 V; Dx_SEL=3.3 V		0.01	2	
	Leakage current (HPDB)	VDD = 3.3 V, Vi = 2 V, $\overline{OE}$ = 3.3 V; Dx_SEL=GND		0.01	2	
I_{off}	Device shut down current	VDD = 3.6 V, $\overline{OE}$ = GND			5	µA
I_{DD}	Supply current	VDD = 3.6 V, Dx_SELx = VCC/GND; Outputs floating		2.5	5	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		1		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5V - 1.5 V, I_O = –40 mA		6.5	10	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	VDD = 3.3 V; -0.35V ≤ VI ≤ 1.2 V; I_O = –40 mA			1.5	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON\ (MAX)}$ – $R_{ON\ (MAIN)}$)	VDD = 3.3 V; -0.35 V ≤ VI ≤ 1.2 V		1.3		Ω
AUXx SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		9		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		3		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5 V - 1.5 V, I_O = -40 mA		7	12	Ω

ELECTRICAL CHARACTERISTICS (continued)

under recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS (under recommended operating conditions; R_L, R_{sc} = 50 Ω unless otherwise noted						
t_{PD}	Switch propagation delay	R_{sc} and RL = 50 Ω, See Figure 5			200	ps
T_{on}	Dx_SEL -to-Switch Ton (Data and AUX)	R_{sc} and RL = 50 Ω, See Figure 4		175	250	ns
T_{off}	Dx_SEL -to-Switch Toff (Data and AUX)			175	250	
T_{on}	Dx_SEL -to-Switch Ton (HPD)	RL = 50 Ω, See Figure 4		275	350	ns
T_{off}	Dx_SEL -to-Switch Toff (HPD)			275	350	
$T_{SK(O)}$	Inter-pair output skew (CH-CH)	R_{sc} and RL = 1 kΩ, See Figure 5			50	ps
$T_{SK(b-b)}$	Intra-pair output skew (bit-bit)			1	4	
RL	Dx Differential return loss(1)	1.35 GHz, See TYPICAL PERFORMANCE PLOTS		–17		dB
		2.7 GHz, See TYPICAL PERFORMANCE PLOTS		–11		
X_{TALK}	Dx Differential crosstalk(1)	2.7 GHz		–50		
O_{IRR}	Dx Differential off-isolation(1)	2.7 GHz, See TYPICAL PERFORMANCE PLOTS		–22		
I_L	Dx Differential insertion loss(1)	f = 1.35 GHz, See TYPICAL PERFORMANCE PLOTS		–0.7		dB
		f = 2.7 GHz, See TYPICAL PERFORMANCE PLOTS		–1.4		
		f = 5.4 GHz, See TYPICAL PERFORMANCE PLOTS		–1.7		
	AUX Differential insertion loss(1)	f = 360 MHz		–1		dB

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

TEST TIMING DIAGRAMS

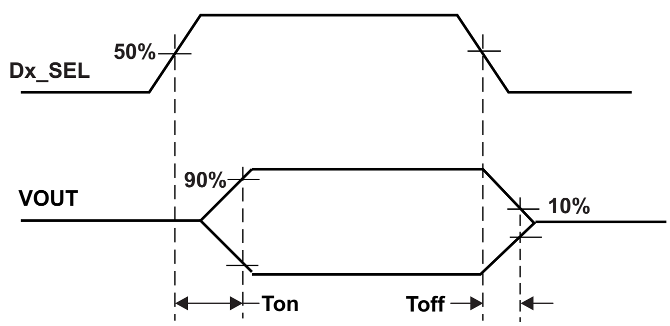
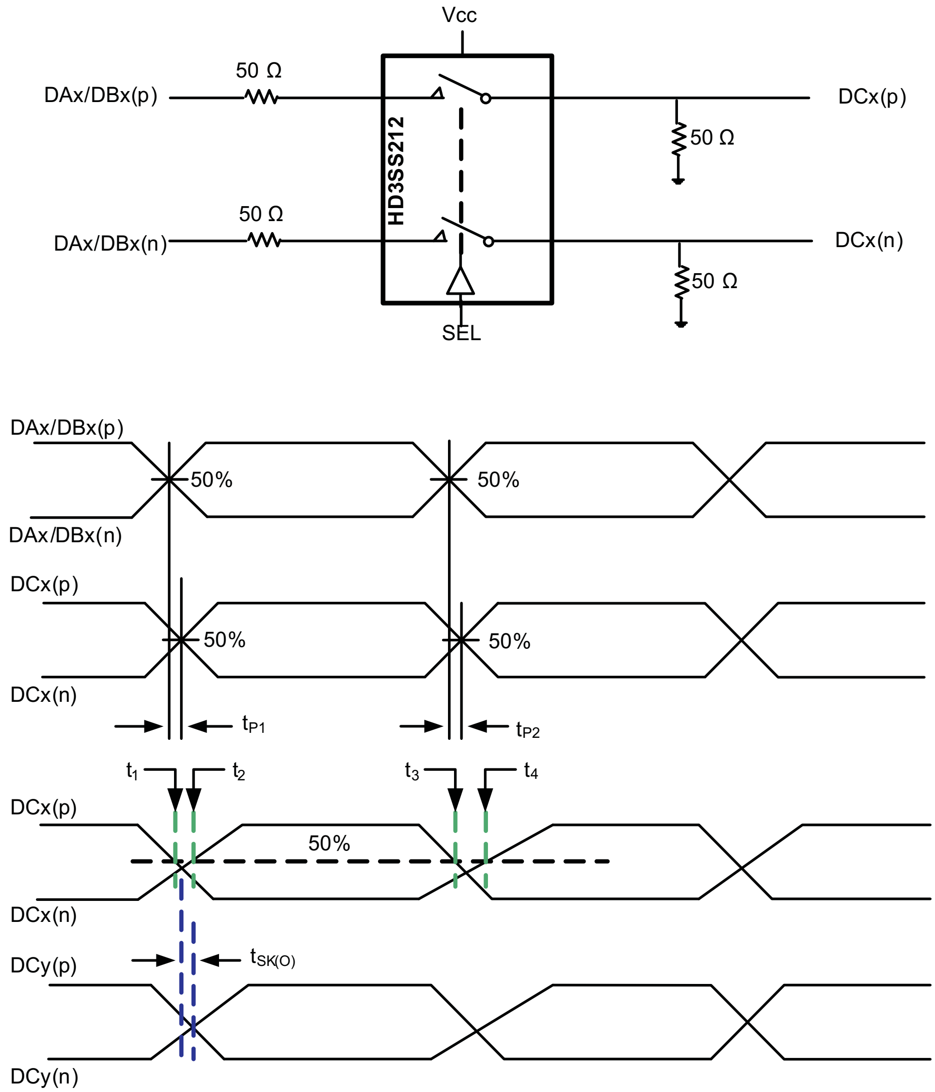


Figure 4. Select to Switch T_{on} and T_{off}



t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b-b)} = 0.5 \times |(t_4 - t_3) + (t_1 - t_2)|$

Figure 5. Propagation Delay and Skew

TYPICAL PERFORMANCE PLOTS

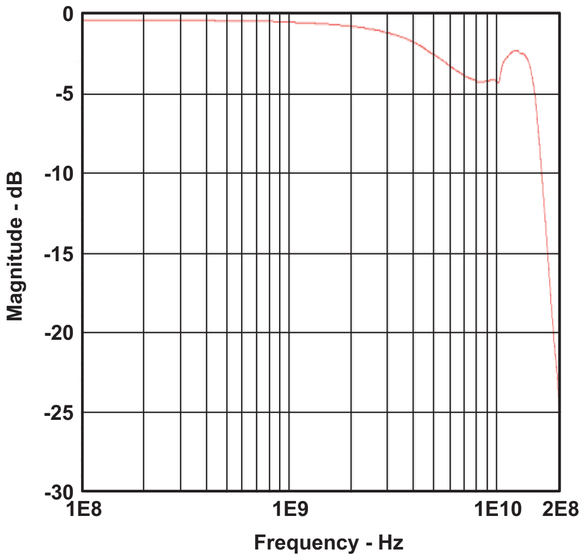


Figure 6. Insertion Loss and -3dB Bandwidth

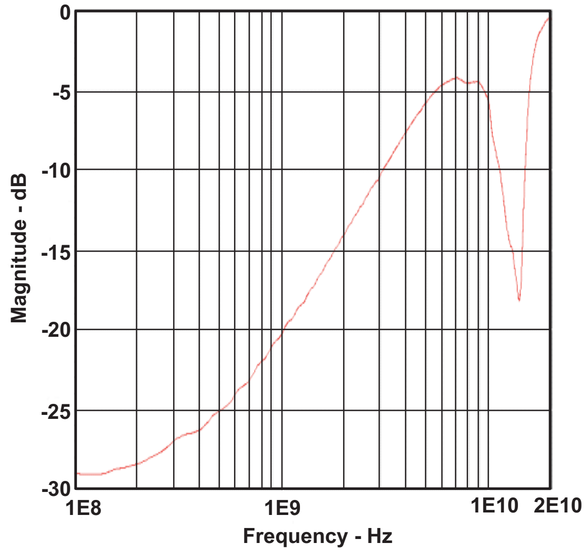


Figure 7. Return Loss

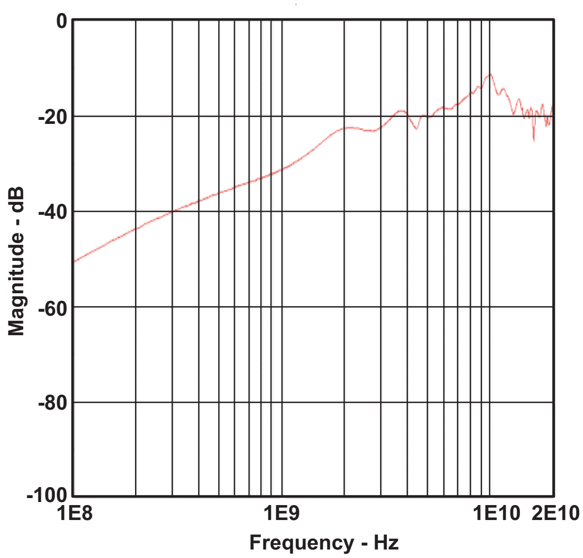


Figure 8. OF Isolation

REVISION HISTORY

Changes from Original (December 2011) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HD3SS212ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
HD3SS212ZQET	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	48	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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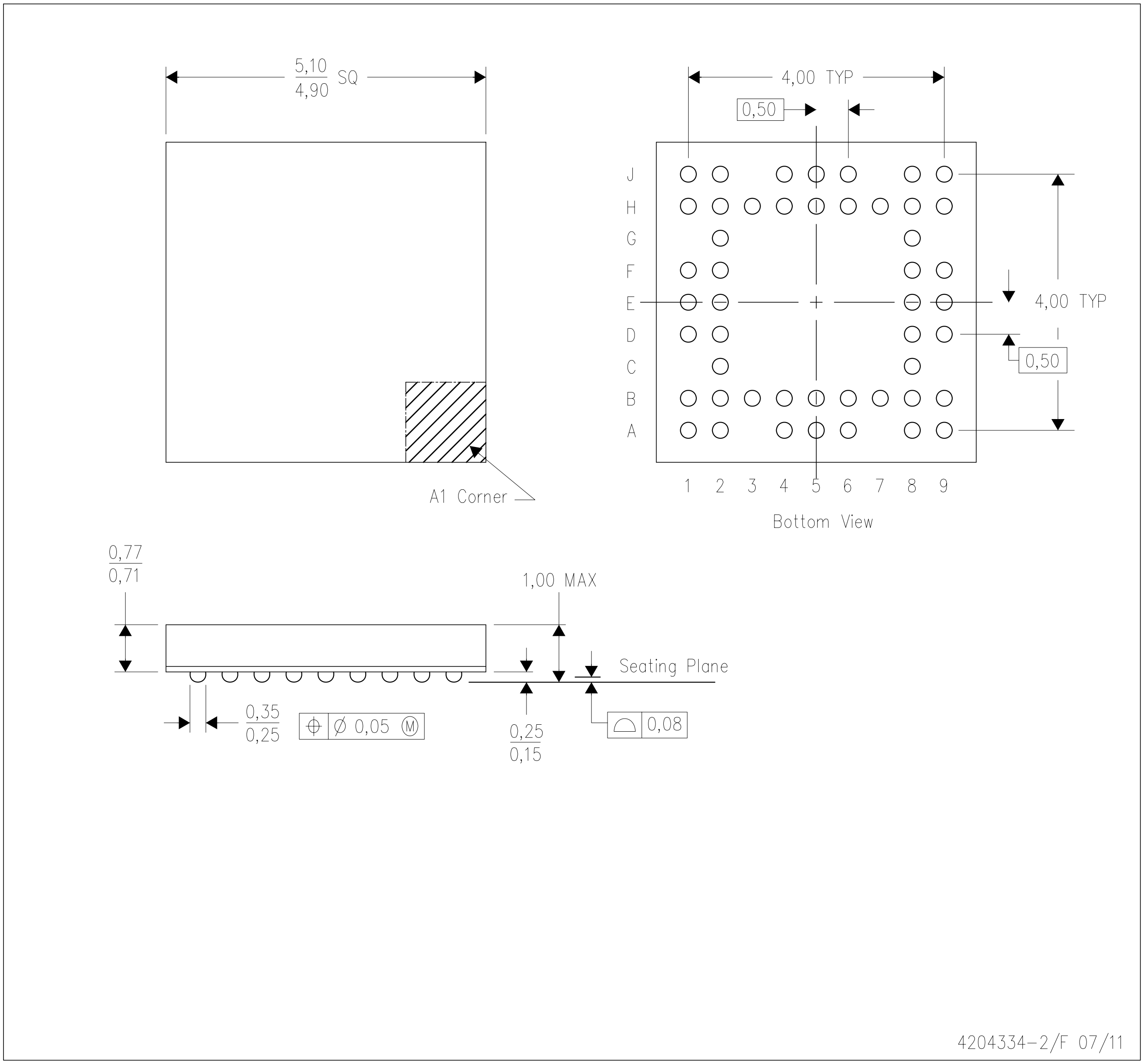
ZQE (S-PBGA-N48) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225
D. This is a Pb-free solder ball design.

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