DYNAMIC NFC INTERFACE TRANSPONDER

FEATURES

- **NFC Tag Type 4**
- **ISO14443B Compliant 13.56-MHz RF Interface Supports up to 848 kbps**
- **SPI or I^2C Interface to Write and Read NDEF Messages to Internal SRAM**
- **3kB SRAM for NDEF Messages**
- **Automatic Checking of NDEF Structure**
- **Interrupt Register and Output Pin to Indicate NDEF Read or Write Completion**

DESCRIPTION

The Texas Instruments Dynamic NFC Interface Transponder RF430CL330H is a NFC Tag Type 4 device that combines a wireless NFC interface and a wired SPI or I^2C interface to connect the device to a host. The NDEF message in the SRAM can be written and read from the integrated SPI or I^2C serial communication interface and can also be accessed and updated wirelessly via the integrated ISO14443B-compliant RF interface that supports up to 848 kbps.

This allows NFC connection handover for an alternative carrier like *Bluetooth*™, *Bluetooth* Low Energy (BLE), and Wi-Fi as an easy and intuitive pairing process or authentication process with only a tap. As a general NFC interface, the RF430CL330H enables end equipments to communicate with the fast-growing infrastructure of NFC-enabled smart phones, tablets, and notebooks.

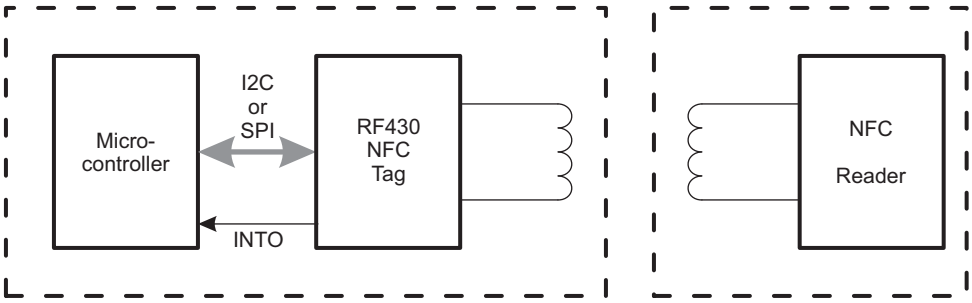


Figure 1. Typical Application

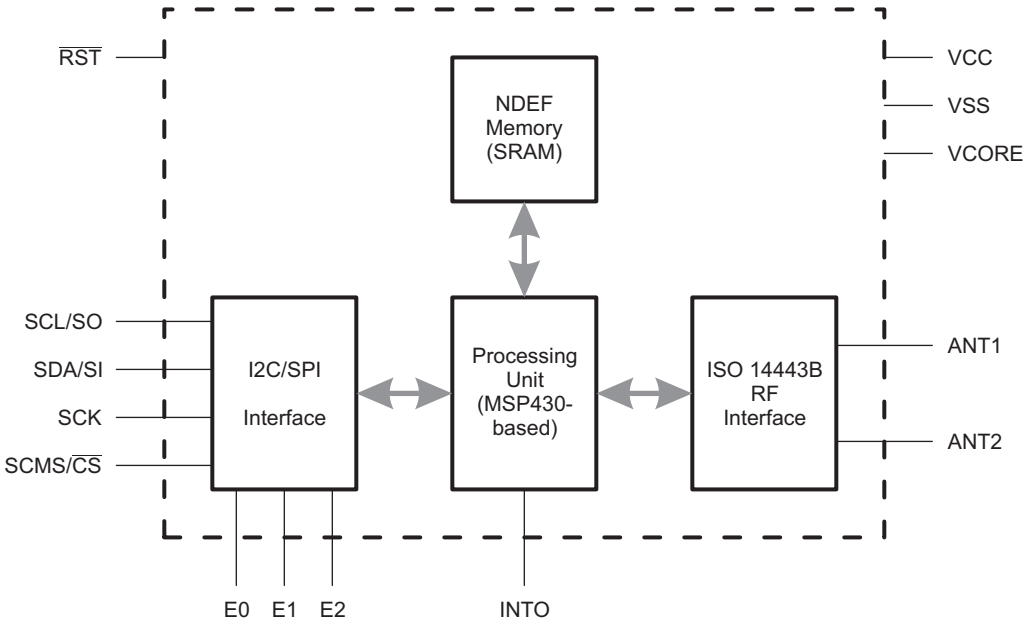
Table 1. Ordering Information(1)

T_A	PACKAGED DEVICES(2)
	PLASTIC 14-PIN TSSOP (PW)
-40ºC to 85ºC	RF430CL330HCPWR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

Functional Block Diagram



PW PACKAGE
(TOP VIEW)

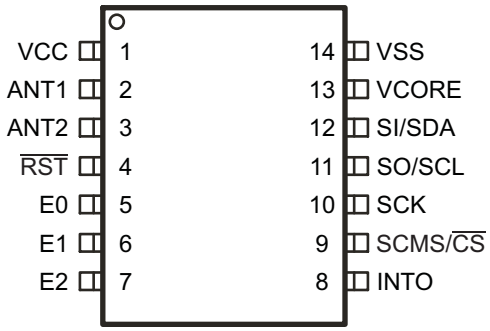


Table 2. Terminal Functions

TERMINAL		I/O[1]	DESCRIPTION
NAME	NO.		
VCC	1	PWR	3.3-V power supply
ANT1	2	RF	Antenna input 1
ANT2	3	RF	Antenna input 2
$\overline{\text{RST}}$	4	I	Reset input (active low)[2]
E0 (TMS)	5	I	I2C address select 0 SPI mode select 0 (JTAG test mode select[3])
E1 (TDO)	6	I (O)	I2C address select 1 SPI mode select 1 (JTAG test data output[3])
E2 (TDI)	7	I	I2C address select 2[4] (JTAG test data in[3])
INTO (TCK)	8	O	Interrupt output (JTAG test clock[3])
SCMS/ $\overline{\text{CS}}$	9	I	Serial Communication Mode Select (during device initialization)[5] Chip select (in SPI mode)
SCK	10	I	SPI clock input (SPI mode)
SO/SCL	11	I/O	SPI slave out (SPI mode) I2C clock (I2C mode)
SI/SDA	12	I/O	SPI slave in (SPI mode) I2C data (I2C mode)
VCORE	13	PWR	Regulated core supply voltage
VSS	14	PWR	Ground supply

(1) I = Input, O = Output, PWR = Power, RF = RF Antenna
(2) With integrated pullup.
(3) This device does not provide JTAG-compliant boundary scan test.
(4) Tie low in SPI mode to avoid floating inputs.
(5) Selects I2C or SPI mode during power-up and initialization (see and). Tie SCMS/$\overline{\text{CS}}$ low to select I2C mode.

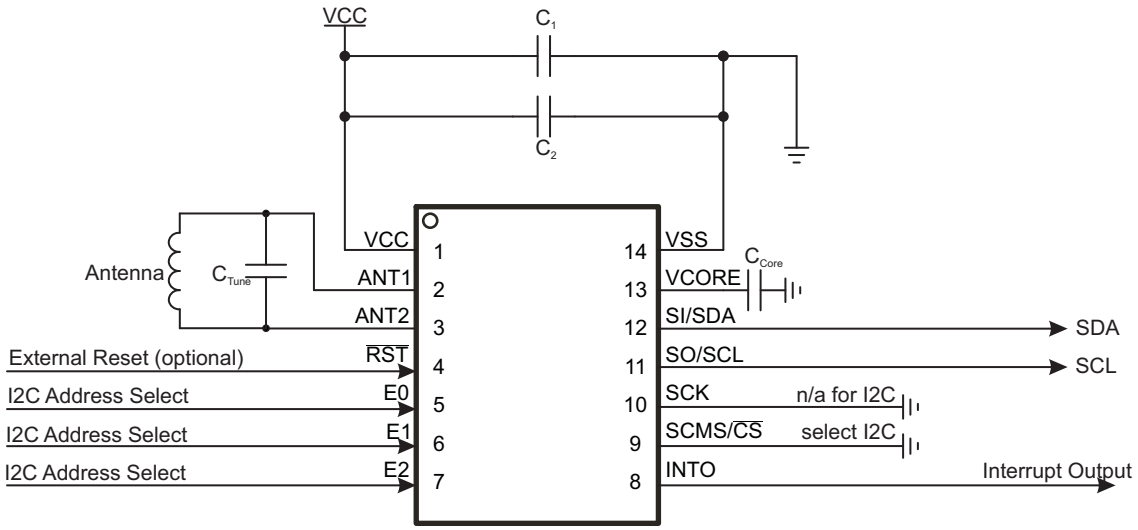


Figure 2. Example Application Diagram (I2C Operation)

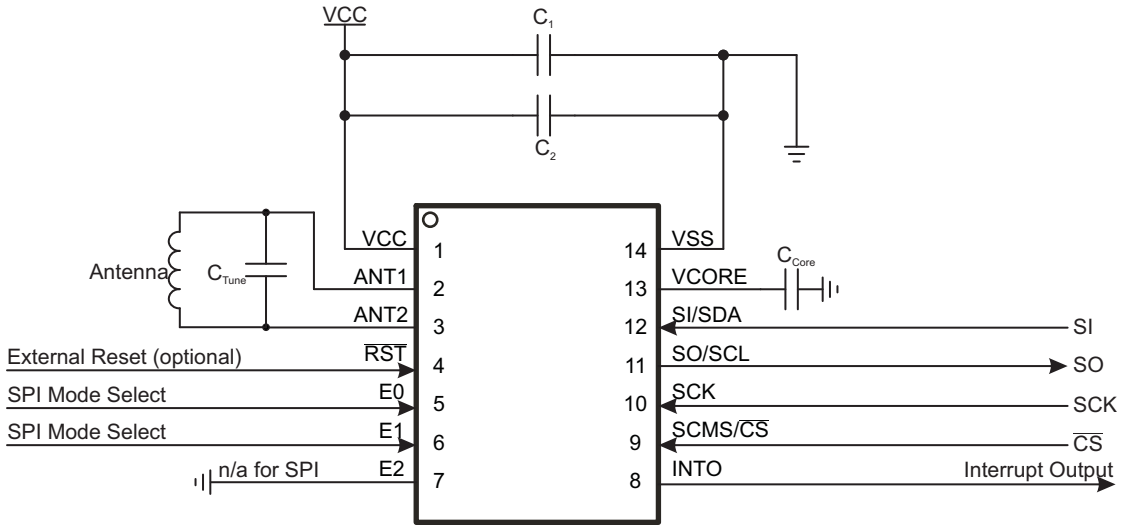


Figure 3. Example Application Diagram (SPI Operation)

Detailed Description

Serial Communication Interface

A "dual-mode" serial communication interface supports either SPI or I2C communication. The serial interface allows writing and reading the internal NDEF message memory as well as configuring the device operation.

SPI or I2C Mode Selection

The selection between I2C or SPI mode takes place during the power-up and initialization phase of the device based on the input level at pin SCMS/$\overline{CS}$ (see Table 3).

Table 3. SPI or I2C Mode Selection

Input Level at SCMS/$\overline{CS}$ During Initialization	Selected Serial Interface
0	I2C
1	SPI

During initialization, an integrated pullup resistor pulls SCMS/$\overline{CS}$ high, which makes SPI the default interface. To enable I2C, this pin must be tied low externally. The pullup resistor is disabled after initialization to avoid any current through the resistor during normal operation. In SPI mode, the pin reverts to its $\overline{CS}$ functionality after initialization.

Communication Protocol

The tag is programmed and controlled by writing data into and reading data from the address map shown in Table 4 via the serial interface (SPI or I2C).

Table 4. User Address Map

Range	Address	Size	Description
Registers	0xFFFE	2B	Control Register
	0xFFFC	2B	Status Register
	0xFFFA	2B	Interrupt Enable
	0xFFF8	2B	Interrupt Flags
	0xFFF6	2B	CRC Result (16-bit CCITT)
	0xFFF4	2B	CRC Length
	0xFFF2	2B	CRC Start Address
	0xFFF0	2B	Communication Watchdog Control Register
	0xFFEE	2B	Version
	0xFFEC	2B	Reserved
	0xFFEA	2B	Reserved
	0xFFE8	2B	Reserved
	0xFFE6	2B	Reserved
	0xFFE4	2B	Reserved
	0xFFE2	2B	Reserved
	0xFFE0	2B	Reserved
Reserved	0x4000 to 0xFFDF		Reserved
	0x0C00 to 0x3FFF	13kB	Reserved (for example, future extension of NDEF Application Memory size)
NDEF	0x0000 to 0x0BFF	3kB	NDEF Application Memory

NOTE

Crossing Range Boundaries

Crossing range boundaries causes writes to be ignored and reads to return undefined data.

I2C Protocol

A command is always initiated by the master by addressing the device using the specified I2C device address. The device address is a 7-bit I2C address. The upper four bits are hard-coded, and the lower three bits are programmable by the input pins E0 through E2.

Table 5. I2C Device Address

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	E2	E1	E0
MSB						LSB

To write data, the device is addressed using the specified I2C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be written and the lower 8 bits of that address. Next (without a repeated start), the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by the STOP condition on the I2C bus.

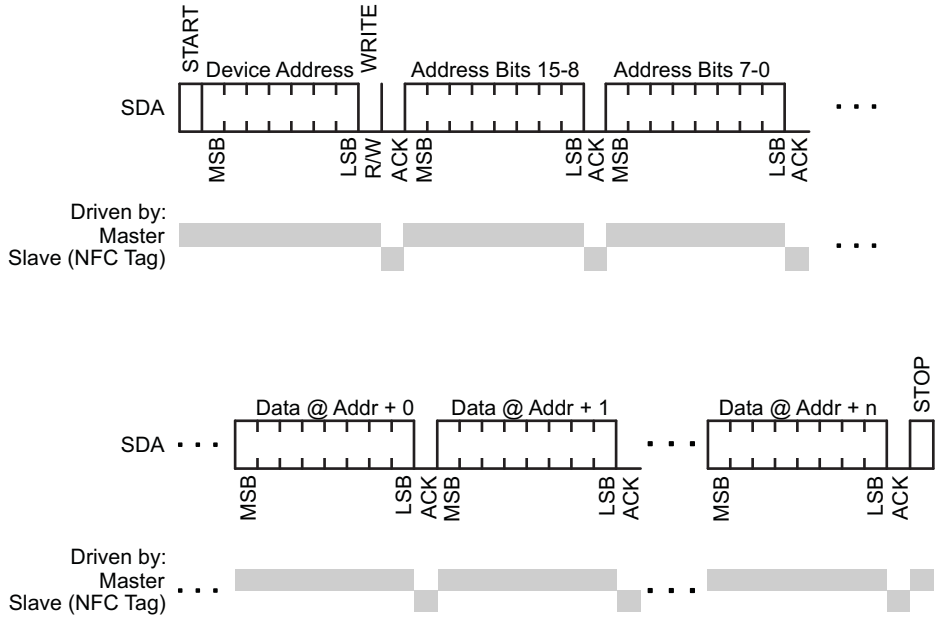


Figure 4. I2C Write Access

To read data, the device is addressed using the specified I2C device address with R/$\overline{W}$ = 0, followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, a repeated start condition is expected with the I2C device address and R/$\overline{W}$ = 1. The device then transmit data starting at the specified address until a non-acknowledgment and a STOP condition is received.

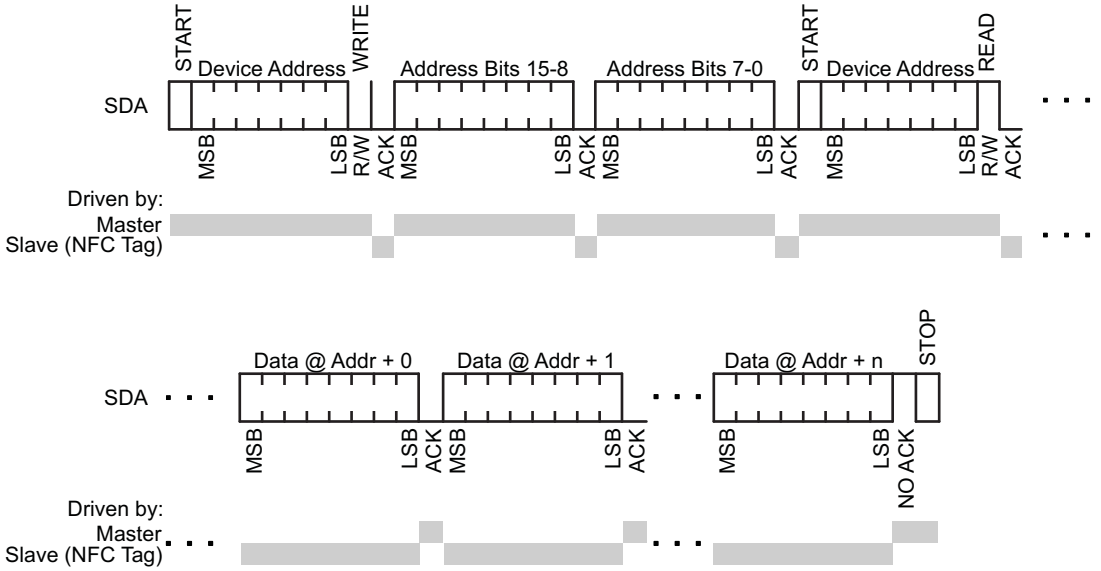


Figure 5. I2C Read Access

BIP-8 Communication Mode With I2C

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

Table 6. Write Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
Slave	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the I2C device address).

Table 7. Read Access

Master	Address Bits 15 to 8	Address Bits 7 to 0	n/a	n/a	n/a
Slave	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access, the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address and the 2 transmitted data bytes, and it is transmitted back to the master. The BIP-8 does not include the device address.

SPI Protocol

The SPI communication mode (SCK idle state and clock phase) is selected by tying E0 and E1 to VSS or VCC according to Table 8.

Table 8. SPI Mode Selection

E1	E0	SPI Mode
0	0	**SPI Mode 0** with CPOL = 0 and CPHA = 0 SCK idle state: 0 SI capture starts on the first edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.
0	1	**SPI Mode 1** with CPOL = 0 and CPHA = 1 SCK idle state: 0 SI capture starts on the second edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	0	**SPI Mode 2** with CPOL = 1 and CPHA = 0 SCK idle state: 1 SI capture starts on the first edge: SI data is captured on the falling edge, and SO data is propagated on the rising edge.
1	1	**SPI Mode 3** with CPOL = 1 and CPHA = 1 SCK idle state: 1 SI capture starts on the second edge: SI data is captured on the rising edge, and SO data is propagated on the falling edge.

An SPI communication is always initiated by the master by pulling the $\overline{CS}$ pin low.

To write data into the device, this is followed by the master sending a write command (0x02) followed by the upper 8 bits of the first address to be written and then the lower 8 bits of that address. Next, the data to be written starting at the specified address is received. With each data byte received, the address is automatically incremented by 1. The write access is terminated by pulling the $\overline{CS}$ pin high.

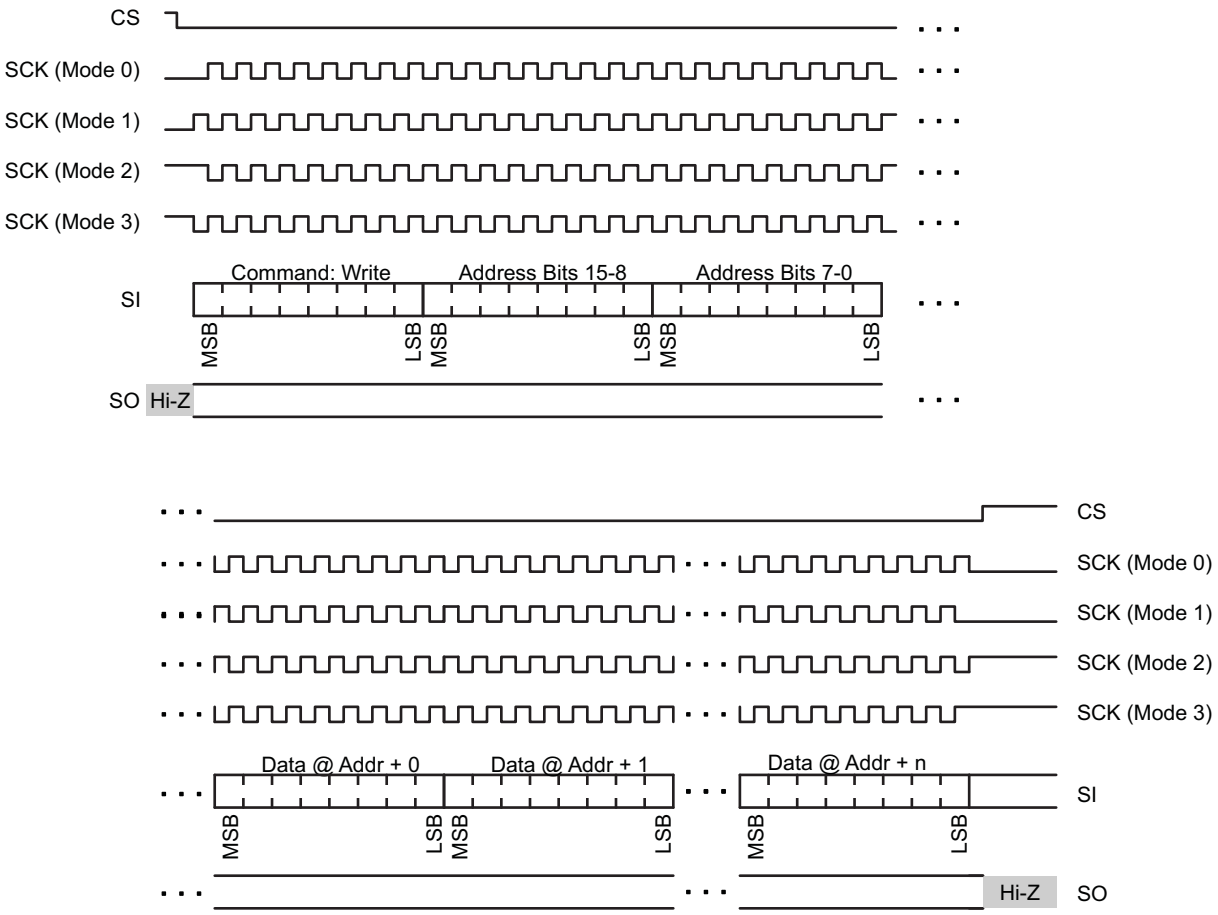


Figure 6. SPI Write Access

To read data from the device, pulling the $\overline{CS}$ pin low is followed by the master sending a read command (0x03 or 0x0B) followed by the upper 8 bits of the first address to be written, the lower 8 bits of that address and a dummy byte. The device responds with the data that is read starting at the specified address until the $\overline{CS}$ pin is pulled high.

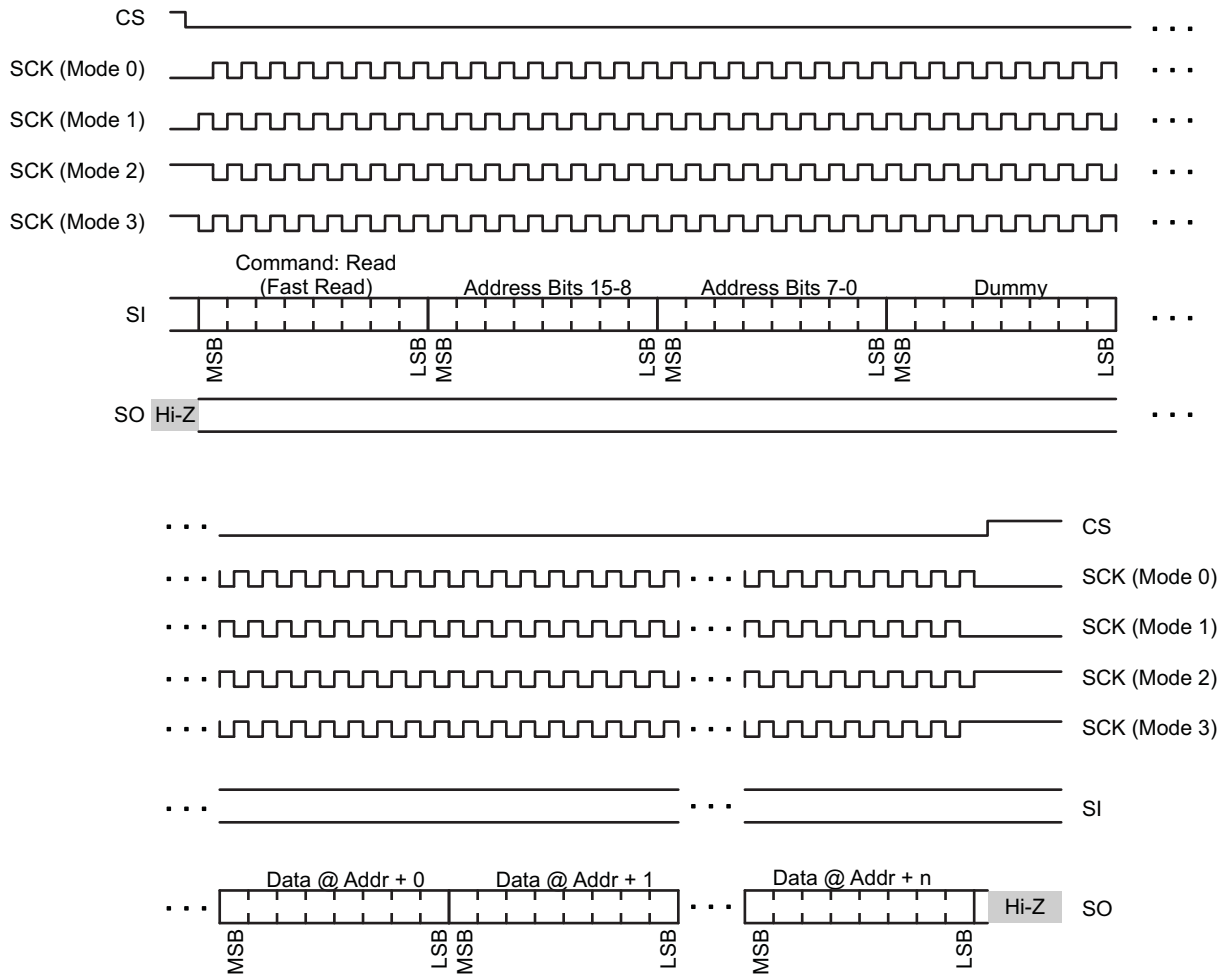


Figure 7. SPI Read Access (Command: 0x03 or 0x0B)

Commands other than write (0x02) and read (0x03 or 0x0B) are ignored. There is no difference in using the read command 0x03 or 0x0B.

BIP-8 Communication Mode With SPI

The BIP-8 communication mode is enabled by setting the BIP-8 bit in the General Control register. All communication after setting this bit uses the following conventions with exactly 2 address bytes (16-bit address) and 2 data bytes (16-bit data).

Table 9. Write Access

SI	Command: Write	Address Bits 15 to 8	Address Bits 7 to 0	Data at Addr + 0	Data at Addr + 1	BIP-8
SO	n/a	n/a	n/a	n/a	n/a	n/a

The Bit-Interleaved Parity (BIP-8) is calculated using 16-bit address and 16-bit data. If the received BIP-8 does not match with received data no write will be performed. (The BIP-8 calculation does not include the write-command byte.)

Table 10. Read Access

SI	Command: Read	Address Bits 15 to 8	Address Bits 7 to 0	Dummy Byte	n/a	n/a	n/a
SO	n/a	n/a	n/a	n/a	Data at Addr + 0	Data at Addr + 1	BIP-8

For read access the Bit-Interleaved Parity (BIP-8) is calculated using the received 16-bit address, the received dummy byte and the 2 transmitted data bytes and transmitted back to the master. It does not include the read-command byte.

Registers

NOTE

Endianness

All 16-bit registers are little-endian: the least significant byte with bits 7-0 is at the lowest address (and this address is always even). The most significant byte with bits 15-8 is at the highest address (always odd).

General Control Register

Table 11. General Control Register

Addr:	15	14	13	12	11	10	9	8
0xFFFF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFE	Reserved	Standby Enable	BIP-8	INTO Drive	INTO High	Enable INT	Enable RF	SW-Reset

Table 12. General Control Register Description

Bit	Field	Type	Reset	Description
0	SW-Reset	W	0	0b = Always reads 0. 1b = Resets the device to default settings and clears memory. The serial communication is restored after t_{Ready}, and the register settings and NDEF data memory must be restored afterward.
1	Enable RF	R/W	0	Global enable of RF interface. The RF interface should be disabled when writing to the NDEF application memory. Enabling the RF interface triggers a basic check of the NDEF structure. If this check fails, the RF interface remains disabled and the NDEF Error interrupt flag is set. When the RF interface is enabled, writes using the serial interface (except to disable the RF interface) are discouraged to avoid any interference with RF communication. 0b = RF interface disabled 1b = RF interface enabled
2	Enable INT	R/W	0	Global Interrupt Output Enable 0b = Interrupt output disabled. The INTO pin is Hi-Z. 1b = Interrupt output enabled. The INTO pin signals any enabled interrupt according to the INTO High and INTO Drive bits.
3	INTO High	R/W	0	Interrupt Output pin INTO Configuration 0b = Interrupts are signaled with an active low 1b = Interrupts are signaled with an active high
4	INTO Drive	R/W	0	Interrupt Output pin INTO Configuration 0b = Pin is Hi-Z if there is no pending interrupt. Application provides an external pullup resistor if bit 3 (INTO Active High) = 0. Application provides an external pulldown resistor if bit 3 (INTO Active High) = 1. 1b = Pin is actively driven high or low if there is no pending interrupt. It is driven high if bit 3 (INTO Active High) = 0. It is driven low if bit 3 (INTO Active High) = 1.
5	BIP-8	R/W	0	Enables BIP-8 communication mode (bit interleaved parity). If BIP-8 is enabled, a separate running tally is kept of the parity (that is, the number of ones that occur) for every bit position in the bytes included in the BIP-8 calculation. The corresponding bit position of the BIP-8 byte is set to 1 if the parity is currently odd and is set to 0 if the parity is even – resulting in an overall even parity for each bit position including the BIP-8 byte. All communication when this bit is set must follow the conventions defined in the BIP-8 communication mode sections for I2C and SPI. 0b = BIP-8 communication mode disabled 1b = BIP-8 communication mode enabled

Table 12. General Control Register Description (continued)

Bit	Field	Type	Reset	Description
6	Standby Enable	R/W	0	Enables a low-power standby mode. The standby mode is entered if the RF interface is disabled, the communication watchdog is disabled, and no serial communication is ongoing. 0b = Standby mode disabled 1b = Standby mode enabled
7	Reserved	R/W	0	
8-15	Reserved	R	0	

Status Register

Table 13. Status Register

Addr:	15	14	13	12	11	10	9	8
0xFFFD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFC	Reserved	Reserved	Reserved	Reserved	Reserved	RF Busy	CRC Active	NDEF Ready

Table 14. Status Register Description

Bit	Field	Type	Reset	Description
0	Ready	R	0	0b = Device not ready to receive updates to the NDEF memory from the serial interface. 1b = Device ready. NDEF memory can be written by the serial interface.
1	CRC Active	R	0	0b = No CRC calculation ongoing 1b = CRC calculation ongoing
2	RF Busy	R	0	0b = No RF communication ongoing 1b = RF communication ongoing
3-15	Reserved	R	0	

Interrupt Registers

The interrupt enable register determines what interrupt events are signaled on the external output pin INTO. Setting any bits high in this register allows the corresponding events to trigger the interrupt signal.

All enabled interrupt signals are ORed together and the result is signaled on the output pin INTO.

Table 15. Interrupt Enable Register

Addr:	15	14	13	12	11	10	9	8
0xFFFB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFFA	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

Table 16. Interrupt Enable Register Description

Bit	Field	Type	Reset	Description
0-15	Interrupt Enables	R/W	0	Enable for the corresponding IRQ. All enabled interrupt signals are ORed together and the result is signaled on the output pin INTO. 0b = IRQ disabled 1b = IRQ enabled

The interrupt flag register is used to report the status of any interrupts that are pending. Setting any bit high in this register acknowledges and clears the interrupt associated with the respective bit.

Table 17. Interrupt Flag Register

Addr:	15	14	13	12	11	10	9	8
0xFFF9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFF8	Generic Error	Reserved	NDEF Error	BIP-8 Error Detected	CRC Calculation Completed	End of Write	End of Read	Reserved

Table 18. Interrupt Flag Register Description

Bit	Field	Type	Reset	Description
0-15	Interrupt Flags	R/W	0	Flag pending IRQ. Read Access: 0b = No pending IRQ. 1b = Pending IRQ. Write Access: 0b = No change. 1b = Clear pending IRQ flag.

Table 19. Interrupts

Bit	Field	Description
0	Reserved	
1	End of Read	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a read of the NDEF message.
2	End of Write	This IRQ occurs when the RF field is turned off by the reader after the reader has performed a write into the NDEF message.
3	CRC Calculation Completed	This IRQ occurs when a CRC calculation that is triggered by writing into the CRC registers is completed and the result can be read from the CRC result register (see CRC Registers).
4	BIP-8 Error Detected	This IRQ occurs when a BIP-8 error is detected (only if the BIP-8 communication mode is enabled).
5	NDEF Error	This IRQ occurs if an error is detected in the NDEF structure after an attempt to enable the RF interface.
6	Reserved	
7	Generic Error	This IRQ occurs for any error that makes the device unreliable or non-operational.
8-15	Reserved	

CRC Registers

Writing the CRC address and the CRC length registers initiates a 16-bit CRC calculation of the specified address range. The length is always assumed to be even (16-bit aligned). Writing the length register starts the CRC calculation.

During the CRC calculation, the CRC active bit is set (=1). When the calculation is complete, the "CRC completion" interrupt flag is set and the result of the CRC calculation can be read from the CRC result register. It is recommended to perform a CRC calculation only when the RF interface is disabled (RF Enable = 0).

Table 20. CRC Result Register

Addr:	15	14	13	12	11	10	9	8
0xFFF7	CRC CCITT Result (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF6	CRC CCITT Result (low byte)							

Table 21. CRC Result Register Description

Bit	Field	Type	Reset	Description
0-15	CRC-CCITT Result	R	0	CRC-CCITT Result

Table 22. CRC Length Register

Addr:	15	14	13	12	11	10	9	8
0xFFF5	CRC Length (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF4	CRC Length (low byte)							

Table 23. CRC Length Register Description

Bit	Field	Type	Reset	Description
0-15	CRC Length	RW	0	CRC Length - always assumed to be even (Bit 0 = 0). Writing into high byte starts CRC calculation.

Table 24. CRC Start Address Register

Addr:	15	14	13	12	11	10	9	8
0xFFF3	CRC Start Address (high byte)							
Addr:	7	6	5	4	3	2	1	0
0xFFF2	CRC Start Address (low byte)							

Table 25. CRC Start Address Register Description

Bit	Field	Type	Reset	Description
0-15	CRC Start Address	RW	0	CRC Start Address. Defines start address within NDEF application data memory. This address is always assumed to be even (bit 0 = 0).

The CRC is calculated based on the CCITT polynomial initialized with 0xFFFF.

CCITT polynomial: $x^{16} + x^{12} + x^5 + 1$

Communication Watchdog Register

When the communication watchdog is enabled, it expects a write or read access within a specified period; otherwise, the watchdog resets the device. If the BIP-8 communication mode is enabled, the transfer must be valid to be accepted as a watchdog reset.

Table 26. Communication Watchdog Register

Addr:	15	14	13	12	11	10	9	8
0xFFF1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Addr:	7	6	5	4	3	2	1	0
0xFFF0	Reserved	Reserved	Reserved	Reserved	Timeout Period Selection			Enable

Table 27. Communication Watchdog Register Description

Bit	Field	Type	Reset	Description
0	Enable	R/W	0	0b = Communication Watchdog disabled 1b = Communication Watchdog enabled
1	Timeout Period Selection	R/W	0	000b = 2 s ± 30%(1) 001b = 32 s ± 30%(1) 010b = 8.5 min ± 30%(1) 011b to 111b = Reserved
4-15	Reserved	R	0	

(1) This value is based on use of the integrated low-frequency oscillator with a frequency of 256 kHz ± 30%.

Version Registers

Provides version information about the implemented ROM code.

Table 28. Version Register

Addr:	15	14	13	12	11	10	9	8
0xFFEF	Software Version							
Addr:	7	6	5	4	3	2	1	0
0xFFEE	Software Identification							

Table 29. Version Register Description

Bit	Field	Type	Reset	Description
0-7	Software Identification	R		0x01: RF430CL330H Firmware
8-15	Software Version	R		Software version

NFC Type-4 Tag Functionality

The device supports an ISO 14443B compliant transponder that operates according to the NFC Forum Tag Type-4 specification and supports the NFC Forum NDEF (NFC Data Exchange Format) requirements. Through the RF interface, the user can read and update the contents in the NDEF data memory. The contents in the NDEF data memory (stored in SRAM) are stored as long as power is maintained.

NOTE

This device does not have nonvolatile memory; therefore, the information stored in the NDEF data memory is lost when power is removed.

This device does not support the peer-to-peer or reader/writer modes in the ISO18092/NFC Forum specification. All RF communication between an NFC forum device and this device is in the passive tag mode. The device responds by load modulation and is not considered an intentional radiator.

This device is intended to be used in applications where the primary reader/writer is an NFC-enabled cell phone. The device enables data transfer to and from an NFC phone by RF to the host application that is enabled with the dual interface device. In this case, the host application can be considered the destination device, and the cell phone or other type of mobile device is treated as the end-point device.

This device supports ISO14443-3, ISO 14443-4, and NFC Forum commands as described in the following sections. A high-level overview of the ISO14443B and NFC commands and responses are shown in Figure 8.

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported.

By default, the device reports only the capability to support 106-kbps, because some cell phones do not work correctly with the information that the device supports higher data rates. To enable higher data rates, a special sequence is required as described in Data Rate Settings .

The ISO14443B command and response structure is detailed in ISO 14443-3, ISO 14443-4, and NFC Forum-TS-Digital Protocol. The applicable ISO 7816-4 commands are detailed in NFC Forum-TS-Type-4-Tag_2.0.

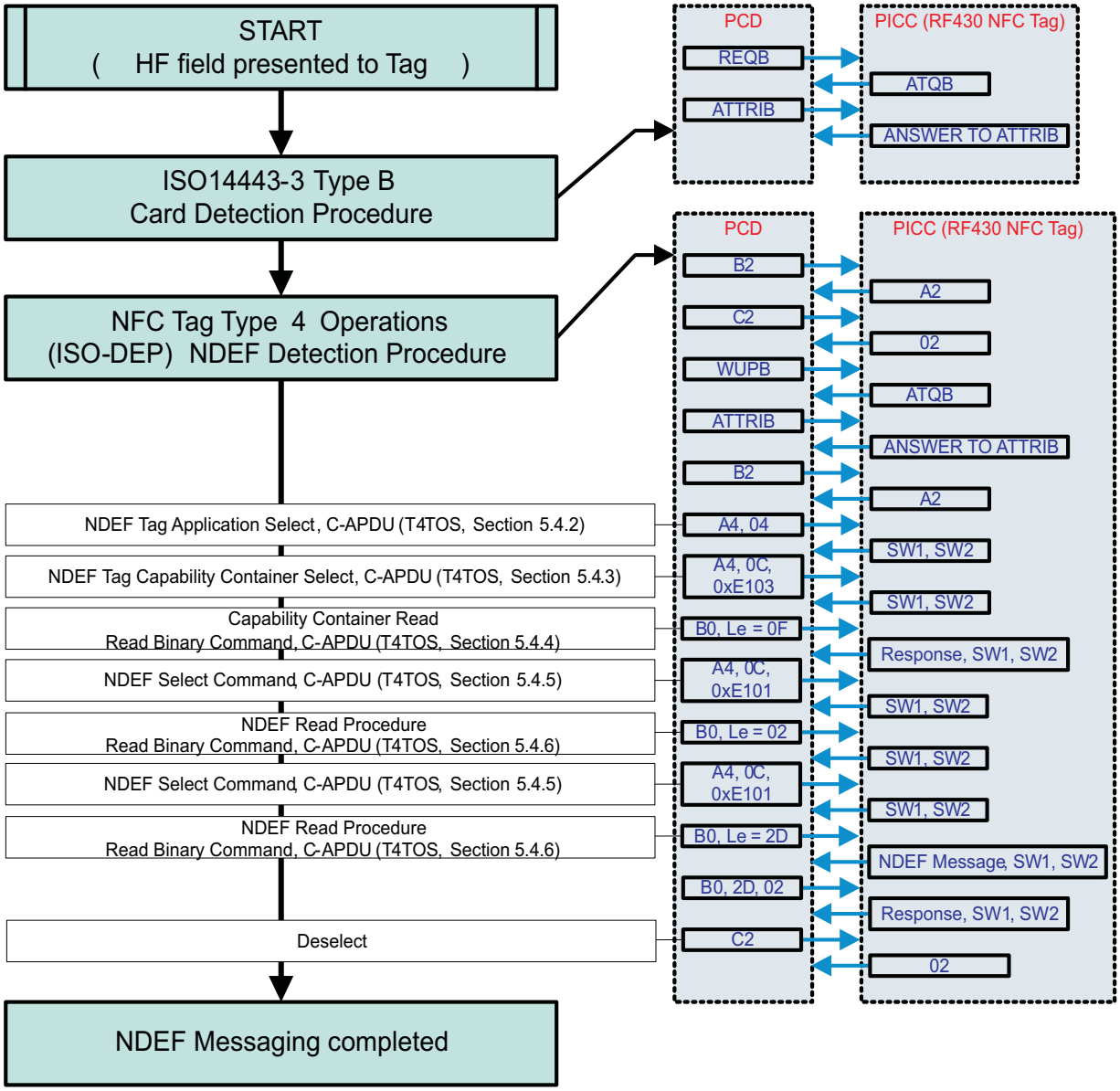


Figure 8. Command and Response Exchange Flow

ISO 14443-3 Commands

These commands use the character, frame format, and timing that are described in ISO 14443-3, clause 7.1. The following commands are used to manage communication:

REQB and WUPB

The REQB and WUPB Commands sent by the PCD are used to probe the field for PICCs of Type B. In addition, WUPB is used to wake up PICCs that are in the HALT state. The number of slots N is included in the command as a parameter to optimize the anticollision algorithm for a given application.

Slot-MARKER

After a REQB or WUPB Command, the PCD may send up to (N-1) Slot-MARKER Commands to define the start of each timeslot. Slot-MARKER Commands can be sent after the end of an ATQB message received by the PCD to mark the start of the next slot or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

ATTRIB

The ATTRIB Command sent by the PCD includes information required to select a single PICC. A PICC receiving an ATTRIB Command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only responds to commands defined in ISO/IEC 14443-4 that include its unique CID.

HLTB

The HLTB Command is used to set a PICC in HALT state and stop responding to a REQB.

After answering to this command, the PICC ignores any commands except the WUPB.

NFC Tag Type 4 Commands

Select

Selection of applications or files

ReadBinary

Read data from file

UpdateBinary

Update (erase and write) data to file

Data Rate Settings

106-kbps, 212-kbps, 424-kbps, and 848-kbps data rates are supported by the device.

By default, the device reports only the capability to support 106-kbps, because some cell phones do not work correctly with the information that the device supports higher data rates. To enable higher data rates the sequence shown in Table 30 must be sent though the selected serial interface.

Table 30. Data Rate Setting Sequence

Access Type	Addr Bits 15 to 8	Addr Bits 7 to 0	Data 0	Data 1
1. Write Access	0xFF	0xE0	0x4E	0x00
2. Write Access	0xFF	0xFE	0x80	0x00
3. Write Access	0x2A	0x78	0xF7 (1)	0x00
4. Write Access	0x28	0x14	0x00	0x00
5. Write Access	0xFF	0xE0	0x00	0x00

(1) Data Rate Capability according to Table 31. 0xF7: all data rates up to 847 kbps are supported.

Table 31. Data Rate Capability

Data Rata Capability Byte								Description
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	PICC supports only 106-kbps in both directions (default).
1	x	x	x	0	x	x	x	Same data rate from PCD to PICC and from PICC to PCD compulsory
x	x	x	1	0	x	x	x	PICC to PCD, data rate supported is 212 kbps
x	x	1	x	0	x	x	x	PICC to PCD, data rate supported is 424 kbps
x	1	x	x	0	x	x	x	PICC to PCD, data rate supported is 847 kbps
x	x	x	x	0	x	x	1	PCD to PICC, data rate supported is 212 kbps
x	x	x	x	0	x	1	x	PCD to PICC, data rate supported is 424 kbps
x	x	x	x	0	1	x	x	PCD to PICC, data rate supported is 847 kbps

NDEF Data Memory

This device implements 3kB of SRAM memory that must be written with the NDEF Application data.

Table 32 shows the mandatory structure. The data can be accessed through the RF interface only after the NDEF application memory is correctly initialized through the serial interface.

While writing into the NDEF application memory, the RF interface must be disabled by clearing the Enable RF bit in the General Control register. After the NDEF application memory is properly initialized, the RF interface can be enabled be setting the Enable RF bit in the General Control register to 1. When the RF interface is enabled, the basic NDEF structure is checked for correctness. If an error in the structure is detected, the NDEF Error IRQ is triggered, and the RF interface remains disabled (the Enable RF bit in the General Control register is cleared to 0).

If the NDEF application data must be modified through the serial interface after the RF interface is enabled, it is recommended to read the RF Busy bit in the Status register. If the RF interface is busy, defer disabling the RF interface until the RF transaction is completed (indicated by RF Busy bit = 0).

Figure 9 shows the recommended flow how to control the access to the NDEF application memory.

The address range for the NDEF application memory is 0x0000 to 0x0BFF.

Table 32. NDEF Application Data (Mandatory)

<table>
<tr><td rowspan="11">NDEF Application
Selectable by Name = D2_7600_0085_0101h</td><td rowspan="7">Capability Container
Selectable by File ID = E103h</td><td colspan="3">2B - CCLen</td><td rowspan="4"></td></tr>
<tr><td colspan="3">1B - Mapping version</td></tr>
<tr><td colspan="3">2B - MLe</td></tr>
<tr><td colspan="3">2B - MLc</td></tr>
<tr><td rowspan="5">NDEF File Ctrl TLV</td><td colspan="2">1B - Tag = 04h</td><td rowspan="5">The NDEF file control TLV is mandatory</td></tr>
<tr><td colspan="2">1B - Len = 06h</td></tr>
<tr><td rowspan="4">6B - Val</td><td>2B - File Identifier</td></tr>
<tr><td>2B - Max file size</td></tr>
<tr><td>1B - Read access</td></tr>
<tr><td>1B - Write access</td></tr>
<tr><td rowspan="4">NDEF File
Selectable by File ID = xxyyh</td><td colspan="3">2B - Len</td><td rowspan="3">Mandatory NDEF file</td></tr>
<tr><td colspan="3">xB - Binary NDEF file content</td></tr>
<tr><td colspan="3">yB - Unused if Len < Max file size in File Ctrl TLV</td></tr>
</table>

Table 33. NDEF Application Data (Includes Proprietary Sections)

NDEF Application Selectable by Name = D2_7600_0085_0101h	Capability Container Selectable by File ID = E103h	2B - CCLen			
		1B - Mapping version			
		2B - MLe			
		2B - MLc			
		NDEF File Ctrl TLV	1B - Tag = 04h		The NDEF file control TLV is mandatory
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
		Proprietary File Ctrl TLV (1)	1B - Tag = 05h		Zero or more proprietary file control TLVs
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
		⋮			
		Proprietary File Ctrl TLV (N)	1B - Tag = 05h		
			1B - Len = 06h		
			6B - Val	2B - File Identifier	
				2B - Max file size	
				1B - Read access	
				1B - Write access	
	NDEF File Selectable by File ID = xxyyh	2B - Len			Mandatory NDEF file
		xB - Binary NDEF file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			
	Proprietary File (1) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			
	⋮				
	Proprietary File (N) Selectable by File ID = xxyyh	2B - Len			Optional proprietary file
		xB - Binary proprietary file content			
		yB - Unused if Len < Max file size in File Ctrl TLV			

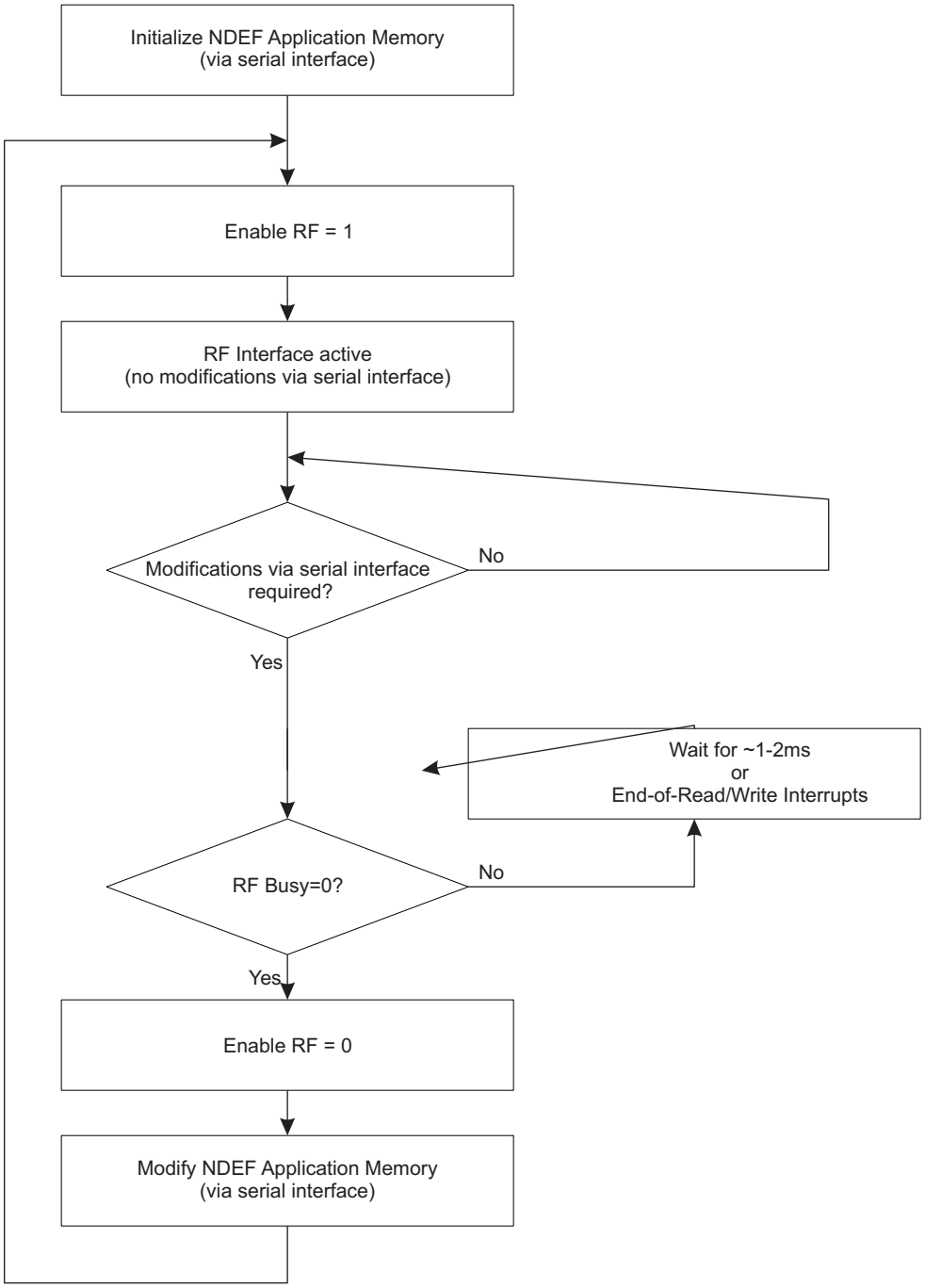


Figure 9. Recommended NDEF Data Memory Flow

NDEF Error Check

With the RF interface is enabled, the basic NDEF structure is automatically checked for correctness. If any of the following conditions are true, the error check fails, an NDEF error IRQ is triggered, and the RF interface remains disabled.

- CCLEN less than 0x000F or greater than 0xFFFE.
- MLe value is less than 0xF.
- MLc is equal to zero.
- TLV tag does not equal 0x4.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

Also the proprietary TLVs are checked. The check fails if any of the following conditions are true.

- TLV tag does not equal 0x05.
- TLV length does not equal 0x6.
- File ID equals 0, or 0xE102, or 0xE103, or 0x3F00, or 0x3FFF, or 0xFFFF.
- Max NDEF size is less than 0x5 or greater than 0xFFFE.
- Read access is greater than 0 and less than 0x80.
- Write Access is greater than 0 and less than 0x80.

Typical Usage Scenario

A typical usage scenario is as follows:

1. Write capability container and messages into the NDEF memory (starting from address 0) using the serial interface.
2. Enable interrupts (especially End of Read and End of Write).
3. Configure the interrupt pin INTO as needed and enable the RF interface.
4. Wait for interrupt signaled by INTO.
5. Disable RF interface (but keep INTO settings unchanged).
6. Read interrupt flag register to determine interrupt sources.
7. Clear interrupt flags. INTO returns to inactive state.
8. Read and modify NDEF memory as needed.
9. Enable RF interface again (keeping INTO settings unchanged) and continue with .

References

ISO/IEC 14443-1:2000, Part 1: Physical characteristics

ISO/IEC 14443-2: 2001, Part 2: Radio frequency interface power and signal interface

ISO/IEC 14443-3: 2001, Part 3: Initialization and anticollision

ISO/IEC 14443-4: 2001, Part 4: Transmission protocols

ISO/IEC 18092, NFC Communication Interface and Protocol-1 (NFCIP-1)

ISO/IEC 21481, NFC Communication Interface Protocol-2 (NFCIP-2)

NDEF NFC Forum Spec, NFC Data Exchange Format Specification

Absolute Maximum Ratings(1)(2)

Voltage applied at V_{CC} referenced to V_{SS} (V_{AMR})	-0.3 V to 4.1 V
Voltage applied at V_{ANT} referenced to V_{SS} (V_{AMR})	-0.3 V to 4.1 V
Voltage applied to any pin (references to V_{SS})	-0.3 V to (V_{CC} + 0.3 V)
Diode current at any device pin	±2 mA
Storage temperature range(3)	-40°C to 125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to VSS.
(3) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution no RF field present	3.0	3.3	3.6	V
	Supply voltage during program execution with RF field present	2.0	3.3	3.6	V
V_{SS}	Supply voltage (GND reference)		0		V
T_A	Operating free-air temperature	-40		85	°C
C_{VCC}	Capacitor on V_{CC}(1)		0.1		µF
C_{VCORE}	Capacitor on V_{CORE}(1)	0.1	0.47	1	µF

(1) Low ESR (equivalent series resistance) capacitor

Recommended Operating Conditions, Resonant Circuit

		MIN	NOM	MAX	UNIT
f_c	Carrier frequency		13.56		MHz
V_{ANT_peak}	Antenna input voltage			3.6	V
Z	Impedance of LC circuit	6.5	15.5		kΩ
L_{RES}	Coil inductance		2.66		µH
C_{RES}	Resonance capacitance		51.8 – C_{IN}(1)		pF
QT	Tank quality factor		20		

(1) Refer to RF143B, Recommended Operating Conditions.

Electrical Characteristics

Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{CC(SPI)}$	SPI, $f_{SCK,MAX}$, SO = Open, Writing into NDEF memory		3.3 V		250		µA
$I_{CC(I2C)}$	I2C, 400 kHz, Writing into NDEF memory		3.3 V		250		µA
$I_{CC(RF\ enabled)}$	RF enabled, no RF field present		3.3 V		200		µA
$I_{CC(Inactive)}$	Standby enable = 0, RF disabled, no serial communication		3.3V		40		µA
$I_{CC(Standby)}$	Standby enable = 1, RF disabled, no serial communication		3.3 V		10	45	µA
$\Delta I_{CC(StrongRF)}$	Additional current consumption with strong RF field present		3.0 V to 3.6 V			160	µA
$I_{CC(RF,lowVCC)}$	Current drawn from VCC < 3.0 V with RF field present (passive operation)		2.0 V to 3.0 V			0	µA

Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.3× V_{CC}	V
V_{IH}	High-level input voltage			0.7× V_{CC}			V
V_{HYS}	Input hysteresis			0.1× V_{CC}			V
I_L	High-impedance leakage current		3.3 V	-50		50	nA
$R_{PU(RST)}$	Integrated $\overline{RST}$ pullup resistor			20	35	50	kΩ
$R_{PU(CS)}$	Integrated SCMS/$\overline{CS}$ pullup resistor (only active during initialization)			20	35	50	kΩ

Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	I_{OL} = 3 mA	3 V			0.4	V
			3.3 V			0.4	
			3.6 V			0.4	
V_{OH}	Output high voltage	I_{OH} = -3 mA	3 V	2.6			V
			3.3 V	2.9			
			3.6 V	3.2			

Serial Communication Protocol Timings

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{SPIvsI2C}$	Time after power-up or reset until SCMS/$\overline{CS}$ is sampled for SPI or I2C decision.(1)			1		10	ms
t_{Ready}	Time after power-up or reset until device is ready to communicate using SPI or I2C.(2)					20	ms

(1) The SCMS/$\overline{CS}$ pin is sampled after $t_{SPIvsI2C}$(MIN) at the earliest and after $t_{SPIvsI2C}$(MAX) at the latest.
(2) The device is ready to communicate after t_{Ready}(MAX) at the latest.

I2C Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 10)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency (with Master supporting clock stretching according to I2C standard, or when the device is not being addressed)		3.3 V	0		400	kHz
	SCL clock frequency (device being addressed by Master not supporting clock stretching)	write	3.3 V	0		120	kHz
		read	3.3 V	0		100	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	3.3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	3.3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		3.3 V	0			ns
$t_{SU,DAT}$	Data setup time		3.3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		3.3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		3.3 V	6.25		75	ns

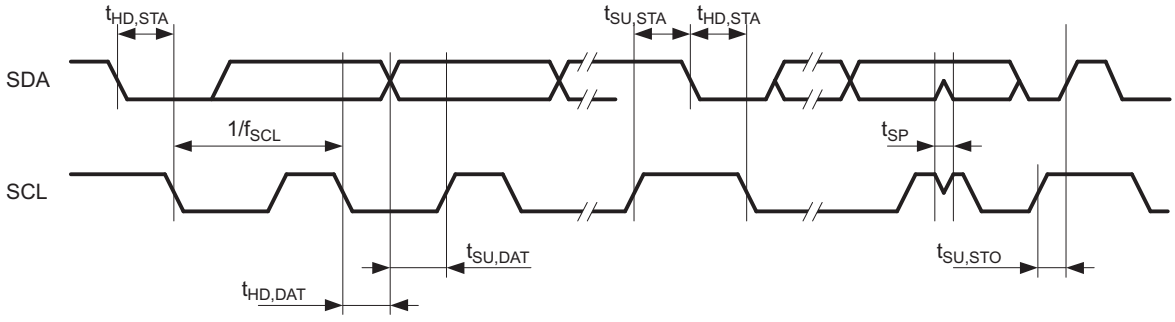


Figure 10. I2C Mode Timing

SPI Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SCK}	SCK clock frequency	write	3.3 V	0		100	kHz
		read	3.3 V	0		110	kHz
$t_{HIGH,CS}$	$\overline{CS}$ high time		3.3 V	50			µs
$t_{SU,CS}$	$\overline{CS}$ setup time		3.3 V	25			µs
$t_{HD,CS}$	$\overline{CS}$ hold time		3.3 V	100			ns
t_{HIGH}	SCK high time		3.3 V	100			ns
t_{LOW}	SCK low time		3.3 V	100			ns
$t_{SU,SI}$	Data In (SI) setup time		3.3 V	50			ns
$t_{HD,SI}$	Data In (SI) hold time		3.3 V	50			ns
$t_{VALID,SO}$	Output (SO) valid		3.3 V	0		50	ns
$t_{HOLD,SO}$	Output (SO) hold time		3.3 V	0			ns

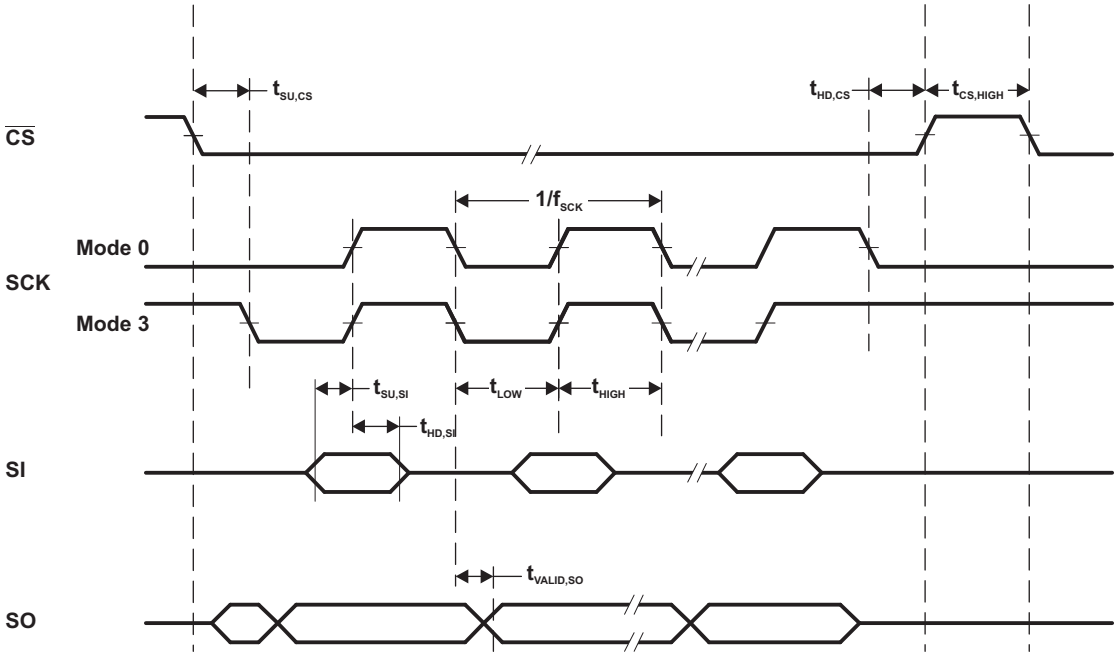


Figure 11. SPI Mode Timing

RF143B, Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDH}	Antenna rectified voltage	Peak voltage limited by antenna limiter	3.0	3.3	3.6	V
I_{DDH}	Antenna load current	RMS, without limiter current			100	µA
C_{IN}	Input capacitance	ANT1 to ANT2, 2 V RMS	31.5	35	38.5	pF

RF143B, ISO14443B ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR_{10}	Input signal data rate 10% downlink modulation, 7% to 30% ASK, ISO1443B		106	848	kbps
m10	Modulation depth 10%, tested as defined in ISO10373	7		30	%

RF143B, ISO14443B Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{PICC}	Uplink subcarrier modulation frequency	0.2		1	MHz
V_{A_MOD}	Modulated antenna voltage, V_{A_unmod} = 2.3 V	0.5			V
V_{SUB14}	Uplink modulation subcarrier level, ISO14443B: H = 1.5 to 7.5 A/m	$22/H^{0.5}$			mV

RF143B, Power Supply

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LIM}	Limiter clamping voltage	I_{LIM} ≤ 70 mA RMS, f = 13.56 MHz	3.0		3.6	V_{pk}
$I_{LIM,MAX}$	Maximum limiter current				70	mA

REVISION HISTORY

REVISION	COMMENTS
SLAS916	Product Preview release
SLAS916A	Production Data release

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RF430CL330HCPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL330H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

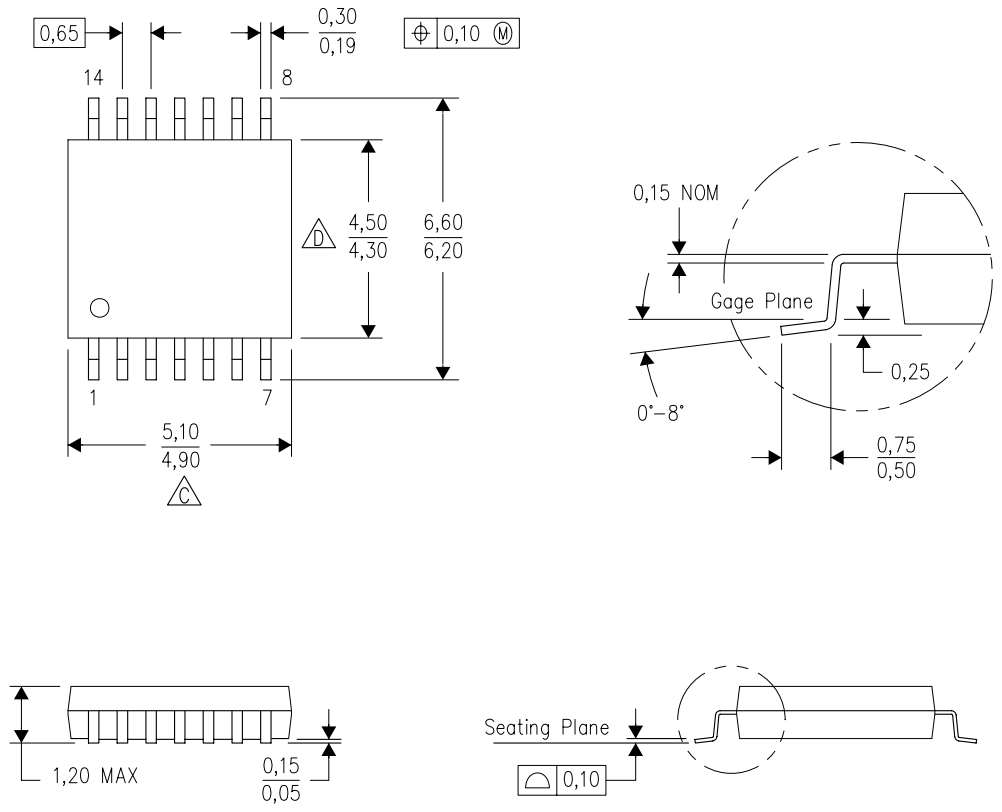
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

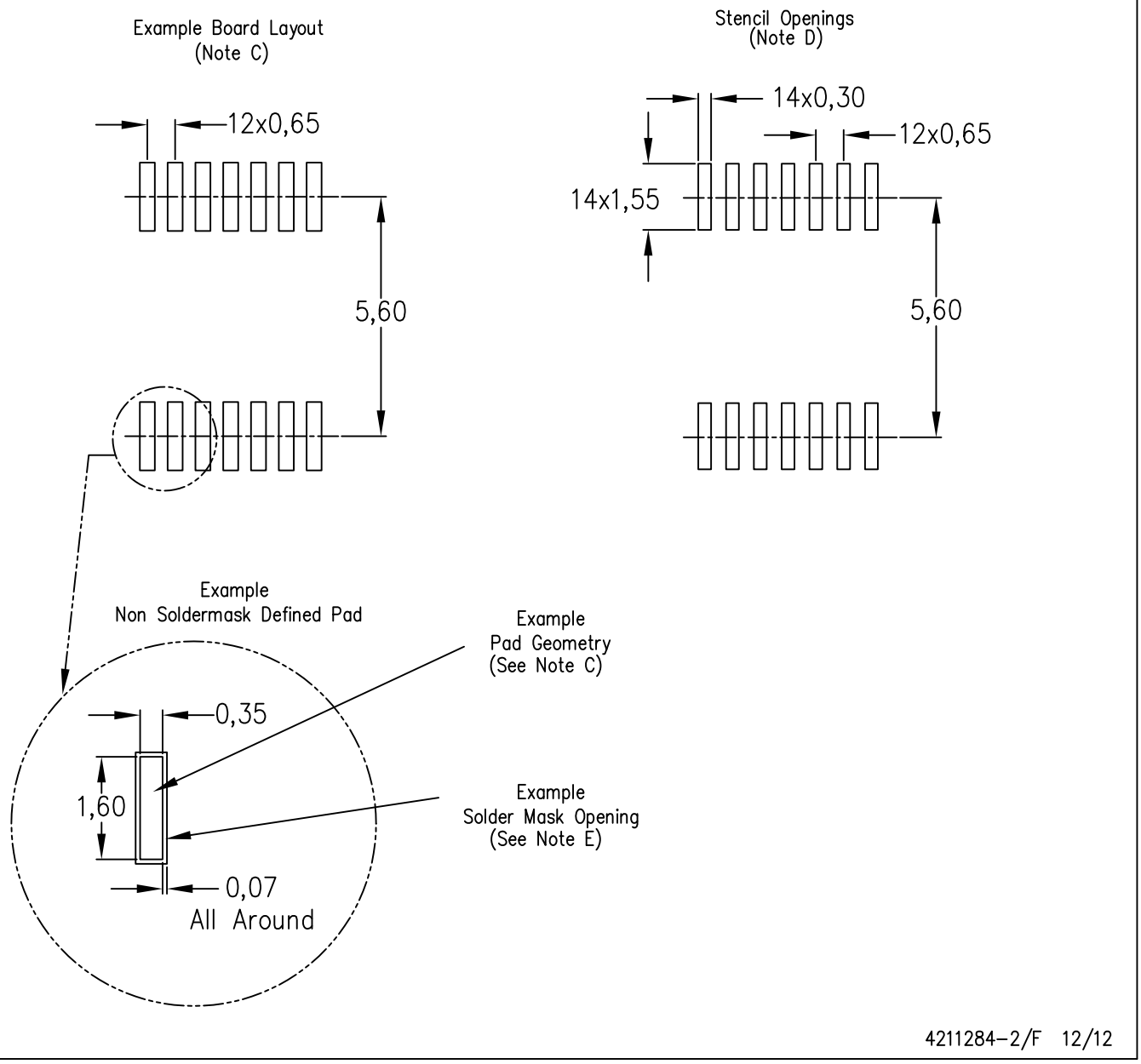
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265