Dual Channel 12-Bit 900Msps Analog-to-Digital Converter

Check for Samples: ADS5409

FEATURES

- **Dual Channel**
- **12-Bit Resolution**
- **Maximum Clock Rate: 900 Msps**
- **Low Swing Full-Scale Input: 1.0 Vpp**
- **Analog Input Buffer with High Impedance Input**
- **Input Bandwidth (3dB): >1.2GHz**
- **Data Output Interface: DDR LVDS**
- **Optional 2x Decimation with Low Pass or High Pass Filter**
- **196-Pin BGA Package (12x12mm)**
- **KEY SPECIFICATIONS**
  - **Power Dissipation: 1.1W/ch**
  - **Spectral Performance at f_{in} = 230 MHz IF**
    - **SNR: 61.0 dBFS**
    - **SFDR: 76 dBc**
  - **Spectral Performance at f_{in} = 700 MHz IF**
    - **SNR: 59.4 dBFS**
    - **SFDR: 70 dBc**

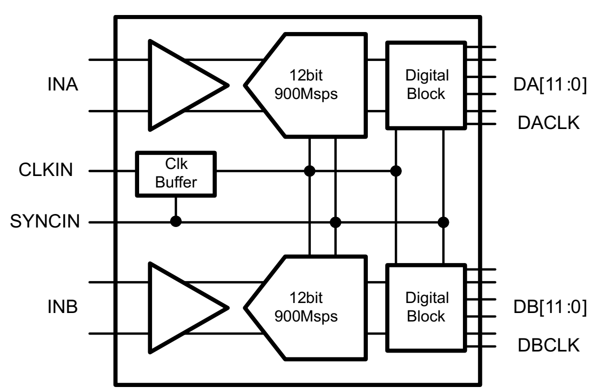
APPLICATIONS

- **Test and Measurement Instrumentation**
- **Ultra-Wide Band Software Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Signal Intelligence and Jamming**
- **Radar and Satellite Systems**
- **Microwave Receivers**
- **Cable Infrastructure**
- **Non-Destructive Testing**

Device Part No.	Number of Channels	Speed Grade
ADS5402	2	800Msps
ADS5401	1	800Msps
ADS5404	2	500Msps
ADS5403	1	500Msps
ADS5407	2	500Msps
ADS5409	2	900Msps

DESCRIPTION

The ADS5409 is a high linearity dual channel 12-bit, 900 Msps analog-to-digital converter (ADC) easing front end filter design for wide bandwidth receivers. The analog input buffer isolates the internal switching of the on-chip track-and-hold from disturbing the signal source as well as providing a high-impedance input. Optionally the output data can be decimated by two. Designed for high SFDR, the ADC has low-noise performance and outstanding spurious-free dynamic range over a large input-frequency range. The device is available in a 196pin BGA package and is specified over the full industrial temperature range (–40°C to 85°C).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DETAILED BLOCK DIAGRAM

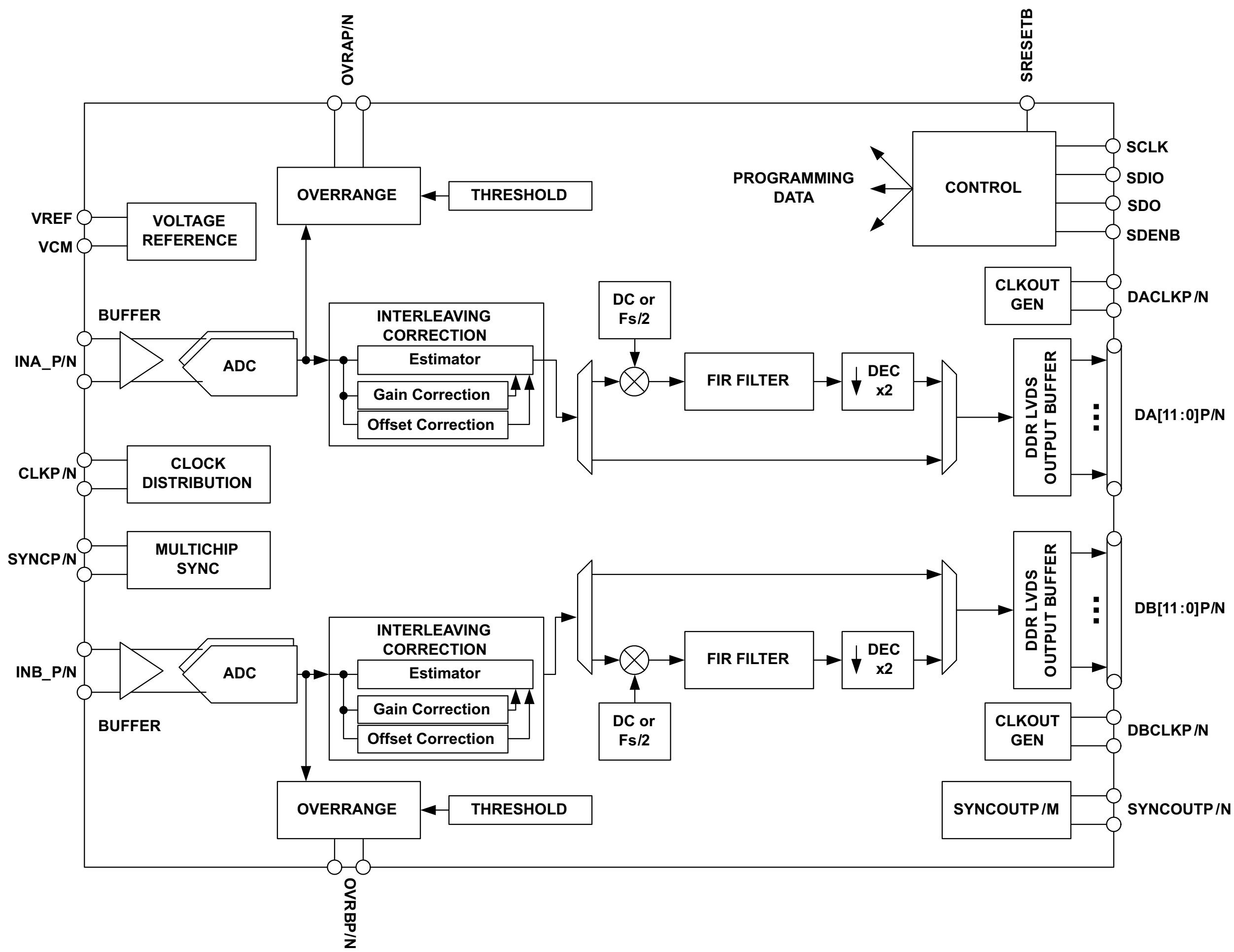


Figure 1. Detailed Block Diagram

PINOUT INFORMATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	VREF	VCM	GND	INB_N	INB_P	GND	AVDDC	AVDDC	GND	INA_P	INA_N	GND	GND	CLKINP	14
13	SDENB	TEST MODE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CLKINN	13
12	SCLK	SRESET B	GND	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	GND	AVDD33	AVDD33	12
11	SDIO	ENABLE	GND	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	GND	AVDD18	AVDD18	11
10	SDO	IOVDD	GND	AVDD18	GND	GND	GND	GND	GND	GND	AVDD18	GND	NC	NC	10
9	DVDD	DVDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	SYNCN	SYNCP	9
8	DVDD	DVDD	DVDD	DVDD	GND	GND	GND	GND	GND	GND	DVDD	DVDD	DVDD	DVDD	8
7	DB0N	DB0P	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	NC	NC	7
6	DB1N	DB1P	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	NC	NC	6
5	DB2N	DB2P	OVRBN	OVRBP	GND	GND	GND	GND	GND	GND	OVRAN	OVRAP	SYNC OUTN	SYNC OUTP	5
4	DB3N	DB3P	DB8P	DB10P	NC	NC	NC	DA0P	DA2P	DA4P	DA6P	DA8P	NC	NC	4
3	DB4N	DB4P	DB8N	DB10N	NC	NC	NC	DA0N	DA2N	DA4N	DA6N	DA8N	DA11N	DA11P	3
2	DB5N	DB5P	DB7P	DB9P	DB11P	SYNC OUTP	DBCLKP	DACLKP	DA1P	DA3P	DA5P	DA7P	DA10N	DA10P	2
1	DB6N	DB6P	DB7N	DB9N	DB11N	SYNC OUTN	DBCLKN	DACLKN	DA1N	DA3N	DA5N	DA7N	DA9N	DA9P	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 2. Pinout in DDR output mode (top down view)

PIN ASSIGNMENTS

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INA_P/N	K14, L14	I	Analog ADC A differential input signal.
INB_P/N	D14, E14	I	Analog ADC B differential input signal.
VCM	B14	O	Output of the analog input common mode (nominally 1.9V). A 0.1µF capacitor to AGND is recommended.
VREF	A14	O	Reference voltage output (2V nominal). A 0.1µF capacitor to AGND is recommended, but not required.
CLOCK/SYNC			
CLKINP/N	P14, P13	I	Differential input clock
SYNCP/N	P9, N9	I	Synchronization input. Inactive if logic low. When clocked in a high state initially, this is used for resetting internal clocks and digital logic and starting the SYNCOUT signal. Internal 100Ω termination.
CONTROL/SERIAL			
SRESET	B12	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal 50kΩ pull up resistor to IOVDD.

PIN ASSIGNMENTS (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ENABLE	B11	I	Chip enable – active high. Power down function can be controlled through SPI register assignment. Internal 50kΩ pull up resistor to IOVDD.
SCLK	A12	I	Serial interface clock. Internal 50kΩ pull-down resistor.
SDIO	A11	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register x00, D16), the SDIO pin is an input only. Internal 50kΩ pull-down.
SDENB	A13	I	Serial interface enable. Internal 50kΩ pull-down resistor.
SDO	A10	O	Uni-directional serial interface data in 4 pin mode (register x00, D16). The SDO pin is tri-stated in 3-pin interface mode (default). Internal 50kΩ pull-down resistor.
TESTMODE	B13	–	Factory internal test, do not connect
DATA INTERFACE			
DA[11:0]P/N	P3, N3, P2, N2, P1, N1, M4, M3, M2, M1, L4, L3, L2, L1, K4, K3, K2, K1, J4, J3, J2, J1, H4, H3	O	ADC A Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output.
DB[11:0]P/N	E2, E1, D4, D3, D2, D1, C4, C3, C2, C1, B1, A1, B2, A2, B3, A3, B4, A4, B5, A5, B6, A6, B7, A7	O	ADC B Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output.
DACLKP/N	H2, H1	O	DDR differential output data clock for Bus A. Register programmable to provide either rising or falling edge to center of stable data nominal timing.
DBCLKP/N	G2, G1	O	DDR differential output data clock for Bus B. Register programmable to provide either rising or falling edge to center of stable data nominal timing. Optionally Bus B can be latched with DACLKP/N.
SYNCOUTP/N	F2, F1, P5, N5	O	Synchronization output signal for synchronizing multiple ADCs. Can be disabled via SPI.
OVRAP/N	M5, L5	O	Bus A, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output.
OVRBP/N	D5, C5	O	Bus B, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output.
NC	E3, E4, F3, F4, G3, G4, N4, N6, N7, N10, P4, P6, P7, P10	–	Don't connect to pin
POWER SUPPLY			
AVDD33	D12, E12, F12, G12, H12, J12, K12, L12, N12, P12	I	3.3V analog supply
AVDDC	G14, H14	I	1.8V supply for clock input
AVDD18	D10, D11, E11, F11, G11, H11, J11, K11, L10, L11, N11, P11	I	1.8V analog supply
DVDD	A8, A9, B8, B9, C8, D8, L8, M8, N8, P8	I	1.8V supply for digital block
DVDDLVDS	C6, C7, D6, D7, L6, L7, M6, M7	I	1.8V supply for LVDS outputs
IOVDD	B10	I	1.8V for digital I/Os
GND		I	Ground

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/ BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5409	196-BGA	ZAY	–40C to 85C	GREEN (RoHS & no Sb/Br)		ADS5409I	ADS5409IZAY	Tray
							ADS5409IZAYR	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, AVDD33		–0.5	4	V
Supply voltage range, AVDDC		–0.5	2.3	V
Supply voltage range, AVDD18		–0.5	2.3	V
Supply voltage range, DVDD		–0.5	2.3	V
Supply voltage range, DVDDLVDS		–0.5	2.3	V
Supply voltage range, IOVDD		–0.5	4	V
Voltage applied to input pins	INA/B_P, INA/B_N	–0.5	AVDD33 + 0.5	V
	CLKINP, CLKINN	–0.5	AVDDC + 0.5	V
	SYNCP, SYNCN	–0.5	AVDD33 + 0.5	V
	SRESET, SDENB, SCLK, SDIO, SDO, ENABLE	–0.5	IOVDD + 0.5	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			150	°C
Storage temperature range		–65	150	°C
ESD, Human Body Model			2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS5409 nFBGA 196 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	6.8	
θ_{JB}	Junction-to-board thermal resistance(4)	16.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Recommended operating junction temperature			105	°C
	Maximum rated operating junction temperature (1)	125			
T_A	Recommended free-air temperature	–40	25	85	°C

(1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ADC Clock Frequency			100		900	MSPS
Resolution			12			Bits
SUPPLY						
AVDD33			3.15	3.3	3.45	V
AVDDC, AVDD18, DVDD, DVDDLVDS			1.7	1.8	1.9	V
IOVDD			1.7	1.8	3.45	V
POWER SUPPLY						
I_{AVDD33}	3.3V Analog supply current			325	365	mA
I_{AVDD18}	1.8V Analog supply current			106	120	mA
I_{AVDDC}	1.8V Clock supply current			46	60	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Enabled		370	420	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled		214		mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled, decimation filter enabled		254		mA
$I_{DVDDLVDS}$	1.8V LVDS supply current			150	170	mA
I_{IOVDD}	1.8V I/O Voltage supply current			1	2	mA
P_{dis}	Total power dissipation	Auto Correction Enabled, decimation filter disabled		2.27	2.6	W
P_{dis}	Total power dissipation	Auto Correction Disabled, decimation filter disabled		1.9		W
PSRR		250kHz to 500MHz	40			dB
Shut-down power dissipation				7		mW
Shut-down wake up time				2.5		ms
Standby power dissipation				7		mW
Standby wake up time				100		µs
Deep-sleep mode power dissipation		Auto correction disabled		435		mW
		Auto correction enabled		570		mW
Deep-sleep mode wakeup time				20		µs
Light-sleep mode power dissipation		Auto correction disabled		770		mW
		Auto correction enabled		900		mW
Light-sleep mode wakeup time				2		µs

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS					
Differential input full-scale			1.0	1.25	Vpp
Input common mode voltage			1.9 ±0.1		V
Input resistance	Differential at DC		1		kΩ
Input capacitance	Each input to GND		2		pF
VCM common mode voltage output			1.9		V
Analog input bandwidth (3dB)			1200		MHz
DYNAMIC ACCURACY					
Offset Error	Auto Correction Disabled	-20	±6	20	mV
	Auto Correction Enabled	-1	0	1	mV
Offset temperature coefficient			-10		µV/°C
Gain error		-10	±2	10	%FS
Gain temperature coefficient			0.003		%FS/°C
Differential nonlinearity	f_{IN} = 230 MHz	-1	±0.8	2	LSB
Integral nonlinearity	f_{IN} = 230 MHz	-10	±0.5	10	LSB
CLOCK INPUT					
Input clock frequency		100		900	MHz
Input clock amplitude			2		Vpp
Input clock duty cycle		40	50	60	%
Internal clock biasing			0.9		V

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Auto Correction				Enabled			Disabled		Vpp
DYNAMIC AC CHARACTERISTICS (1)									
SNR	Signal to Noise Ratio (excluding Fs/2-Fin spur)	f_{IN} = 10 MHz		61.5			61.5		dBFS
		f_{IN} = 100 MHz		61.5			61.4		
		f_{IN} = 230 MHz	58	61.0			61.0		
		f_{IN} = 400 MHz		60.2			60.3		
		f_{IN} = 700 MHz		59.4			59.8		
HD2,3	Second and third harmonic distortion	f_{IN} = 10 MHz		78			81		dBc
		f_{IN} = 100 MHz		77			80		
		f_{IN} = 230 MHz	65	77			77		
		f_{IN} = 400 MHz		71			72		
		f_{IN} = 700 MHz		75			76		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion and Fs/2 – F_{IN} spur)	f_{IN} = 10 MHz		78			78		dBc
		f_{IN} = 100 MHz		79			78		
		f_{IN} = 230 MHz	65	79			79		
		f_{IN} = 400 MHz		76			76		
		f_{IN} = 700 MHz		72			77		
IL	Fs/2-Fin interleaving spur	f_{IN} = 10 MHz		88			80		dBc
		f_{IN} = 100 MHz		80			77		
		f_{IN} = 230 MHz	63	76			71		
		f_{IN} = 400 MHz		72			68		
		f_{IN} = 700 MHz		70			66		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		61.3			61.3		dBFS
		f_{IN} = 100 MHz		61.2			61.2		
		f_{IN} = 230 MHz	56	60.9			60.8		
		f_{IN} = 400 MHz		59.7			59.8		
		f_{IN} = 700 MHz		59.2			59.5		
THD	Total Harmonic Distortion	f_{IN} = 10 MHz		74			74		dBc
		f_{IN} = 100 MHz		73			74		
		f_{IN} = 230 MHz	63	75			74		
		f_{IN} = 400 MHz		68			68		
		f_{IN} = 700 MHz		72			72		
IMD3	Inter modulation distortion	F_{in} = 229.5 and 230.5 MHz, -7dBFS		79			77		dBFS
		F_{in} = 649.5 and 650.5 MHz, -7dBFS		73			71		
	Crosstalk			90			90		dB
ENOB	Effective number of bits	f_{IN} = 230 MHz		9.8			9.8		Bit

(1) SFDR and SNR calculations do not include the DC or Fs/2 bins when Auto Correction is disabled.

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVER-DRIVE RECOVERY ERROR						
	Input overload recovery	Recovery to within 5% (of final value) for 6dB overload with sine wave input		2		Output Clock
SAMPLE TIMING CHARACTERISTICS						
rms	Aperture Jitter	Sample uncertainty		100		fs rms
	Data Latency	ADC sample to digital output, auto correction disabled		38		Clock Cycles
		ADC sample to digital output, auto correction enabled		50		
		ADC sample to digital output, Decimation filter enabled, Auto correction disabled		74		Sampling Clock Cycles
	Over-range Latency	ADC sample to over-range output		12		Clock Cycles

ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS – SRESET, SCLK, SDENB, SDIO, ENABLE						
	High-level input voltage	All digital inputs support 1.8V and 3.3V logic levels.	0.7 x IOVDD			V
	Low-level input voltage				0.3 x IOVDD	V
	High-level input current		–50		200	µA
	Low-level input current		–50		50	µA
	Input capacitance			5		pF
DIGITAL OUTPUTS – SDO						
	High-level output voltage	Iload = -100µA	IOVDD – 0.2			V
		Iload = -2mA	0.8 x IOVDD			
	Low-level output voltage	Iload = 100µA			0.2	V
		Iload = 2mA			0.22 x IOVDD	
DIGITAL INPUTS – SYNCP/N						
V_{ID}	Differential input voltage		250	350	450	mV
V_{CM}	Input common mode voltage		1.125	1.2	1.375	V
t_{SU}			500			ps
DIGITAL OUTPUTS – DA[11:0]P/N, DACLKP/N, OVRAP/N, SYNCOUTP/N, DB[11:0]P/N, DBCLKP/N, OVRBP/N						
V_{OD}	Output differential voltage	Iout = 3.5mA	250	350	450	mV
V_{OCM}	Output common mode voltage	Iout = 3.5mA	1.125	1.25	1.375	V
t_{su}		F_s = 900Msps, Data valid to zero-crossing of DACLK, DBCLK	230	336		ps
t_h		F_s = 900Msps, Zero-crossing of DACLK, DBCLK to data becoming invalid	230	380		ps
t_{PD}		F_s = 900Msps, CLKIN falling edge to DACLK, DBCLK rising edge	3.36	3.69	3.92	ns
t_{RISE}		10% - 90%	100	150	200	ps
t_{FALL}		90% - 10%	100	150	200	ps

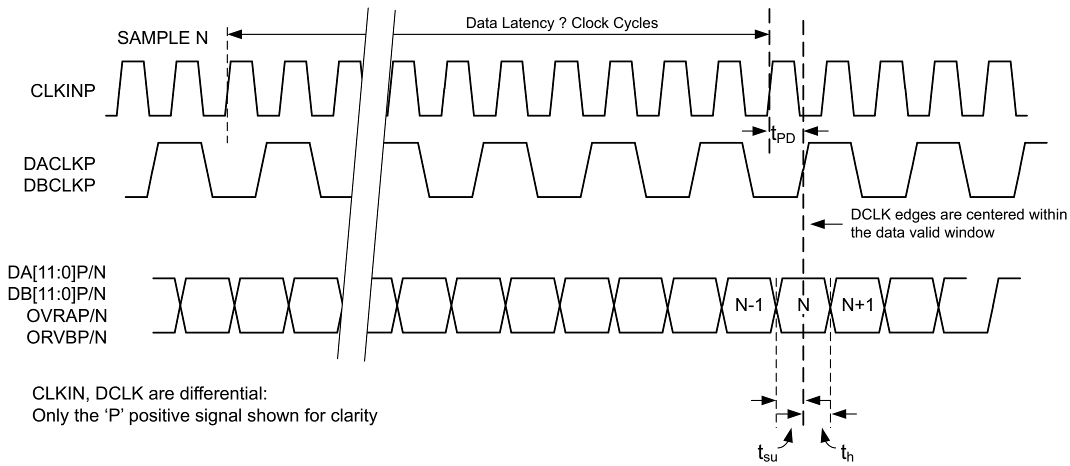


Figure 3. Timing Diagram for 12-bit DDR Output

TYPICAL CHARACTERISTICS

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

FFT FOR 10 MHz INPUT SIGNAL (auto on)

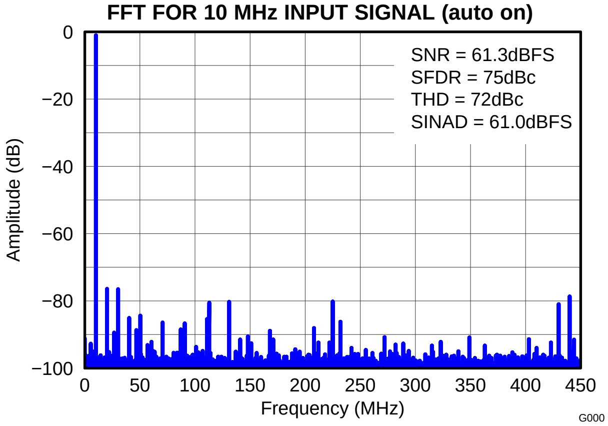


Figure 4.

FFT FOR 10 MHz INPUT SIGNAL (auto off)

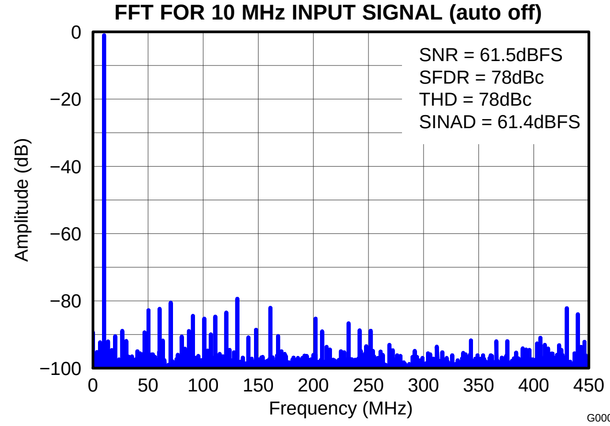


Figure 5.

FFT FOR 230 MHz INPUT SIGNAL (auto on)

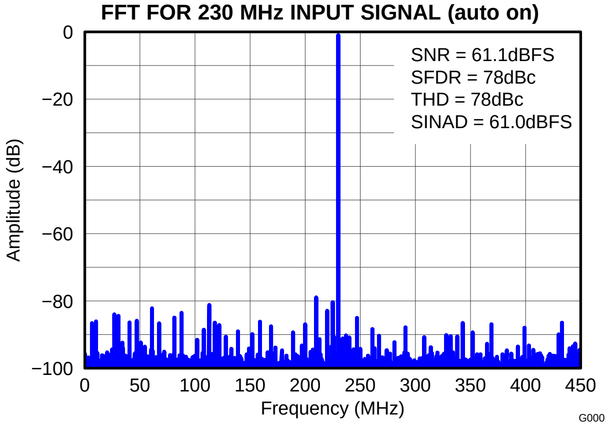


Figure 6.

FFT FOR 230 MHz INPUT SIGNAL (auto off)

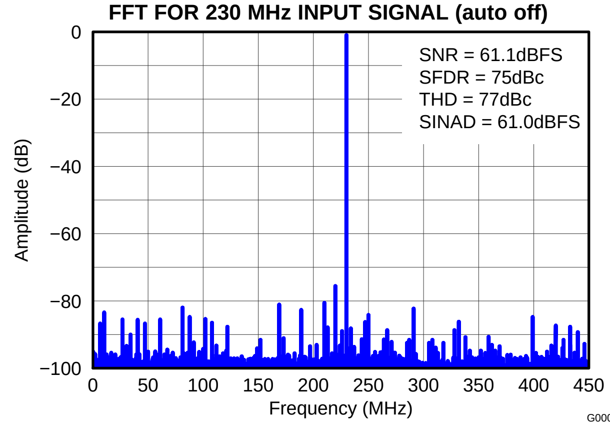


Figure 7.

FFT FOR 400 MHz INPUT SIGNAL (auto on)

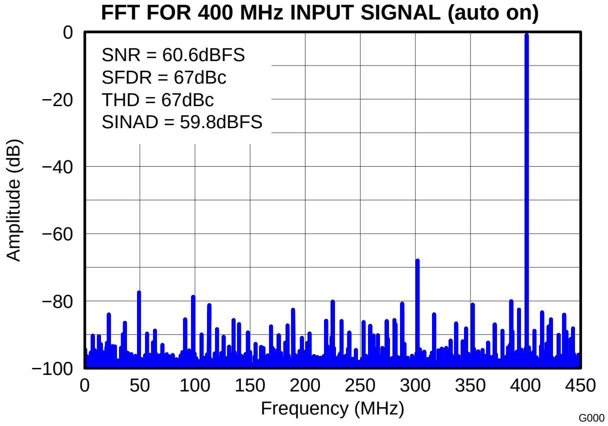


Figure 8.

FFT FOR 400 MHz INPUT SIGNAL (auto off)

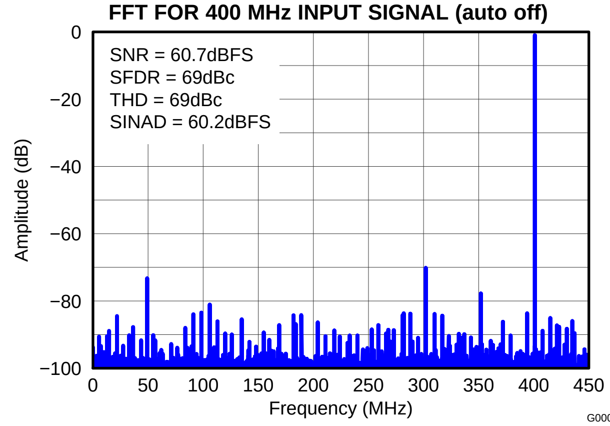


Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

FFT FOR 700 MHz INPUT SIGNAL (auto on)

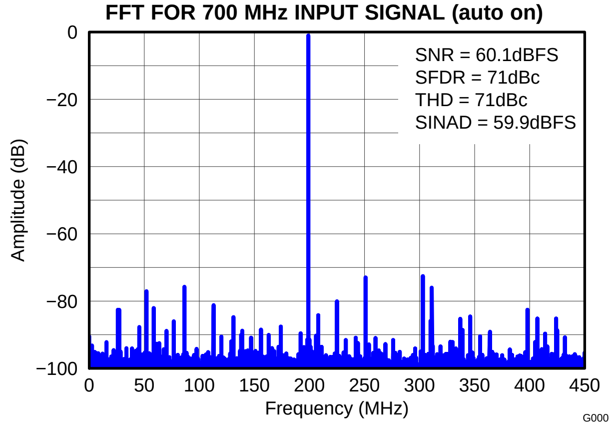


Figure 10.

FFT FOR 700 MHz INPUT SIGNAL (auto off)

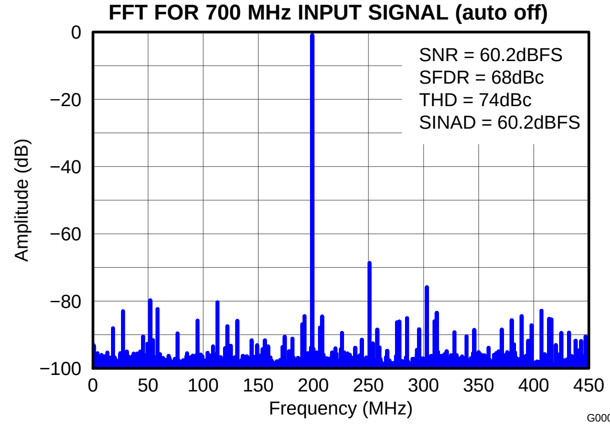


Figure 11.

FFT FOR TWO TONE INPUT SIGNAL (auto on)

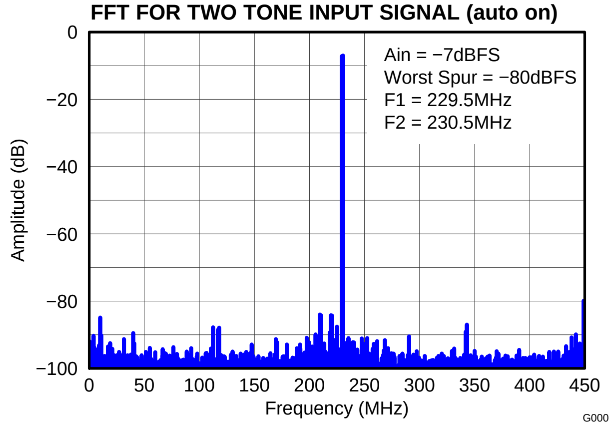


Figure 12.

FFT FOR TWO TONE INPUT SIGNAL (auto off)

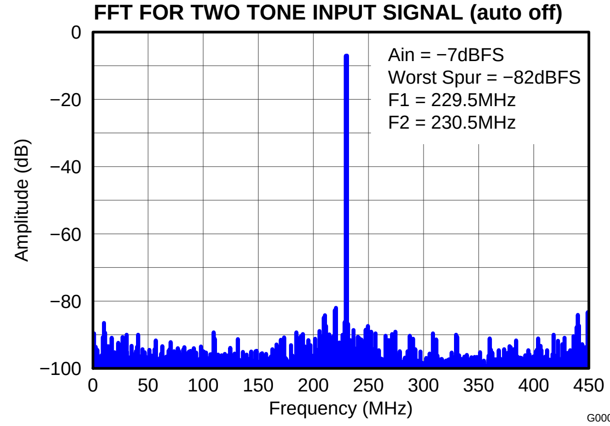


Figure 13.

SFDR vs INPUT FREQUENCY

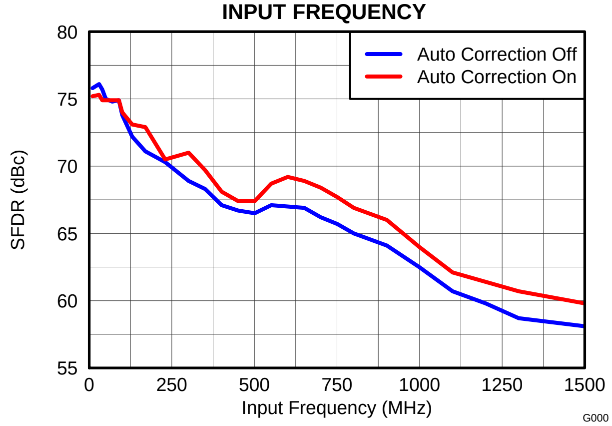


Figure 14.

SNR vs INPUT FREQUENCY

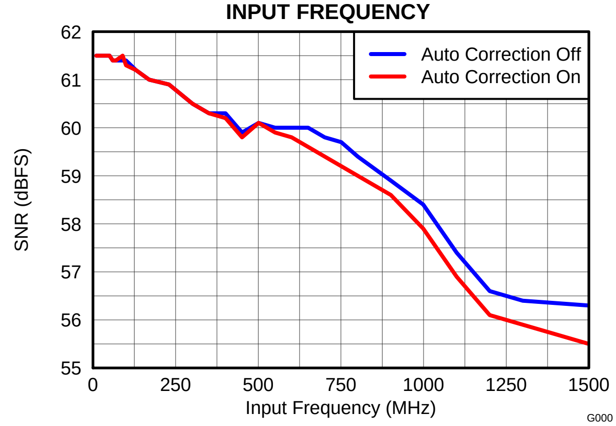


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

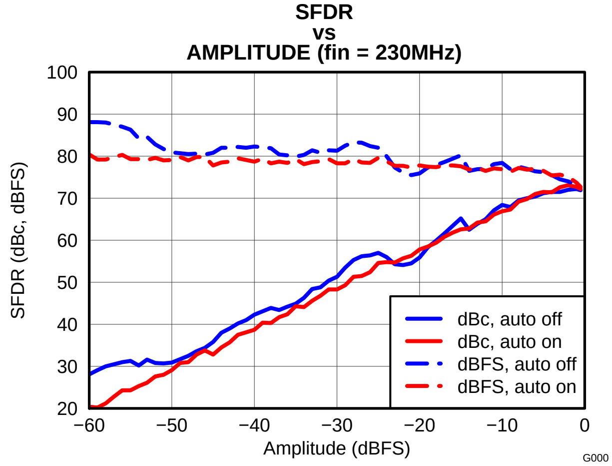


Figure 16.

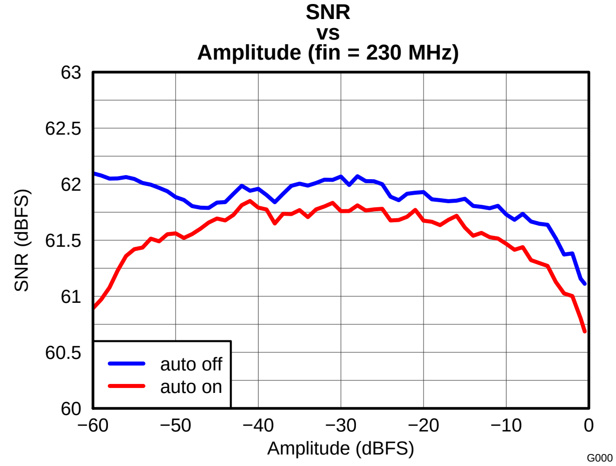


Figure 17.

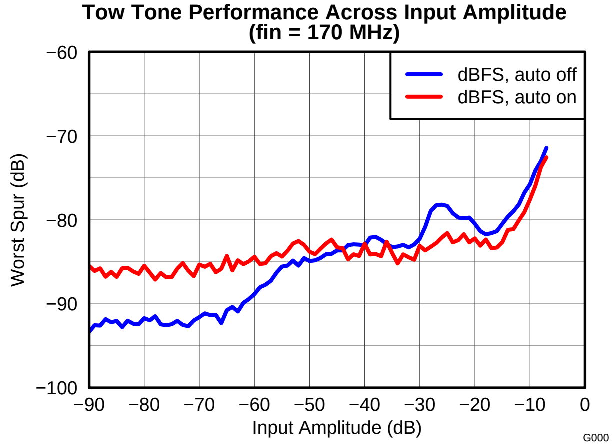


Figure 18.

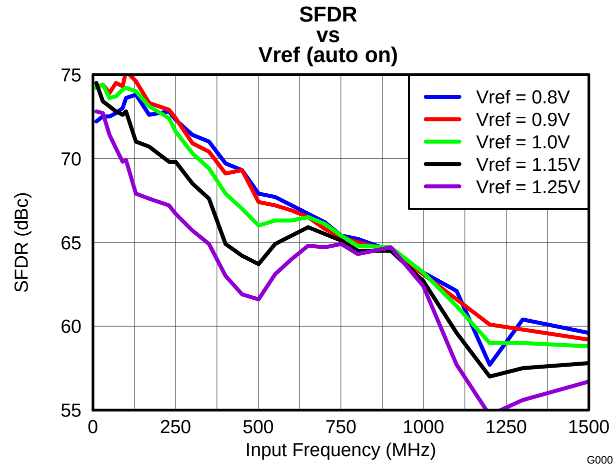


Figure 19.

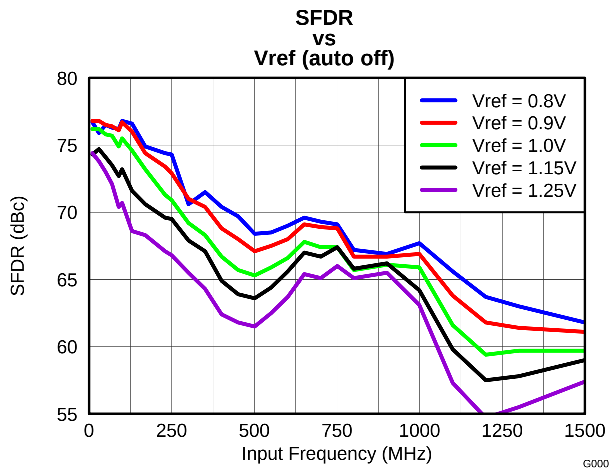


Figure 20.

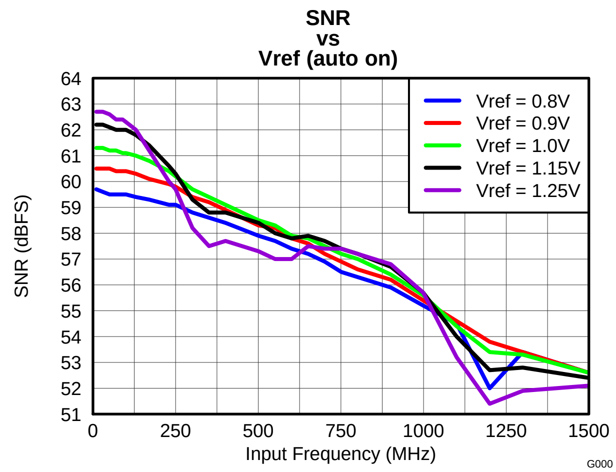


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

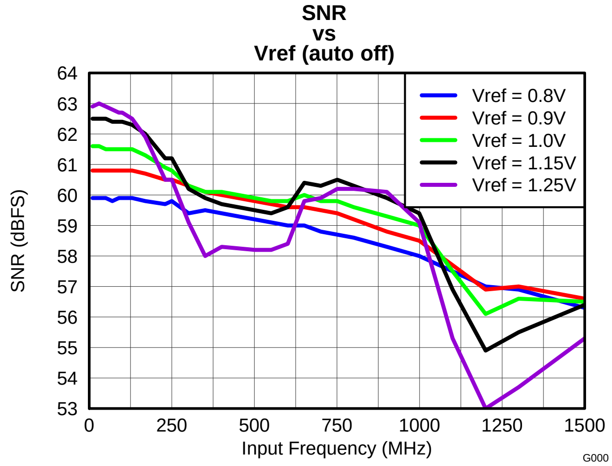


Figure 22.

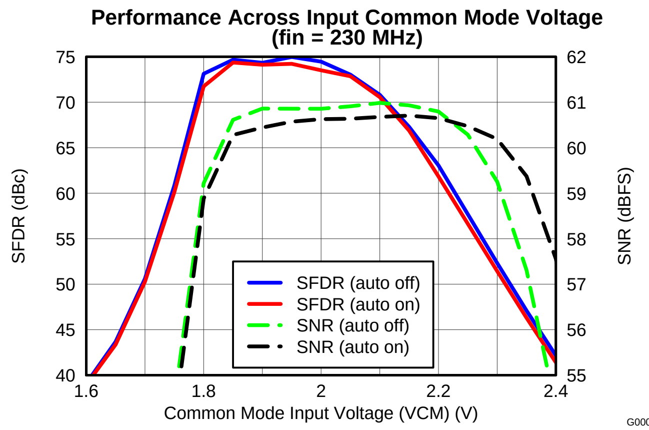


Figure 23.

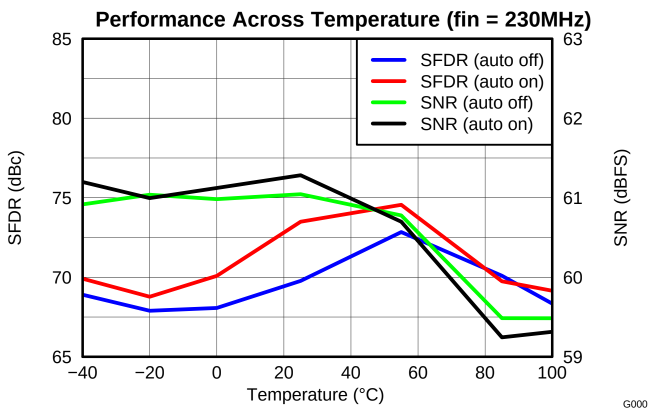


Figure 24.

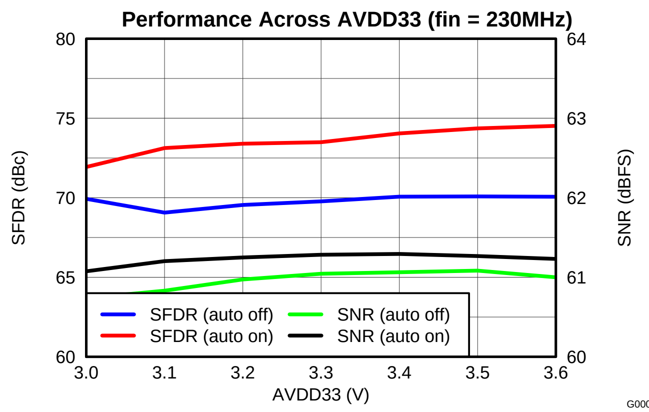


Figure 25.

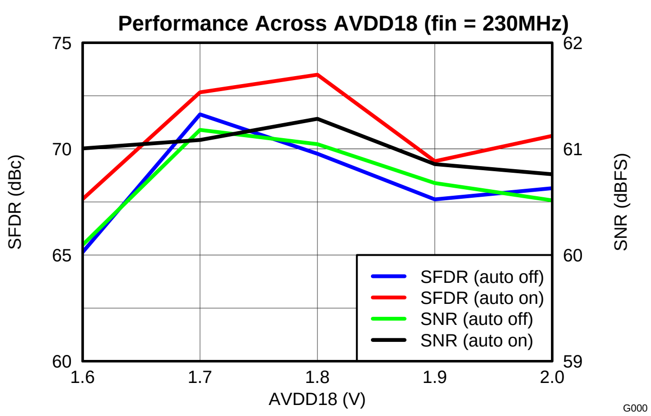


Figure 26.

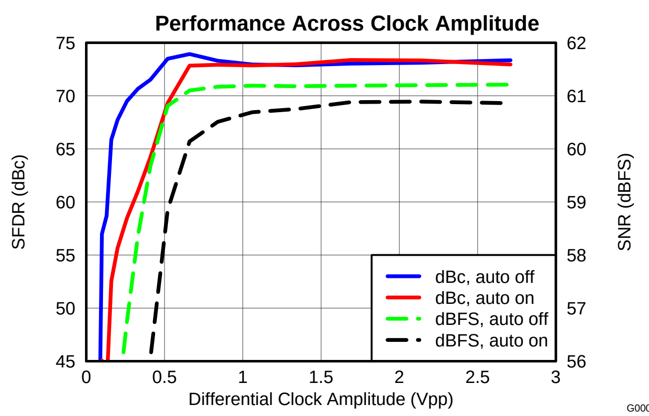


Figure 27.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

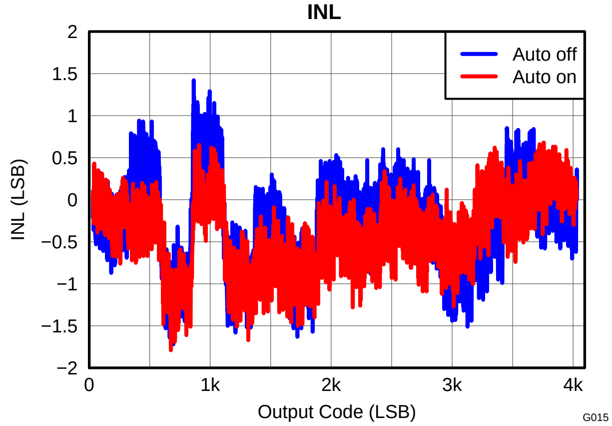


Figure 28.

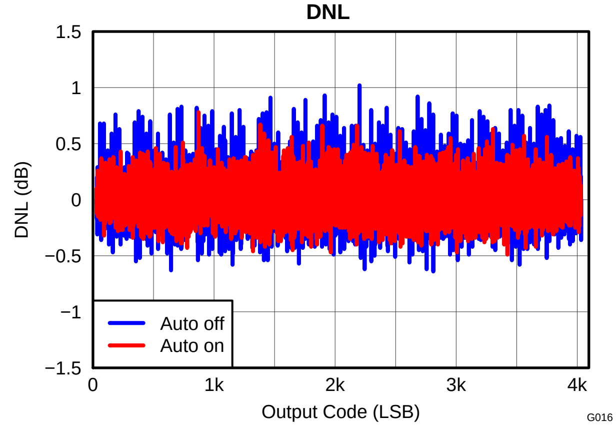


Figure 29.

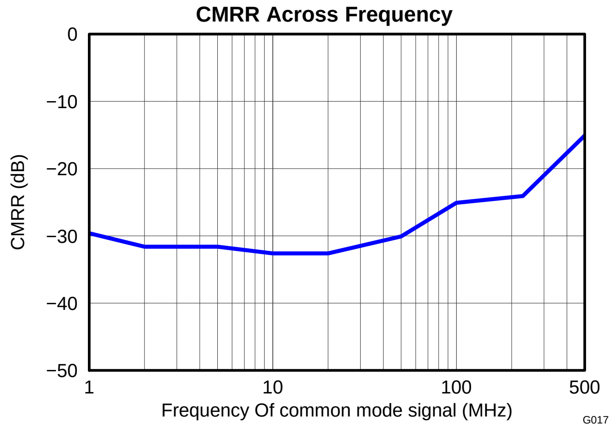


Figure 30.

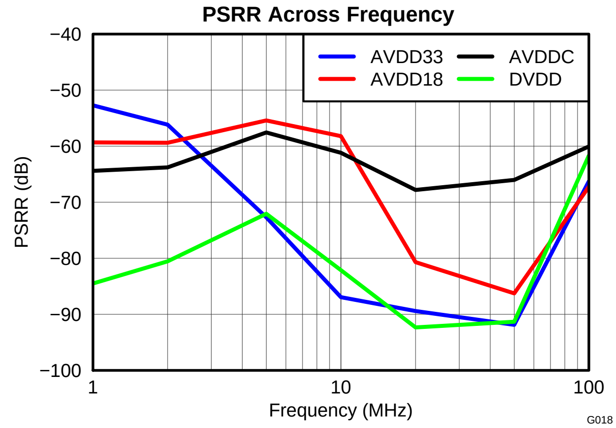


Figure 31.

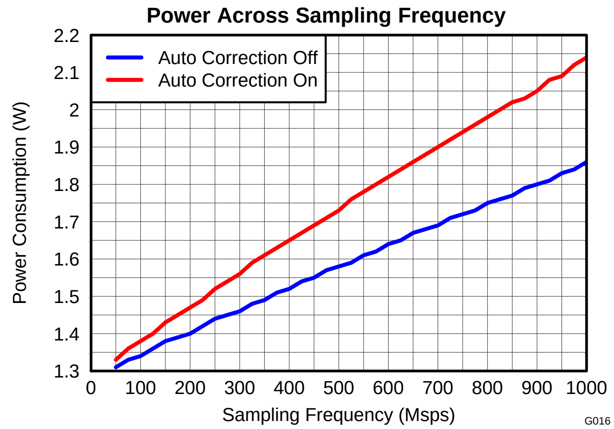


Figure 32.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SFDR Across Input and Sampling Frequencies (auto on)

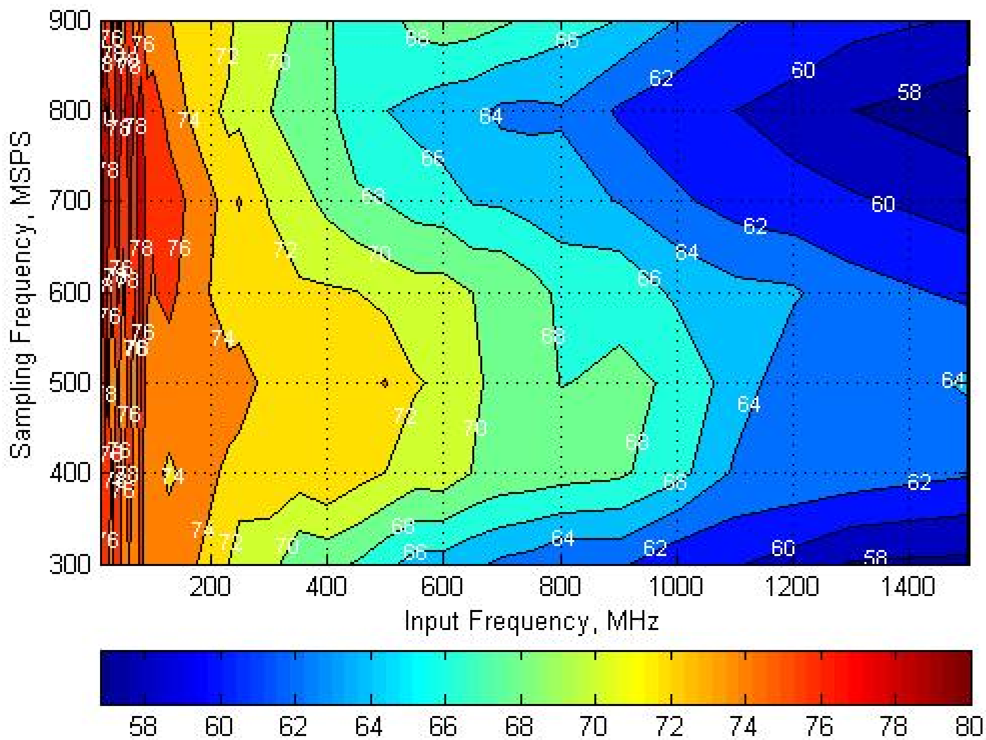


Figure 33.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SFDR Across Input and Sampling Frequencies (auto off)

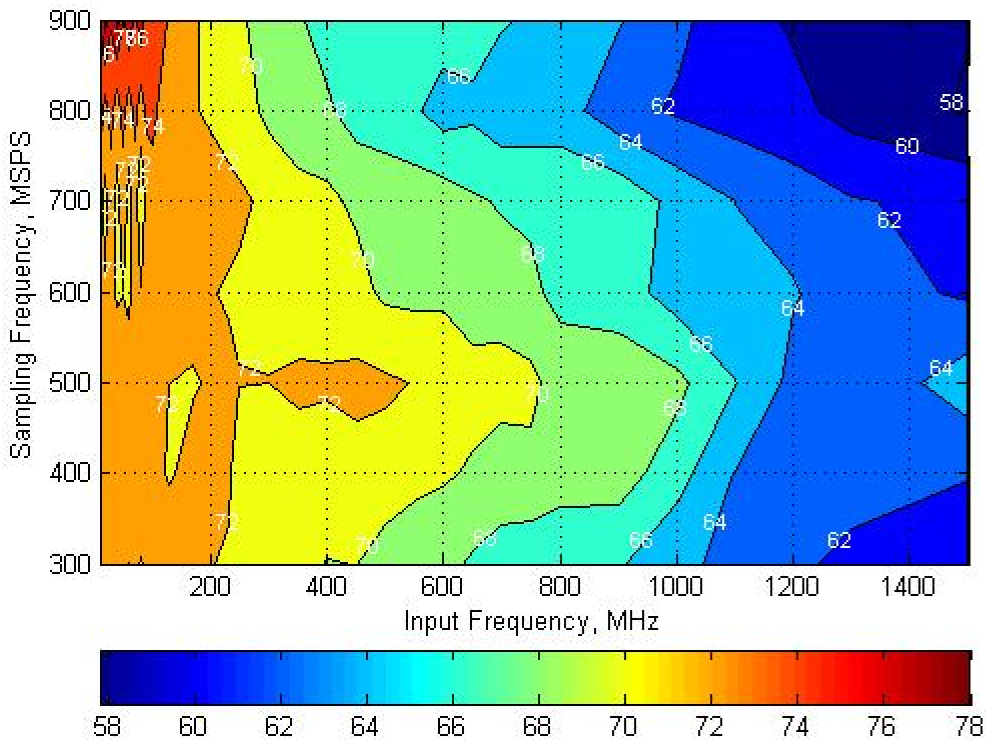


Figure 34.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SNR Across Input and Sampling Frequencies (auto on)

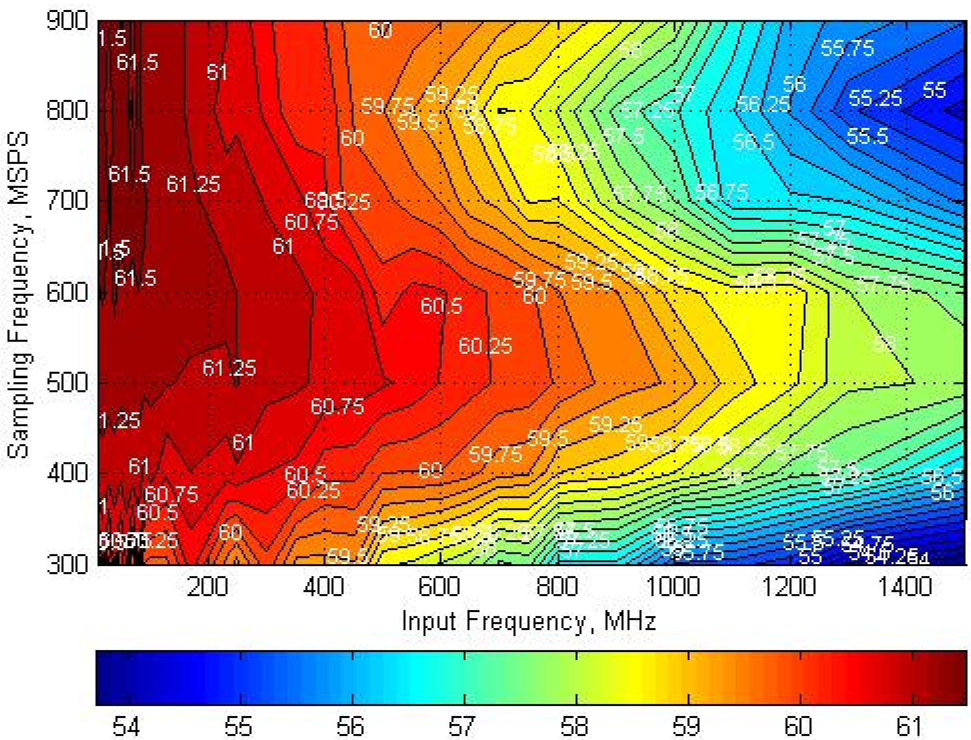


Figure 35.

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 900Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SNR Across Input and Sampling Frequencies (auto on)

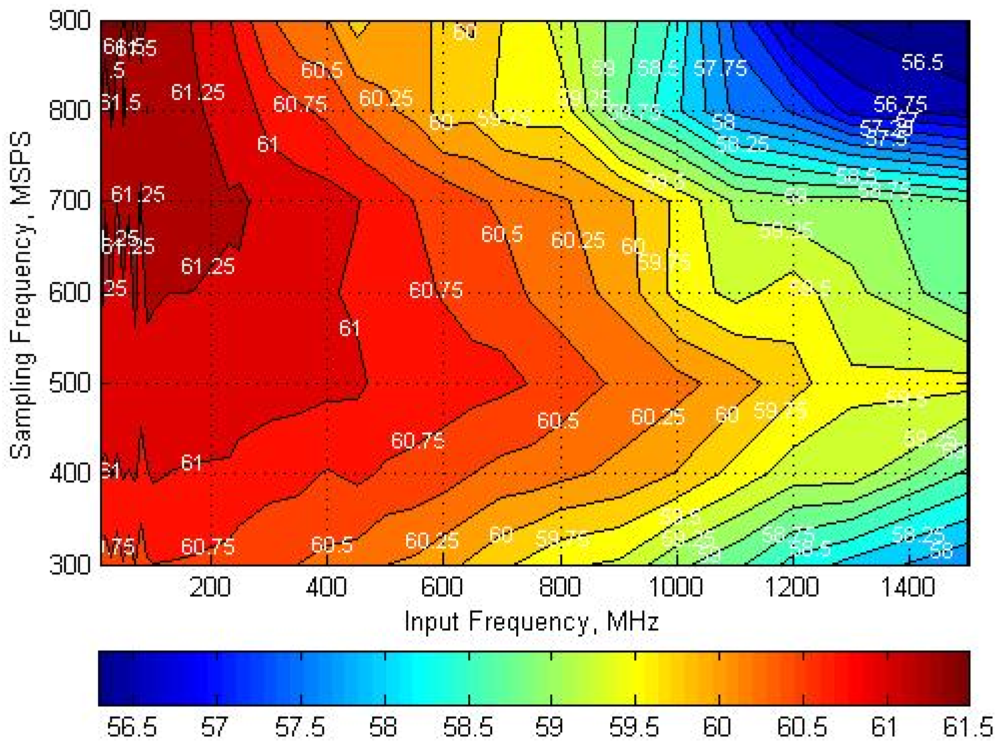


Figure 36.

DESCRIPTION

POWER DOWN MODES

The ADS5409 can be configured via SPI write (address x37) to a stand-by, light or deep sleep power mode which is controlled by the ENABLE pin. The sleep modes are active when the ENABLE pin goes low. Different internal functions stay powered up which results in different power consumption and wake up time between the two sleep modes.

Sleep mode	Wake up time	Power Consumption Auto correction disabled	Power Consumption Auto correction enabled
Complete Shut Down	2.5 ms	7mW	7mW
Stand-by	100µs	7mW	7mW
Deep Sleep	20µs	435mW	570mW
Light Sleep	2µs	770mW	900mW

TEST PATTERN OUTPUT

The ADS5409 can be configured to output different test patterns that can be used to verify the digital interface is connected and working properly. To enable the test pattern mode, the high performance mode 1 has to be disabled first via SPI register write. Then different test patterns can be selected by configuring registers x3C, x3D and x3E. All three registers must be configured for the test pattern to work properly.

First set HP1 = 0 (Addr 0x01, D01)

Register Address	All 0s	All 1s	Toggle (0xAAA => 0x555)	Toggle (0xFFF => 0x000)
0x3C	0x8000	0xBFFC	0x9554	0xBFFC
0x3D	0x0000	0x3FFC	0x2AA8	0x0000
0x3E	0x0000	0x3FFC	0x1554	0x3FFC

<table>
<tr><th>Register Address</th><th colspan="16">Custom Pattern</th></tr>
<tr><th></th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>x3C</td><td>1</td><td>0</td><td rowspan="3">D11</td><td rowspan="3">D10</td><td rowspan="3">D9</td><td rowspan="3">D8</td><td rowspan="3">D7</td><td rowspan="3">D6</td><td rowspan="3">D5</td><td rowspan="3">D4</td><td rowspan="3">D3</td><td rowspan="3">D2</td><td rowspan="3">D1</td><td rowspan="3">D0</td><td>0</td><td>0</td></tr>
<tr><td>x3D</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>x3E</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

For normal operation, set HP1 = 1 (Addr 0x01, D01) and 0x3C, 0x3D, 0x3E all to 0.

CLOCK INPUT

The ADS5409 clock input can be driven differentially with a sine wave, LVPECL or LVDS source with little or no difference in performance. The common mode voltage of the clock input is set to 0.9V using internal 2kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.

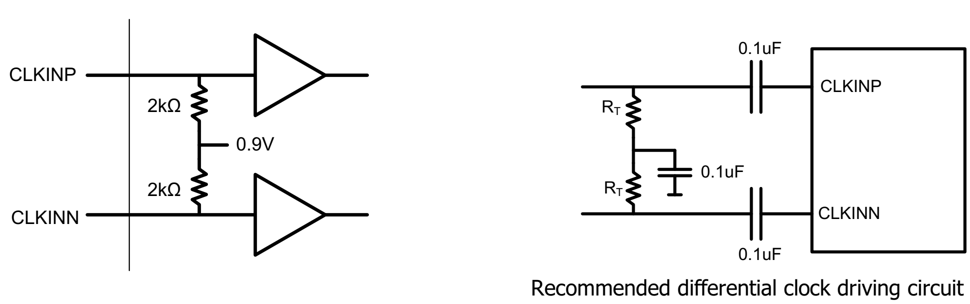


Figure 37. Recommended Differential Clock Driving Circuit

SNR AND CLOCK JITTER

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 74dB for a 12bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantization\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{ThermalNoise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated as following:

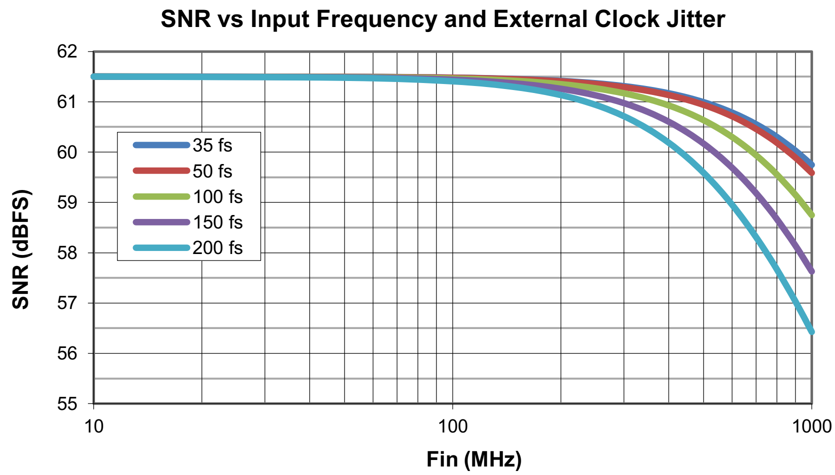
$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{in} \times T_{Jitter}) \quad (2)$$

The total clock jitter (TJitter) has three components – the internal aperture jitter (100fs for ADS5409) which is set by the noise of the clock input buffer, the external clock jitter and the jitter from the analog input signal. It can be calculated as following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2 + (T_{Jitter,Analog\_input})^2} \quad (3)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

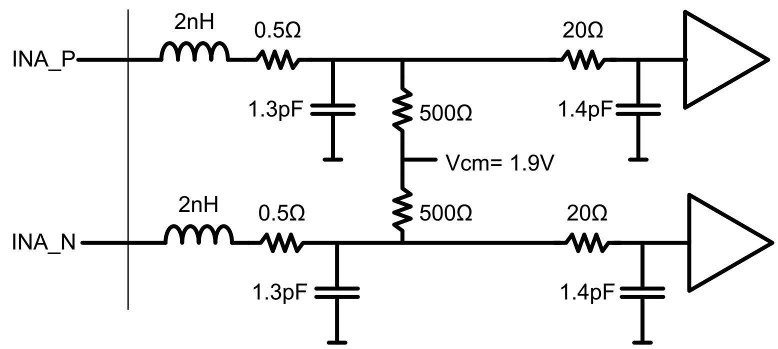
The ADS5409 has a thermal noise of 61.5 dBFS and internal aperture jitter of 100fs. The SNR depending on amount of external jitter for different input frequencies is shown in the following figure.



ANALOG INPUTS

The ADS5409 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50Ω matching for RF applications. The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

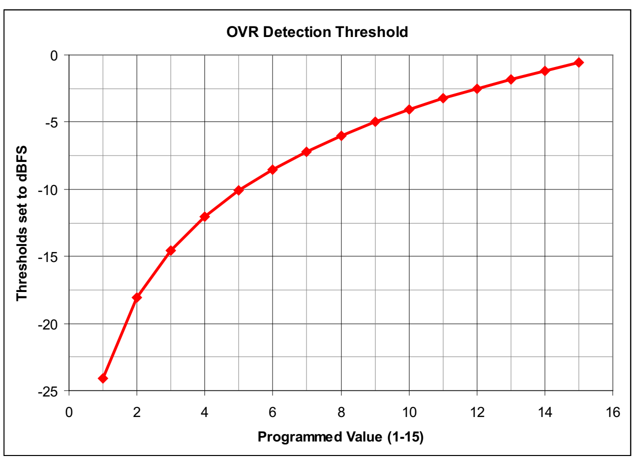
The common-mode voltage of the signal inputs is internally biased to 1.9V using 500Ω resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.25V) and (VCM – 0.25V), resulting in a 1.0Vpp (default) differential input swing. The input sampling circuit has a 3dB bandwidth that extends up to 1.2GHz.



OVER-RANGE INDICATION

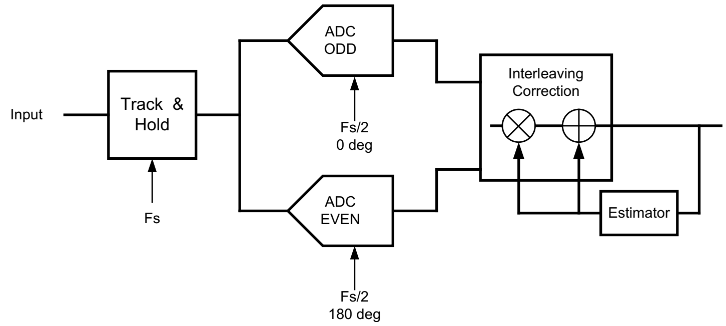
The ADS5409 provides a fast over-range indication on the OVRA/B pins. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 12 clock cycles enabling a quicker reaction to an overrange event. The OVR threshold can be configured using SPI register writes.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the Over-range threshold bits. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] /16). After reset, the default value of the over-range threshold is set to 15 (decimal) which corresponds to a threshold of 0.56dB below full scale (20*log(15/16)).



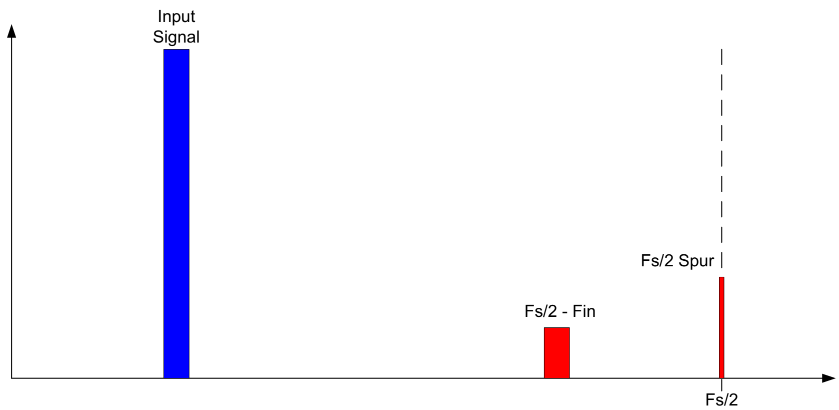
INTERLEAVING CORRECTION

Each of the two data converter channels consists of two interleaved ADCs each operating at half of the ADC sampling rate but 180º out of phase from each other. The front end track and hold circuitry is operating at the full ADC sampling rate which minimizes the timing mismatch between the two interleaved ADCs. In addition the ADS5409 is equipped with internal interleaving correction logic that can be enabled via SPI register write.



The interleaving operation creates 2 distinct and interleaving products:

- Fs/2 – Fin: this spur is created by gain timing mismatch between the ADCs. Since internally the front end track and hold is operated at the full sampling rate, this component is greatly improved and mostly dependent on gain mismatch.
- Fs/2 Spur: due to offset mismatch between ADCs



The auto correction loop can be enabled via SPI register write in address 0x01 and resetting the correction circuit in addresses 0x03 and 0x1A. By default it is disabled for lowest possible power consumption. The default settings for the auto correction function should work for most applications. However please contact Texas Instruments if further fine tuning of the algorithm is required.

The auto correction function yields best performance for input frequencies below 250MHz. For input frequencies greater than 250MHz it is recommended to disable the auto gain correction loop.

RECEIVE MODE: DECIMATION FILTER

Each channel has a digital filter in the data path as shown in Figure 38. The filter can be programmed as a low-pass or a high-pass filter and the normalized frequency response of both filters is shown in Figure 39.

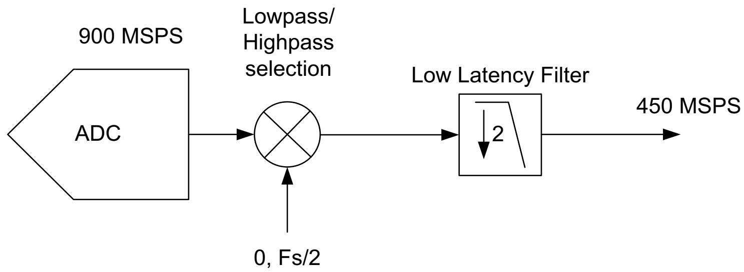


Figure 38.

The decimation filter response has a 0.1dB pass band ripple with approximately 41% pass-band bandwidth. The stop-band attenuation is approximately 40dB.

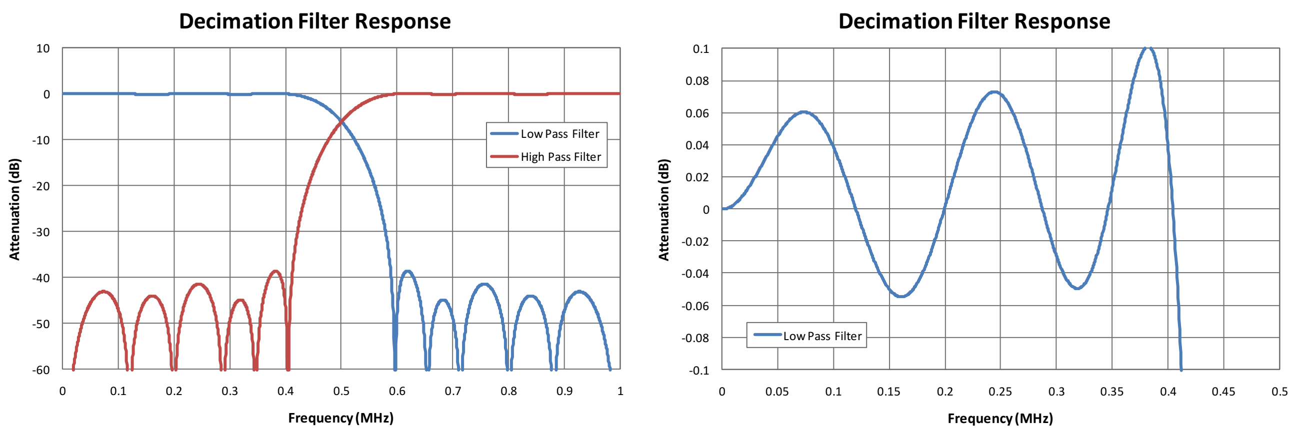
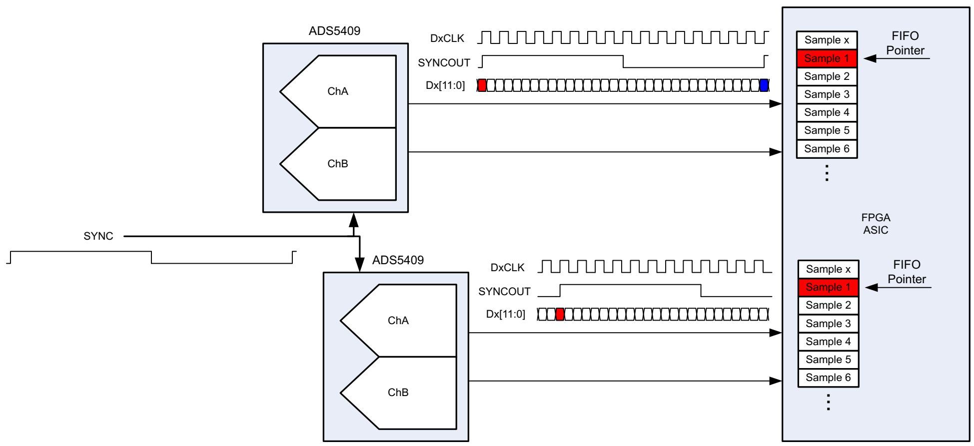


Figure 39.

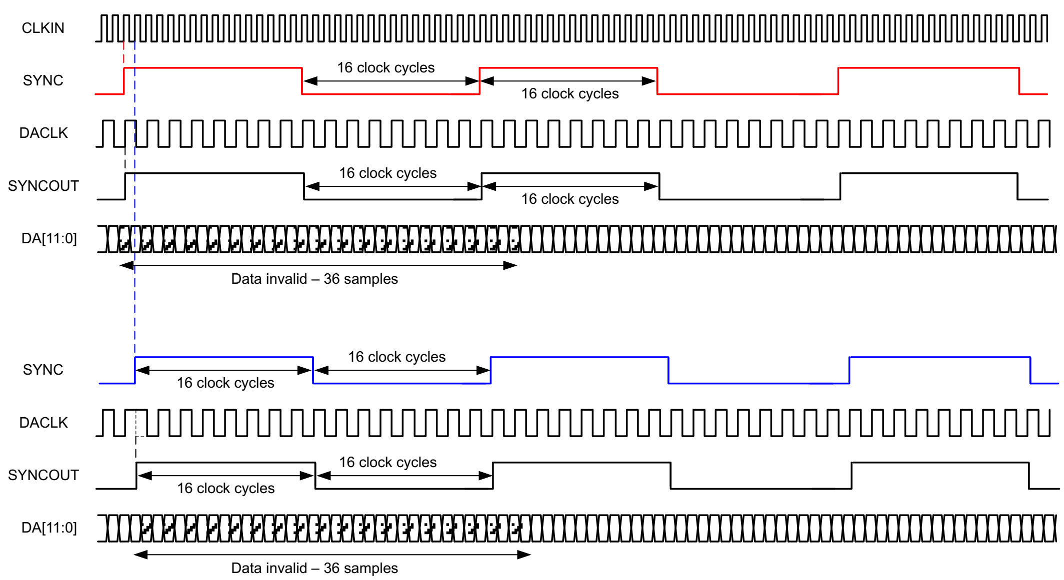
MULTI DEVICE SYNCHRONIZATION

The ADS5409 simplifies the synchronization of data from multiple ADCs in one common receiver. Upon receiving the initial SYNC input signal, the ADS5409 resets all the internal clocks and digital logic while also starting a SYNCOUT signal which operates on a 5bit counter (32 clock cycles). Therefore by providing a common SYNC signal to multiple ADCs their output data can be synchronized as the SYNCOUT signal marks a specific sample with the same latency in all ADCs. The SYNCOUT signal then can be used in the receiving device to synchronize the FIFO pointers across the different input data streams. Thus the output data of multiple ADCs can be aligned properly even if there are different trace lengths between the different ADCs.



The SYNC input signal should be a periodic signal repeating every 32 CLKIN clock cycles. It gets registered on the rising edge of the ADC input clock (CLKIN). Upon registering the initial rising edge of the SYNC signal, the internal clocks and logic get reset which results in invalid output data for 36 samples (1 complete sync cycle and 4 additional samples). The SYNCOUT signal starts with the next output clock (DACLK) rising edge and operates on a 5-bit counter independent from the SYNC signal frequency and duty cycle.

Since the ADS5409 output interface operates with a DDR clock, the synchronization can happen on the rising edge or falling edge sample. Synchronization on the falling edge sample will result in a half cycle clock stretch of DA/BCLK. For convenience the SYNCOUT signal is available on the ChA/B output LVDS bus. When using decimation the SYNCOUT signal still operates on 32 clock cycles of CLKIN but since the output data is decimated by 2, only the first 18 samples should be discarded.



PROGRAMMING INTERFACE

The serial interface (SIF) included in the ADS5409 is a simple 3 or 4 pin interface. In normal mode, 3 pins are used to communicate with the device. There is an enable (SDENB), a clock (SCLK) and a bi-directional IO port (SDIO). If the user would like to use the 4 pin interface one write must be implemented in the 3 pin mode to enable 4 pin communications. In this mode, the SDO pin becomes the dedicated output. The serial interface has an 8-bit address word and a 16-bit data word. The first rising edge of SCLK after SDENB goes low will latch the read/write bit. If a high is registered then a read is requested, if it is low then a write is requested. SDENB must be brought high again before another transfer can be requested. The signal diagram is shown below:

Register Initialization

After power up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a low pulse on SRESET pin
2. By applying a software reset. When using the serial interface, a reset can be performed by addressing register x2C. This setting initializes the internal registers to the default values and then self-resets the RESET register to 0. In this case the SRESET pin can be kept high.

Serial Register Write

The internal register of the ADS5409 can be programmed following these steps:

1. Drive SDENB pin low
2. Set the R/W bit to ‘0’ (bit A7 of the 8 bit address)
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be written
4. Write 16bit data which is latched on the rising edge of SCLK

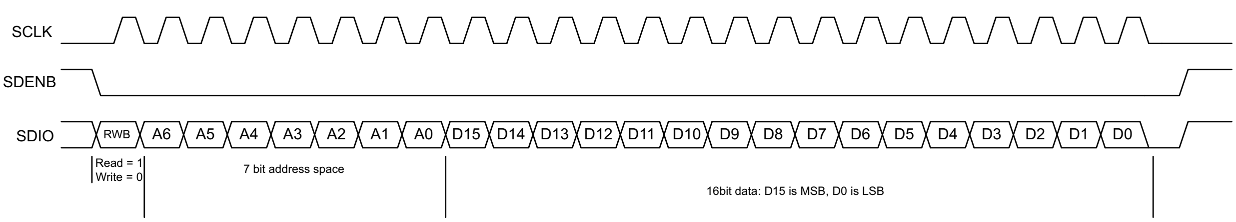


Figure 40. Serial Register Write Timing Diagram

PARAMETER		MIN	TYP(1)	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/tSCLK)	>DC		20	MHz
t_{SLOADS}	SDENB to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SDENB hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD33 = 3.3V, AVDD, DRVDD = 1.9V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDO/SDIO pins. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SDENB pin low
2. Set the RW bit (A7) to '1'. This setting disables any further writes to the registers
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be read.
4. The device outputs the contents (D15 to D0) of the selected register on the SDO/SDIO pin
5. The external controller can latch the contents at the SCLK rising edge.
6. To enable register writes, reset the RW register bit to '0'.

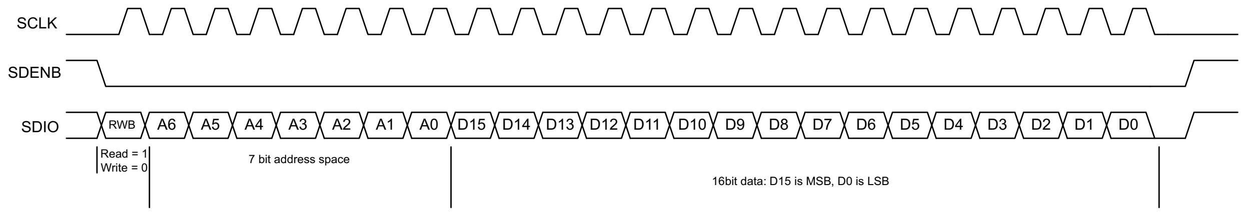


Figure 41. Serial Register Read Timing Diagram

SERIAL REGISTER MAP(2)

(2) Multiple functions in a register can be programmed in a single write operation.

Register Address	Register Data															
A7–A0 IN HEX	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	3/4 Wire SPI	Decima-tion Filter EN	0	ChA High/ Low Pass	0	0	ChB High/ Low Pass	0	0	0	0	0	0	0	0	0
1	ChA Corr EN	0	0	0	0	0	ChB Corr EN	0	0	0	0	0	Data Format	0	Hp Mode1	0
2	0	0	0	0	0	Over-range threshold				0	0	0	0	0	0	0
3	0	Start Auto Corr ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0
E	Sync Select														0	0
F	Sync Select				0	0	0	0	0	VREF Set			0	0	0	0
1A	0	Start Auto Corr ChB	0	0	1	0	1	1	0	0	0	1	1	0	0	0
2B	0	0	0	0	0	0	0	Temp Sensor								
2C	Reset															
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0
38	HP Mode2									BIAS EN	SYNC EN	LP Mode 1	0	0	0	0
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	DBCLK EN	0	OVRA EN	OVRB EN
66	LVDS Output Bus A EN															
67	LVDS Output Bus B EN															

DESCRIPTION OF SERIAL INTERFACE REGISTERS

Register Address	Register Data															
A7-A0 in hex	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	3/4 Wire SPI	Dec-ima-tion Filter EN	0	ChA High/ Low Pass	0	0	ChB High/ Low Pass	0	0	0	0	0	0	0	0	0

D15 **3/4 Wire SPI** Enables 4-bit serial interface when set
Default 0

0 3 wire SPI is used with SDIO pin operating as bi-directional I/O port

1 4 wire SPI is used with SDIO pin operating as data input and SDO pin as data output port.

D14 **Decimation Filter EN** 2x decimation filter is enabled when bit is set
Default 0

0 Normal operation with data output at full sampling rate

1 2x decimation filter enabled

D12 **ChA High/Low Pass** (Decimation filter must be enabled first: set bit D14)
Default 0

0 Low Pass

1 High Pass

D9 **ChB High/Low Pass** (Decimation filter must be enabled first: set bit D14)
Default 0

0 Low Pass

1 High Pass

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	ChA Corr EN	0	0	0	0	0	ChB Corr EN	0	0	0	0	0	Data Format	0	HP Mode1	0

D15 **ChA Corr EN (should be enabled for maximum performance)**
Default 0

0 Auto correction disabled

1 Auto correction enabled

D9 **ChB Corr EN (should be enabled for maximum performance)**
Default 0

0 Auto correction disabled

1 Auto correction enabled

D3 **Data Format**
Default 0

0 Two's complement

1 Offset Binary

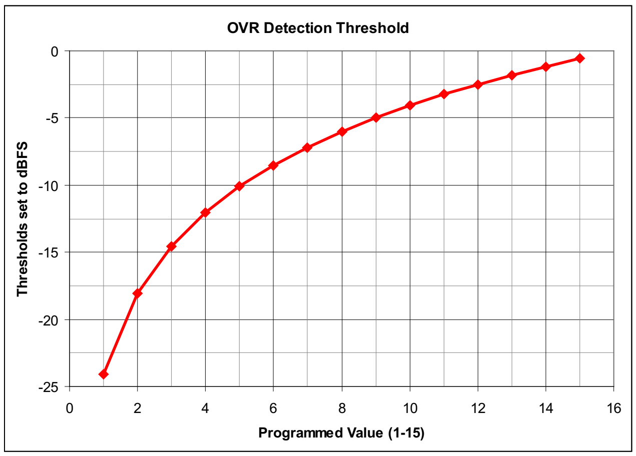
D1 **HP Mode 1**
Default 1

1 Must be set to 1 for optimum performance

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	0	0	0	0	0	Over-range threshold				0	0	0	0	0	0	0

D10-D7 **Over-range threshold** The over-range detection is triggered 12 output clock cycles after the overload condition occurs. The threshold at which the OVR is triggered = 1.0V x [decimal value of <Over-range threshold>]/16. After power up or reset, the default value is 15 (decimal) which corresponds to a OVR threshold of 0.56dB below fullscale (20*log(15/16)). This OVR threshold is applicable to both channels.

Default 1111



Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3	0	Start Auto Coff ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0

D14 **Start Auto Corr ChA** Starts DC offset and Gain correction loop for ChA
Default 1

0 Starts the DC offset and Gain correction loops

1 Clears DC offset correction value to 0 and Gain correction value to 1

D11, 9, 8, 4, 3 Must be set to 1 for maximum performance
Default 1

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
E	Sync Select														0	0

D15-D2	**Sync Select** Default 1010 1010 1010 10	Sync selection for the clock generator block (also need to see address 0x0F)
0000 0000 0000 00	Sync is disabled	
0101 0101 0101 01	Sync is set to one shot (one time synchronization only)	
1010 1010 1010 10	Sync is derived from SYNC input pins	
1111 1111 1111 11	not supported	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F	Sync Select				0	0	0	0	0	VREF Sel			0	0	0	0

D15-D12	**Sync Select** Default 1010	Sync selection for the clock generator block
0000	Sync is disabled	
0101	Sync is set to one shot (one time synchronization only)	
1010	Sync is derived from SYNC input pins	
1111	not supported	
D6-D4	**VREF SEL** Default 000	Internal voltage reference selection
000	1.0V	
001	1.25V	
010	0.9V	
011	0.8V	
100	1.15V	
Others	external reference	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1A	0	Start Auto Corr ChB	0	0	1	0	1	1	0	0	0	1	1	0	0	0

D14	**Start Auto Corr ChB** Default 1	Starts DC offset and Gain correction loop for ChB
0	Starts the DC offset and Gain correction loops	
1	Clears DC offset correction value to 0 and Gain correction value to 1	
D11, 9, 8, 4, 3	Must be set to 1 for maximum performance Default 1	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2B	0	0	0	0	0	0	0	Temp Sensor								

D8-D0 **Temp Sensor** Internal temperature sensor value – read only

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2C	Reset															

D15-D0	**Reset** Default 0000	This is a software reset to reset all SPI registers to their default value. Self clears to 0.
1101001011110000		Perform software reset

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0

D15-D14	**Sleep Modes** Default 00	Sleep mode selection which is controlled by the ENABLE pin. Sleep modes are active when ENABLE pin goes low.
000000	Complete shut down	Wake up time 2.5 ms
100000	Stand-by mode	Wake up time 100 µs
110000	Deep sleep mode	Wake up time 20 µs
110101	Light sleep mode	Wake up time 2 µs

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38	HP Mode 2									Bias EN	SYNC EN	LP Mode 1	0	0	0	0

D15-D7 **HP Mode 2**
Default 111111111

1 Set to 1 for normal operation

D6 **BIAS EN** Enables internal fuse bias voltages – can be disabled after power up to save power.
Default 1

0 Internal bias powered down

1 Internal bias enabled

D5 **SYNC EN** Enables the SYNC input buffer.
Default 1

0 SYNC input buffer disabled

1 SYNC input bffer enabled

D4 **LP Mode 1** Low power mode 1 to disable unused internal input buffer.
Default 1

0 Internal input buffer disabled

1 Internal input buffer enabled

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	DBCLK EN	0	OVRA EN	OVRB EN

D15-D13 **LVDS Current Strength** LVDS output current strength.
Default 110

000	2 mA	100	3 mA
001	2.25 mA	101	3.25 mA
010	2.5 mA	110	3.5 mA
011	2.75 mA	111	3.75 mA

D12-D11 **LVDS SW** LVDS driver internal switch setting – correct range must be set for setting in D15-D13
Default 01

01 2 mA to 2.75 mA
11 3mA to 3.75mA

D10-D9 **Internal LVDS Termination** Internal termination
Default 00

00 2 kΩ
01 200 Ω
10 200 Ω
11 100 Ω

D4 **DACLK EN** Enable DACLK output buffer
Default 1

0 DACLK output buffer powered down
1 DACLK output buffer enabled

D3 **DBCLK EN** Enable DBCLK output buffer
Default 1

0 DBCLK output buffer powered down
1 DBCLK output buffer enabled

D1 **OVRA EN** Enable OVRA output buffer
Default 1

0 OVRA output buffer powered down
1 OVRA output buffer enabled

D0 **OVRB EN** Enable OVRB output buffer
Default 1

0 OVRB output buffer powered down
1 OVRB output buffer enabled

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
66	LVDS Output Bus A EN															

D15-D10 **LVDS Output Bus A EN** Individual LVDS output pin power down for channel A
Default FFFF

0 Output is powered down

1 Output is enabled

D15 Pins N7, P7 (no connect pins) which are not used and should be powered down for power savings

D14 Pins N6, P6 (no connect pins) which are not used and should be powered down for power savings

D13 SYNCOUTP/N (pins P5, N5)

D12 Pins N4, P4 (no connect pins) which are not used and should be powered down for power savings

D11-D0 corresponds to DA11-DA0

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
67	LVDS Output Bus B EN															

D15-D10 **LVDS Output Bus B EN** Individual LVDS output pin power down for channel B
Default FFFF

0 Output is powered down

1 Output is enabled

D15 Pins G3, G4 (no connect pins) which are not used and should be powered down for power savings

D14 Pins F3, F4 (no connect pins) which are not used and should be powered down for power savings

D13 SYNCOUTP/N (pins F1, F2)

D12 Pins E3, E4 (no connect pins) which are not used and should be powered down for power savings

D11-D0 corresponds to DB11-DB0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5409IZAY	ACTIVE	NFBGA	ZAY	196	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS5409I	Samples
ADS5409IZAYR	ACTIVE	NFBGA	ZAY	196	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS5409I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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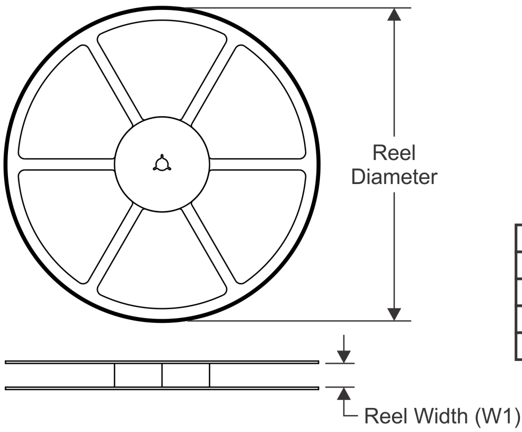
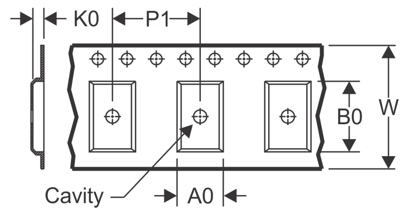
TAPE AND REEL INFORMATION

REEL DIMENSIONS

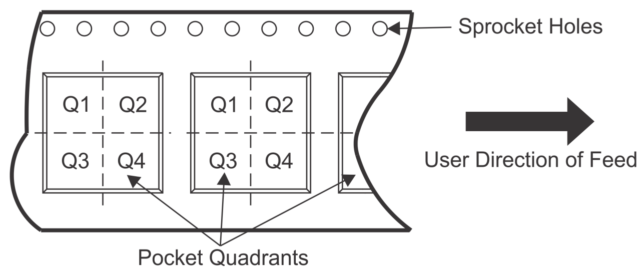


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

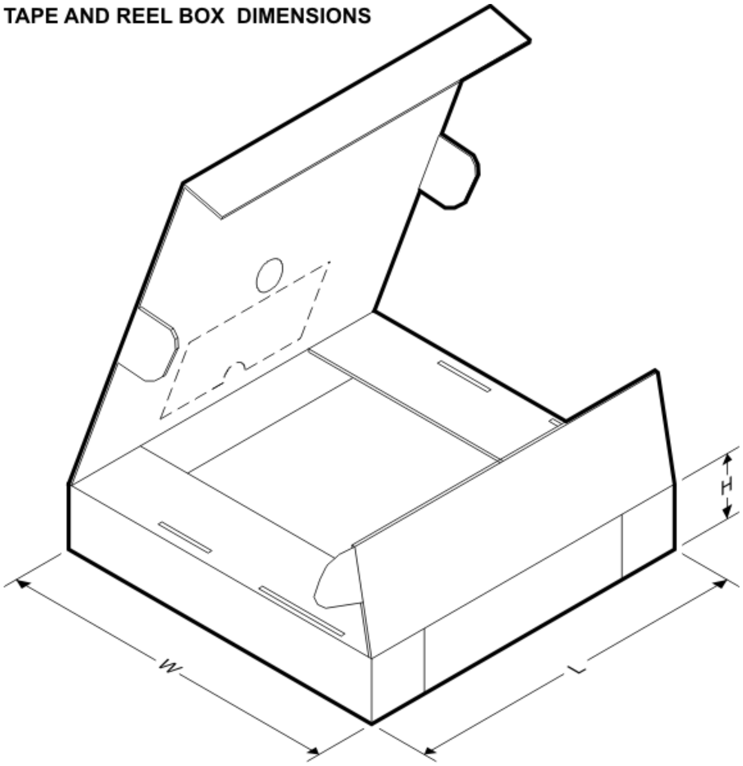
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5409IZAYR	NFBGA	ZAY	196	1000	330.0	24.4	12.3	12.3	2.3	16.0	24.0	Q1

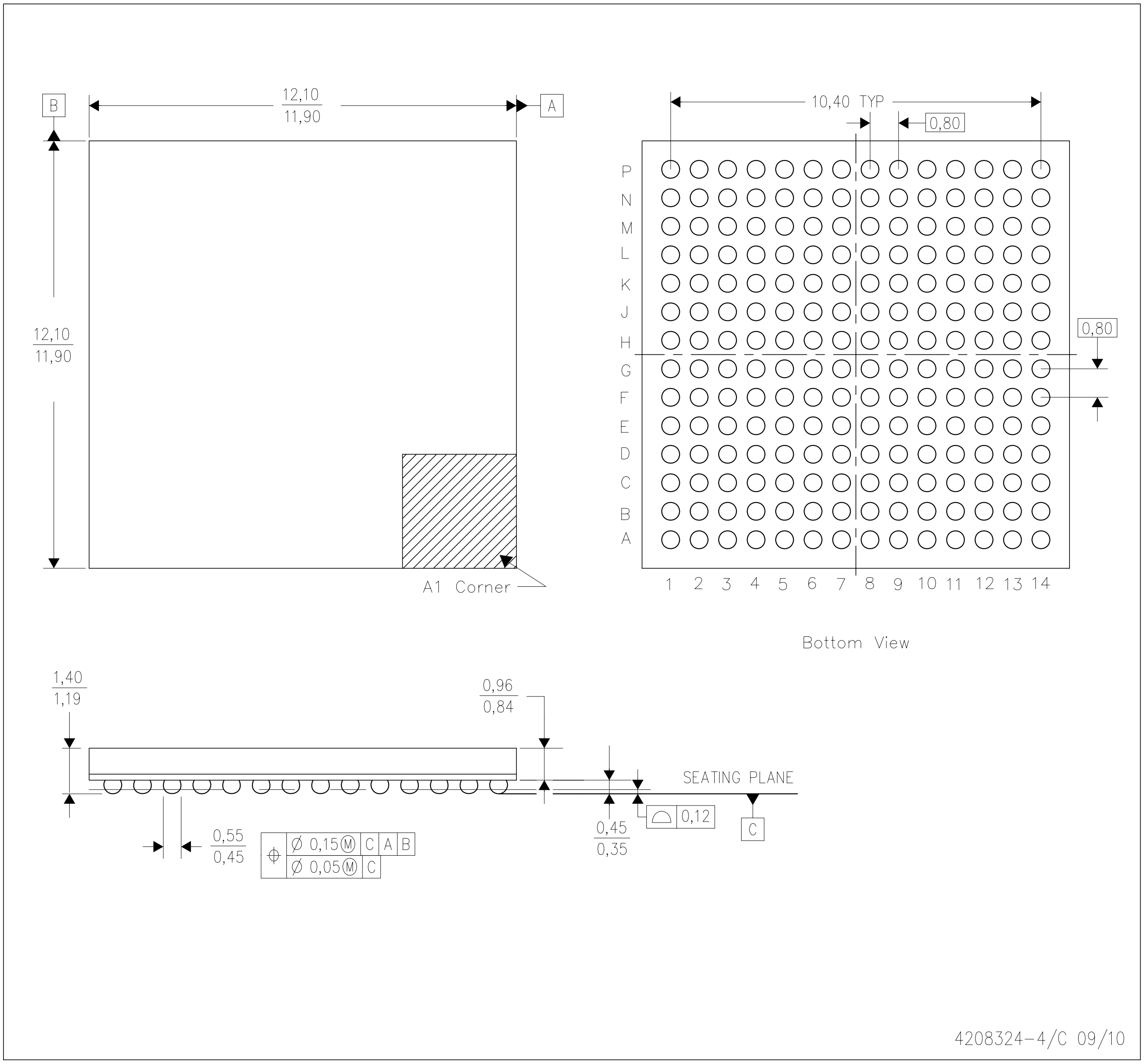
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5409IZAYR	NFBGA	ZAY	196	1000	336.6	336.6	31.8

ZAY (S-PBGA-N196) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. This is a Pb-free solder ball design.

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