TWO-PHASE HALF-WAVE MOTOR PREDRIVER

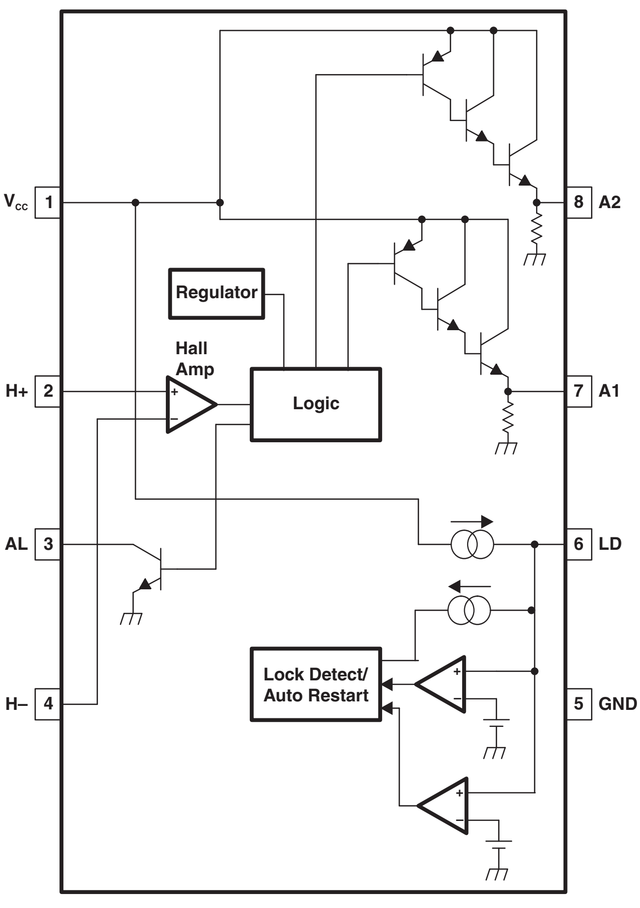
FEATURES

- **Built-In Lock Detection and Rotational Speed Sensing Mechanisms**
- **Compact 8-Pin Package Reduces Number of External Components Required**
- **Automatic Restart When Motor Lock Is Undone**
- **Hall Amplifier Inputs Have Hysteresis**

DESCRIPTION

The TMP821 is a two-phase half-wave motor predriver suited for fan motors.

BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	TMP821DR	TMP821

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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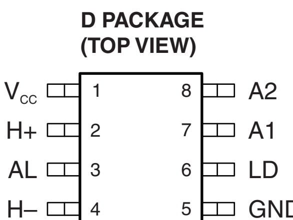
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
VCC	1	Power input (4 V to 28 V)
H+	2	Positive Hall input
AL	3	Speed indication Note: May remain high for several hundred milliseconds after power-on.
H–	4	Negative Hall input
GND	5	Ground
LD	6	Timing capacitor
A1	7	Driver output
A2	8	Driver output

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ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage	30	V
V_{AL}	Output voltage (AL)	30	V
I_{OUT}	Continuous output current (A1, A2)	70	mA
I_{AL}	Continuous output current (AL)	8	mA
θ_{JA}	Package thermal impedance[2]	97	°C/W
T_J	Operating junction temperature range	–40 to 125	°C
T_{stg}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	28	V
V_H	Hall amplifier input voltage	1	V_{CC} – 0.5	V
T_A	Operating free-air temperature	–40	100	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hall amplifier input voltage hysteresis			±3		±15	mV
V_{AL}	Lock alarm signal low-level output voltage	AL	I_{AL} = 5 mA			0.5	V
I_{AL}	Lock alarm signal low-level output current	AL	V_{AL} = 2 V	8			mA
I_{LDC}	Lock detection capacitor charge current	LD	V_{LD} = 1.5 V	2	3.45	5.25	µA
I_{LDD}	Lock detection capacitor discharge current	LD	V_{LD} = 1.5 V	0.35	0.8	1.45	µA
r_{CD}	Lock detection capacitor charge/discharge current ratio	LD	$r_{CD} = I_{LDC}/I_{LDD}$	3	4.5	8	
V_{LDCL}	Lock detection capacitor clamp voltage	LD		2.2	2.6	3	V
V_{LDCP}	Lock detection capacitor comparator voltage	LD		0.4	0.6	0.8	V
V_{7H}	High-level output voltage	A1	I_{OH} = –10 mA	10	10.5		V
V_{8H}	High-level output voltage	A2	I_{OH} = –10 mA	10	10.5		V
I_{CC}	Supply current		Output off		3.2	5	mA

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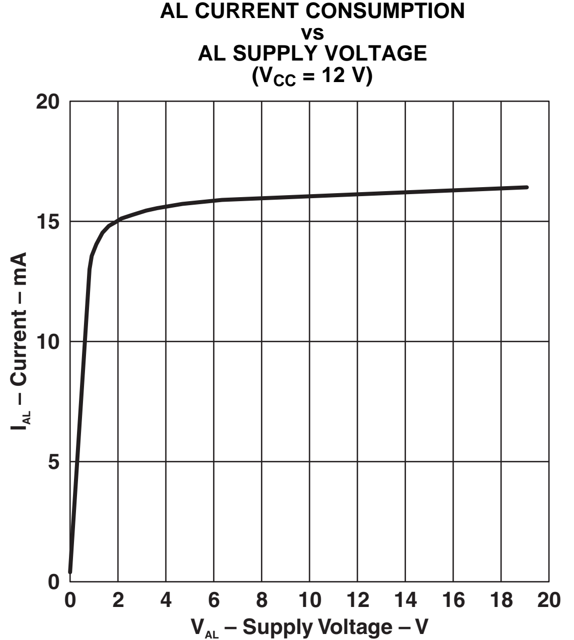
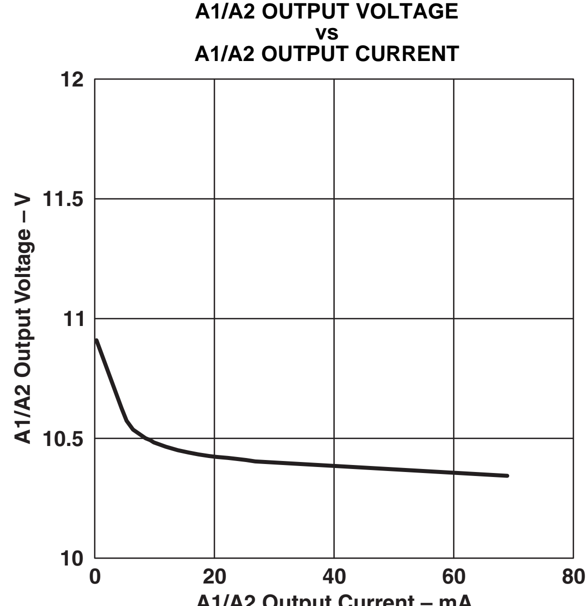
TYPICAL CHARACTERISTICS





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APPLICATION INFORMATION

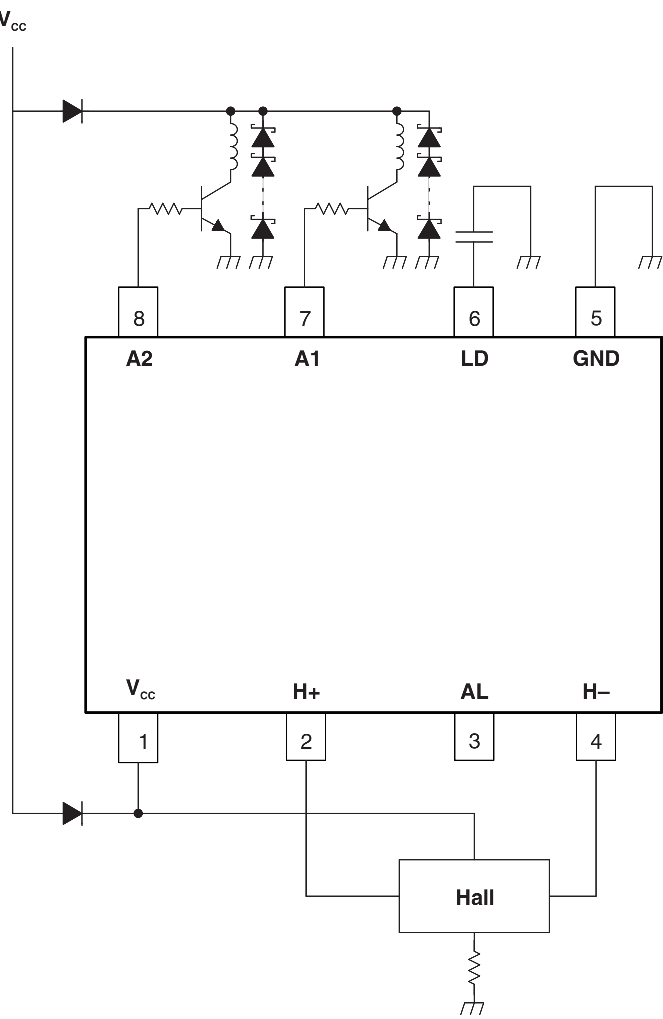

Figure 1. Typical Application Circuit

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Lock Detection

When a motor lock is detected, the TMP821 automatically shuts down its output current. When the motor lock is removed, the TMP821 automatically restarts. Motor lock is detected when the Hall signal stops switching, as shown in Figure 2.

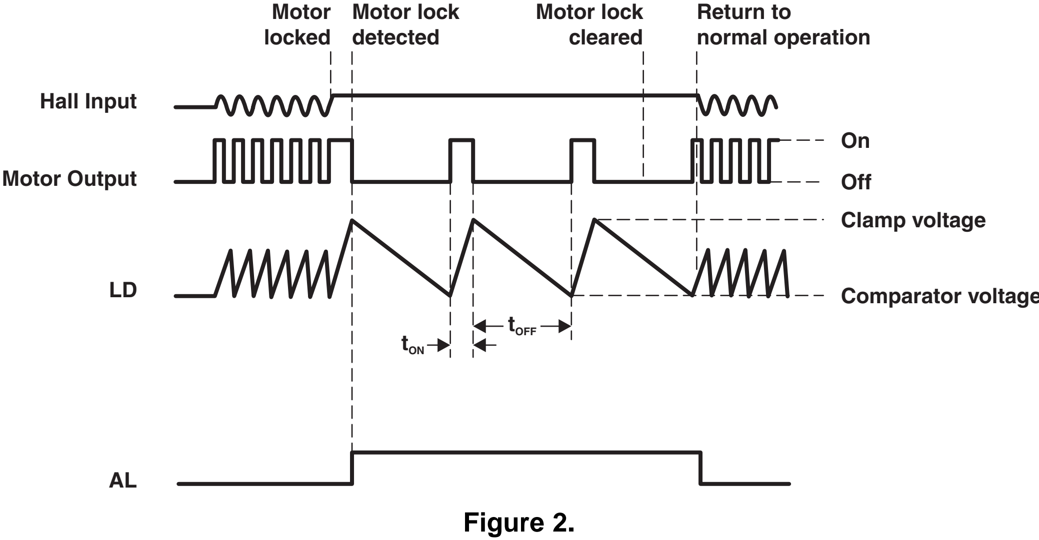

Figure 2.

t_{ON} and t_{OFF} are determined by the capacitor connected to LD:

$t_{ON} = (C_{LD} \times (V_{LD_CLAMP} - V_{LD_COMP}) / I_{LD_CHARGE}$ (seconds)

$t_{OFF} = (C_{LD} \times (V_{LD_CLAMP} - V_{LD_COMP}) / I_{LD_DISCHARGE}$ (seconds)

Where:

C_{LD} = capacitance of the external capacitor on LD
V_{LD_CLAMP} = LD clamp voltage
V_{LD_COMP} = LD comparator voltage
I_{LD_CHARGE} = LD charge current
$I_{LD_DISCHARGE}$ = LD discharge current

NOTE:

After power is supplied to the device, the the lock detection pin (AL) may remain high for a few hundred milliseconds (see Figure 3).

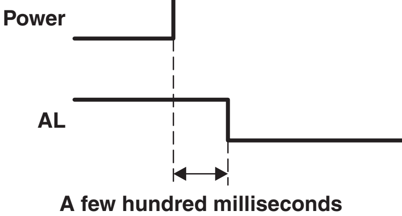

Figure 3. Power-On to AL Delay

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Power Dissipation

Figure 4 shows allowable power dissipation versus ambient temperature.

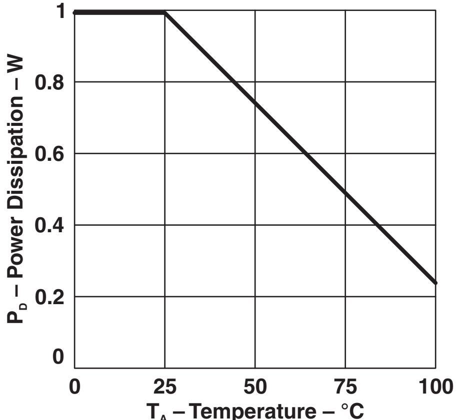

Figure 4. Power Dissipation

Total power consumption can be calculated as shown in Equation 1.

$$P_{total} = P_{C1} + P_{C2} + P_{C3} \quad (1)$$

Where:

- P_{C1} = circuit power dissipation
  - $P_{C1} = V_{CC} \times I_{CC}$
- P_{C2} = output power dissipation
  - $P_{C2} = (V_{CC} - V_{OH}) \times I_O$
  - V_{OH} = A1 and A2 high-level voltage
  - P_{C2} can be reduced by increasing the external output transistor's hFE rank to reduce the I_O consumption.
- P_{C3} = AL power dissipation
  - $P_{C3} = V_{AL_LOW} \times I_{AL}$

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMP821DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMP821DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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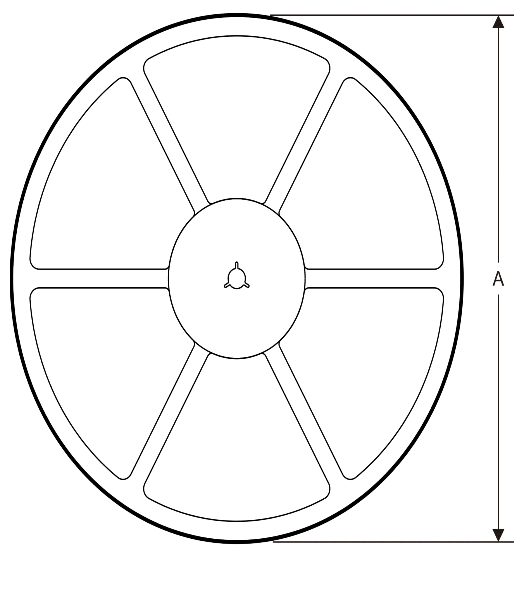
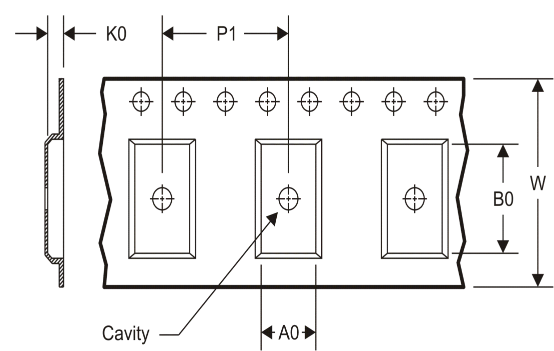
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



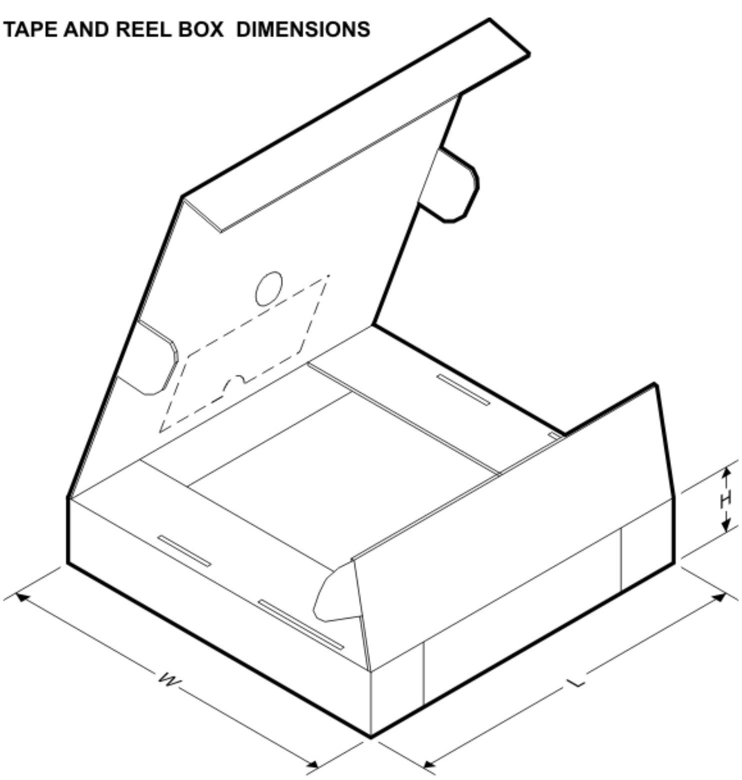
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP821DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP821DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP821DR	SOIC	D	8	2500	340.5	338.1	20.6
TMP821DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80) (C)

8 5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) (D)

Pin 1
Index Area

1 4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- (D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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