PRESSURE SENSOR SIGNAL CONDITIONER

Check for Samples: PGA400-Q1

1 DEVICE OVERVIEW

1.1 FEATURES

- Analog Features
  - Analog Front-End for Resistive Bridge Sensors
  - Self-Oscillating Demodulator for Capacitive Sensors
  - On-Chip Temperature Sensor
  - Programmable Gain
  - 16-Bit, 1MHz Sigma-Delta Analog-to-Digital Converter for Signal Channel
  - 10-Bit Sigma-Delta Analog-to-Digital Converter for Temperature Channel
  - Two 12–Bit DAC Outputs
- Digital Features
  - Microcontroller Core
    - 10 MHz 8051 WARP Core
      - 2 Clocks Per Instruction Cycle
    - On–Chip Oscillator
  - Memory
    - 8 KB of OTP Memory
    - 89 Bytes of EEPROM
    - 256 Bytes Data SRAM
- Peripheral Features
  - Serial Peripheral Interface (SPI™)
  - Inter-Integrated Circuit (I^2C™)
  - One-Wire Interface
  - Two Input Capture Ports
  - Two Output Compare Ports
  - Software Watchdog Timer
  - Oscillator Watchdog
  - Power Management Control
  - Analog Low-Voltage Detect
- General Features
  - Automotive Temperature Range: –40°C to 125°C
  - Power Supply: 4.5 V to 5.5 V Operational, –5.5 V to 16 V Abs Max
  - Qualified in accordance with AEC-Q100
  - WCSP-36 package

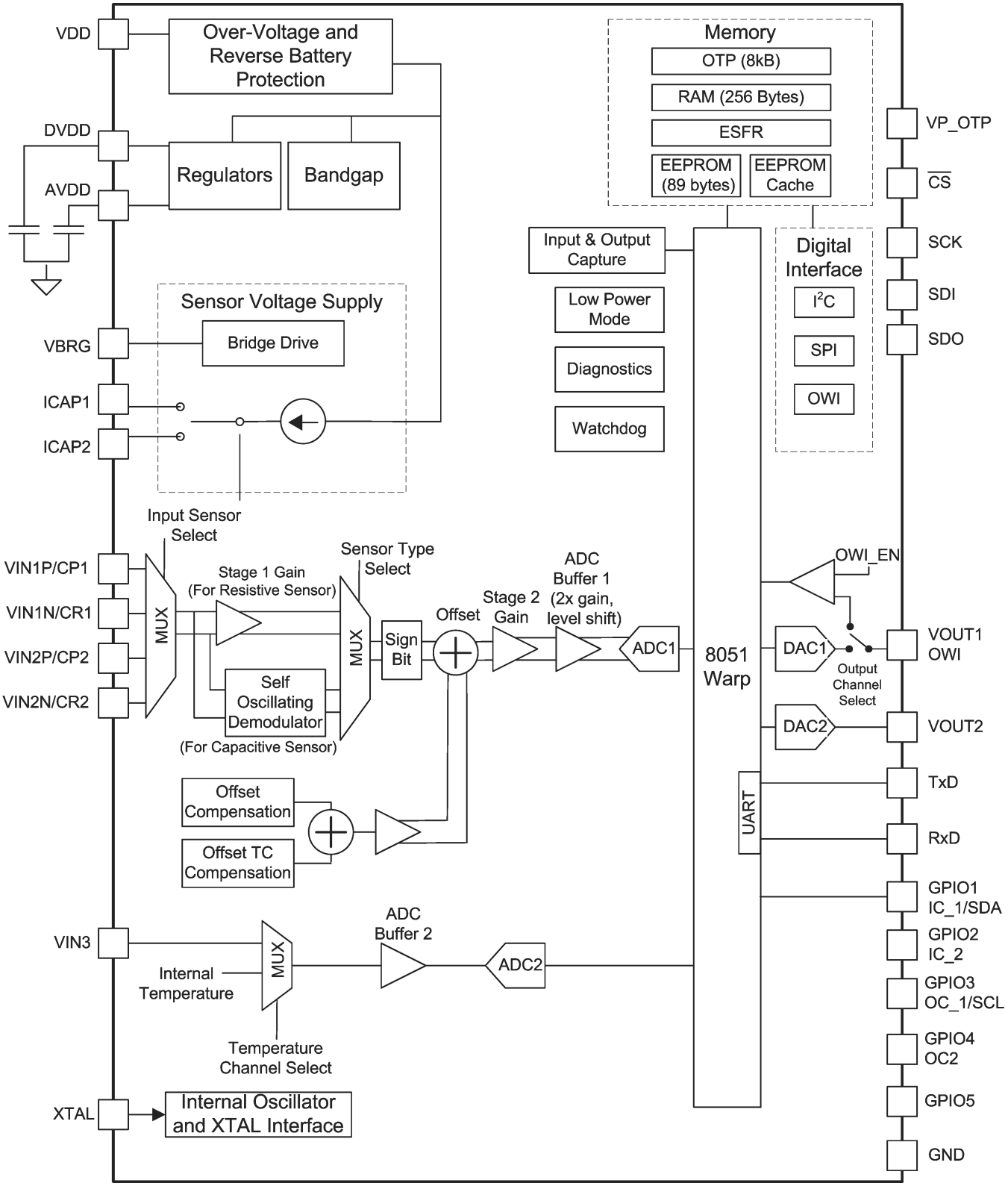
1.2 APPLICATIONS

- Pressure Sensor Signal Conditioning
- Level Sensor Signal Conditioning
- Humidity Sensor Signal Conditioning

1.3 DEVICE OVERVIEW

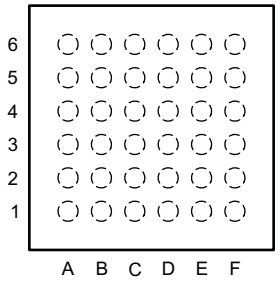
The PGA400-Q1 is an interface device for piezoresistive, strain gauge and capacitive sense elements. The device incorporates the analog front end that directly connects to the sense element and has voltage regulators and oscillator. The device also includes sigma-delta analog-to-digital converter, 8051 WARP core microprocessor and OTP memory. Sensor compensation algorithms can be implemented in software. The PGA400-Q1 also includes 2 DAC outputs.

2 FUNCTIONAL BLOCK DIAGRAM



3 DEVICE INFORMATION

DIE-SIZE BALL GRID ARRAY (WCSP)
36 PINS
(TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
AVDD	C6	Linear regulator output for internal analog circuit supply
$\overline{CS}$	F5	Serial peripheral interface chip select
DVDD	F6	Linear regulator output for internal digital circuit supply
GND	B2, B3, B5, B6, C3, C4, C5, D5, E5, E6	Ground
GPIO_1 / IC_1 / SDA	C2	General purpose IO 1 / input capture port 1 / I^2C Data
GPIO_2 / IC_2	D2	General purpose IO 2 / input capture port 2
GPIO_3 / OC_1/SCL	E3	General purpose IO 3 / output compare port 1 / I^2C Clock
GPIO_4 / OC_2	D3	General purpose IO 4 / output compare port 2
GPIO_5	F1	General purpose IO 5
ICAP1	A2	Capactive sensor drive current 1
ICAP2	A5	Capactive sensor drive current 2
SDO	F4	Serial peripheral interface slave data out
SDI	F3	Serial peripheral interface slave data in
RXD	D4	8051 UART Rx (Port 3_0)
SCK	F2	Serial Peripheral Interface clock
TXD	E4	8051 UART Tx (Port 3_1)
VBRG	B1	Resistive bridge supply voltage
VDD	D6	Input power supply
VIN1N / CR1	A3	Resistive sensor 1 negative input / capacitive sensor 1 reference input
VIN1P / CP1	A1	Resistive sensor 1 positive input / capacitive sensor 1 positive input
VIN2N / CR2	A6	Resistive sensor 2 negative input / capacitive sensor 2 reference input
VIN2P / CP2	A4	Resistive sensor 2 positive input / capacitive sensor 2 positive input
VIN3	B4	External temperature sensor input
VOUT1/OWI	D1	DAC1 output / One-wire interface
VOUT2	C1	DAC2 output
VP_OTP	E1	One-time programmable memory programming voltage
XTAL	E2	External crystal input

4 ABSOLUTE MAXIMUM RATINGS

4.1 ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER		MIN	MAX	UNIT
VDD, Continuous	Power Supply Voltage	–5.5	16	V
	Voltage at VP_OTP	–0.3	8.0	V
	Voltage at sensor input and drive pins	–0.3	3.6	V
	Voltage at any IO pin except at VOUT1/OWI	–0.3	VDD + 0.3	V
	Voltage at VOUT1/OWI pin	–0.3	7.5	V
I_{DD}, Short on VOUT1 or VOUT2	Supply Current	–45	45	mA
Iout1, Iout2	Output Current	–30	30	mA
ESD	Human Body Model (HBM) - AEC-Q100-002D	±2		KV
	Field Induced Charge Device Model (CDM) - AEC-Q100-11B	±500		V
T_{jmax}	Maximum Junction Temperature		150	°C
T_{stg}	Storage Temperature	–40	150	°C
T_{lead}	Lead Temperature (Soldering, 10sec)		260	°C

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Power supply voltage		4.5	5	5.5	V
I_{DD}	Power supply current - normal mode	V_{DD} = 5V, No load on VBRG, No load on DAC1 and DAC2			13.6	mA
	Power supply current - low power mode	V_{DD} = 5.5V, No load on VBRG, No load on DAC1 and DAC2, AFE turned OFF			9.5	mA
VP_OTP	OTP programming voltage		7.0	7.4	7.8	V
I_VP_OTP	OTP programming current	During OTP Programming			3	mA
tprog_OTP	OTP programming timing per byte		120			µs
T_A	Operating ambient temperature		–40		125	°C
	Programming temperature	OTP or EEPROM	–40		140	°C
	Micro start-up time	VDD ramp rate 1V/µs			250	µs

5 ELECTRICAL CHARACTERISTICS

5.1 Overvoltage Protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV	Overvoltage protection threshold		5.5	6.1	7.0	V
OV_{hyst}	Overvoltage protection hysteresis			410		mV

5.2 Regulators

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	AVDD voltage	C_{AVDD} = 100 nF		3.3		V
I_AVDD	AVDD current	V_{AVDD} = 3.3 V			5	mA
V_{DVDD}	DVDD voltage	No EEPROM Programming		3.3		V
		EEPROM Programming		3.6		V

5.3 Internal Oscillator and External Crystal Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL OSCILLATOR						
	Internal Oscillator frequency	T_{amb} = 25 °C	38.4	40	41.6	MHz
	Internal Oscillator frequency	Accross operating temperature	36.3		43.7	MHz
EXTERNAL 40-MHZ CRYSTAL						
	Low-level input voltage on XTAL		–0.3		0.1× VDD	V
	High-level input voltage on XTAL		0.7 × VDD		VDD + 0.3	V

5.4 Sensor Supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBRG SUPPLY FOR RESISTIVE BRIDGE SENSORS						
V_{BRG}	Supply Voltage	0.44 kΩ ≤ R_{BRG} ≤ 20 kΩ	3.2	3.33	3.4	V
R_{BRG}	Resistive Bridge Resistance		0.44		20	KΩ
C_{BRG}	Capacitive Load	R_{BRG} = 20 kΩ			500	pF
	Line regulation	V_{DD} = 4.5V, 5.5V, R_{BRG} = 0.44 kΩ	-40		40	mV
	Load regulation	V_{DD} = 5.0 V, 10 µA ≤ I_{LOAD} ≤ 10 mA	-40		40	mV
ICAPx SUPPLY FOR CAPACITIVE SENSORS						
ICAP_A	Supply Current Amplitude on ICAP, T_A = 25°C	CI[2:0] = 000, ICAP_V = 100 mV	-5.3		-4.3	µA
		CI[2:0] = 001, ICAP_V = 100 mV	-8		-6.6	
		CI[2:0] = 010, ICAP_V = 100 mV	-10.8		-8.8	
		CI[2:0] = 011, ICAP_V = 100 mV	-13.5		-11.1	
		CI[2:0] = 100, ICAP_V = 100 mV	-16.2		-13.3	
		CI[2:0] = 101, ICAP_V = 100 mV	-18.9		-15.5	
		CI[2:0] = 110, ICAP_V = 100 mV	-21.6		-17.8	
		CI[2:0] = 111, ICAP_V = 100 mV	-24.4		-20.1	
		CI[2:0] = 000, ICAP_V = 3.2 V	4.5		5.6	
		CI[2:0] = 001, ICAP_V = 3.2 V	6.9		8.5	
		CI[2:0] = 010, ICAP_V = 3.2 V	9.2		11.3	
		CI[2:0] = 011, ICAP_V = 3.2 V	11.5		14.1	
		CI[2:0] = 100, ICAP_V = 3.2 V	13.6		16.7	
		CI[2:0] = 101, ICAP_V = 3.2 V	15.8		19.2	
		CI[2:0] = 110, ICAP_V = 3.2 V	18.1		22.1	
		CI[2:0] = 111, ICAP_V = 3.2 V	20.4		24.8	
	Variation over temperature		-5.0		+5.0	%
CPx_V, CRx_V	Capacitive Sensor Drive - Voltage at CPx and CRx pins	CV[1:0] = 00	70	90	110	mV
		CV[1:0] = 01	255	300	345	
		CV[1:0] = 10	425	500	575	
		CV[1:0] = 11	595	700	805	
SELF OSCILLATING CURRENT MODE DEMODULATOR FOR CAPACITIVE SENSORS						
R_F / R_{REF}	Gain in Transimpedance amplifier	CR[1:0] = 00, R_{REF} = 78 kΩ	-1.07	-1.01	-0.94	V/V
		CR[1:0] = 01, R_{REF} = 78 kΩ	-2.13	-1.97	-1.82	
		CR[1:0] = 10, R_{REF} = 78 kΩ	-4.24	-3.93	-3.63	
		CR[1:0] = 11, R_{REF} = 78 kΩ	-8.45	-7.85	-7.26	
Cf	Feedback Capacitor in Transimpedance amplifier		14	16	18	pF

5.5 Temperature Sensor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature Range		–40		150	°C
	Temperature ADC Resolution			10		bits
	Temperature ADC Update Rate			8		ms
	Gain (1)		2.7	2.8	2.9	LSB/°C
	Offset (1)		-105		-66	LSB
	Total Error		-4		4	°C

(1) The Temperature ADC Value is given by the equation: ADC Code = Gain*Temperature (in °C) + Offset

5.6 Analog Front Ends

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAGE 1 GAIN FOR RESISTIVE BRIDGE SENSORS					
Gain Steps	Sx_G1[2:0] = 000		3.0		V/V
	Sx_G1[2:0] = 001		4.4		
	Sx_G1[2:0] = 010		6.8		
	Sx_G1[2:0] = 011		10.2		
	Sx_G1[2:0] = 100		14.6		
	Sx_G1[2:0] = 101		25.5		
	Sx_G1[2:0] = 110		34.0		
	Sx_G1[2:0] = 111		51.0		
Bandwidth	–3 dB, Gain = 111		7		KHz

5.7 Stage 2 Gain

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain Steps	Sx_G2[4:0] = 00000	0.97	1.01	1.05	V/V
		Sx_G2[4:0] = 00001	1.06	1.11	1.16	
		Sx_G2[4:0] = 00010	1.18	1.23	1.28	
		Sx_G2[4:0] = 00011	1.31	1.37	1.42	
		Sx_G2[4:0] = 00100	1.45	1.52	1.58	
		Sx_G2[4:0] = 00101	1.61	1.68	1.76	
		Sx_G2[4:0] = 00110	1.79	1.87	1.94	
		Sx_G2[4:0] = 00111	1.98	2.07	2.16	
		Sx_G2[4:0] = 01000	2.20	2.29	2.39	
		Sx_G2[4:0] = 01001	2.44	2.55	2.65	
		Sx_G2[4:0] = 01010	2.71	2.83	2.94	
		Sx_G2[4:0] = 01011	3.00	3.13	3.26	
		Sx_G2[4:0] = 01100	3.34	3.48	3.62	
		Sx_G2[4:0] = 01101	3.74	3.90	4.06	
		Sx_G2[4:0] = 01110	4.12	4.30	4.48	
		Sx_G2[4:0] = 01111	4.61	4.81	5.01	
		Sx_G2[4:0] = 10000	5.09	5.31	5.54	
		Sx_G2[4:0] = 10001	5.67	5.92	6.16	
		Sx_G2[4:0] = 10010	6.26	6.52	6.79	
		Sx_G2[4:0] = 10011	6.93	7.23	7.53	
		Sx_G2[4:0] = 10100	7.70	8.04	8.37	
		Sx_G2[4:0] = 10101	8.57	8.95	9.32	
		Sx_G2[4:0] = 10110	9.54	9.96	10.37	
		Sx_G2[4:0] = 10111	10.62	11.06	11.51	
		Sx_G2[4:0] = 11000	11.76	12.27	12.79	
		Sx_G2[4:0] = 11001	13.02	13.58	14.15	
		Sx_G2[4:0] = 11010	14.48	15.10	15.72	
		Sx_G2[4:0] = 11011	16.03	16.71	17.40	
		Sx_G2[4:0] = 11100	17.72	18.53	19.34	
		Sx_G2[4:0] = 11101	19.61	20.49	21.37	
		Sx_G2[4:0] = 11110	21.72	22.70	23.68	
		Sx_G2[4:0] = 11111	23.85	25.06	26.28	
	Bandwidth	–3 dB, Gain Setting = 11111	120			KHz

5.8 Offset and Offset TC Compensation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset Compensation Low	Offset Setting = 0x000, Stage 1 Gain Setting = 0b000	-385	-324	-279	mV
	Offset Compensation High	Offset Setting = 0x3FF, Stage 1 Gain Setting = 0b000	279	324	385	mV
	Offset Compensation Resolution	Stage 1 Gain Setting = 0b000	0.59		0.72	mV/step
	Offset TC Compensation Low	Offset TC Setting = 0x00, Stage 1 Gain Value = 0b000		-371		µV/°C
	Offset TC Compensation H igh	Offset TC Settin g= 0x3F, Stage 1 Gain Value = 0b000		361		µV/°C
	Offset TC Compensation Resolution	Stage 1 Gain Value = 0b000		11.6		µV/V/°C/step
	Reference Temperature			22		°C

5.9 Analog to Digital Converter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC BUFFER FOR 16-BIT AD CONVERTER 1						
	Gain		1.9	2	2.1	V/V
	DC Level Shift	ADC_BUF bit = 1	-1.74	–1.65	-1.55	V
	DC Offset		-15		15	mV
ADC BUFFER FOR 10-BIT AD CONVERTER 2						
	VIN3 Input Voltage Range		0.425		1.7	V
	Gain		1.09	1.15	1.21	V/V
	DC Offset		-15		15	mV
VIN3 VOLTAGE VERSUS ADC CODE						
	Gain (1)		740	760	780	LSB/V
	Offset (1)		-850	-820	-790	LSB
	Gain Temperature Coefficient	T_{amb} = 25 °C		0.02		LSB/V/°C
	Offset Temperature Coefficient	T_{amb} = 25 °C		-0.02		LSB/°C
	Integral Nonlinearity		-1		1	LSB

(1) ADC Code = Gain*VIN3+Offset

5.10 One Wire Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Communication Baud Rate		2400		115000	Bits Per Second
OWI_EN	OWI Enable		6.5		7.0	V
OWI_EN_{hys}	OWI Enable Hysteresis			50		mV
	Internal Pullup			10		KΩ
	Activation Signal Pulse Low time		12			ms
	Activation Signal Pulse High time		12			ms
OWI_VIH	OWI Transceiver Rx Threshold		0.7 × VDD		VDD + 0.3	V
OWI_VIL	OWI Transceiver Rx Threshold		–0.3		0.3 × VDD	V
OWI_VOH	OWI Transceiver Tx Threshold	VDD = 5 V	4.0			
OWI_VOL	OWI Transceiver Tx Threshold	VDD = 5 V			0.8	V

5.11 Serial Peripheral Interface (SPI) Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
V_{OH}	High-level output voltage		4.0			V
V_{OL}	Low-level output voltage				0.8	V
f_{SCK}	SPI Frequency				4	MHz
t_{CSSCK}	$\overline{CS}$ Low to First SCK Rising Edge		25			ns
t_{SCKCS}	Last SCK Rising Edge to $\overline{CS}$ Rising Edge		125			ns
t_{CSD}	$\overline{CS}$ Disable Time		500			ns
t_{DS}	SDI Setup Time		25			ns
t_{DH}	SDI Hold Time		25			ns
t_{SDIS}	SDI Fall/Rise Time				7	ns
t_{SCKR}	SCK Rise Time				7	ns
t_{SCKF}	SCK Fall Time				7	ns
t_{SCKH}	SCK High Time		125			ns
t_{SCKL}	SCK Low Time		125			ns
t_{SDOE}	SDO Enable Time		15			ns
t_{ACCS}	SCK Rising Edge to SDO Data Valid		15			ns
t_{SDOD}	SDO Disable Time				15	ns
t_{SDOS}	SDO Rise/Fall Time		3		11	ns
$C_{L(SDO)}$	Capacitive Load for Data Output (SDO)			10		pF

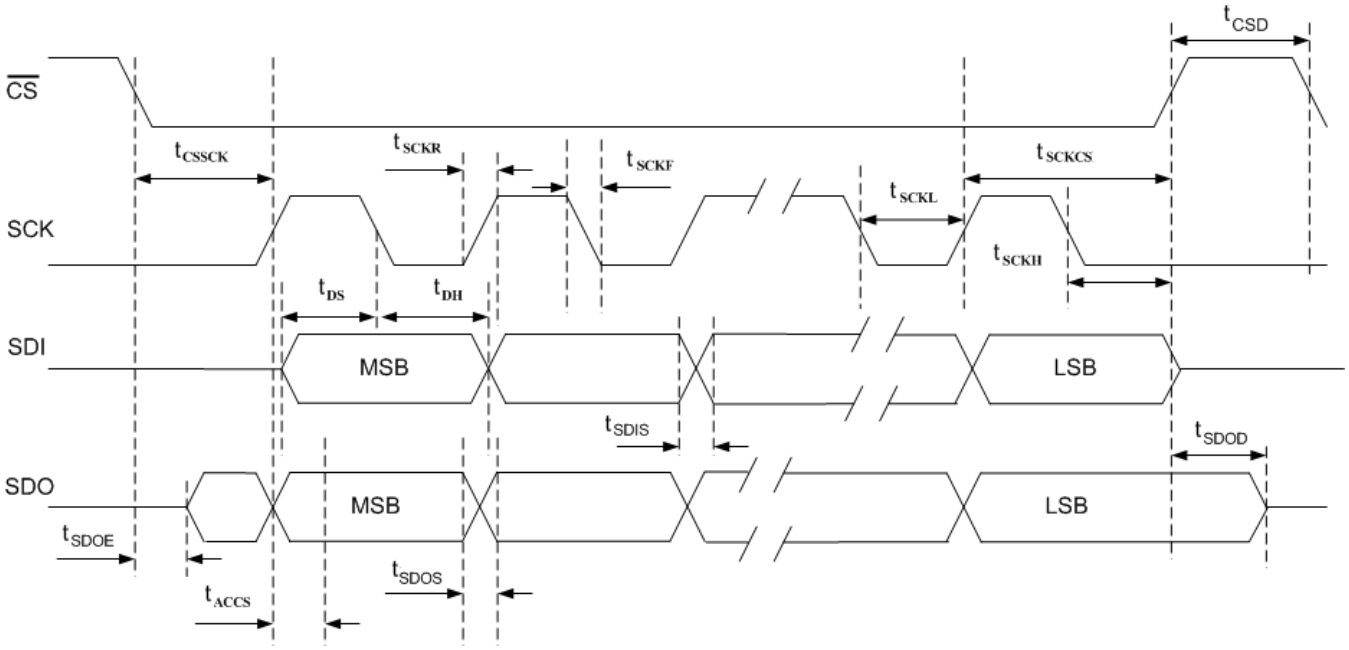


Figure 5-1. SPI Timing

5.12 I2C Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
V_{OH}	High-level output voltage		4.0			V
V_{OL}	Low-level output voltage				0.8	V
f_{SCL}	SCL clock frequency				400	KHz
t_{STASU}	START condition set-up time		500			ns
t_{STAHD}	START condition hold time		500			ns
t_{LOW}	SCL low time		1.25			µs
t_{HIGH}	SCL high time		1.25			µs
t_{RISE}	SCL and SDA rise time				7	ns
t_{FALL}	SCL and SDA fall time				7	ns
t_{DATSU}	Data setup time		500			ns
t_{DATHD}	Data hold time		500			ns
t_{STOSU}	STOP condition set-up time		500			ns

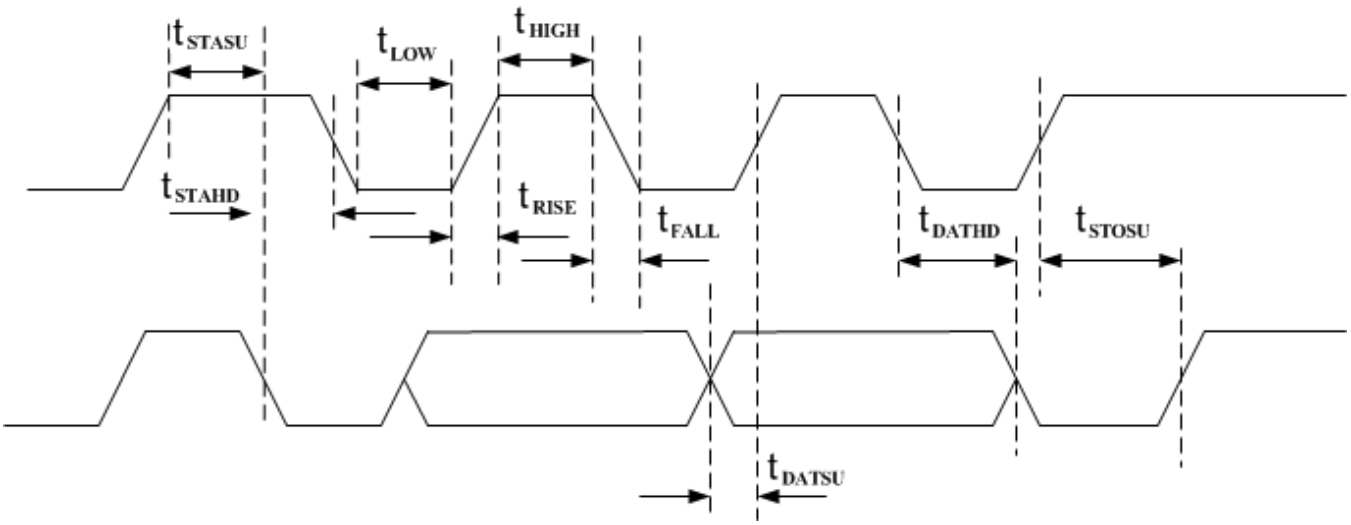


Figure 5-2. I²C Timing

5.13 Non-Volatile Memory

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTP			8		KB
OTP Number of Erase/Write Cycles	Erase using UV light			10	Cycles
EEPROM	Programmable using SPI or OWI		89		Bytes
	Number of bytes writeable by 8051		16		Bytes
EEPROM Erase/Write Cycles				1000	Cycles

5.14 GPIO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V	0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V	–0.3		0.3 × VDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	4.0			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.8	V
I_{OH}	High-level output current	V_{OH} = 4.5 V			1	mA
I_{OL}	Low-level output current	V_{OL} = 0.5 V			1	mA
R_{PU}	Pull-up resistance			160		kΩ

5.15 DAC1 and DAC2 Output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Settling time	DAC Code 000h to FFFh step.Output is 90% of Full Scale. R_{LOAD} = 5 kΩ, C_{LOAD} = 500 pF			7	µs
	Zero scale error	DAC code = 000h, I_{DAC} = 1.5 mA			46	mV
	Full scale voltage	Output when DAC code is FFFh, I_{DAC} = - 1.5 mA	4.85		4.95	V
	Output current amplitude	DAC Code = 0FFFh , DAC Code = 0000h			1.5	mA
	Short circuit source current	VDD = 5V, DAC code = 000h	-34		-10	mA
	Short circuit sink current	VDD = 5V, DAC code = FFFh	10		34	mA
	INL (best-fit line)		-3.5		3.5	LSB

5.16 Input Capture and Output Compare

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CAPTURE PORTS						
V_{IH}	High-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V	0.7 × VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage	R_{LOAD} ≥ 10 kΩ to V_{DD} or to 0 V	–0.3		0.3 × VDD	V
	Input capture timer clock frequency	10_20_MHZ bit = 1		10		MHz
		10_20_MHZ bit = 0		20		
	Input capture timer bits			16		Bits
OUTPUT COMPARE PORTS						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	VDD – 1.0			V
V_{OL}	Low-level output voltage	I_{OL} = -1 mA			0.8	V
	Output compare timer frequency	10_20_MHZ bit = 1		10		MHz
		10_20_MHZ bit = 0		20		
	Output compare timer bits			16		Bits
I_{OH}	High-level output current				1	mA
I_{OL}	Low-level output current				1	mA

5.17 Diagnostics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	8051 Software watchdog			500		ms
	Main clock normal operation range		35	40	45	MHz
VBRG_OV	Sensor supply over voltage threshold		3.55	3.65	3.75	V
VBRG_UV	Sensor supply under voltage threshold		2.9	3.0	3.11	V
	AVDD OV threshold		3.75		3.95	V
	AVDD UV threshold		2.72		3.1	V
$Sensor_{OV}$	Output overvoltage threshold for gain stage 1 and 2		2.4	2.5	2.6	V
$Sensor_{UV}$	Output undervoltage threshold for gain stage 1 and 2		0.7	.85	1.0	V
f_cap_{High}	Capacitive sensor interface clock high frequency fault threshold		1.5		2.5	MHz
f_cap_{Low}	Capacitive sensor interface clock low frequency fault threshold		30		50	kHz
	EEPROM CHG PUMP overvoltage threshold			14.65		V
	EEPROM CHG PUMP undervoltage threshold			11.45		V
	DAC loop back voltage gain		0.537	0.545	0.557	V/V
	Open wire leakage current 1 - open VDD with pull-up on VOUT1				2	µA
	Open wire leakage current 2 - open GND with pull-down on VOUT1				20	µA

6 FUNCTIONAL DESCRIPTIONS

In this section, individual blocks in the Section 2 are described in more detail.

6.1 Overvoltage / Reverse Voltage Protection Block

The PGA400-Q1 includes an Overvoltage and Reverse Voltage Protection block. This block protects the device from overvoltage and reverse-battery conditions on the external power supply. In this block, a control circuit monitors the input supply line for reverse-battery and overvoltage fault conditions protects the device if these voltage conditions occur on the external power supply.

6.2 Linear Regulators and Bandgap + Current Blocks

The PGA400-Q1 contains two precision low-drift bandgap supply voltage references for other blocks of the device. One bandgap provides the reference voltage for internal linear regulators that supply AVDD and DVDD. The other bandgap reference provides the voltage reference for the all the other internal circuitry, including sensor supply regulators, sensor offset compensation, etc.

The PGA400-Q1 has two main linear regulators: AVDD Regulator and DVDD Regulator. The AVDD regulator provides the 3.3 V voltage source for internal analog circuitry while the DVDD regulator provides the 3.3 V regulated voltage for the digital circuitry. The user needs to connect bypass capacitors of 100nF on both the AVDD and DVDD pins of the device.

Figure 6-1 shows the Power-On Reset sequence for AVDD and DVDD with respect to the voltage applied to the VDD pin.

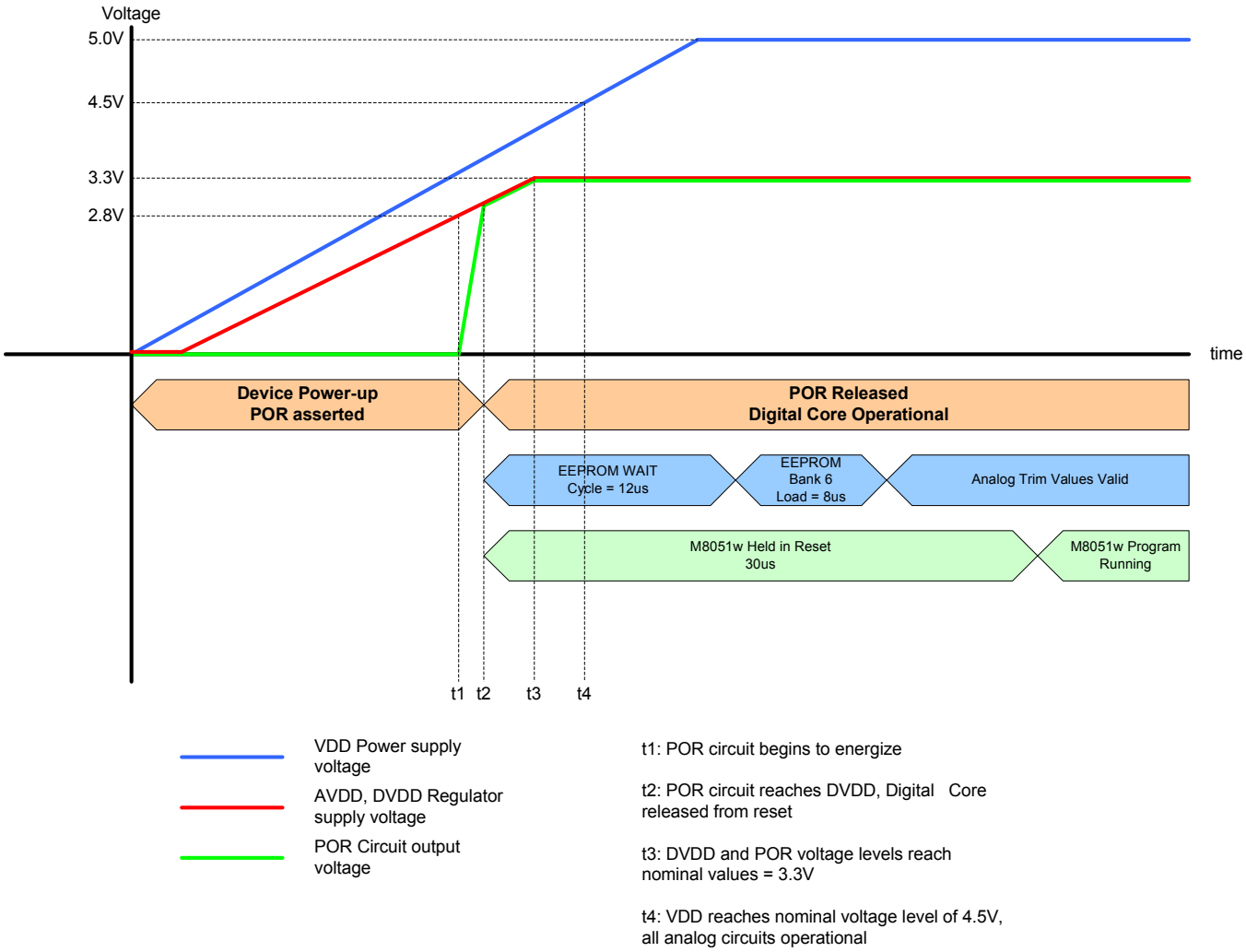


Figure 6-1. POR Sequence Diagram

6.3 Internal OSC/XTAL I/F Block

The device includes an internal 40 MHz oscillator, which by default provides the internal clocks required. The device can also be configured to use an external 40-MHz crystal as a time base via the XTAL_EN bit in the Sensor Control Register (SENCTRL). When the XTAL_EN bit is set high, the internal 40-MHz oscillator is disabled and control of the main system clock is driven by the external clock source connected to the XTAL pin. For more information on programming this device please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).).

NOTE

Do not use the XTAL pin as an output for sourcing a clock signal to other devices.

6.4 Sensor Voltage Supply Block

The Sensor Voltage Supply block of the PGA400-Q1 supplies both the VBRG output for resistive bridge sensors and the ICAP supply for capacitive sensors.

6.4.1 VBRG Supply for Resistive Bridges

The VBRG pin on the PGA400-Q1 is a 3.3-V nominal output supply from a linear regulator with a precise internal temperature independent band-gap reference.

6.4.2 ICAP Supply for Capacitive Sensors

A functional schematic of the capacitive sensor drive circuit is shown in Figure 6-2. The common node of the sensor capacitances is tied to the ICAP pin and the current and voltage at this point are referred to as I_X and V_X respectively. For the sake of understanding the operation of the drive circuit by itself, the other terminals of the sensor may be treated as if they were tied to ground, because the sensor signal measurement circuit regulates the voltage at these nodes. This circuit is essentially a relaxation oscillator where the capacitance of the sensor, the charging current I_C, and the comparator hysteresis V_H determine the frequency of oscillation.

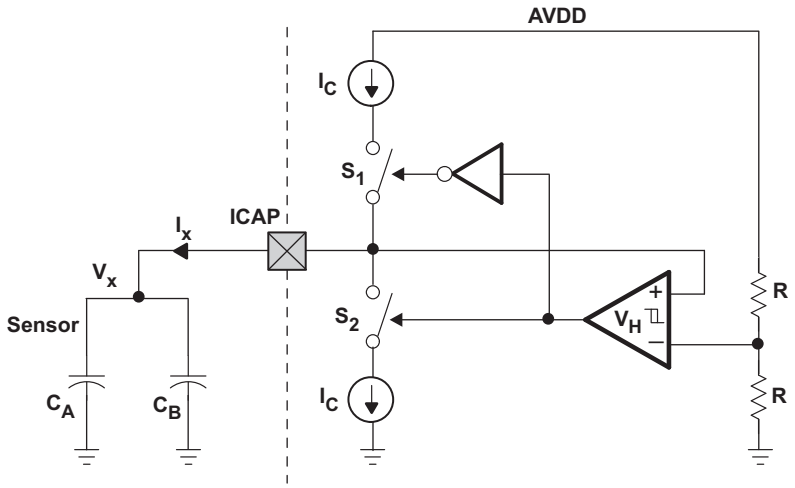


Figure 6-2. Capacitive Sensor Drive Circuit

To illustrate the circuit operation, the sensor voltage V_X is initially set to 0 V. In this state, the positive terminal of the hysteretic comparator is lower than its negative reference terminal, producing a logical zero at the output. This results is switch S2 is open and switch S1 is closed, allowing the upper current source to charge the sensor capacitance. Figure 6-3 shows the resulting waveform. Equation 1 calculates the linear ramp up slope of the voltage, V_X:

$$\frac{dV_x}{dt} = \frac{1_C}{C_A + C_B} \tag{1}$$

After V_X is charged up to the high threshold of the comparator, the circuit inverts the states of switches S_1 and S_2. By closing S_2 and opening S_1 the lower current source begins to discharge the sensor capacitances, making V_X ramp down with an equal but opposite rate as before. Once V_X reaches the low threshold of the comparator, the circuit again inverts the states of the switches and returns to the positive charging state. This process of charging and discharging repeats with a period characterized as shown in Equation 2.

$$T = \frac{2 \cdot V_H}{I_C} \cdot (C_A + C_B) \tag{2}$$

Both the comparator hysteresis voltage V_H and capacitor charging current I_C are configurable to allow control of the oscillation period for a particular sensor. Bits CV[1..0] in the Capacitive Sensor Settings Register (CAPSEN) can be used to set V_H. V_H can be set between 100 mV and 700 mV with four possible steps. Bits CI[2..0] in the Capacitive Sensor Settings Register (CAPSEN) can be used to set I_C, with possible values between 5 µA and 22 µA with eight possible steps. For more information on programming this device please refer to the *PGA400-Q1 Programming Application Note* (SLDA015)

NOTE

For capacitive sensors, one common set of configurations registers are implemented. If different settings are needed for the two capacitive sensors, then the software must dynamically update the register values.

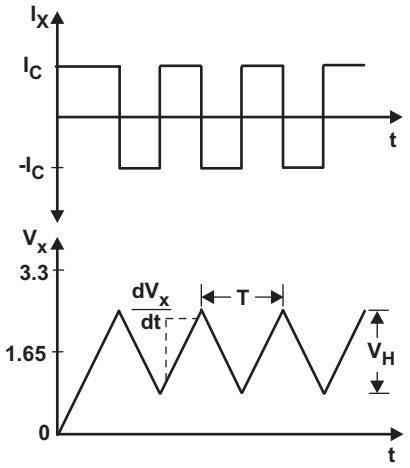


Figure 6-3. Capacitive Sensor Drive Waveforms

6.5 Internal Temperature Block and External Temperature Sensing

The device has the ability to perform temperature compensation via an internal or external temperature sensor. The user can select the source of the sensor with the TEMP_SEN bit in the Sensor Control Register (SENCTRL). When the TEMP_SEN bit is set to "0" the internal temperature sensor is used, and when the TEMP_SEN bit is set to "1" the external temperature sensor is used. For more information on programming this device please refer to the *PGA400-Q1 Programming Application Note* (SLDA015)

6.5.1 Internal Temperature Sensor

The device contains an internal temperature sensor which is converted by an ADC and made available to the 8051 microprocessor so that appropriate temperature compensation algorithms can be implemented in software. The nominal relationship between the device temperature and the ADC Code is shown in Equation 3.

ADC Code = *2.8* TEMP -80*, *TEMP* is temperature in °C. (3)

6.5.2 External Temperature Sensor

The device accepts a temperature from an external temperature sensor via the VIN3 pin. The input temperature needs to be in the form of a voltage.

NOTE

The Offset TC block has been configured to operate with the internal temperature sensor transfer function. If an external temperature sensor is used and the user needs to use Offset TC compensation, then the temperature-to-voltage transfer function of the external temperature sensor has to match the transfer function of the internal temperature sensor.

6.6 Using the Analog Front End

The PGA400 can be used to interface with Resistive Bridge Sensors as well as Capacitive Sensors. To enable multiple sensors of either type a series of muxes are used. These muxes are controlled by the Sensor Control Register (SENCTRL) and Capacitve Sensor Setting Register (CAPSEN).

The SEN_TYP bit of the Capacitive Sensor Settings Register (CAPSEN) configures the device to be used with either resisitive or capacitve sensor types. When this bit is set to '0', the device is configured for capacitive sensors and when the bit is set to "1" the device is configured for resistive bridge sensors. When either front-end is selected, the other option is disabled and placed in a low quiescent current state.

The Analog Front End (AFE) can also be configured to measure two sensors sequentially. This is controlled via the SEN_CHNL bit in the Sensor Control Register (SENCTRL). When this bit is set to '0', the analog MUX at the input of the AFE is switched to pass the signals present at VIN1P and VIN1N pins. For capacitive sensors, the capacitive sensor drive current is also applied to the ICAP1 pin. When this bit is set to '1', the VIN2P, VIN2N and ICAP2 pins become active. The SEN_CHNL bit also controls which External Special Function Registers (ESFRs) are applied to the Stage 1 Gain, Stage 2 Gain, Offset, Offset TC and the Sign bits.

In addition the sensor supply regulator can be independently enabled or disabled via the VBRG_EN bit in the Sensor Control Register (SENCTRL). This allows the VBRG 3.3 V output to be used with external temperature sensors while the AFE is configured in capacitive sensor mode. For more information on programming the PGA400-Q1 please refer to the

6.7 Stage 1 Gain Block

When the device is configured to interface with resistive sensors, the first gain block that the signal passes through in the AFE is the Stage 1 Gain block. This gain block is designed with precision, low drift, low flicker noise amplifiers.

The gain of this stage is adjustable to accommodate sensors with a wide-range of signal spans and can be set from 3V/V to 51V/V in 8 possible steps. The Stage 1 Gain has two independent registers, Sensor 1 Gain Register (SEN1GAIN) and Sensor 2 Gain Register (SEN2GAIN), so that two different resistive sensors can be connected with different gain settings. For Stage 1 Gain settings use either the S1_G1 bits or the S2_G2 bits in the registers mentioned above. The gain setting that is used depends on the SEN_CHNL bit in Sensor Control Register (SENCTRL). For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

Table 6-1 outlines the ranges of of resistive bridge sensor characteristics that are compatible.

Table 6-1. Target Resistive Bridge Sensors

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Resistive bridge resistance	$-40°C \le T_A \le 150°C$	2		20	KΩ
Resistive bridge resistance TC		–350		4800	PPM/°C
Resistive bridge offset (compensated in Analog Front End)	$T_A = 25°C$	–33		33	mV/V
Resistive bridge offset TC (compensated in Analog Front End)		–40		40	µV/V/°C
Resistive bridge span	$T_A = 25°C$	1.4		75	mV/V

6.8 Self Oscillating Demodulator Block

Figure 6-4 shoes an essential schematic of the capacitive sensor signal measurement circuit. . The Sensor Voltage Supply block discussed in is depicted only as a functional block called Sensor Drive that provides the sensor drive current via the ICAPx pin and the clock signals S_1 and S_2 that are used by the synchronous demodulator in the measurement circuit. As with the ICAP supply circuitry the demodulator block circuitry toggles between two states during normal operation. In one state the S_1 switches are closed while the S_2 switches are open and in the other state the S_1 switches are open while the S_2 switches are closed.

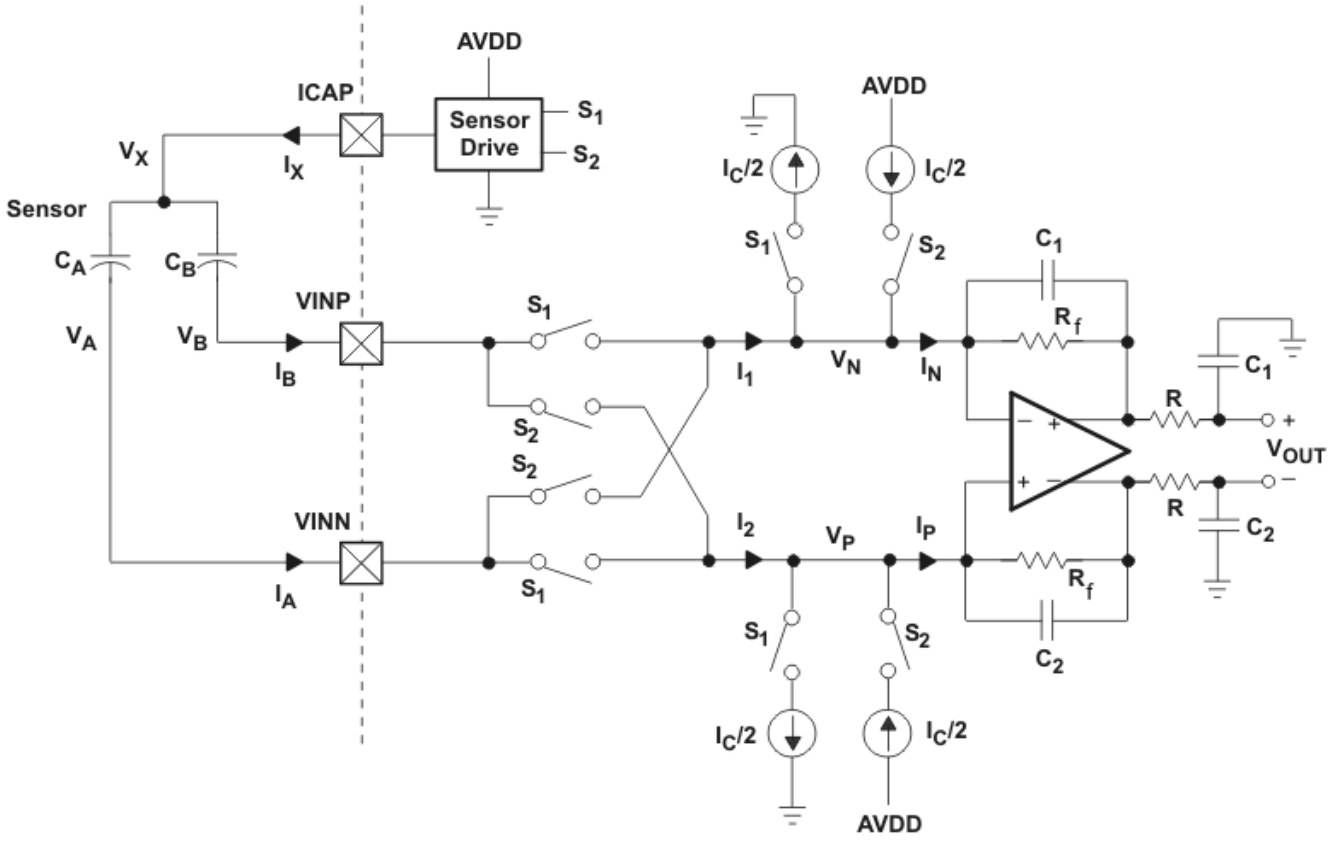


Figure 6-4. Capacitive Sensor Signal Measurement Circuit

To illustrate the operation of the circuit, assume that it has been given sufficient time to settle and is now operating in its normal steady-state mode of operation. During the positive charging phase, I_X is positive and the S_1 switches are closed. In this state, the amplifier seeks to regulate its input terminals to the same potential, creating a virtual ground at the VINP and VINN pins. This allows Equation 4 to be expresses for $I_X$as:

$$I_X = (C_A + C_B) \bullet \frac{dV_X}{dt} \tag{4}$$

In a similar manner, Equation 5 describes the currents through C_A and C_B and the difference between these currents.

$$I_A = C_A \bullet \frac{dV_X}{dt} \tag{5}$$

$$I_B = C_B \bullet \frac{dV_X}{dt} \tag{6}$$

$$\Delta I = (I_A - I_B) = (C_A - C_B) \bullet \frac{dV_X}{dt} = I_X \bullet \left(\frac{C_A - C_B}{C_A + C_B} \right) \tag{7}$$

The drive current is split between the capacitors in proportion to their relative difference. Measuring ΔI provides a means to infer the value of the difference in capacitance (C_A – C_B) or the value of one of the capacitors if the other is known. Also, driving the sensor with a current source and measuring the resulting difference in current has the benefit of being fully differential and thus less susceptible to common-mode disturbances and non-idealities. Note that the expressions for I_A and I_B may are rewritten in terms of common-mode and differential-mode components in Equation 8 and Equation 9.

$$I_A = \frac{I_X}{2} + \frac{\Delta I}{2} \tag{8}$$

$$I_B = \frac{I_X}{2} - \frac{\Delta I}{2} \tag{9}$$

The capacitive sensor signal measurement circuit extracts and amplifies ΔI. Figure 6-5 illustrates the current waveforms at different points in the circuit of Figure 6-4. The currents into and out of the sensor are shown on axis (a). Initially, the circuit is in the discharge phase where I_X is negative and S_2 switches are closed. After some time, the state switches to the charge phase where the S_1 switches are closed. This process of changing the state of the circuit continues periodically with a frequency set by the sensor drive circuit.

During each half cycle the I_X current is split into the individual capacitor currents I_A and I_B. As shown in Figure 6-5(b), while the S_1 switches are closed $I_2 = I_A$ and $I_1 = I_B$, but when the S_2 switches are closed the currents are inverted such that $I_2 = I_B$ and $I_1 = I_A$. Because the sign of I_X is also changing, the difference between I_2 and I_1 remains constant and equal to ΔI (ignoring the glitches that occur at phase transitions).

While the S_1 switches are closed, half the sensor drive current (I_C/2) is subtracted from I_2 and I_1 and while the S_2 switches are closed, half the sensor drive current is added to them. This removes the cycle-to-cycle offset in Figure 6-5(b), delivering the DC currents I_P and I_N to the trans-impedance amplifier, as shown in Figure 6-5(c) where I_P – I_N = ΔI. For low frequency signals, the output voltage of the amplifier is shown in Equation 10.

$$V_{out} = R_f \cdot \Delta I = R_f \cdot I_C \cdot \left(\frac{C_A - C_B}{C_A + C_B} \right) \tag{10}$$

For a given sensor, the drive current I_C should be adjusted to keep V_{OUT} < 1.65 V over the expected operating conditions of the sensor to avoid saturating the ADC input.

NOTE

for some types of wide span sensors, it may be necessary to reduce the gain set by the value of R_f in the transimpedance amplifier. The drive current I_C and feedback resistance R_f can be adjusted via Capacitive Sensor Settings Register (CAPSEN). For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

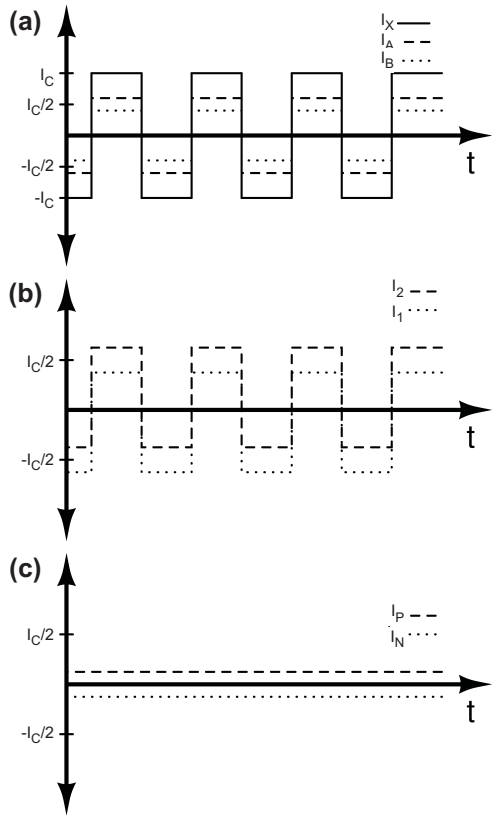


Figure 6-5. Current Waveforms in the Sensor Signal Measurement Circuit

This process of changing the state of the circuit continues periodically with a frequency set by the sensor drive circuit described in Equation 11.

$$f = \frac{I_C}{2 \cdot V_H \cdot (C_A + C_B)} \tag{11}$$

BEcause the op-amp must settle at each switching cycle, there is an upper bound imposed on the sensor drive frequency. Using a minimum half-cycle time of seven times the op-amp settling time and a minimum op-amp GBW of 7 MHz, shows the following upper bound on the switching frequency:

$$f_{MAX} \leq 800 \text{ kHz}$$

In reality, there are glitches and residual up-converted noise in the I_P and I_N signals. For this reason, the trans-impedance amplifier has a low-pass characteristic, with one pole set by the feedback elements R_f and C_f, and a second pole at the output set by R and the same capacitance C_f. For most sensor types, R is equal to R_f. In this case, the frequency dependent trans-impedance may be expressed as shown in Equation 12.

$$Z(s) = \frac{R_f}{1 + s \cdot R_f \cdot C_f)^2} \ \Omega \tag{12}$$

Where with nominal values of R_f = 625 kΩ and C_f = 16 pF, the corner frequency of the filter is 15.9 kHz. If the minimum permissible ripple suppression is chosen to be 40 dB at the switching frequency, and the corner frequency is rounded up to 20 kHz, illustrates the lower bound on the switching frequency:

$$f_{min} \geq 200 \text{ kHz}$$

For a given sensor, the drive circuit comparator hysteresis value V_H and the drive current I_C should be chosen so that the switching frequency remains within the range of 200 to 800 kHz as the sensor capacitance varies within its expected range.

Table 6-2 outlines the ranges of compatible capacitive bridge sensor characteristics.

Table 6-2. Target Capacitive Sensors

PARAMETER	CONDITION	MIN	MAX	UNIT
Capacitive sensor initial capacitance (Cp+Cr)		10	310	pF
Capacitive sensor offset (compensated in Analog Front End)	(Cp,0 – Cr,0)/(Cp,0 + Cr,0)	–0.16	0.16	
Capacitive sensor span	(Cp,100 – Cr,100)/(Cp,100 + Cr,100)	0.04	1.00	
Capacitive sensor offset TC			0.8	%Cv,0/ °C

6.8.1 Configuring the Capacitive Sensor Interface for a Particular Sensor

A general procedure for choosing what values to use for the capacitive sensor drive current (I_C), drive voltage comparator hysteresis (V_H) and trans-impedance (R_f) is the following:

- Find the values of I_C that maintain V_{OUT} below 1.65 V for the maximum sensor span plus offset
- Using the largest allowed value for I_C and the minimum and maximum total sensor capacitance (C_A+C_B), find a value for V_H that maintains the switching frequency within the range of 200 kHz to 800 kHz
- If the frequency constraints cannot be met, reduce the value of I_C and iterate to find an optimal solution

This procedure can be applied to configure the capacitive sensor interface with total capacitances ranging from 10 pF to 300 pF and span plus offset ratios (C_A–C_B)/(C_A+C_B) up to 0.36.

The Stage 1 gain has two independent registers for the two sensors that can be potentially connected. The Stage 1 gain setting used depends on the SEN_CHNL bit in the Sensor Control Register. For more information on programming the PGA400-Q1 please refer to the the *PGA400-Q1 Programming Application Note* (SLDA015).

6.9 Sign Bit Block

The device has a sign bit block that is used for span sign compensation. This block is used to change the polarity of the first stage output, and it is implemented through the use of four switches. The switches are set through the use of the S1_INV bit for sensor 1 and the S2_INV bit for sensor 2 in the Sensor Control Register (SENCTRL). There are two independent sign bit settings to accommodate configuring the polarity for two independent sensors. The sensor sign bit used is based on the SEN_CHNL bit in the Sensor Control Register. For more information on programming the PGA400-Q1 please refer to the the *PGA400-Q1 Programming Application Note* (SLDA015).

6.10 Offset and Offset TC Compensation Blocks

The offset compensation circuit can be configured to null out the sensor offset and first order offset temperature coefficient. The offset compensation block is located between the Sign Bit block and the Stage 2 Gain block as shown in the Section 2.

The offset compensation, V_{COMP}, is a value that is subtracted from the output of the sign bit block. This offset provides a means to null the sensor offset prior to Stage 2 Gain. The offset compensation circuit block provides ten bits of zero-order compensation and six bits of first-order TC compensation.

A more detailed block diagram of the offset compensation subsystem is shown in Figure 6-6. As shown V_{comp} is derived from two references, V_{BG} and V_{PTAT}. Where V_{BG} is a precise temperature independent band-gap reference voltage, and V_{PTAT} is a proportional-to-absolute-temperature voltage. In PGA400-Q1, the gains in the offset compensation circuitry (A, B, C) have been designed assuming the following characteristics about the reference signals:

$$V_{BG} = 1.23\ V \quad (13)$$

$$V_{PTAT}(T) = k_{PTAT} \bullet (T + 273) + \xi_{PTAT} \quad (14)$$

where

$$k_{PTAT} = 3.7\ mV/°C \text{ and } \xi_{PTAT} = -47\ mV \quad (15)$$

NOTE

If an external temperature sensor is used, the signal applied to the VIN3 pin must have the same temperature dependency as the above mentioned V_{PTAT} signal or else the offset TC compensation does not work as intended.

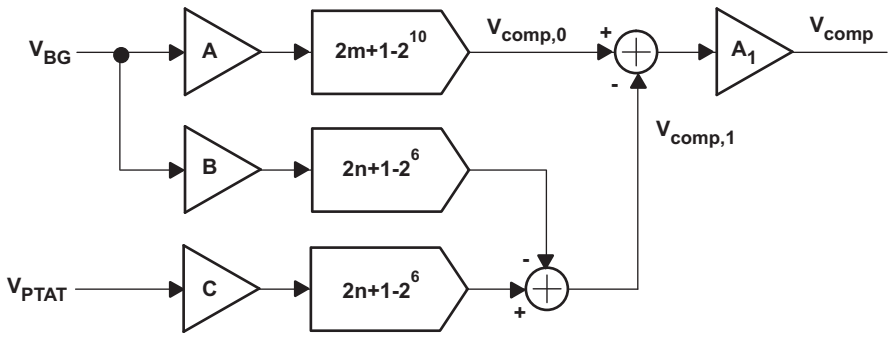


Figure 6-6. Block Diagram of Offset Compensation Circuit

The zero-order portion of V_{COMP} is produced by scaling V_{BG} by the gain A to generate the reference for a 10-bit DAC. The DAC scales this reference by $2m+1-2^{10}$, where m is decimal equivalent of the DAC's digital input and ranges from 0 to 1023. The zero-order portion of the compensation voltage is expressed as a function of m as shown in Equation 16.

$$V_{COMP,0}(m) = V_{BG} \bullet A \bullet (2 \bullet m + 1 - 2^{10})\ V \quad (16)$$

The first order portion of V_{COMP} is constructed from the difference between scaled versions of V_{PTAT} and V_{BG}. The reason for this is that the temperature compensation signal should pivot about a particular reference temperature, which ideally would be the same temperature at which the zero-order portion of the sensor offset is calibrated out. Because V_{PTAT} pivots about 0 K, a temperature independent offset must be introduced to shift the pivot temperature up to a practical value like 22°C. The first-order portion of the compensation voltage is expressed in Equation 17.

$$Vcomp,1(n,T) = (C \bullet [k_{PTAT} \bullet (T + 273) + \xi_{PTAT}] - B \bullet V_{BG}) \bullet (2 \bullet n + 1 - 2^{6})\ V \quad (17)$$

Where the reference temperature about which this function pivots may be expressed in terms of the other variables as shown in Equation 18.

$$T_R = \frac{1}{k_{PTAT}} \bullet \left(\frac{V_{BG} \bullet B}{C} - \varepsilon_{PTAT} \right) - 273°C \quad (18)$$

The gains B and C are set to produce a reference temperature of approximately 22°C.

When Equation 17 and Equation 18 are combined and consolidate the values of the constants, the final output voltage of the offset compensation circuit is expressed as a function of m, n, T, and A_1 in the following way:

$$V_{comp}(m, n, T, A1) = A_1 \bullet \frac{1277}{3} \bullet \left[250 \bullet (2 \bullet m + 1 - 2^{10}) + 4.921 \bullet (T-22) g (2 \bullet n + 1 - 2^{6})\right] nV \quad (19)$$

For resistive sensors, the gain used for the offset compensation calculation is always the same as the first stage gain in the AFE and is controlled by the same registers. For capacitive sensors, A_1 is an independent variable that may be set to meet a specific sensor or noise requirements.

NOTE

The above voltage V_{comp} is subtracted (differentially) from the output of the first stage.

The Offset and Offset TC has two independent registers, Sensor 1 Offset Register (SEN1OFF1 and SEN1OFF2) and Sensor 2 Offset Register (SEN2OFF1 and SEN2OFF2), to accomodate for two independent sensors that can be potentially connected. The sensor offset value used is based on the SEN_CHNL bit in the Sensor Control Register (SENCTRL). For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.11 Stage 2 Gain Block

The Stage 2 Gain block is contructed with a low flicker noise, low offset amplifier. Both resistive bridge sensors and capacitive sensors share this gain stage. The gain setting for this stage ranges from 1 V/V to 25 V/V in 32 possible steps.

The Stage 2 Gain block has two independent registers, Sensor 1 Gain Register (SEN1GAIN) and Sensor 2 Gain Register (SEN2GAIN). This accomodates two different sensors that can be connected with different gain settings. The Stage 2 gain is determined by the SEN_CHNL bit in Sensor Control Register. For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.12 ADC Buffer Blocks

The device has two buffer blocks, one for the pressure signal path and one for the temperature signal path.

6.12.1 Analog to digital Converter Buffer 1

The ADC Buffer 1 is a differential amplifier with 2X gain that is used to condition the pressure signal before reaching the Analog to Digital Converter (ADC).

In addition to gain this block can be configured to provide a level shift using the ADC_BUF bit in Sensor Control Register (SENCTRL). When this bit is set to ‘0’, no offset is introduced to the signal, and the output of the ADC buffer is simply two times the output of Gain Stage 2. When this bit is set to ‘1’, a –1.65 V offset is introduced such that the output of the ADC buffer is equal to two times the output of Gain Stage 2 minus 1.65 V. The Level Shift feature of the ADC Buffer shifts the output of the Stage 2 Gain so that the full dynamic range of the sigma-delta modulator can be used.

6.12.2 Analog to digital Converter Buffer 2

The ADC Buffer 2 is a unity gain differential amplifier. This buffer block conditions the temperature signal before reaching the ADC.

6.13 Sigma Delta Modulator Blocks

There are two independent Sigma Delta Modulator ADCs, one for the pressure signal and another for the temperature signal.

6.13.1 Sigma Delta Modulator for AD Converter 1

The Sigma Delta Modulator 1 block is a 1-bit 1MHz sigma-delta modulator for the pressure sensor signal. To further condition the signal this stage is followed by two stages of digital decimation filters.

6.13.2 Sigma Delta Modulator for AD Converter 2

The Sigma Delta Modulator 2 block is a 1-bit 128kHz sigma-delta modulator for the temperature signal. The input signal to the sigma-delta modulator can come from either the internal or external temperature. The output of this ADC is followed by a single decimation filter.

6.14 Decimation Filter Blocks

The device contains three Signal Decimation FIlters. Two back to back decimation filters for the pressure sensor signal path and one decimation filter for the termperature path.

6.14.1 ADC1 Decimation Filter Blocks

The sensor signal path contains two decimation filters in series with each other. The first decimation filter has a fixed decimation ratio and a second decimation filter that has a variable decimation ratio.

The 1st Stage Decimator Filter has a fixed decimation ratio of 32. Based on the 1MHz sampling frequency of the sigma-delta modulator, the output rate of the 1st stage decimator is fixed at 32 µs per sample.

The 2nd Stage Decimator has a variable decimation ratio. This filter further decimates the output of the first stage decimator. The decimation ratios of the second stage can be configured for a decimation ratio of 2, 4, or 8 using the OSR[1..0] bits in the Decimator and Low Power Control Register (DECCTRL). For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

The output of the second decimation filter in the sensors signal path is a 16 bit **signed** value. Some example second stage decimation output codes for given differential voltages at the input of the sigma delta modulator are shown in Table 6-3:

Table 6-3. Input Voltage to Output Counts for the Signal Channel ADC

SIGMA DELTA MODULATOR DIFFERENTIAL INPUT VOLTAGE	NOISE-FREE OUTPUT
–3.3V	–32768
–1.65V	–16384
0	0
1.65V	16383
3.3V	32767

6.14.2 Decimation Filters for AD Converter 2

The temperature path contains one fixed ratio decimation filter block after the sigma delta modulator. The filter is 10-bit with fixed decimation ratio of 1024. Based on the 128-kHz sampling frequency, the output rate of the fixed ratio decimation filter is fixed at 8 ms per sample.

The output of the temperature channel decimation filter is a 10 bit **signed** value. The equation to calculate the relationship between the input voltage at VIN3 and the output of the decimator block is shown below.

ADC Code = *760* VIN3 -820*, *VIN3* is voltage at the input of the buffer in volts. (20)

Table 6-4 summarizes the relationship between the internal temperature sensor and the decimator output.

Table 6-4. Input Voltage to Output Counts for the Temperature Channel ADC

INTERNAL TEMPERATURE	NOISE-FREE OUTPUT OF TEMPERATURE CHANNEL DECIMATOR
–40°C	-196
–20°C	-140
0°C	-83
20°C	-27
40°C	28
150°C	338

6.14.3 Accessing the ADC Values for the 8051

the ADC Decimator Output Register (ADCMSB and ADCLSB) makes available the output of all three decimators that are available to the microprocessor.

The microprocessor specifies which decimator is loaded by writing a "1" to the appropiate bit in the Load ADC Decimator Shadow Register (LD_DEC).

If more than 1 bit in the LD_DEC register is set to 1 simultaneously, then only one decimator output is loaded into ADCMSB and ADCLSB register. The priority used to determine which decimator output gets loaded is as follows:

- Decimator 1 Output
- Decimator 2 Output
- Temperature Decimator

For more information on programming the PGA400-Q1 please refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.15 8051 WARP Microprocessor Block

The 8051 WARP microprocessor is an exceptionally high-performance version of this popular 8-bit microcontroller, requiring only 2 clocks per machine cycle rather than the 12 clocks per cycle of the industry standard device while it maintains functional compatibility with the standard device

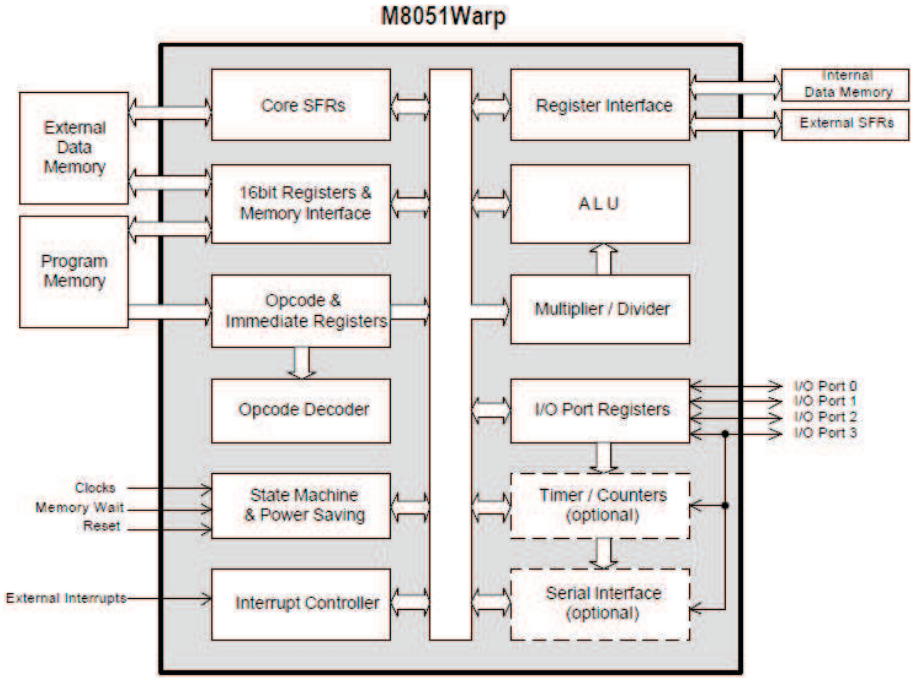


Figure 6-7. 8051W Core. The 8051W core includes two 16-bit timers and serial interface.

6.16 Digital Interface

The digital interfaces are used to access (read as well as write) the internal memory spaces described in Section 6.20. Each interface uses different pin(s) for communication. The device has three separate modes of communication:

1. One-Wire Interface (OWI)
2. Serial Peripheral Interface (SPI)
3. Inter-Integrated Circuit (I^2C)

Each communication mode has its own protocol of communication, but all three access the same memory elements within the device. For all three communication modes the PGA400-Q1 device operates as a slave device.

Figure 6-8 shows the interface between the 8051W, the Memory block and the Digital Interface. **In the PGA400-Q1, only the Digital Interface OR the 8051W can access can access the internal memory spaces.** It is not possible for both 8051W and the Digital Interface to access the memory spaces simultaneously. Therefore there is an access selection bit called IF_SEL in the Micro/Interface Control Register (MICRO_IF_SEL_T) that allows either the 8051W microprocessor or the digital interfaces to have access to the OTP, EEPROM, ESFR and RAM memory spaces.

Figure 6-8 also shows that a special memory space called the Test Registers are only accessible only via the Digital interface. Since the Micro/Interface Control Register is in the Test Register memory block which is only accessible via the digital interface, only the digital interfaces can change the memory access selection.

To select the specific digital interface that is used for communication the DI_CTRL[1:0] bits in the Digital Interface Control Register (DI_CTRL) need to be set. If DI_CTRL is configured for I2C, then GPIO1 and GPIO3 automatically configures for I^2C operation.

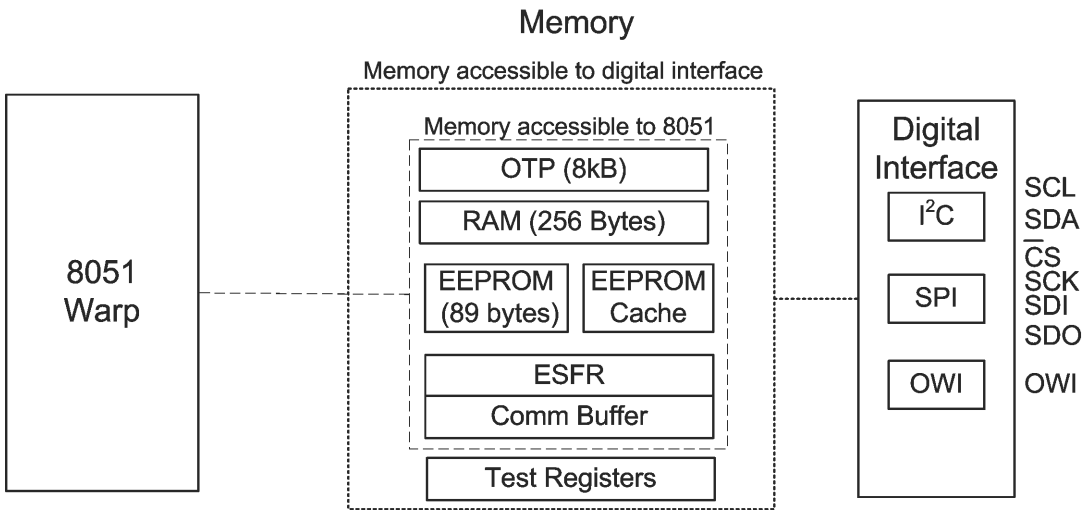


Figure 6-8. Digital Interface

NOTE

If Digital Interface is used to access the internal memory, the 8051W must enter reset state (to prevent the 8051W from accessing the memory. The 8051W operates in reset state using the "MICRO_RESET" bit in the Micro/Interface Control Register (MICRO_IF_SEL_T).

NOTE

The internal memory space internal is accessible via the Digital Interface without the need for the user to implement any communication software in the 8051W. The user must implement communication software, in the form of an interupt service routine, only if the user wishes to communicate with the PGA400-Q1 while 8051W is not in reset state. This interupt service routine is used in conjuction with a communication buffer interface, that is available in both the ESFR and Test Memory address spaces.

NOTE

While the 8051W is not in a reset state, it transfers data to the internal memory space using the Digital Interface. This transfer is accomplished using the communication buffer that exists between the Test Register memory space and the ESFR memory space (shown as COMM BUFFER in Figure 6-8).

6.17 One-Wire Interface (OWI)

The device includes a One-Wire Interface (OWI) digital communication interface. The main function of the OWI is to enable writes to and reads from all addresses available for OWI access. These include access to most Test Register and ESFR memory locations.

6.17.1 Overview of OWI Interface

The OWI digital communication is a master-slave communication link in which the PGA400-Q1 operates as a slave device only. The master device controls when data transmission begins and ends. The slave device does not transmit data back to the master until it is commanded to do so by the master. A logic 1 (high) value on the one wire interface is defined as a *recessive* value, while a logic 0 (low) value on the one-wire interface is defined as a *dominant* value.

The VOUT1/OWI pin acts as both an analog DAC output and the interface communication pin, so that when the device is embedded inside of a system module only three pins are needed (VOUT1/OWI pin, VDD and GND). The 8051 microprocessor has the ability to control the activation and deactivation of the OWI interface based upon the signal driven into the VOUT1/OWI pin.

During normal operation the DAC is the last stage of the sensor signal path, and drives data out on the VOUT1/OWI pin in the form of an analog signal. To change to OWI communication mode this pin must be driven with an appropiate activation signal described in Section 6.17.2.

Figure 6-9 shows a functional equivalent circuit for the structure of the OWI and DAC circuitry.

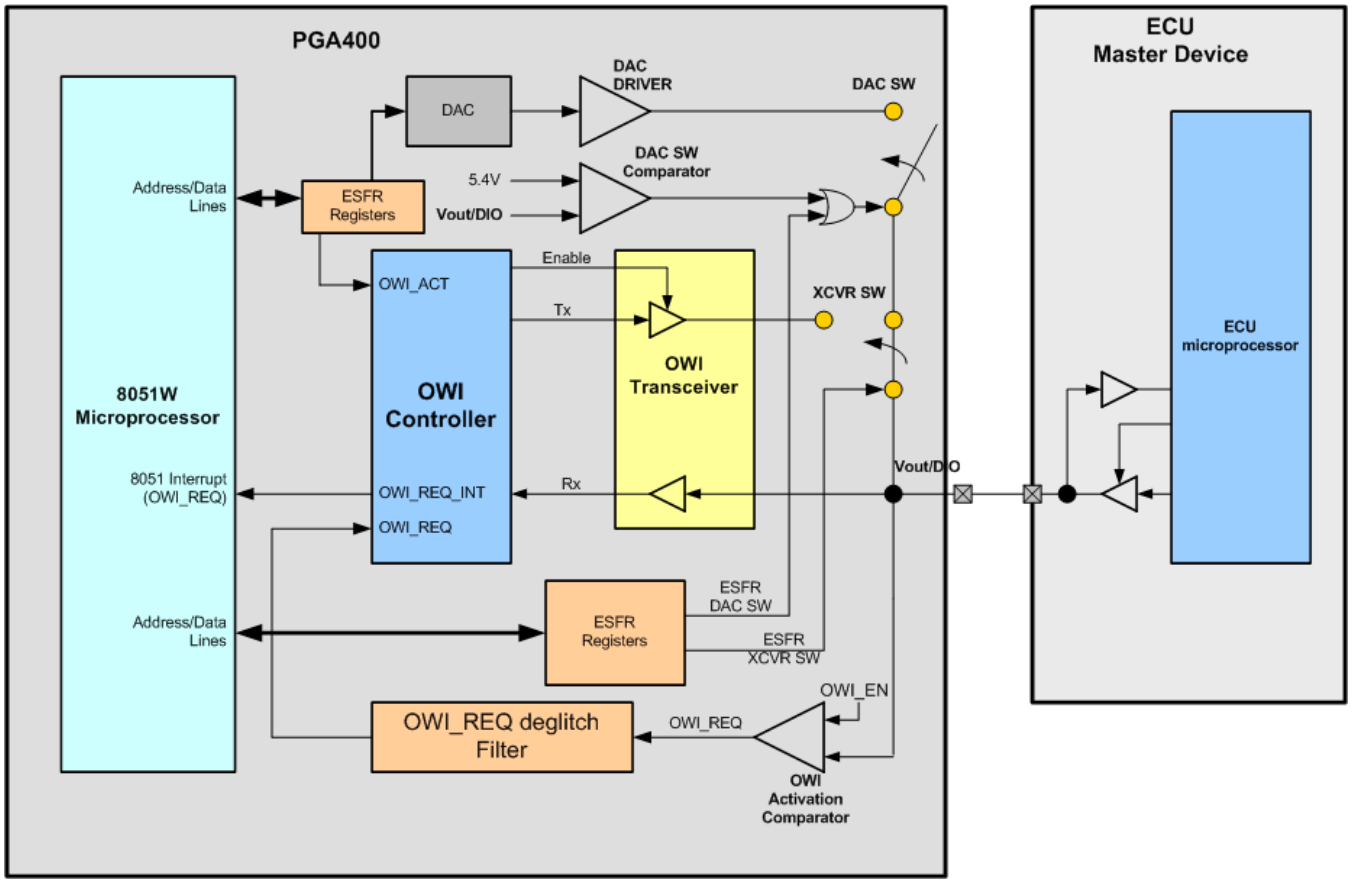


Figure 6-9. OWI System Components

6.17.2 Activating and Deactivating the OWI Interface

6.17.2.1 Activating OWI Communication

If the device is operating in the normal operation where the DAC is active and I2C or SPI communication modes are not enabled the following activation signal can be driven into the VOUT1/OWI pin to place it into OWI communication mode. The process begins with driving the OWI_EN voltage on the VOUT1/OWI pin. As soon as the DAC voltage exceeds 5.4 volts the DAC is switched off by by a comparator. Once the pin voltage reaches the OWI_EN voltage threshold a deglitch timer begins. Once the pin voltage has been asserted for a time greater than the deglitch time the OWI Activation Comparator transmits a logic 1 value to the OWI Controller.

This deglitch time is set by the OWI_DEGLITCH_SEL bit in the Digital Interface Control Register (DI_CTRL), and has the following properties:

- OWI_DEGLITCH_SEL = ‘0’ → OWI Activation deglitch time = 1ms

- OWI_DEGLITCH_SEL = ‘1’ → OWI Activation deglitch time = 10ms
- The default value for OWI_DEGLITCH_SEL bit is ‘0’, which corresponds to deglitch time of 1ms.

When the high voltage has been maintained for the proper deglitch time, the pin must then be driven back to the standard 5V IO voltage for an additional deglitch time set by the same bit as before. During this second deglitch time the DAC becomes active again only until the the second deglitch time has passed. Once this second deglitch period is over the OWI controller generates an OWI activation interrupt that is sent to the 8051. This user interrupt service routine switches the VOUT1/OWI pin's mode by writing to the appropriate registers. The OWI transceiver is switched to the VOUT1/OWI pin and the DAC is placed back into the OFF state. The capability to drive the appropiate OWI_EN voltage must be provided in the test environment.

The XCVR switch, controlled by an ESFR register, changes the output drive from the unidirectional DAC analog signal to the bi-directional OWI digital signal interface. Once this switch is selecting the OWI transceiver, OWI data can be transmitted and received through the VOUT1/OWI pin. The OWI transceiver is responsible for translating voltage levels to appropriate logic levels so that the OWI controller may process the OWI data. The OWI_REQ deglitch filter ensures that no invalid activation signals are transmitted from the analog OWI Activation Comparator to the 8051 interrupt input. Both the DAC switch ESFR and the XCVR switch ESFR must be set via the OWI interrupt service routine. It is recommended to set the DAC switch to the OFF position before setting the XCVR switch to the OWI mode.

If the device is already in SPI communication mode or I_2C communication mode, enabling OWI communication changing the DAC enable bit and the OWI transceiver enable bit in the Digital Interface Control Register (DI_CTRL) is the only requirement. The register bits can be set manually in the following order.

1. The register bits DI_CTRL[1:0] in the Digital Interface Control Register (DI_CTRL) need to be set to 0b10. This activates the OWI controller and deactivates the DAC via the DAC switch.
2. The OWI_XCR_EN bit in the Digital Interface Control Register (DI_CTRL) must be set to 1. This turns on the OWI transceiver and switches the VOUT1/OWI pin to the OWI transceiver.

NOTE

Note that DI_CTRL[1:0] and OWI_XCR_EN bits can be written simultaneously (in 1 write command). However, because the state of the VOUT1/OWI is unknown during the transition from VOUT1 to OWI, it is recommended that the master wait at least 15 ms before transmitting the OWI command.

6.17.2.2 Deactivating OWI Communication

In order to deactivate the OWI communication the following two steps must be performed in any order.

- The OWI_XCR_EN bit in the Digital Interface Control Register (DI_CTRL) must be set to 0. This turns off the OWI transceiver and switch the VOUT1/OWI pin to the DAC driver.
- The register bits DI_CTRL[1:0] in the Digital Interface Control Register (DI_CTRL) must to be a value other than 0b10. This selects a different Digital Interface (either I2C or SPI) and it also switchs on the DAC driver.

6.17.3 OWI Communication Error Status

The device has the ability to detect and report errors in OWI communication. The OWI Error Status 1 Register (OWI_ERR_1), and OWI Error Status 2 Register (OWI_ERR_2) contain the error bits. The communication errors that are reported with the registers include

- Out of range communication baud rate
- Invalid SYNC field
- Invalid STOP bits in command and data
- Invalid OWI command

For more information on OWI protocol, operation, avaialble commands and example communication refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.18 Serial Peripheral Interface (SPI) Interface

The device includes a Serial Peripheral Interface (SPI) digital communication interface. The main function of the SPI is to enable writes to and reads from all addresses available for SPI access.

6.18.1 Overview of SPI Interface

SPI is a synchronous, serial, master-slave, communication standard that requires the following four pins:

- SDI: SPI slave in master out, serial input pin.
- SDO:SPI slave out master in, serial output pin (tri-state output)
- SCK: SPI clock which controls the communication.
- $\overline{CS}$: chip select (active low)

SPI comminucates in a master/slave style where only one device, the master, can initiate data transmissions. The PGA400-Q1 always acts as the slave in SPI communication, where whatever external device that is communicating to it becomes the master mode. Both devices begin data transmission with the most significant bit (MSB) first.

Because multiple slave devices can exist on one bus, the master node is able to notify the specific slave node that it is ready to begin communicating with by driving the $\overline{CS}$ line to a low logic level. In the absence of active transmission, the master SPI device places the device in reset by driving the $\overline{CS}$ pin to a high logic level. During a reset state the SDO pin operates in tri-state mode. For the SPI interface to have access to memory locations other than test register space, the IF_SEL bit in the Micro/Interface Control Test register (MICRO_IF_SEL_T) has to be set to ‘1’.

6.18.2 Activating the SPI Interface

To activate SPI communication the following steps must be made in order:

1. Place the 8051W in reset by setting the MICRO_RESET bit in the Micro/Interface Control Register (MICRO_IF_SEL_T) to logic "high"
2. Give control of the memory block to the digital interface by setting the IF_SEL bit in the Micro/Interface Control Register (MICRO_IF_SEL_T)to logic "high"
3. Set the DI_CTRL bits in the Digital Interface Control Register (DI_CTRL) to 0b00 for SPI interface

6.18.3 Clocking Details of SPI Interface

Input data on the SDI pin must be valid on the rising edge of the SCK clock, whereas output data on the SDO pin changes during the rising edge of the SCK clock. For SPI timing information the SPI Timing diagram is shown in Figure 5-1.

For more information on SPI protocol, operation, avaialble commands and example communication refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.19 Inter-Integrated Circuit Interface

The device includes an Inter-Integrated Circuit (I^2C) digital communication interface. The main function of the I^2C is to enable writes to, and reads from, all addresses available for I^2C access.

6.19.1 Overview of I2C Interface

I^2C is a synchronous serial communication standard that requires the following two pins for communication:

- GPIO_1/IC_1/SDA: I^2C Serial Data Line (SDA)
- GPIO_3/OC_1/SCL: I^2C Serial Clock Line (SCL)

I²C communicates in a master/slave style communication bus where one device, the master, can initiate data transmission. The device always acts as the slave device in I²C communication, where the external device that is communicating to it acts as the master node. The master device is responsible for initiating communication over the SDA line and supplying the clock signal on the SCL line. When the I²C SDA line is pulled low it is considered a logical zero, and when the I²C SDA line is floating high it is considered a logical one. For the I²C interface to have access to memory locations other than test register space, the IF_SEL bit in the Micro/Interface Control Test register (MICRO_IF_SEL_T) has to be set to logic one.

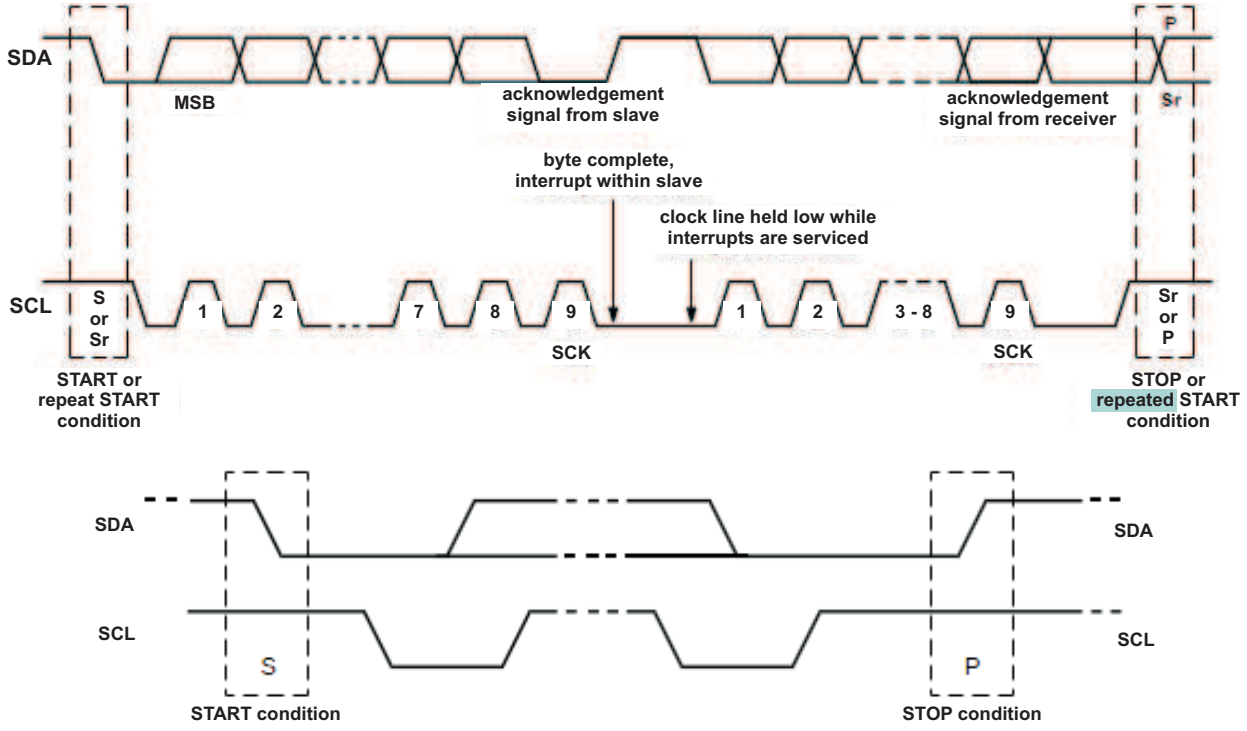
6.19.2 Activating the I²C Interface

To activate I²C communication the following steps must be made in order:

1. Place the 8051W into a reset state by setting the MICRO_RESET bit in the Micro/Interface Control Register (MICRO_IF_SEL_T) to logic "high"
2. Give control of the memory to digital interface by setting the IF_SEL bit in the Micro/Interface Control Register (MICRO_IF_SEL_T)to logic "high"
3. Set the DI_CTRL bits in the Digital Interface Control Register (DI_CTRL) to 0b01 for I²C interface

6.19.3 Clocking Details of I2C Interface

The device samples the data on the SDA line when the rising edge of the SCL line is high, and is changed when the SCL line is low. The only exceptions to this indication a start, stop or repeated start condition as shown in Figure 6-10



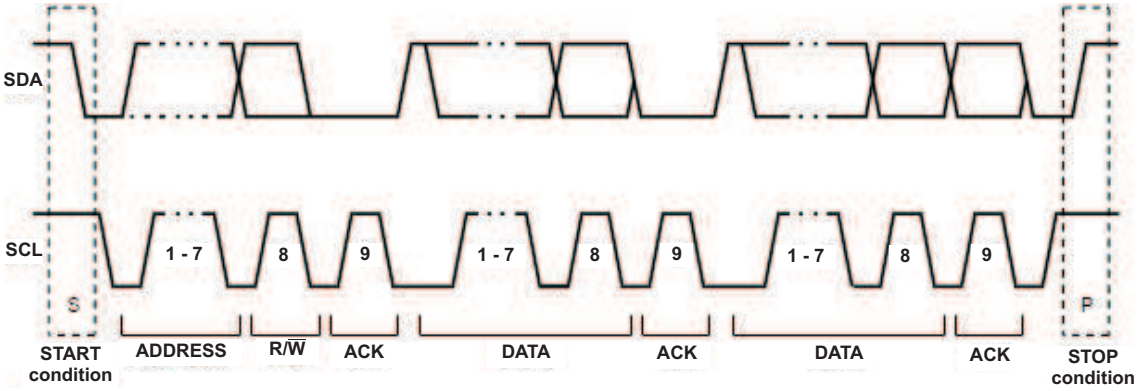


Figure 6-10. I2C Clocking Details

For more information on I^2C protocol, operation, avaialble commands and example communication refer to the *PGA400-Q1 Programming Application Note* (SLDA015).

6.20 Memory

6.20.1 OTP Memory

The OTP Memory space is 8 kB and is located at memory pages 3 and 4. This memory space contains program instructions for the 8051W microprocessor. To program the OTP memory an external VP_OTP voltage needs to be applied to the VP_OTP pin.

The device has the ability to lockout access to all memory spaces except the Test Register space from the digital interface. This helps protect firmware intellectual property. The locking/unlocking of the access to the OTP memory is achieved using 8051W Port 0 in the SFR memory space (P0[7:0]) in the following way:

- If P0(7:0) is set to 0xAA, the Digital Interface is in locked state. In this state, memories cannot be read via Digital Interface. Note that once the Digital Interface is locked, the Micro/Interface Control Test register is also not accessible via the Digital Interface.
- If P0(7:0) is set to 0x00 while the Digital Interface is in locked state, then the memories are accessible via Digital Interface.

The 8051W microprocessor can access all memories even when the memories are in locked state, allowing software programs to execute. If the Digital Interface is in locked state and the CPU watchdog causes a 8051W reset, the Digital Interface maintains the lockout state.

6.20.2 EEPROM Memory

Figure 6-11 shows the EEPROM Bank structure. EEPROM cells within a bank are activated only when reading from or writing to their specific EEPROM bank. Therefore the contents of each EEPROM must be transferred to the EEPROM Cache before reads and writes can occur to that bank. There are a total of six banks of EEPROM, and they are located at memory page 5.

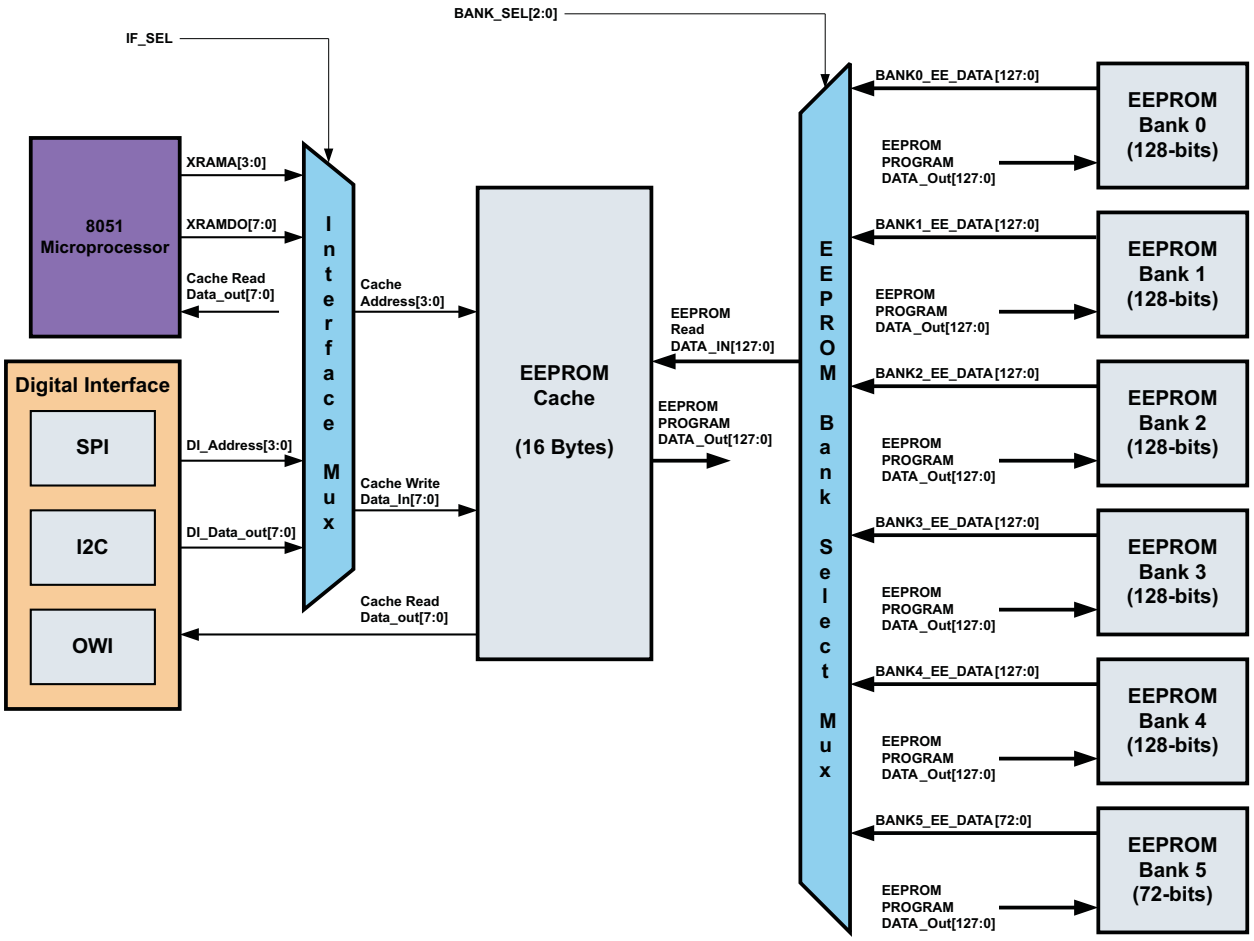


Figure 6-11. Structure of EEPROM Interface

6.20.2.1 EEPROM Memory Organization

6.20.2.1.1 EEPROM Cache

The EEPROM Cache serves as temporary storage of data being transferred to/from a selected EEPROM bank. Data transferred to the EEPROM cache from either a digital interface or from the M8051 is byte addressable and one byte at time can be written to or read from. The only exception being a special OWI burst write/read access in which 8 bytes of data can be accessed at a time. Selection of the EEPROM Cache interface is determined by the IF_SEL bit in the EEPROM Access Control register.

Data transferred to the Cache from an EEPROM bank is loaded 128-bits at a time during the EEPROM Cache load cycle. EEPROM Bank selection is determined by the value placed in the BANK_SEL bits in the EEPROM Access Control Register. When programming an EEPROM bank, the EEPROM Cache holds the programming data for the amount of time necessary to complete the EEPROM programming process.

6.20.2.1.2 Bank 0

Bank 0 is used for storage of customer data and is the only bank which can be programmed by both the 8051W and the Digital Interface. 16 bytes of EEPROM data are provided in bank 0. No CRC validation against a pre-stored CRC value occurs when Bank 0 is programmed, and thus, there are no dedicated EEPROM Cells used for CRC storage.

Due to limited number of erase/write cycles, the user has to keep track of the number of writes to EEPROM Bank 0 and store the value inside the bank because it is the only bank that is accessable when the write is occuring.

6.20.2.1.3 Banks 1-4

Banks 1–4 are used for storage of customer data. Each bank 1 through 4 provides 128-bits of data storage for a total of 512 bits (64 bytes) of storage data. Since the 8051W does not have access to these banks, only the digital interfaces can program them. Each time one of these banks is programmed a CRC is calculated based upon the data held in the EEPROM Cache during program. This calculated CRC value is stored internally and validated after bank programming is complete.

6.20.2.1.4 Bank 5

The firse 64-bits (8 bytes) of Bank 5 are provided to the customer for calibration value and/or general storage. Byte 9 is used for the storage of the cummulative CRC values for banks 1-4 and the first half of Bank 5. When programming Bank 5 it is required to place the cumulative CRC value for banks 1–5 in the EEPROM Cache Address 0x558. This CRC value covers all data in banks 1 through 4 and the first 64-bits of data in bank 5. Everytime programming of Bank 5 is completed the CRC value is validated. The remaining 7 bytes of Bank 5 (0x559 - 0x55F) are not used.

6.20.3 RAM Memory

This memory space is used for 8051W scratchpad memory, such as intermediate calculation results. It is a 256 byte memory space, and located at memory page 1.

6.20.4 SFR/ESFR Memory

The 8051W uses two types of memory storage, Special Function Registers (SFR) and External Special Function Registers (ESFR). The SFR registers are used for 8051W internal operations, and cannot be accessed external to the 8051W. The ESFR register exists on the same address space as the SFR, however these registers can be accessed via the digital interface. The ESFR registers are used for calibration, configuration, fault reporting and memory storage. The SFR/ESFR total memory space is 256 bytes, and they are located at memory page 2.

6.20.5 Test Register Memory

The test register memory space is used for diagnostic configuration, and testing for sensor calibration. The test registers are located at memory page 0, and can only be accessed by the Digital Interface.

6.21 General Purpose Input Output (GPIO) Pins

The GPIO_x pins have multiple functions, including general purpose inputs/outputs (GPIO), input capture, output compare or I2C. In the GPIO mode, the GPIO_x pins are connected directly to 8051W port pins. The state of the pins can then be controlled through software by setting the appropriate I/O port SFRs in the 8051W. Table 6-5 shows the mapping of the GPIO_x pins to specific 8051W ports.

6.21.1 Setting the GPIO Functions

Table 6-5. GPIO_x Pin Functionality

PIN	8051W PORT	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
GPIO_1/IC_1/SDA	2.0	Input Capture 1	I2C Data
	Default	Set IC1_ACT to 1 in IC_OC_GPIO	Set DI_CTRL[1:0] = 0b01 in DI_CTRL
GPIO_2/IC_2	2.1	Input Capture 2	-
	Default	Set IC2_ACT to 1 in IC_OC_GPIO	

Table 6-5. GPIO_x Pin Functionality (continued)

PIN	8051W PORT	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
GPIO_3/OC_1/SCL	2.2	Output Compare 1	I2C Clock
	Default	Set OC1_ACT to 1 in IC_OC_GPIO	Set DI_CTRL[1:0] = 0b01 in DI_CTRL
GPIO_4/OC_2	2.3	Output Compare 2	
	Default	Set OC2_ACT to 1 in IC_OC_GPIO	
GPIO_5	3.2	-	-
	Default		

After power up or reset, the default configuration for all of these pins is the input GPIO function. To change the function of a pin a write command to the appropriate ESFR will automatically reconfigure it. Table 6-5 shows the appropiate bits in each ESFR that need to be set to enable different functions for each GPIO pin.

As Table 6-5 shows, some GPIOx pins can be configured for multiple alternate functionalities and therefore the device implements a priority level for each GPIO configuration. The priority level is as follows:

1. I^2C
2. Input Capture / Output Compare
3. General Purpose I/Os

This means that if the IC1_ACT bit is set to 1 (enabling Input Capture 1 functionality on GPIO_1 pin) and the DI_CTRL[1:0] bits are set to 0x01 (enabling I2C functionality on GPIO_1) then the GPIO_1 pin is configured as I2C pin.

6.21.2 GPIO Buffers

The device includes five general purpose digital input/output buffers, one for each of the GPIO_x pin. The buffers can be configured to operate as standard 8051W I/O buffers or other alternate functions such as I2C and input capture/output compare. The direction of the buffers are controlled digitally depending on the mode of the GPIO_x pin.

The device also offers a strong drive mode which allows the user to override the digital control signals generated by the 8051W GPIO interface. This mode is set for a given IO buffer via the GPIO Strong Output Drive Mode ESFR. When a '1' is written to the ST_GPOx bit, a switch at the output of the Output buffer is always closed, providing a means to strongly pull up or down the voltage on the GPIO_x pin regardless of whether output data is low or high. It is important to note that the *GPIO Strong Output Drive Mode* ESFR can be set independent of the function assigned to the GPIO buffers. Strong drive mode should be disabled if the buffer should operate as an input or in I2C mode.

6.22 8051W UART

The TxD and RxD pins are connected to the 8051W UART. These pins can either be used for software debugging or for implementing application-specific protocols. Both the TxD and RxD pins have their respective unidirectional buffers.

6.23 DAC Output

The device includes two 12-bit digital to analog converters that produce a ratiometric output voltage with respect to the VDD supply. The digital input comes from the DAC 1 or DAC 2 registers, where the 4 MSBs reside in a separate address from the 8 LSBs. **In order to update the analog outputs on the VOUTx pins in a coherent manner, the software must update the MSBs first, followed by the LSBs.**

NOTE

Changes in the VDD voltage result in a proportional change in the output voltage because the current reference for the DAC is derived from VDD.

6.24 Input Capture and Output Compare

The device has two Input Capture and two Output Compare ports. Table 6-5 shows the GPIO pins of the device that can be used for Input Capture and Output Compare ports. The capture and compare functionality uses a 16-bit Free Running Timer for the events.

6.24.1 Free Running Timer

The Free Running Timer is a 16-bit timer that is different from the 8051W native timers. The resolution of the Free Running Timer can be set to either 1µs/bit or 0.5µs/bit using 10_20_MHZ bit in Input Capture/Output Compare Control Register (IC_OC_CTRL) in the ESFR memory spacer.

The current value of the Free Running Timer can be accessed using the Free Running Timer Shadow Registers (FRTMSB & FRTLSB). This register in only updated upon request, it is not continuously updated. When the IC_OC_TIM_LAT bit in the Input Capture/Output Compare Control Register (IC_OC_CTRL) is set to logic 1, the current value of the Free Running Timer is written to the Free Running Timer Shadow registers.

6.24.2 Input Capture

The device has 2 Input Capture ports. The Input Capture functionality can be enabled when the pin is configured to be a GPIO by setting ICx_ACT (x = 1,2) bits in the Input Capture/Output Compare GPIO Register (IC_OC_GPIO) in the ESFR memory space. When the user sets the corresponding bit to logic high, the GPIO pin is configured for Input Capture functionality automatically.

The Input Capture port can be configured to either capture the Free Running Timer value on a rising edge or falling edge using the ICx_EDGE bits in the Input Capture/Output Compare Control Register (IC_OC_CTRL) in the ESFR memory space. Both IC_1 and IC_2 each have unique 16-bit timer capture registers associated with them called Input Capture 1 Register and Input Capture 2 Register respectively. When the corresponding rising or falling edge occurs the Input Capture peripheral transfers the value of the Free Running Timer into the corresponding capture register and generates an interrupt to the 8051W.

6.24.3 Output Compare

The device has 2 Output Compare ports. The Output Compare functionality can be enabled when the pin is configured to be a GPIO by setting OCx_ACT (x = 1,2) bits in the Input Capture/Output Compare GPIO Register (IC_OC_GPIO) in the ESFR memory space.

The Output Compare port can be configured to either (1) Set the pin to High level when the match occurs or (2) Set the pin to Low level when the match occurs. The user can configure the desired state of the OC_1 and OC_2 pins at match using OC1_LVL and OC2_LVL bits in the Input Capture/Output Compare Control Register (IC_OC_CTRL) .

Each Output Compare port has a unique 16-bit timer compare register associated with it. When the value programmed in the compare register matches the value of the Free Running Timer, the Output Compare peripheral changes the state of the corresponding pin to the configured value and generates a unique interrupt to the 8051W. This occurs every time the value in the Compare register matches the value of the Free Running Timer.

NOTE

For correct function of the output compare it is recommended that the MSB be updated first and then the LSB.

6.25 Diagnostics

This section describes the diagnostics.

6.25.1 Power Supply Diagnostics

The device includes modules to monitor the power supply for faults. The internal power rails that are monitored are AVDD, DVDD, VBRG, and EEPROM charge pump. Please refer to the electrical specifications for the thresholds.

When a fault is detected, an appropriate bit in the PSMON1 and PSMON2 registers is set. If the faulty condition is removed, the fault bits will remain latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.

6.25.2 Resistive Bridge Sensor Connectivity Diagnostics

The device includes modules to monitor for sensor faults. Specifically, the device monitors the sensor pins for opens (including loss of connection from the sensor), short-to-ground, and short to sensor supply.

When a fault is detected, an appropriate bit in the AFEDIAG register is set. All three types of sensor faults will result in the setting of the same bit, meaning it is not possible to distinguish the type of fault that has occured. Even after the faulty condition is removed, the fault bits remains latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.

Open Sensor Faults are detected through the use of an internal pull-down resistor. The value of the resistor can be configured using DIS_R1M and DIS_R2M bits in Decimator and Low Power Control Register (DECCTRL) in the ESFR memory space. This configurability allows the detection of open sensor faults for various Stage 1 Gain settings. For more information on programming this device please refer to the*PGA400-Q1 Programming Application Note* (SLDA015).

6.25.3 AFE Diagnostics

The device includes modules that verify that the input signal of each stage is within a certain range. This ensures that every stage of the signal chain is working normally. Overvoltage and undervoltage range flags are implemented in four locations along the signal chain (Sensor Input, Stage 1 Gain output, Stage 2 Gain output, and ADC Buffer output). When a fault is detected, the corresponding bit is set in the AFEDIAG registers. It is noted both overvoltage and undervoltage conditions set a common bit; i.e., it is not possible to distinguish between overvoltage and undervoltage.

The AFE Diagnostics also includes the monitoring of the frequency of the Self-Oscillating Demodulator circuit used for capacitive sensor interface. If the frequency is less than 40KHz (typical) or more than 1MHz (typical), a fault flag is set in the AFEDIAG register. The monitoring of this frequency can be enabled or disabled using the CTOV_CLK_MON_EN bit in the ENABLE CONTROL register. Both over-frequency and under-frequency conditions set same bit which means it is not possible to distinguish which type of fault occured that resulting in the flag.

The typical threshold values for these faults are in boxes in Figure 6-12.

When a fault is detected, an appropriate bit in the AFEDIAG register is set. All sensor faults will result in the setting of the same bit, meaning there is no way to distinguish the type of fault. Even after the faulty condition is removed, the fault bits will remain latched. To remove the fault the 8051W software should read the fault bit and write a logic zero back to the bit. In addition a system reset will clear the fault.

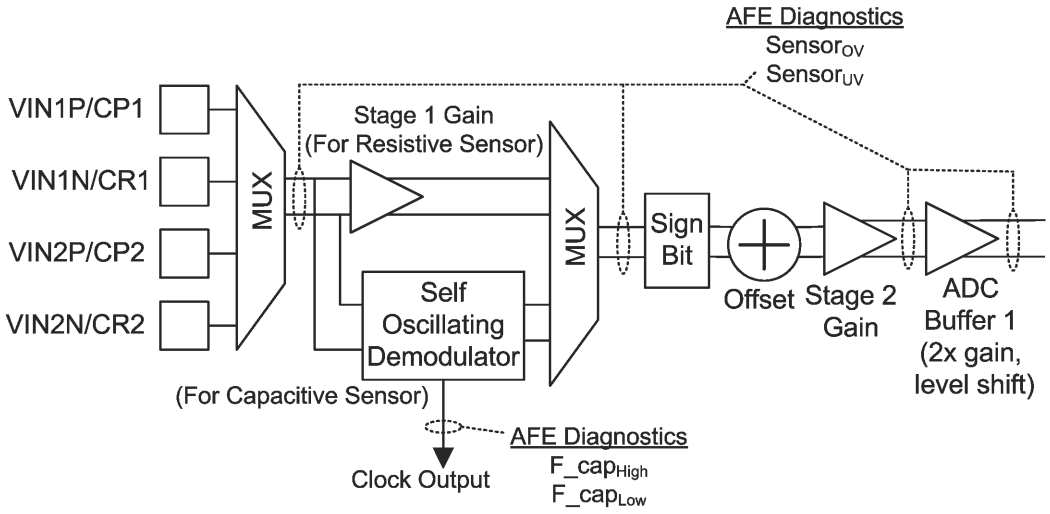


Figure 6-12. Block Diagram of AFE Diagnostics

6.25.4 *Internal Capacitors for Capacitive Sensor Diagnostics*

The device includes Cp and Cr Test capacitors that can be connected to the capacitive AFE via software control. This allows the software to check the integrity of the capacitive signal chain in the IC.

Figure Figure 6-13 shows the block diagram with the Cp and Cr Test capacitors. The Cp Test capacitor is 10pF and Cr Test capacitor is 8pF.

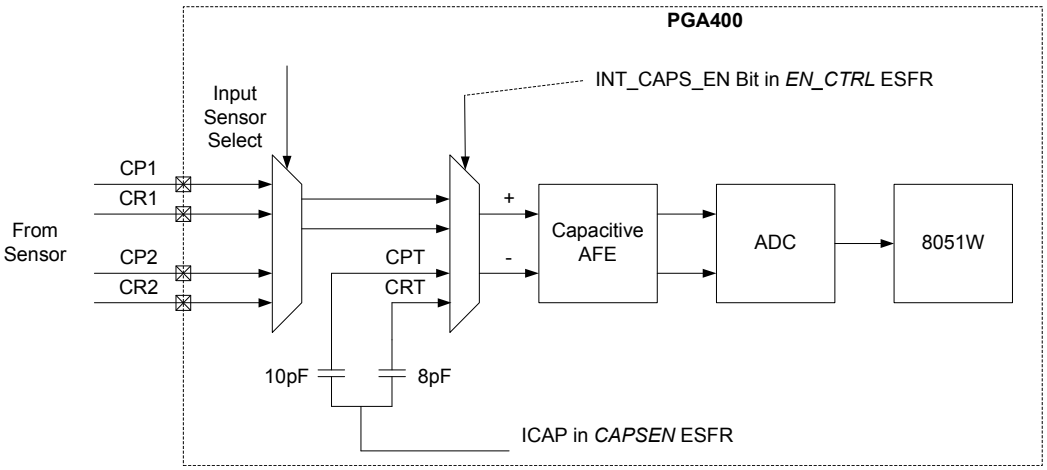


Figure 6-13. Internal Capacitors for Capacitive Sensor Diagnostics.

6.25.5 *DAC Diagnostics*

The device implements a “Loop Back” feature to check the integrity of the two DAC outputs. Figure Figure 6-14 shows the block diagram representation of the Loop Back feature. This figure shows that DAC1 output is connected to positive side of the differential input while DAC2 is connected to negative side of the differential input.

The DAC outputs are voltage divided by a nominal factor of 6/11 before being connected to the AFE inputs.

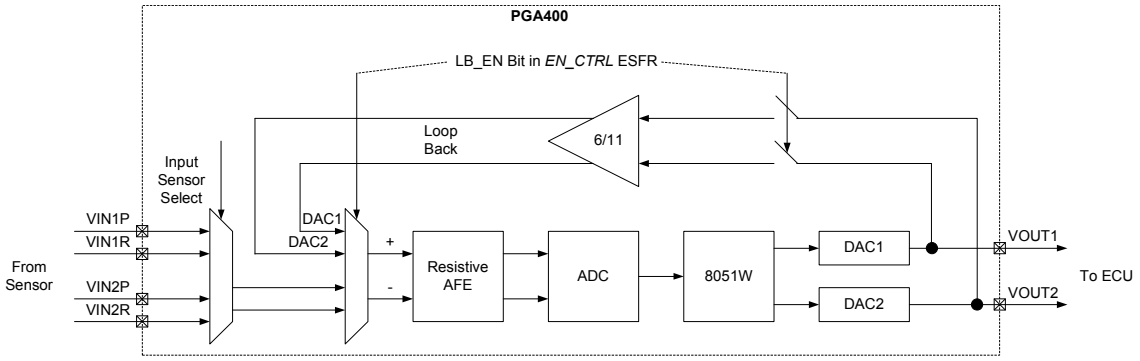


Figure 6-14. DAC Loop Back.

DAC loop back is enabled by setting LB_EN bit in EN_CTRL to 1. In this mode, Sensor 1 Channel gain and offset settings are used. Note that ADC output represents the voltage difference between DAC1 and DAC2 outputs scaled by the voltage divider and the AFE gains/offsets.

Note that when LB_EN is set to 1, the AFE is switched to resistive mode, even if SEN_TYP bit is set to Capacitive mode.

The DAC outputs continue to be available on VOUT1 and VOUT2 pins in the Loop Back mode.

6.25.6 EEPROM CRC and TRIM Error

The 9th Byte in Bank 5 of the EEPROM stores the CRC for all the data in EEPROM Banks 1 through 5.

The user can verify the EEPROM CRC at any time by loading Banks 1 through 5 in sequence into the EEPROM Cache. When Bank 5 is loaded into the Cache, the device automatically calculates the CRC and updates the CRC_ERR bit in EE_STATUS ESFR.

The device also has analog trim values. The validity of the analog trim values is checked on power up and before the 8051W reset is de-asserted. The validity of the trim values can be inferred using the TRIM_ERR bit in EE_STATUS ESFR.

Note that Banks 0 can be updated by software in the field, but the user has to maintain CRC (or checksum) for this bank using software.

6.25.7 RAM MBIST

The device implements RAM MBIST (Memory Built-In Self-Test). This diagnostic checks the integrity of the internal RAM on an on-demand basis.

The procedure to start this diagnostic and check for status is as below:

- 1. Set EN_IRAM_MBIST to 1 in EN_CTRL2 register. This starts the RAM MBIST.
- 2. Wait for IRAM_MBIST_DONE in RAM_MBIST_ST to be set to 1 by the RAM MBIST algorithm
- 3. Check IRAM_MBIST_FAIL bit in RAM_MBIST_ST register after IRAM_MBIST_DONE flag is set to 1. If IRAM_MIBIST_FAIL is 1, then RAM MBIST failed, indicating faulty RAM. If IRAM_MBIST_FAIL is 0, then RAM has no faults.

The RAM MBIST can be run only once every power cycle.

NOTE

While the RAM MBIST is running, the 8051W should not access the RAM.

6.25.8 Main Oscillator Watchdog

There is watch dog monitor for the main oscillator clock whether using the internal 40MHz oscillator or the external crystal input. When the frequency is outside the range of 35-45MHz the entire device is reset. The main oscillator watchdog can be disabled using MAIN_OSC_WD_EN bit in the ENABLE CONTROL register.

6.25.9 Software Watchdog

The device also implements a software watchdog. This watchdog has to be serviced by software every 500ms. If the software does not service the watchdog within 500ms of the last service, then the 8051W core is reset. The software services the watchdog by toggling the state of an internal pin between the two blocks. The state of this pin cannot be read back to the 8051W. If this function is not desired the software watchdog can be disabled using CPU_WD_EN bit in the ENABLE CONTROL register.

When the software watchdog times out and resets the 8051W, DAC1 and DAC2 registers are reset to 0, which causes VOUT1 and VOUT2 to be driven to 0V. The remaining ESFRs retains the settings from prior to the reset events. This implies that CPU_WD_EN also remains set.

6.26 Low Power Mode

The device has multiple low power modes. In each mode, certain functional blocks can be turned on or off through the use of different ESFRs. Table 6-6 lists which bits in each ESFR that disables certain blocks of the device.

Table 6-6. Low Power Control

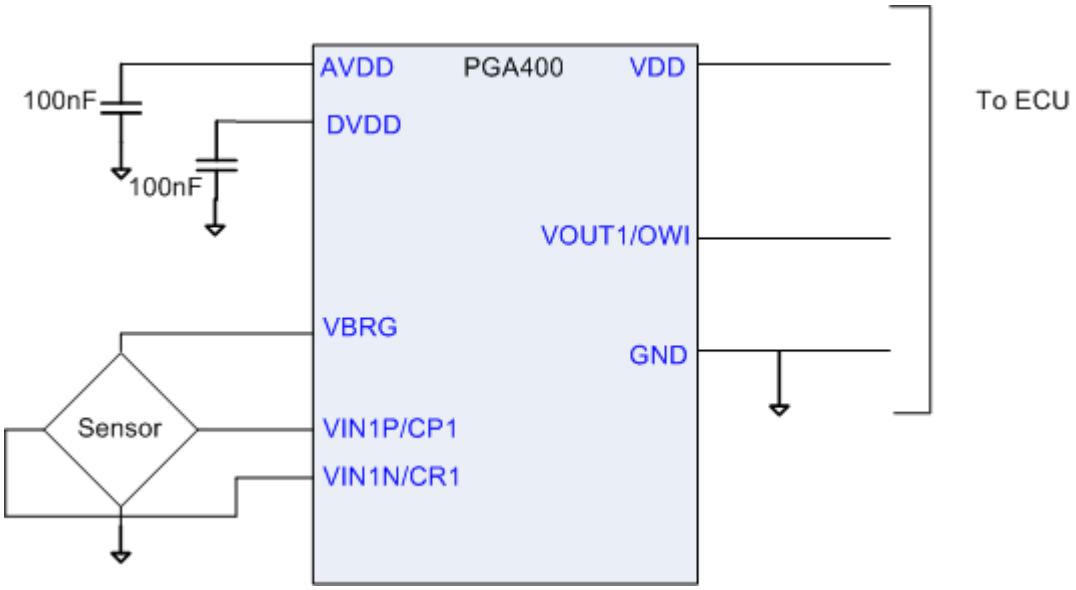
CONTROL BIT	ESFR	CONTROL ACTION
VBRG_EN	SENCTRL	Enables/Disables VBRG supply
DAC2_EN	DECCTRL	Enables/Disables DAC2
AFE_EN	DECCTRL	Enables/Disable AFE
EN_DI_IF_CLK	EN_CTRL2	Enable/Disable Digital Interface
EN_EEPROM_CTRL_CLK	EN_CTRL2	Enable/Disable EEPROM clock

The following blocks does not enter low power mode at any time:

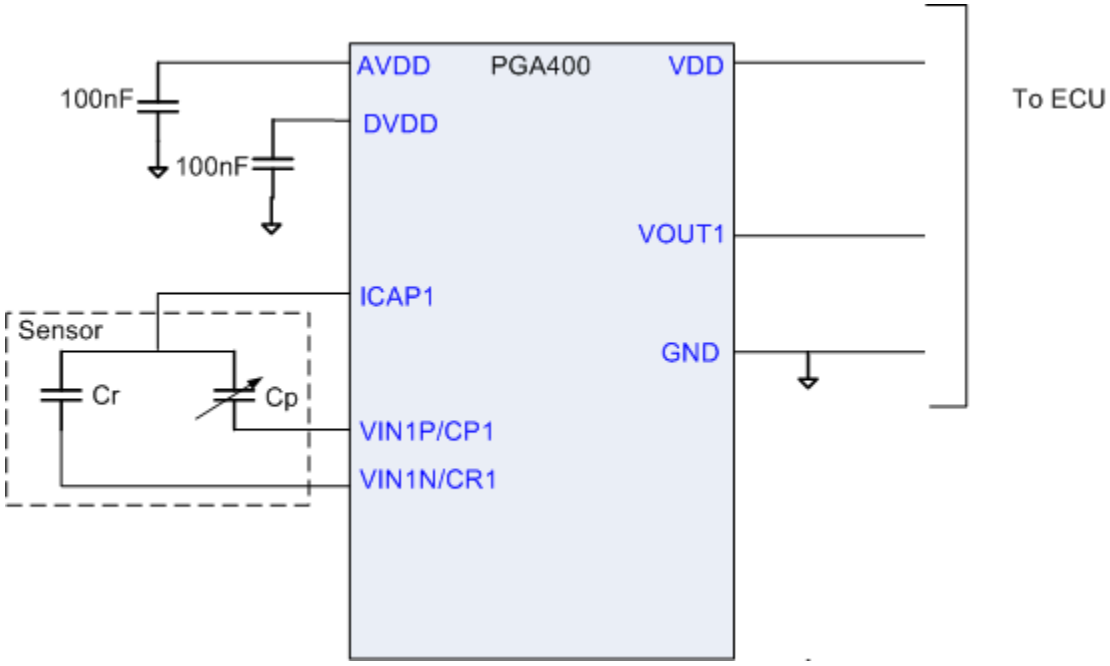
- Microprocessor – the microprocessor continues to operate at the same frequency
- OTP/EEPROM – The memory is kept alive and runs at the same speed VOUT1/OWI

7 Application Schematic

7.1 Resistive Bridge Interface



7.2 Capacitive Sensor Interface



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PGA400QYZSRQ1	ACTIVE	DSBGA	YZS	36	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	PGA400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

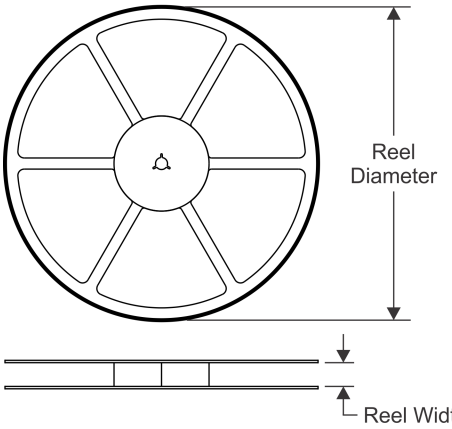
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

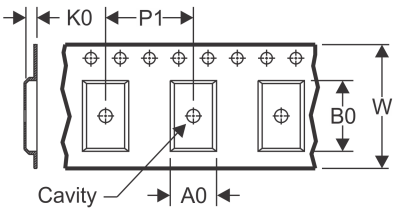
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

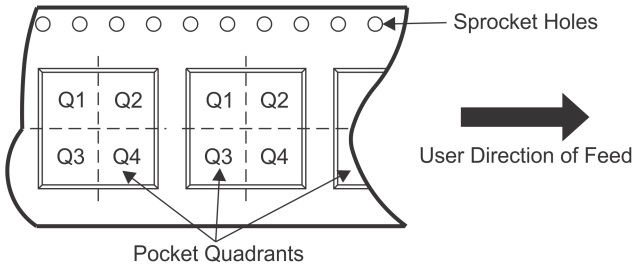


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

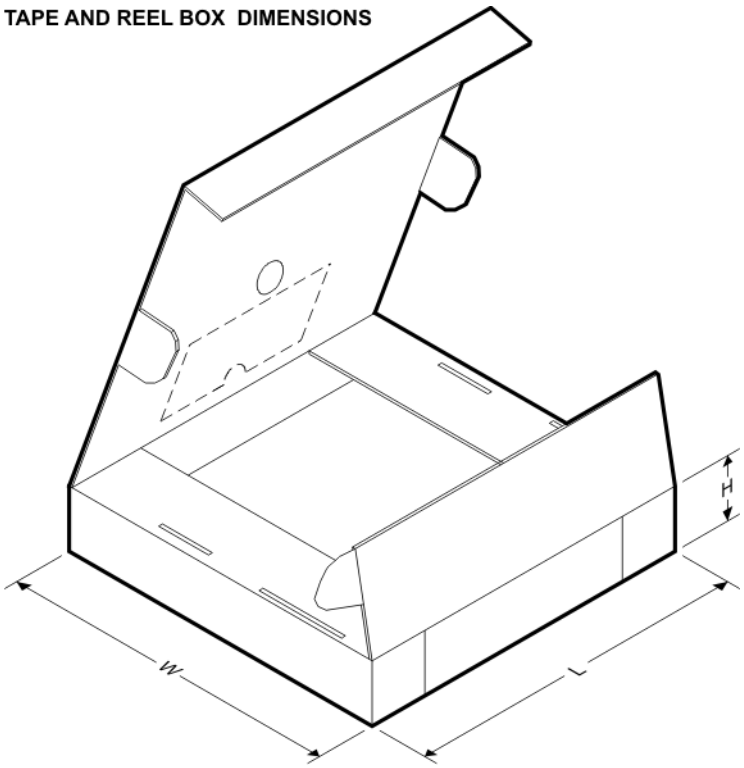
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA400QYZSRQ1	DSBGA	YZS	36	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

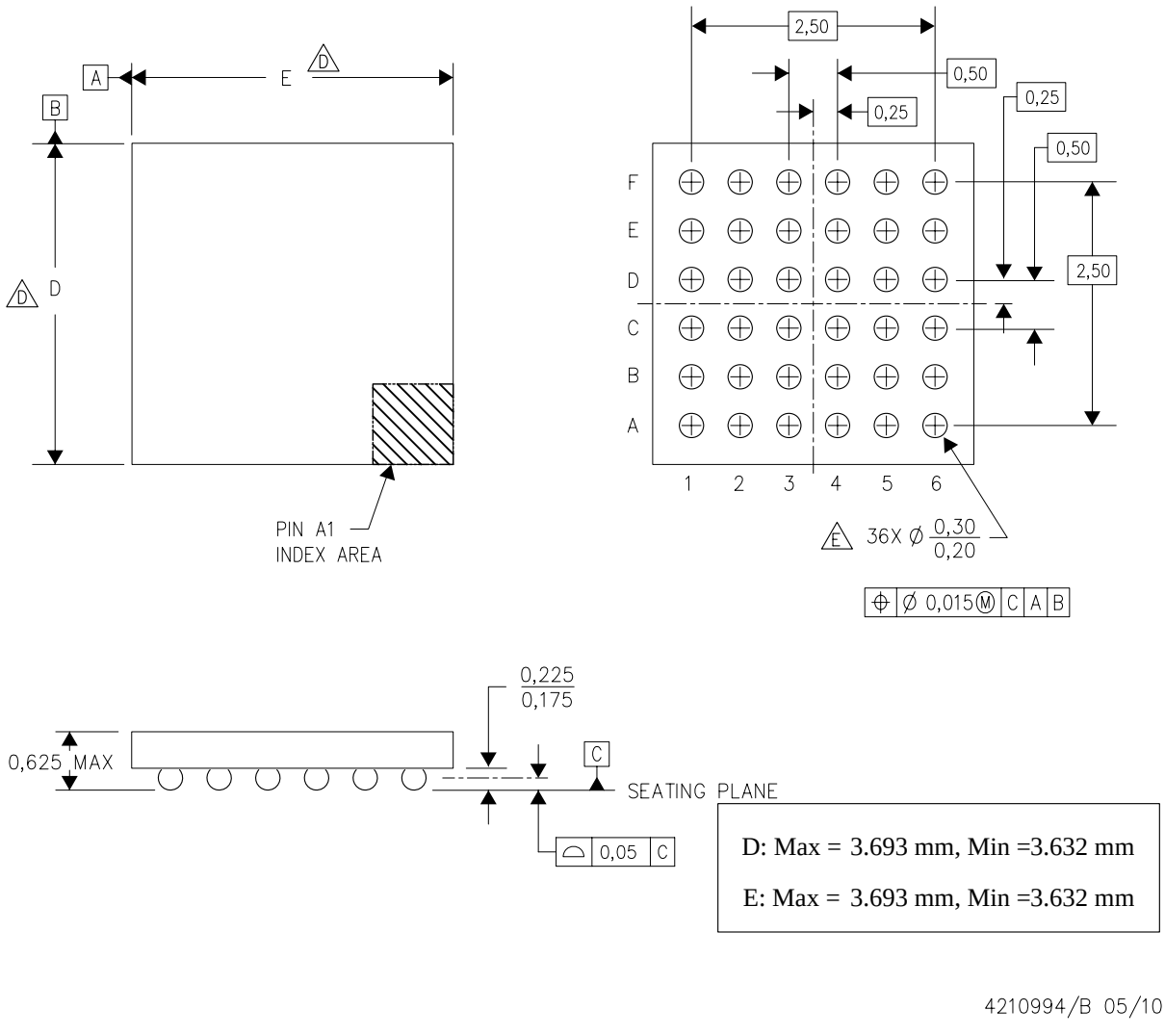
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA400QYZSRQ1	DSBGA	YZS	36	1500	210.0	185.0	35.0

YZS (S–XBGA–N36) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZS package can have dimension D ranging from 2.94 to 3.90 mm and dimension E ranging from 2.94 to 3.90 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 6 x 6 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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