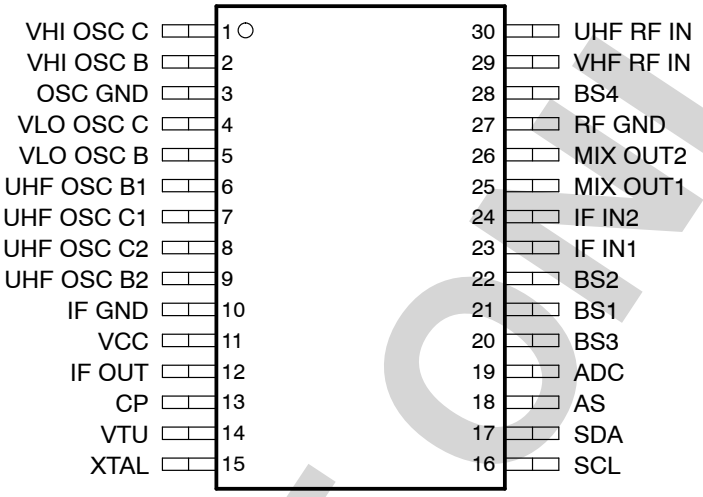
- **Single Chip Mixer/Oscillator and Synthesizer**
- **3-Band Local Oscillator**
- **I²C Bus Protocol**
- **Bidirectional Data Transmission**
- **30-V Tuning Voltage Output**
- **4-Channel NPN-Type Bandswitch Drivers**
- **Programmable Reference Divider Ratio (512, 640, or 1024)**
- **5-V Power Supply**
- **30-Pin TSSOP Package**

DBT PACKAGE
(TOP VIEW)



description

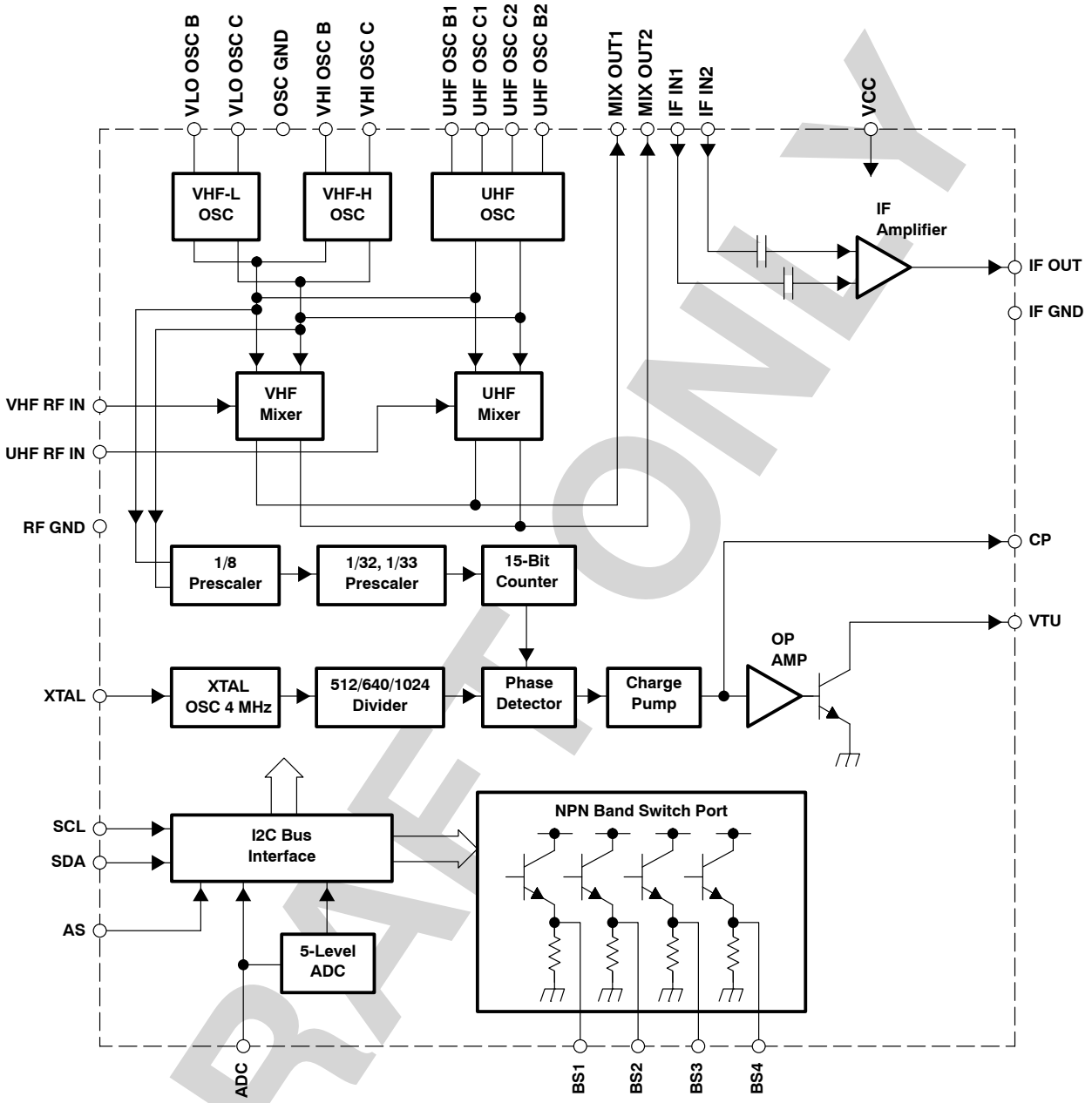
The SN761678 is a single-chip, synthesized tuner IC designed for TV/VCR tuning systems. The circuit consists of a PLL synthesizer, 3-band local oscillators and mixer, 30-V output tuning amplifier, four NPN band switch drivers, and is available in a small package outline. Fifteen-bit programmable counter and reference divider is controlled by I²C bus protocol. Tuning step frequency is selectable by this reference divider ratio for a 4-MHz XTAL oscillator.

NOTE: The products, their specifications, service and other information appearing in this publication are subjected to change by Texas Instruments without notice.

This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

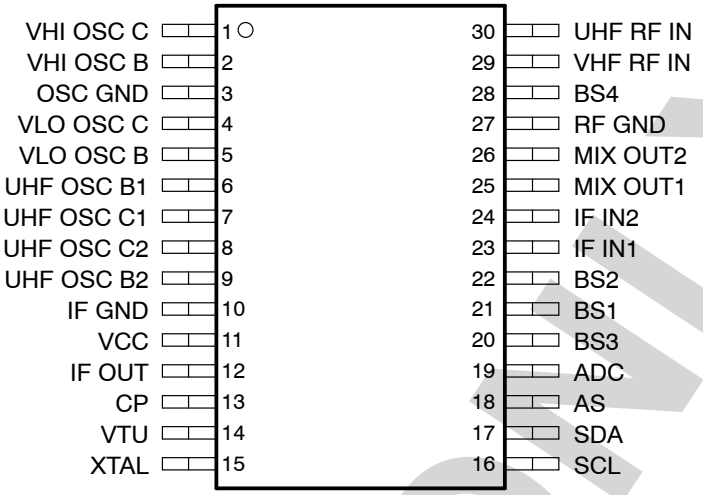
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



pin assignments

DBT PACKAGE
(TOP VIEW)



Terminal Functions

Table 1 provides a cross-reference between the terminal number and the signal name.

Table 1. Signal Names Sorted by DBT Terminal Number

TERMINAL		DESCRIPTION	SCHEMATIC
NUMBER	SIGNAL NAME		
1	VHI OSC C	VHF HIGH oscillator collector	See Figure 1
2	VHI OSC B	VHF HIGH oscillator base	See Figure 1
3	OSC GND	OSC ground	
4	VLO OSC C	VHF LOW oscillator collector	See Figure 2
5	VLO OSC B	VHF LOW oscillator base	See Figure 2
6	UHF OSC B1	UHF oscillator base 1	See Figure 3
7	UHF OSC C1	UHF oscillator collector 1	See Figure 3
8	UHF OSC C2	UHF oscillator collector 2	See Figure 3
9	UHF OSC B2	UHF oscillator base 2	See Figure 3
10	IF GND	IF ground	
11	VCC	Supply voltage for mixer/oscillator/PLL: 5 V	
12	IF OUT	IF output	See Figure 4
13	CP	Charge pump output	See Figure 5
14	VTU	Tuning voltage amplifier output	See Figure 5
15	XTAL	4-MHz crystal oscillator input	See Figure 6
16	SCL	Serial data input/output	See Figure 7
17	SDA	Serial clock input	See Figure 7
18	AS	Address selection input	See Figure 7
19	ADC	ADC input	See Figure 7
20	BS3 (FMST)	Bandswitch 1 output/FM (NPN emitter follower)	See Figure 8
21	BS1 (VHFL)	Bandswitch 2 output/VHF-LOW (NPN emitter follower)	See Figure 8
22	BS2 (VHFH)	Bandswitch 3 output/VHF-HIGH (NPN emitter follower)	See Figure 8
23	IF IN1	IF amplifier input	See Figure 9
24	IF IN2	IF amplifier input	See Figure 9
25	MIX OUT1	Mixer output	See Figure 10
26	MIX OUT2	Mixer output	See Figure 10
27	RF GND	RF ground	
28	BS4 (UHF)	Bandswitch 4 output/UHF (NPN emitter follower)	See Figure 8
29	VHF RF IN	VHF RF input	See Figure 11
30	UHF RF IN	UHF RF input	See Figure 12

Terminal Functions (continued)

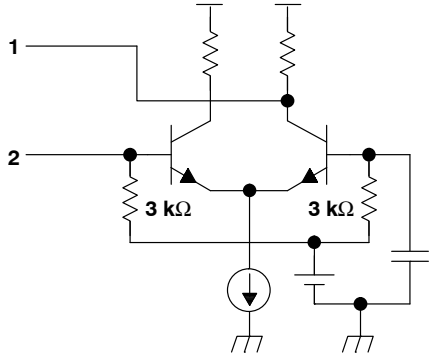


Figure 1

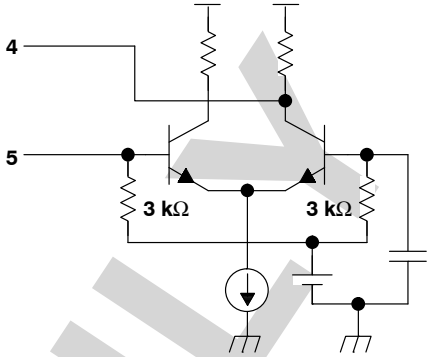


Figure 2

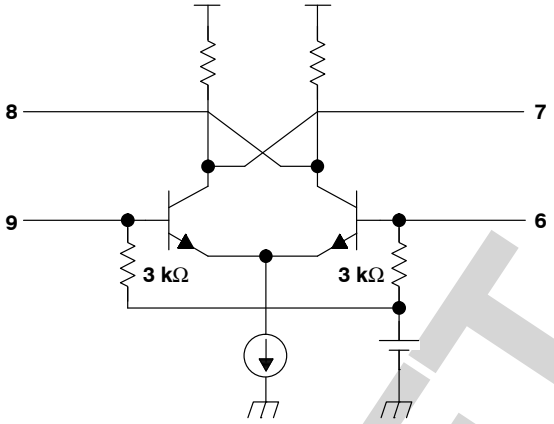


Figure 3

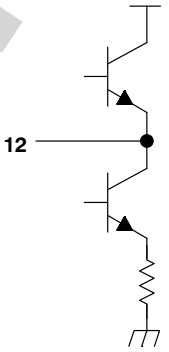


Figure 4

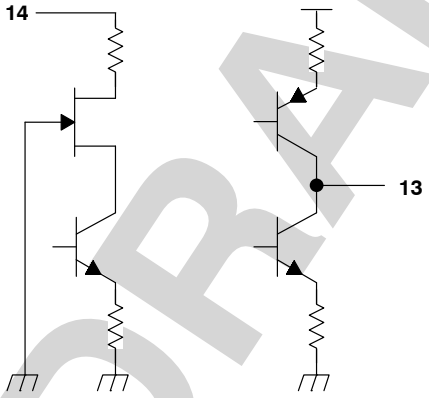


Figure 5

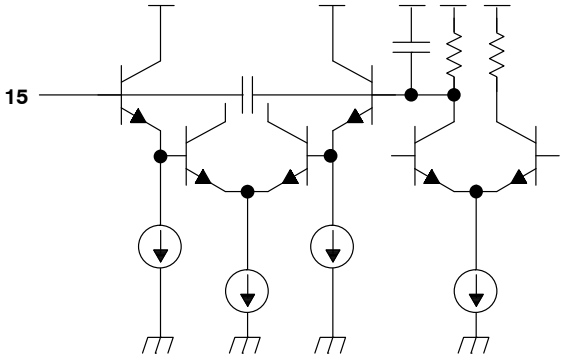


Figure 6

Terminal Functions (continued)

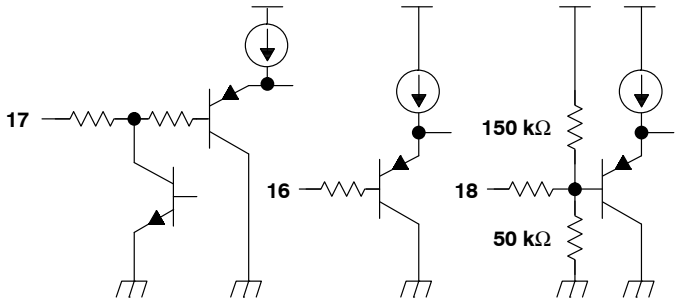


Figure 7

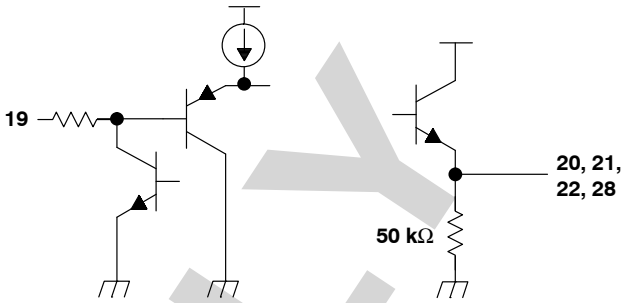


Figure 8

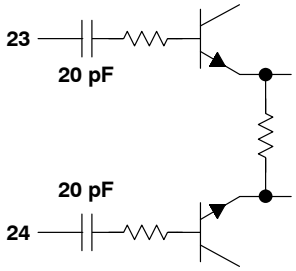


Figure 9

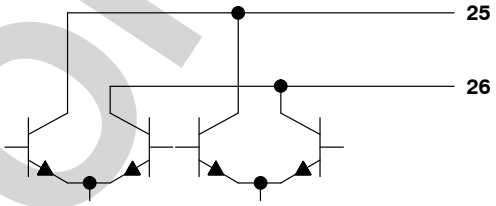


Figure 10

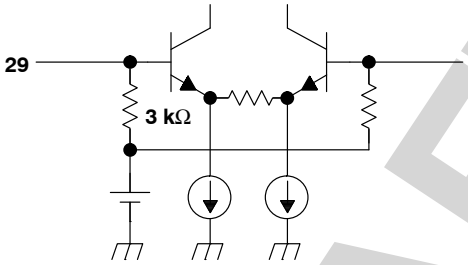


Figure 11

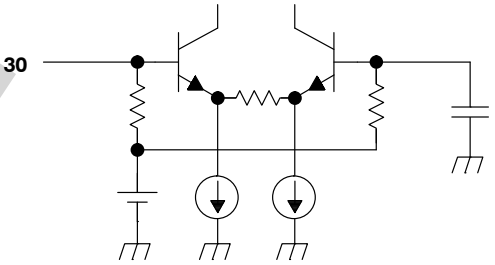


Figure 12

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (terminal 11) (Note 1) . . . . . –0.4 V to 6.5 V
Input voltage 1, V_{GND} (terminals 3 and 27) (Note 1) . . . . . –0.4 V to 0.4 V
Input voltage 2, V_{VTU} (terminal 14) (Note 1) . . . . . –0.4 V to 35 V
Input voltage 3, V_{IN} (terminals 1, 2, 4–9, 12, 13, 15–26, 28–30) (Note 1) . . . . . –0.4 V to 6.5 V
Continuous total power dissipation, $T_A \leq 25°C$, P_D (Note 2) . . . . . 1071 mW
Operating free-air temperature, T_{OPE} . . . . . –20 to 85°C
Storage temperature range, T_{STG} . . . . . –65 to 150°C
Maximum junction temperature, T_{JC} . . . . . 150°C
Maximum lead temperature (1.6 mm (1/16 inch) from case for 10 seconds) . . . . . 260°C
Maximum short circuit time, $t_{SC(max)}$
(All terminals to V_{CC}. All terminals to IFGND, OSCGND, RFGND except for terminal 26) . . . . . 10 s

† Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the IF GND of the circuit.
2. Derating factor is 8.57 mW/°C for $T_A \leq 25°C$.

recommended operating conditions

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{TU}	Tuning supply voltage			30	33	V
I_{BS}	Output current of bandswitch	One port On			10	mA
T_{OPE}	Operating free-air temperature		–20		85	°C

CAUTION: It is advised that precautions be taken to avoid damage due to high static voltages or electrostatic fields in handling this device.

electrical characteristics

total device and serial interface

V_{CC} = 4.5 to 5.5 V, T_{OPE} = –20 to 85°C, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Icc1	Supply current 1			60		mA
Icc2	Supply current 2	One band switch On (I_{BS} = 10 mA)		70		mA
V_{IH}	High level input voltage (SCL, SDA)		2.8		Vcc	V
V_{IL}	Low level input voltage (SCL, SDA)				1.4	V
I_{IH}	High level input current (SCL, SDA)				10	µA
I_{IL}	Low level input current (SCL, SDA)		–10			µA
V_{POR}	Power on reset supply voltage	Threshold of supply voltage between reset and operation mode	2.1	2.8	3.5	V
I2C interface						
V_{ASH}	Address select high input voltage (AS)	V_{CC} = 5 V	4.5		5.0	V
V_{ASM1}	Address select mid1 input voltage (AS)	V_{CC} = 5 V	2.0		3.0	V
V_{ASM2}	Address select mid2 input voltage (AS)	V_{CC} = 5 V	1.0		1.5	V
V_{ASL}	Address select low input voltage (AS)	V_{CC} = 5 V			0.5	V
I_{ASH}	Address select high input current (AS)				120	µA
I_{ASL}	Address select low input current (AS)		–10			µA
V_{ADC}	ADC input voltage	See Table 9	0		V_{CC}	V
I_{ADH}	ADC high level input current	V_{ADC} = V_{CC}			10	µA
I_{ADL}	ADC low level input current	V_{ADC} = 0 V	–10			µA
F_{SCL}	Clock frequency (SCL)			100	400	kHz
V_{OL}	Low level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High level output leakage current (SDA)	V_{SDA} = 5.5 V			10	µA
$t_{HLD-DAT}$	Data hold time	See timing chart, Figure 1	0			µs
t_{BUF}	Bus free time		1.3			µs
t_{HD-STA}	Start hold time		0.6			µs
t_{LOW}	SCL low hold time		1.3			µs
t_{HIGH}	SCL high hold time		0.6			µs
t_{SU-STA}	Start setup time		0.6			µs
t_{SU-DAT}	Data setup time		0.1			µs
t_R	SCL, SDA rise time				0.3	µs
t_F	SCL, SDA fall time				0.3	µs
t_{ST-STO}	Stop setup time		0.6			µs

electrical characteristics (continued)

PLL and bandswitch

V_{CC} = 4.5 to 5.5 V, T_{OPE} = −20 to 85°C, unless otherwise noted

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	256		32767	
F_{XTAL}	Crystal oscillator	R_{XTAL} = 25 Ω to 300 Ω	3.2	4	4.48	MHz
Z_{XTAL}	Crystal oscillator input impedance			1.6		kΩ
V_{IXTAL2}	Minimum reference input sensitivity (XTAL)	4 MHz, ac coupling with 0.1 µF			100	mVp-p
V_{VTUL}	Tuning amplifier low level output voltage	R_L = 27 kΩ, V_{TU} = 33 V	0.2	0.3	0.46	V
I_{VTUOFF}	Tuning amplifier leakage current (off)	OS = 1, V_{TU} = 33 V			10	µA
I_{CPH}	Charge pump high level input current	CP = 1		280		µA
I_{CPL}	Charge pump low level input current	CP = 0		60		µA
V_{CP}	Charge pump output voltage	In-lock		1.95		V
I_{CPOFF}	Charge pump leakage current	T2 = 0, T1 = 1, V_{CP} = 2 V, T_A = 25°C	−15		+15	nA
I_{BS}	Band switch driver output current				10	mA
V_{SBS1}	Band switch driver output voltage	I_{BS} = 10 mA	3.0			V
V_{SBS2}		I_{BS} = 10 mA, Vcc = 5 V, T_A = 25°C	3.5	3.9		V
I_{BSOFF}	Band switch driver leakage current	V_{BS} = 0 V			3	µA

electrical characteristics (continued)

mixer, oscillator, IF amplifier

V_{CC} = 5 V, T_A = 25°C, measured in reference measurement circuit at 50-Ω system, IF filter characteristics: f_{PEAK} = 43 MHz; unless otherwise noted

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
G_{c1} G_{c3}	Conversion gain (mixer to IF amplifier) VHF-low	F_{in} = 58 MHz (Note 3) F_{in} = 130 MHz	22 22	25 25	28 28	dB
G_{c4} G_{c6}	Conversion gain (mixer to IF amplifier) VHF-high	F_{in} = 136 MHz (Note 3) F_{in} = 364 MHz	22 22	25 25	28 28	dB
G_{c7} G_{c9}	Conversion gain (mixer to IF amplifier) VHF-UHF	F_{in} = 370 MHz (Note 3) F_{in} = 804 MHz	26 25	29 28	32 31	dB
NF_1 NF_3	Noise figure VHF-low	F_{in} = 55.25 MHz F_{in} = 127.25 MHz		(9.5) (9.5)		dB
NF_4 NF_6	Noise figure VHF-high	F_{in} = 133.25 MHz F_{in} = 361.25 MHz		(10) (10)		dB
NF_7 NF_9	Noise figure UHF	F_{in} = 367.25 MHz F_{in} = 801.25 MHz		(11) (11)		dB
CM_1 CM_3	1% cross modulation distortion VHF-low	F_{in} = 55.25 MHz (Note 4) F_{in} = 127.25 MHz		(89) (89)		dBμV
CM_4 CM_6	1% cross modulation distortion VHF-high	F_{in} = 133.25 MHz (Note 4) F_{in} = 361.25 MHz		(86) (86)		dBμV
CM_7 CM_9	1% cross modulation distortion UHF	F_{in} = 367.25 MHz (Note 4) F_{in} = 801.25 MHz		(87) (87)		dBμV
V_{IFO1} V_{IFO3}	IF output voltage VHF-low	F_{in} = 55.25 MHz (Note 5) F_{in} = 127.25 MHz		117 117		dBμV
V_{IFO4} V_{IFO6}	IF output voltage VHF-high	F_{in} = 133.25 MHz (Note 5) F_{in} = 361.25 MHz		117 117		dBμV
V_{IFO7} V_{IFO9}	IF output voltage UHF	F_{in} = 367.25 MHz (Note 5) F_{in} = 801.25 MHz		117 117		dBμV
Φ_{OSC1} Φ_{OSC3}	Phase noise VHF-low	F_{in} = 55.25 MHz (Note 6) F_{in} = 127.25 MHz		88 88		dBc/Hz
Φ_{OSC4} Φ_{OSC6}	Phase noise VHF-high	F_{in} = 133.25 MHz (Note 6) F_{in} = 361.25 MHz		86 86		dBc/Hz
Φ_{OSC7} Φ_{OSC9}	Phase noise UHF	F_{in} = 367.25 MHz (Note 6) F_{in} = 801.25 MHz		84 84		dBc/Hz
	Prescaler beat (Note 7)				(25)	dBμV

NOTES: 3. IF = 43 MHz, RF input level = 80 dBμV
4. $F_{undes} = F_{des} \pm 6$ MHz, Pin = 80 dBμV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
5. IF = 45.75 MHz
6. Offset = 10 kHz, RF input level = 70 dBμV
7. Design parameter, not tested.

PRINCIPLES OF OPERATION

I²C bus mode

(1) I²C write mode (R/W = 0)

Table 2. Write Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Bandswitch byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

A: Acknowledge

Table 3. Description of Data Symbols

SYMBOL	DESCRIPTION	DEFAULT
MA1, MA0	Address set bits (see Table 4)	
N14...N0	Programmable counter set bits N = N14*2^14 + N13*2^13 + ... + N1*2 + N0 Oscillation frequency = fr x 8 x N fr = reference frequency = 4 MHz / Reference divider	Nn = 0
CP	Charge pump current set bit 60 µA (CP = 0) 280 µA (CP = 1)	CP = 1
T2, T1, T0	Test bits (see Table 5) Normal mode: T2 = 0, T1 = 0, T0 = 1/0	T2 = 0, T1 = 0, T0 = 1
RSA, RSB	Reference divider ratio selection bits (see table 6 reference divider ratio)	RSA = 0, RSB = 1
OS	Tuning amplifier control bit Tuning voltage on (OS = 0) Tuning voltage off, high impedance (OS = 1)	OS = 0
BS4...BS1	Band switch ports control bits BSn = 0: OFF, BSn = 1: ON Band selection by BS1, 2, 4 (x: don't care) VHF-LO: BS1 (VL) = 1, BS2 (VH) = 0, BS4 (U) = 0 VHF-HI: BS1 (VL) = x, BS2 (VH) = 1, BS4 (U) = 0 UHF: BS1 (VL) = x, BS2 (VH) = x, BS4 (U) = 1	BSn = 0
X	Don't care	

Table 4. Address Selection

VOLTAGE APPLIED ON AS INPUT	MA1	MA0
Low: 0 V to 0.1 V_{CC}	0	0
MID2: Open, or, 0.2 V_{CC} to 0.3 V_{CC}	0	1
MID1: 0.4 V_{CC} to 0.6 V_{CC}	1	0
High: 0.9 V_{CC} to V_{CC}	1	1

PRINCIPLES OF OPERATION

Table 5. Test Bits (Note 8)

T2	T1	T0	FUNCTION
0	0	0	Normal operation
0	0	1	Normal operation (default)
0	1	X	Charge pump off
1	1	0	Charge pump sink
1	1	1	Charge pump source
1	0	X	Test mode (not available ADC)

NOTE 8: Not used for other bit patterns.

Table 6. Ratio Select Bits

RSA	RSB	REFERENCE DIVIDER RATIO
X	0	640
0	1	1024
1	1	512

(2) I^2C Read mode (R/W = 1)

Table 7. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W = 1	A
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	A

A: Acknowledge

Table 8. Description of Data Symbols

SYMBOL	DESCRIPTION	DEFAULT
MA1, MA0	Address set bits (see Table 4 address selection)	
POR	Power-on reset flag POR set = power on POR reset = end-of-data transmission procedure	POR = 1
FL	In-lock flag PLL lock (FL = 1) unlock (FL = 0)	
A2...A0	Digital data of ADC (see Table 9)	

Table 9. ADC Level

VOLTAGE APPLIED ON ADC INPUT	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

NOTE 9: Note 9: Accuracy is 0.03 x V_{CC}.

PRINCIPLES OF OPERATION

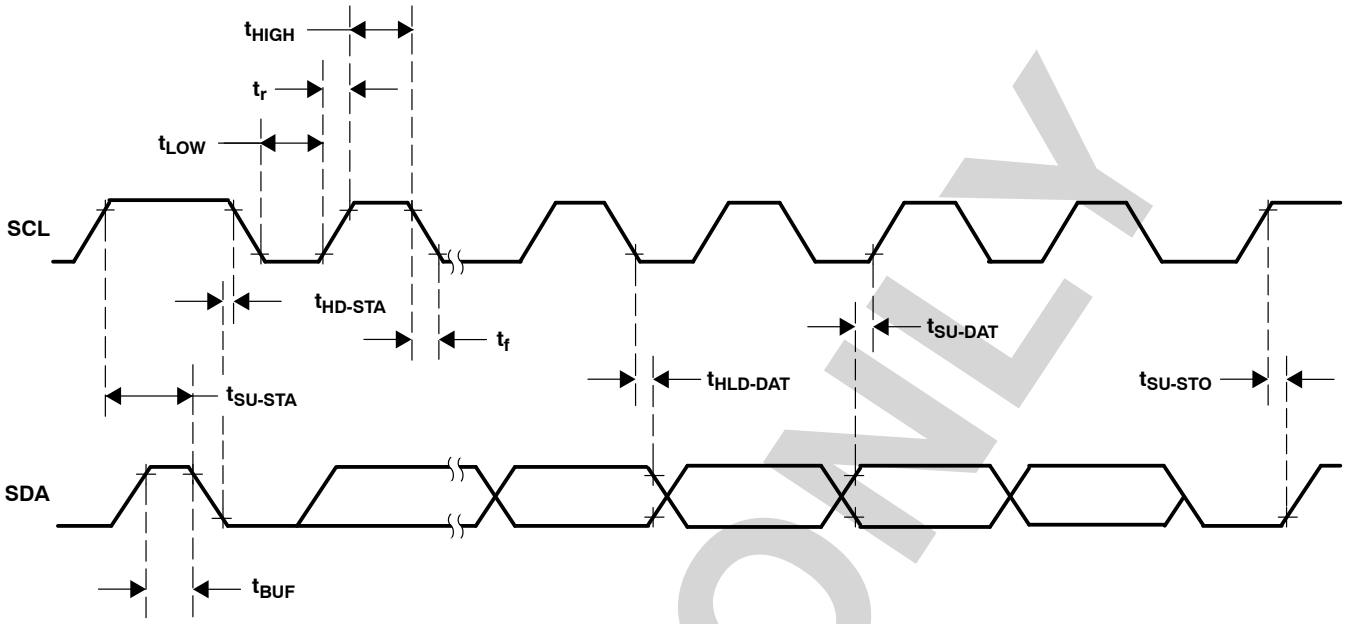


Figure 13. I²C Timing Chart

APPLICATION INFORMATION

reference measurement circuit

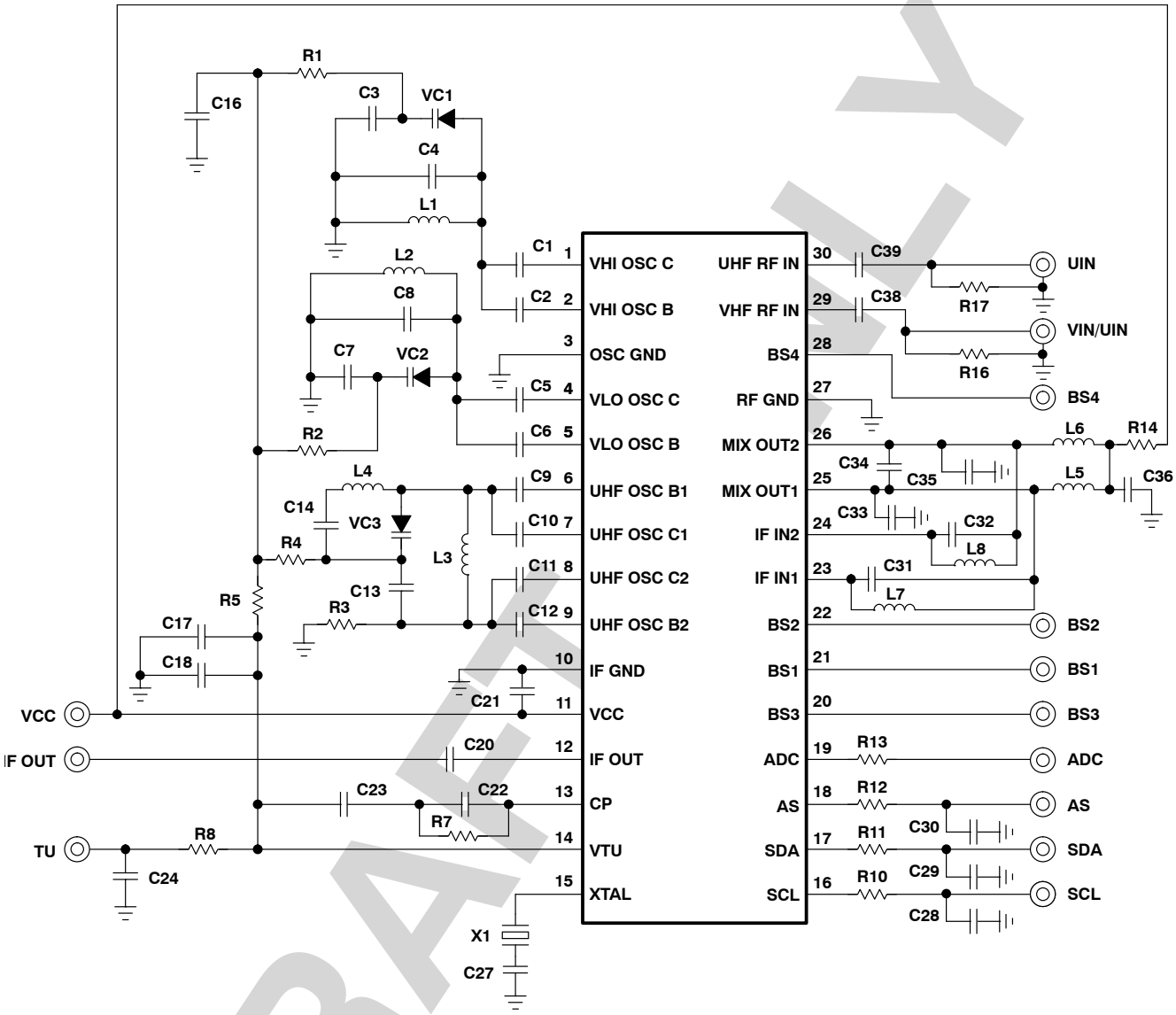


Figure 14. Reference Measurement Circuit

NOTE 10: This application information is advisory and performance check is required at actual application circuits.

TI assumes no responsibility for the consequences of use of this circuit nor for any infringement of patent or patent rights of third parties which may result from its use.

APPLICATION INFORMATION

component values for measurement circuit

PARTS NAME	VALUE	PARTS NAME	VALUE
U1	SN761678	C1	2 pF
		C2	3 pF
VC1	1T363A	C3	68 pF
VC2	1T363A	C4	open
VC3	1T363A	C5	1 pF
		C6	1 pF
L1	ϕ2.4mm 4T 0.4mm	C7	47 pF
L2	ϕ3.0mm 8T 0.32mm	C8	3 pF
L3	ϕ3.0mm 2T 0.4mm	C9	1.5 pF
L4	ϕ2.0mm 3T 0.4mm	C10	1.5 pF
L5	ϕ2.4mm 16T 0.26mm	C11	1.5 pF
L6	ϕ2.4mm 16T 0.26mm	C12	1.5 pF
L7	open	C13	12 pF
L8	open	C14	100 pF
		C15	–
X1	4 MHz	C16	2.2 nF/50 V
		C17	2.2 nF/50 V
R1	33 kΩ	C18	2.2 nF/50 V
R2	33 kΩ	C19	–
R3	22 kΩ	C20	2.2 nF
R4	33 kΩ	C21	4.7 nF
R5	22 kΩ	C22	2.2 nF
R6	–	C23	0.1 μF/50 V
R7	22 kΩ	C24	2.2 nF/50 V
R8	22 kΩ	C25	–
R9	–	C26	–
R10	330 Ω	C27	68 pF
R11	330 Ω	C28	open
R12	330 Ω	C29	open
R13	short	C30	open
R14	short	C31	short
R15	–	C32	short
R16	open	C33	open
R17	open	C34	22 pF
		C35	open
		C36	4.7 nF
		C37	–
		C38	2.2 nF
		C39	2.2 nF

APPLICATION INFORMATION

test circuit

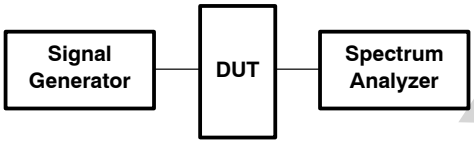


Figure 15. Measurement Circuit of Conversion Gain

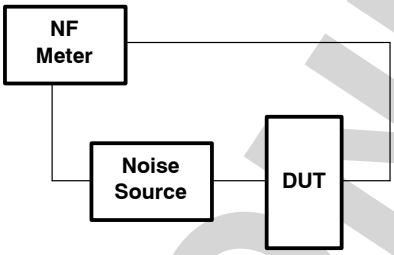


Figure 16. Noise Figure Measurement Circuit

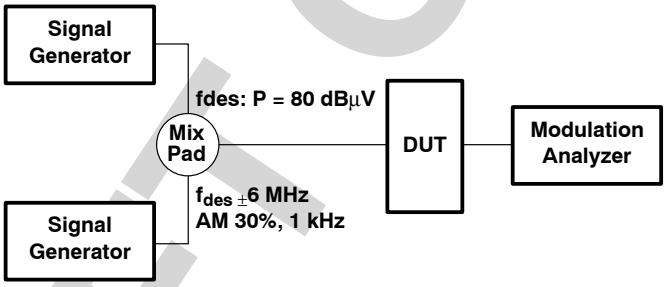
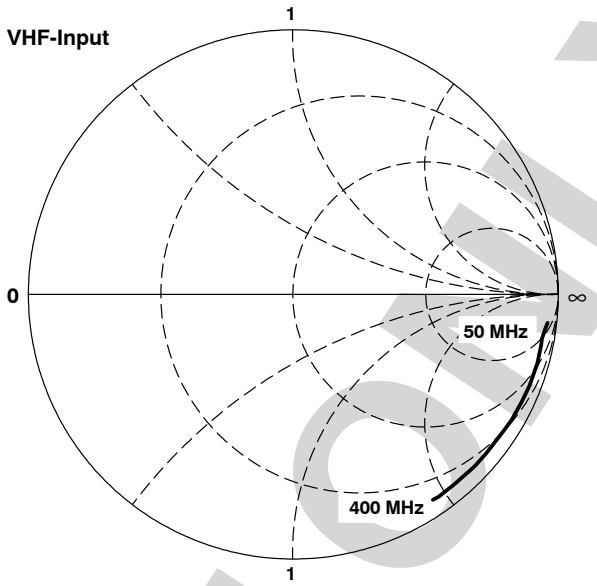


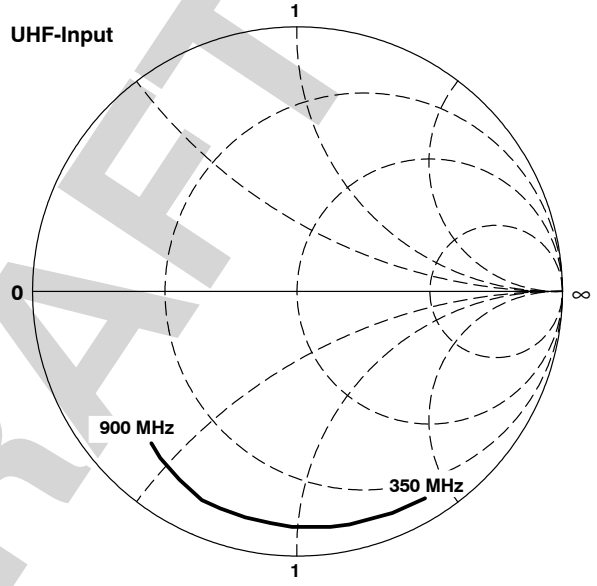
Figure 17. 1% Cross Modulation Distortion Measurement Circuit

APPLICATION INFORMATION

typical characteristics

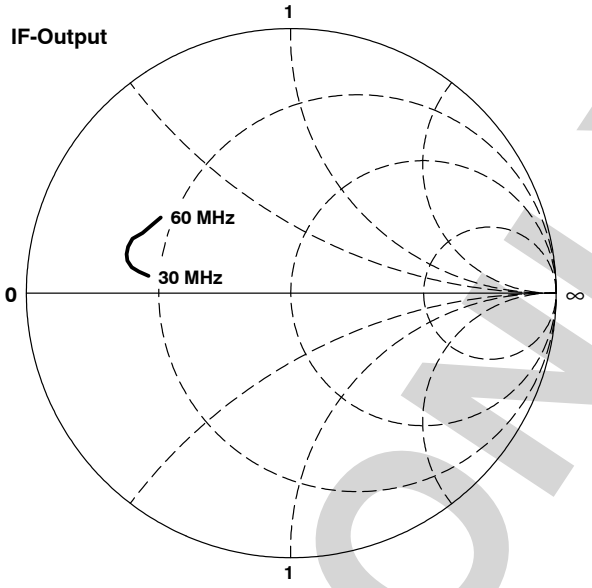
S-parameter



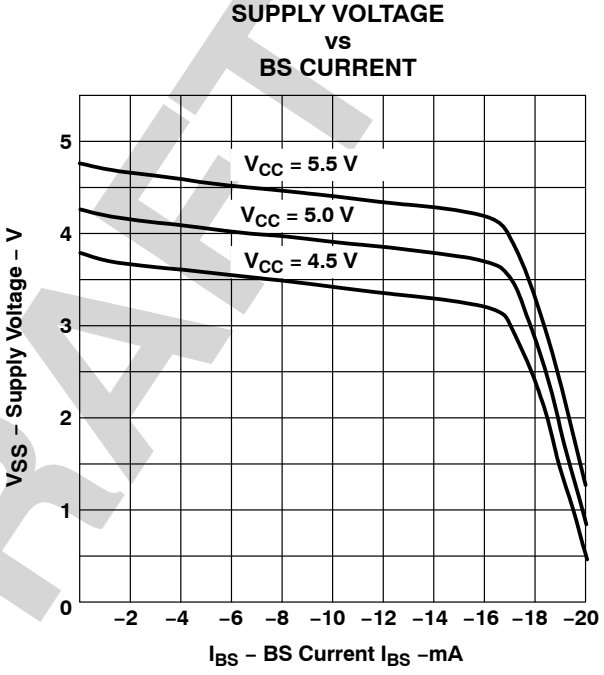


APPLICATION INFORMATION

IF-output



bandswitch driver output voltage

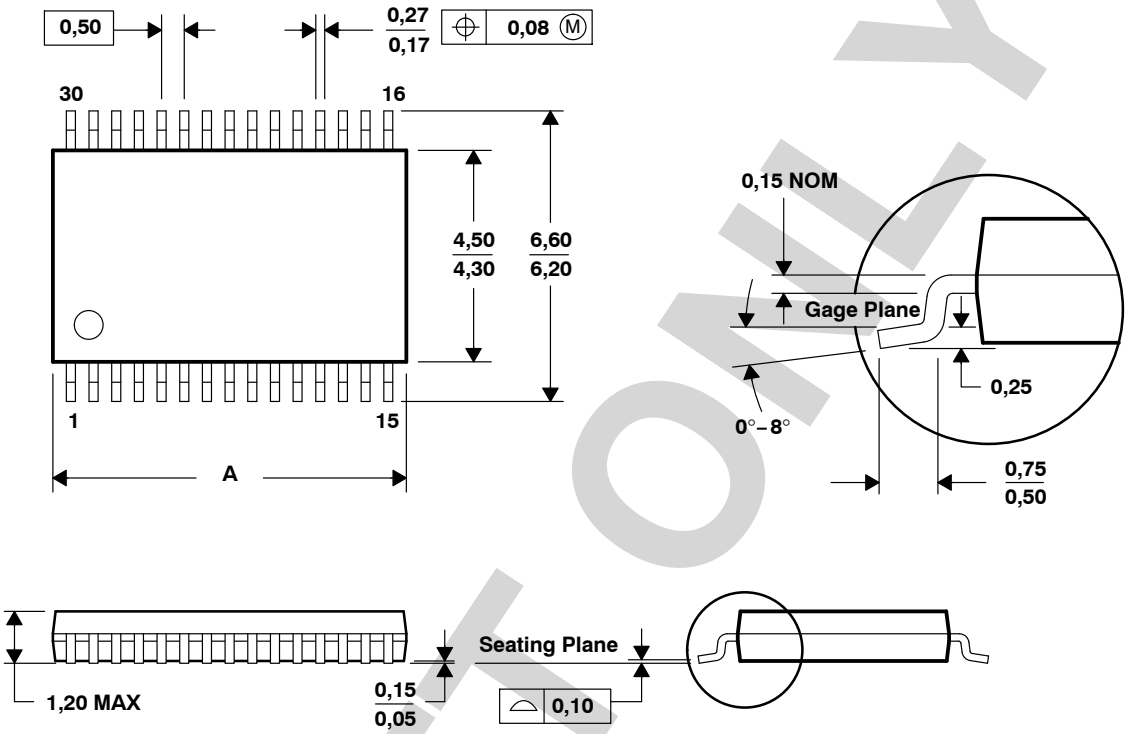


MECHANICAL DATA

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

The SN761678 tuner is encased in a thin shrink small outline package (TSSOP).

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

4073252/E 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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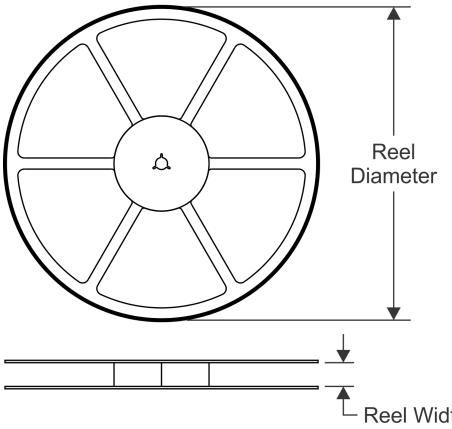
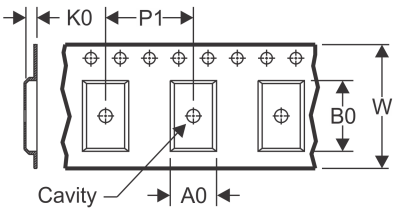
TAPE AND REEL INFORMATION

REEL DIMENSIONS

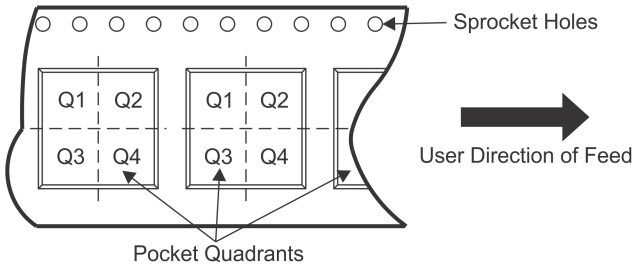


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

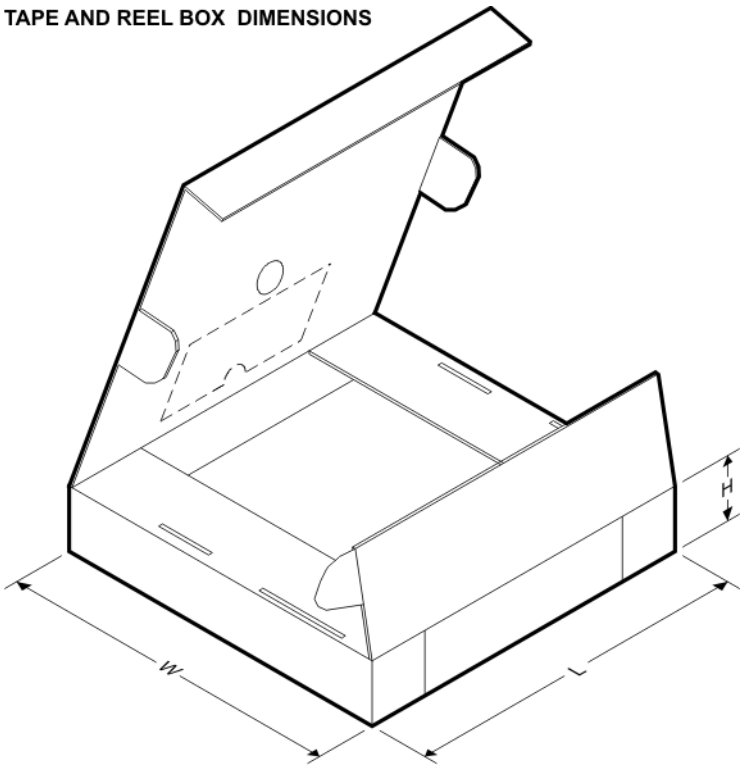
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN761678DCHR	TSSOP	DCH	30	0	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN761678DCHR	TSSOP	DCH	30	0	367.0	367.0	38.0

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