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TAS5176

SLES196 – JUNE 2007

6-Channel, 100-W, Digital-Amplifier Power Stage

FEATURES

- **Total Output Power at 10% THD+N**
  - **5 × 15 W at 8 Ω + 1 × 25 W at 4 Ω (Single-Ended)**
  - **2 x 30 W at 8 Ω (BTL)**
  - **1 x 40 W at 6 Ω (BTL)**
- **105-dB SNR (A-Weighted), with TAS5086 Modulator**
- **< 0.05% THD+N at 1 W**
- **Power Stage Efficiency > 90% Into Recommended Loads (SE)**
- **Integrated Self-Protection Circuits**
  - **Undervoltage**
  - **Overtemperature**
  - **Overload**
  - **Short Circuit**
- **Integrated Active-Bias Control to Avoid DC Pop**
- **Footprint Compatible with the TAS5186A for Scaleable Designs**
- **Thermally Enhanced 44-pin HTSSOP Package with PowerPad located on the bottom of the device**
- **EMI-Compliant When Used With Recommended System Design**

APPLICATIONS

- **DVD Receiver**
- **Home Theater in a Box**
- **Televisions**

DESCRIPTION

The TAS5176 is a high-performance, six-channel, digital-amplifier power stage with an improved protection system. The TAS5176 is capable of driving a 8-Ω, single-ended load up to 15 W per each front/satellite channel and a 4-Ω, single-ended subwoofer greater than 25 W at 10% THD+N performance.

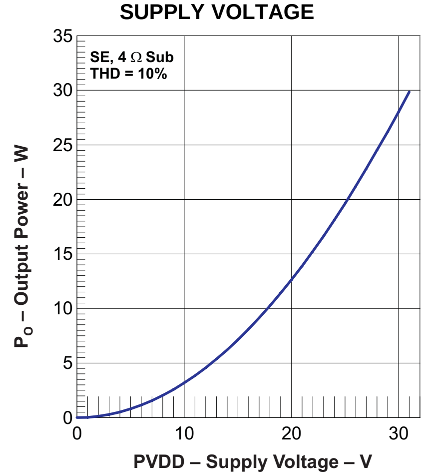
Furthermore, the TAS5176 can drive three-channels in BTL mode, with the same high-performance but with a higher power level. In BTL mode, the TAS5176 is capable of driving 8-Ω loads to greater than 30 Watts at 10% THD+N performance.

A low-cost, high-fidelity audio system can be built using a TI chipset comprising a modulator (e.g., TAS5086) and the TAS5176. This device does not require power-up sequencing because of the internal power-on reset.

The TAS5176 requires only simple passive demodulation filters on its outputs to deliver high-quality, high-efficiency audio amplification. The efficiency of the TAS5176 is greater than 90% when driving 8-Ω satellites and a 4-Ω subwoofer speaker.

The TAS5176 has an innovative protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overload protection, undervoltage protection, and overtemperature protection. The TAS5176 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level music transients. A new programmable overcurrent detector allows the use of lower-cost inductors in the demodulation output filter.

OUTPUT POWER vs SUPPLY VOLTAGE



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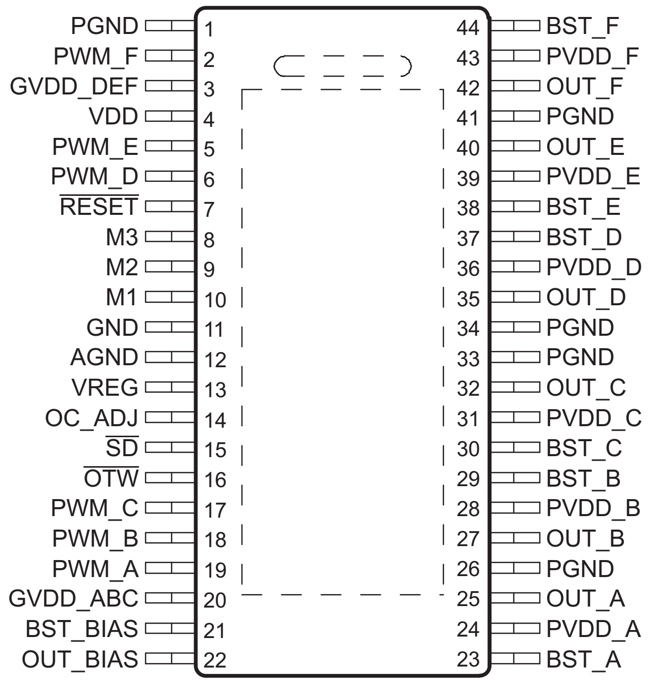
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

TERMINAL ASSIGNMENT

The TAS5176 is available in a thermally enhanced 44-pin HTSSOP PowerPAD™ package. The heat slug is located on the bottom side of the device for convenient thermal coupling to the printed circuit board which is used as the heatsink for this device.

DDW PACKAGE
(TOP VIEW)



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DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
AGND	12	P	Analog ground
BST_A	23	P	HS bootstrap supply (BST), capacitor to OUT_A required
BST_B	29	P	HS bootstrap supply (BST), external capacitor to OUT_B required
BST_BIAS	21	P	BIAS bootstrap supply, external capacitor to OUT_BIAS required
BST_C	30	P	HS bootstrap supply (BST), external capacitor to OUT_C required
BST_D	37	P	HS bootstrap supply (BST), external capacitor to OUT_D required
BST_E	38	P	HS bootstrap supply (BST), external capacitor to OUT_E required
BST_F	44	P	HS bootstrap supply (BST), external capacitor to OUT_F required
GND	11	P	Chip ground
GVDD_ABC	20	P	Gate drive voltage supply
GVDD_DEF	3	P	Gate drive voltage supply
M1	10	I	Mode selection pin
M2	9	I	Mode selection pin
M3	8	I	Mode selection pin
OC_ADJ	14	O	Overcurrent threshold programming pin, resistor to AGND required
$\overline{\text{OTW}}$	16	O	Overtemperature warning open-drain output signal, active-low
OUT_A	25	O	Output, half-bridge A, satellite
OUT_B	27	O	Output, half-bridge B, satellite
OUT_BIAS	22	O	BIAS half-bridge output pin
OUT_C	32	O	Output, half-bridge C, subwoofer
OUT_D	35	O	Output, half-bridge D, satellite
OUT_E	40	O	Output, half-bridge E, satellite
OUT_F	42	O	Output, half-bridge F, satellite
PGND	1, 26, 33, 34, 41	P	Power ground
PVDD_A	24	P	Power-supply input for half-bridge A
PVDD_B	28	P	Power-supply input for half-bridge B
PVDD_C	31	P	Power-supply input for half-bridge C
PVDD_D	36	P	Power-supply input for half-bridge D
PVDD_E	39	P	Power-supply input for half-bridge E
PVDD_F	43	P	Power-supply input for half-bridge F
PWM_A	19	I	PWM input signal for half-bridge A
PWM_B	18	I	PWM input signal for half-bridge B
PWM_C	17	I	PWM input signal for half-bridge C
PWM_D	6	I	PWM input signal for half-bridge D
PWM_E	5	I	PWM input signal for half-bridge E
PWM_F	2	I	PWM input signal for half-bridge F
$\overline{\text{RESET}}$	7	I	Reset signal (active-low logic)
$\overline{\text{SD}}$	15	O	Shutdown open-drain output signal, active-low
VDD	4	P	Power supply for digital voltage regulator
VREG	13	O	Digital regulator supply filter pin, output

(1) I = input; O = output; P = power

Table 1. MODE Selection Pins

MODE PINS[1]		MODE	
M2	M3	NAME	DESCRIPTION
0	0	2.1 mode	Channels A, B, and C enabled; channels D, E, and F disabled
0	1	5.1 mode	All channels enabled
1	0	3.0 mode	BTL Mode
1	1	Reserved	

(1) M1 must always be connected to ground. 0 indicates a pin connected to GND; 1 indicates a pin connected to VREG.

PACKAGE HEAT DISSIPATION RATINGS[1]

PARAMETER	TAS5176DDW
$R_{\theta JC}$ (°C/W)—1 satellite (sat.) FET only	10.3
$R_{\theta JC}$ (°C/W)—1 subwoofer (sub.) FET only	5.2
$R_{\theta JC}$ (°C/W)—1 sat. half-bridge	5.2
$R_{\theta JC}$ (°C/W)—1 sub. half-bridge	2.6
$R_{\theta JC}$ (°C/W)—5 sat. half-bridges + 1 sub.	1.74
Typical pad area[2]	24.72 mm^2

(1) JC is junction-to-case, CH is case-to-heatsink.
(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heatsink. The $R_{\theta CH}$ with this condition is typically 2°C/W for this package.

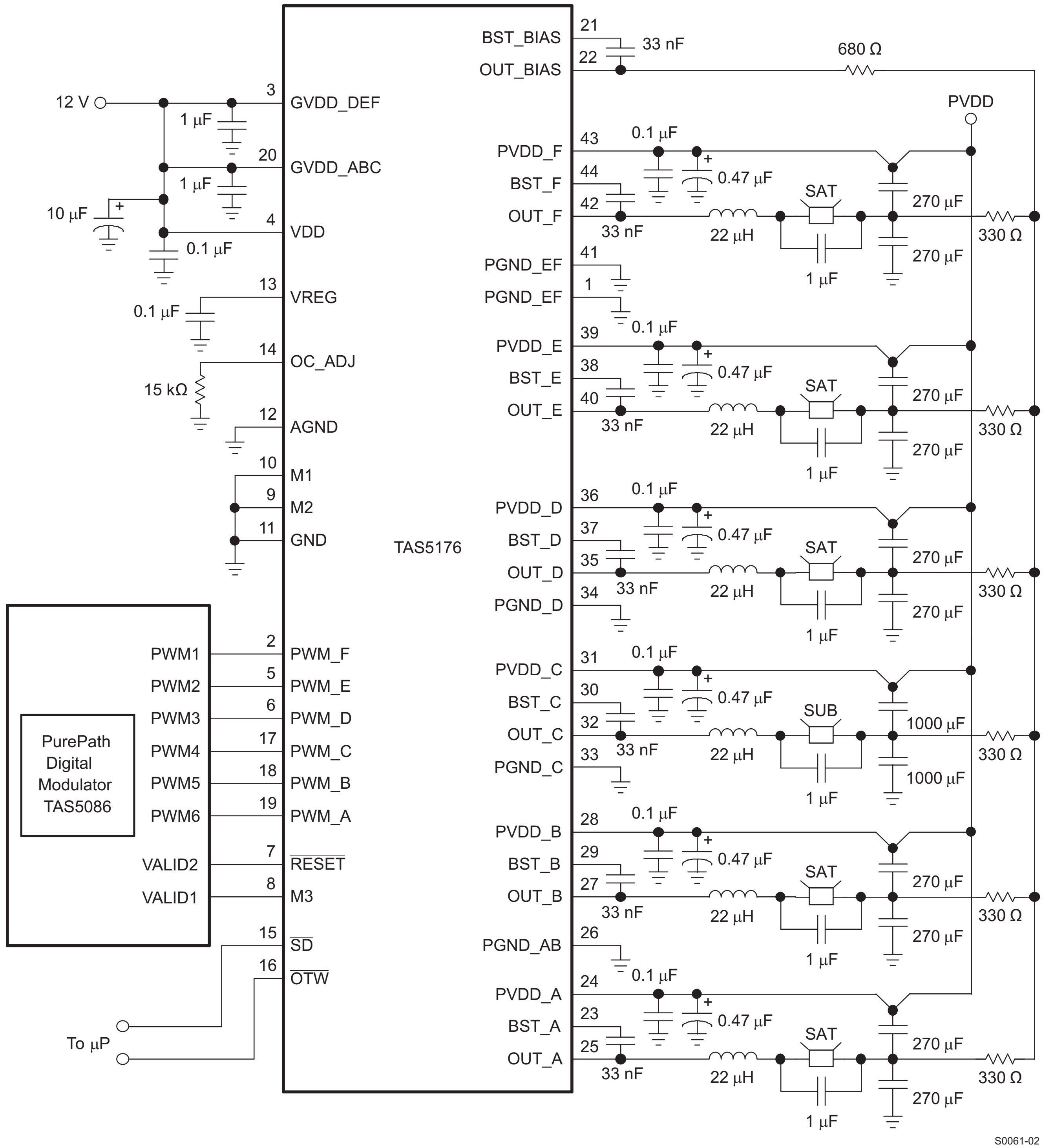
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

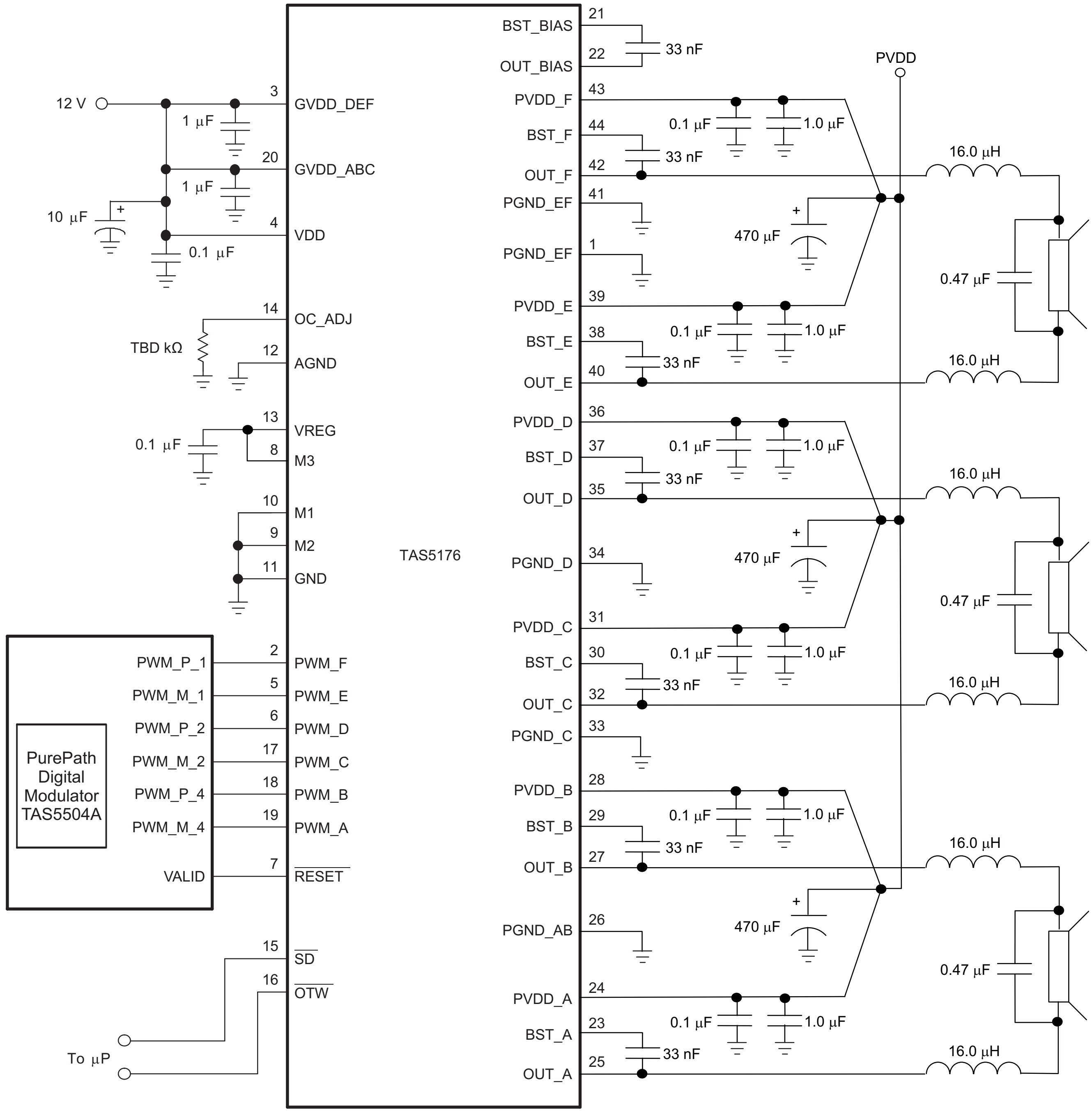
	UNITS
VDD to AGND	–0.3 V to 13.2 V
GVDD_X to AGND	–0.3 V to 13.2 V
PVDD_X to PGND_X [2]	–0.3 V to 50 V
OUT_X to PGND_X [2]	–0.3 V to 50 V
BST_X to PGND_X [2]	–0.3 V to 63.2 V
VREG to AGND	–0.3 V to 4.2 V
PGND_X to GND	–0.3 V to 0.3 V
PGND_X to AGND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7 V
Maximum operating junction temperature range (T_J)	0 to 125°C
Storage temperature	–40°C to 125°C
Lead temperature – 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Minimum PWM pulse duration, low	30 ns

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

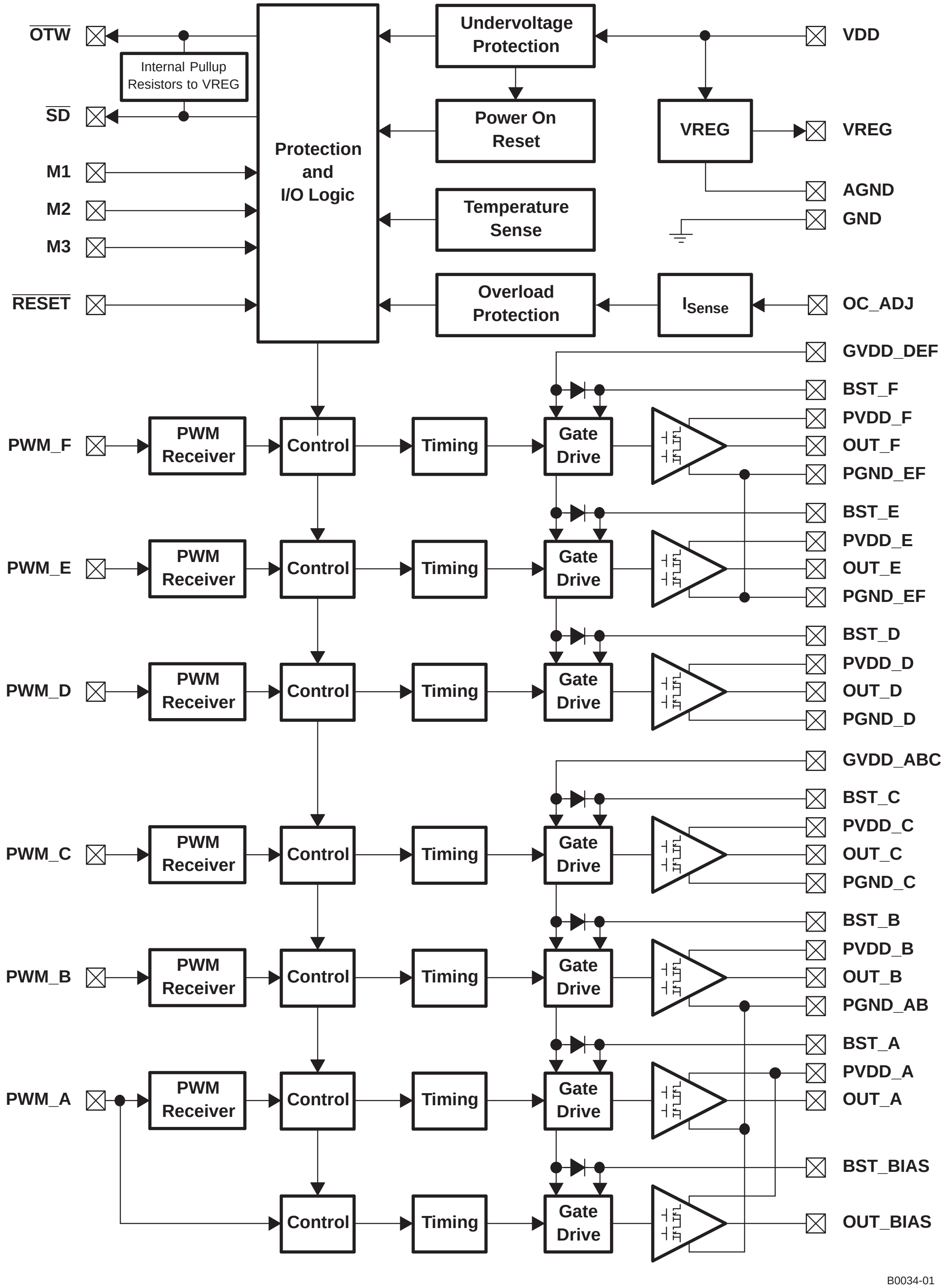
TYPICAL SYSTEM DIAGRAM (Single-ended Mode)



TYPICAL SYSTEM DIAGRAM (BTL Mode)



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
PVDD_X	Half-bridge supply, SE	DC supply voltage at pin(s)	0	31	34	V
GVDD	Gate drive and guard ring supply voltage	DC voltage at pin(s)	10.8	12	13.2	V
VDD	Digital regulator supply	DC supply voltage at pin	10.8	12	13.2	V
$R_{L,SAT}$	Resistive load impedance, satellite channels(1)	Recommended demodulation filter	6	8		Ω
$R_{L,SUB}$	Resistive load impedance, subwoofer channel	Recommended demodulation filter	3.5	4		Ω
L_{output}	Demodulation filter inductance	Minimum output inductance under short-circuit condition	5	22		µH
$C_{output,sat}$	Demodulation filter capacitance			1		µF
$C_{output,sub}$	Demodulation filter capacitance			1		µF
F_{PWM}	PWM frame rate		192	384	432	kHz

(1) Load impedance outside range listed might cause shutdown due to OLP, OTE, or NLP.

AUDIO SPECIFICATION (Single-Ended Operation)

PVDD_X = 31 V, GVDD = 12 V, audio frequency = 1 kHz, AES17 measurement filter, F_{PWM} = 384 kHz, case temperature = 75°C. Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 97%. All performance is in accordance with the foregoing specifications and recommended operating conditions unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O,sat}$	Power output per satellite channel	R_L = 8 Ω, 10% THD, clipped input signal		15		W
		R_L = 8 Ω, 0 dBFS, unclipped input signal		12		
$P_{O,sub}$	Power output, subwoofer	R_L = 4 Ω, 10% THD, clipped input signal		25		W
		R_L = 4 Ω, 0 dBFS, unclipped input signal		22		
THD + N	Total harmonic distortion + noise, satellite	R_L = 8 Ω, P_O = 10 W		.1		%
		R_L = 8 Ω, 1 W		.05		
	Total harmonic distortion + noise, subwoofer	R_L = 4 Ω, P_O = 20 W		.1		
		R_L = 4 Ω, 1 W		.05		
V_n	Output integrated noise, satellite	A-weighted		55		µV
	Output integrated noise, subwoofer	A-weighted		60		
SNR	System signal-to-noise ratio	A-weighted		105		dB
DNR	Dynamic range(1)	A-weighted, –60 dBFs input signal		105		dB
P_{idle}	Power dissipation due to idle losses (IPVDDX)	P_O = 0 W, all channels running 5.1 mode(2)		4.5		W
		P_O = 0 W, 2.1 mode		2.2		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATION (BTL Operation)

PVDD_X = 24 V, GVDD = 12 V, audio frequency = 1 kHz, AES17 measurement filter, F_{PWM} = 384 kHz, case temperature = 75°C. Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 97%. All performance is in accordance with the foregoing specifications and recommended operating conditions unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O,sat}$	Power output per satellite channel	R_L = 8 Ω, 10% THD, clipped input signal		30		W
		R_L = 8 Ω, 0 dBFS, unclipped input signal		20		
$P_{O,sub}$	Power output subwoofer channel	R_L = 6 Ω, 10% THD, clipped input signal		40		W
		R_L = 6 Ω, 0 dBFS, unclipped input signal		30		
THD + N	Total harmonic distortion + noise	R_L = 8 Ω, P_O = 20 W		.2		%
		R_L = 8 Ω, 1 W		.05		
		R_L = 6 Ω, P_O = 30 W		.2		
		R_L = 6 Ω, 1 W		.05		
V_n	Output integrated noise, satellite	A-weighted		60		μV
	Output integrated noise, subwoofer	A-weighted		65		
SNR	System signal-to-noise ratio	A-weighted		105		dB
DNR	Dynamic range (1)	A-weighted, –60 dBFs input signal		105		dB
P_{idle}	Power dissipation due to idle losses (IPVDDX)	P_O = 0 W, all channels running 5.1 mode (2)		4.5		W
		P_O = 0 W, 2.1 mode		2.2		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

F_{PWM} = 384 kHz, PVDD = 31V, GVDD = 12 V, VDD = 12 V, T_C (case temperature) = 25°C, unless otherwise noted. All performance is in accordance with recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node	VDD = 12 V	3	3.3	3.6	V
IVDD	VDD supply current	Operating, 50% duty cycle		7	20	mA
		Idle, reset mode		6	16	
IGVDD_X	Gate supply current per half-bridge	50% duty cycle		5	22	mA
		Idle, reset mode		1	3	
IPVDD_X	Half-bridge idle current	50% duty cycle, without output filter or load, 5.1 mode		180		mA
		50% duty cycle, without output filter or load, 2.1 mode		100		
OUTPUT STAGE MOSFETs						
$R_{DS(on)}$, LS Sat	Drain-to-source resistance, low side, satellite	T_J = 25°C, includes metallization resistance		210		mΩ
$R_{DS(on)}$, HS Sat	Drain-to-source resistance, high side, satellite	T_J = 25°C, includes metallization resistance		210		mΩ
$R_{DS(on)}$, LS Sub	Drain-to-source resistance, low side, subwoofer	T_J = 25°C, includes metallization resistance		110		mΩ
$R_{DS(on)}$, HS Sub	Drain-to-source resistance, high side, subwoofer	T_J = 25°C, includes metallization resistance		110		mΩ
I/O PROTECTION						
$V_{UVP, G}$	Undervoltage protection limit GVDD_X			10		V
$V_{UVP, hyst}$ (1)	Undervoltage protection hysteresis			250		mV
OTW (1)	Overtemperature warning			125		°C
OTW_{hyst} (1)	Temperature drop needed below OTW temp. for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event			25		°C
OTE (1)	Overtemperature error			155		°C
OTE_{HYST} (1)	Temperature drop needed below OTE temp. for $\overline{SD}$ to be released after the $\overline{OTE}$ event			25		°C
OLCP	Overload protection counter		1.25			ms
I_{OC}	Overcurrent limit protection, sat.	Resistor programmable, high end, Rocp = 18 kΩ		4.5		A
	Overcurrent limit protection, sub.	Resistor programmable, high end, Rocp = 18 kΩ		8		A
I_{OCT}	Overcurrent response time			210		ns
Rocp	OC programming resistor range	Resistor tolerance = 5%		27		kΩ
STATIC DIGITAL SPECIFICATION						
V_{IH}	High-level input voltage	PWM_X, M1, M2, M3, $\overline{RESET}$	2			V
V_{IL}	Low-level input voltage				0.8	
I_{lkg}	Input leakage current	Static condition	–80		80	μA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistor to DREG (3.3 V) for $\overline{SD}$ and $\overline{OTW}$			26		kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	3	3.3	3.6	V
		External pullup: 4.7-kΩ resistor to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	
FANOUT	Device fanout $\overline{OTW}$, $\overline{SD}$	No external pullup		30		Devices

(1) Specified by design.

TYPICAL CHARACTERISTICS, 5.1 MODE

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

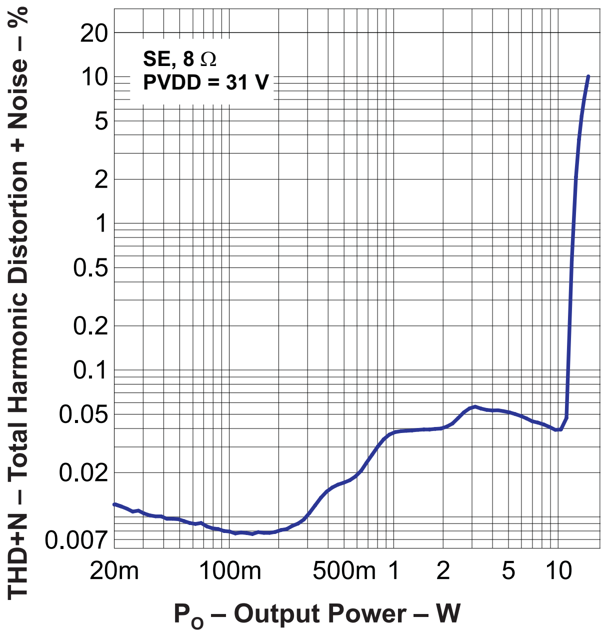


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

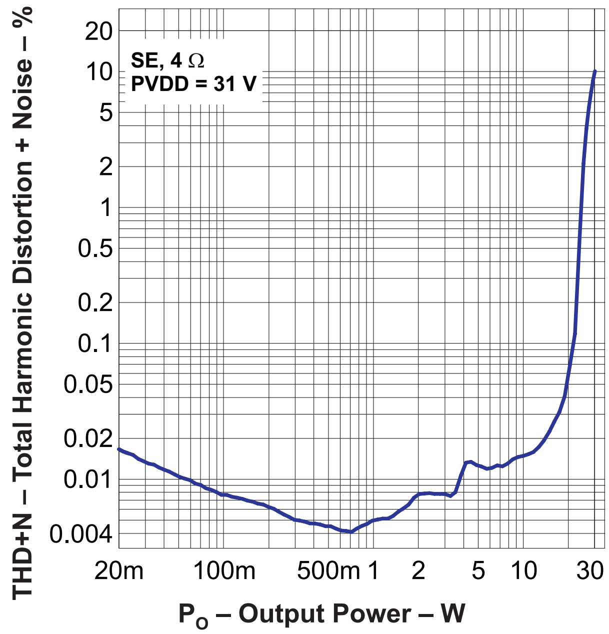


Figure 2.

OUTPUT POWER
vs
SUPPLY VOLTAGE

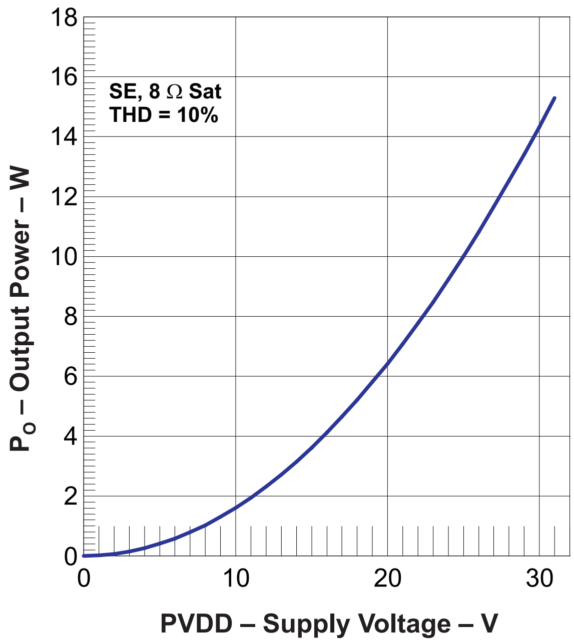


Figure 3.

OUTPUT POWER
vs
SUPPLY VOLTAGE

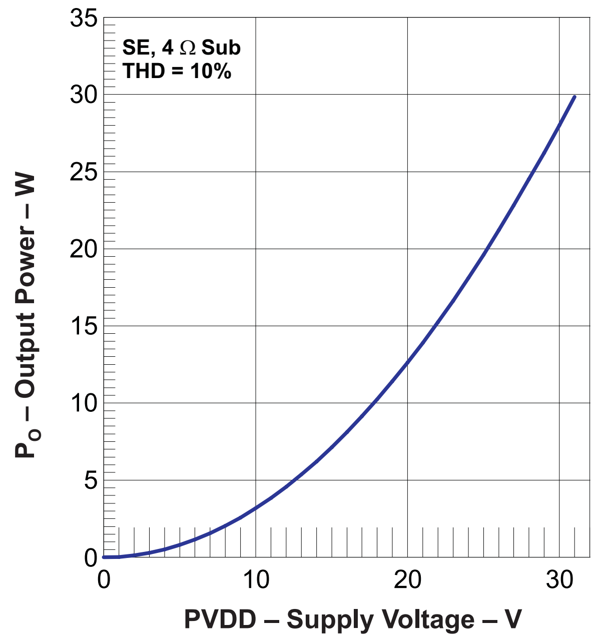


Figure 4.

OUTPUT POWER
vs
SUPPLY VOLTAGE

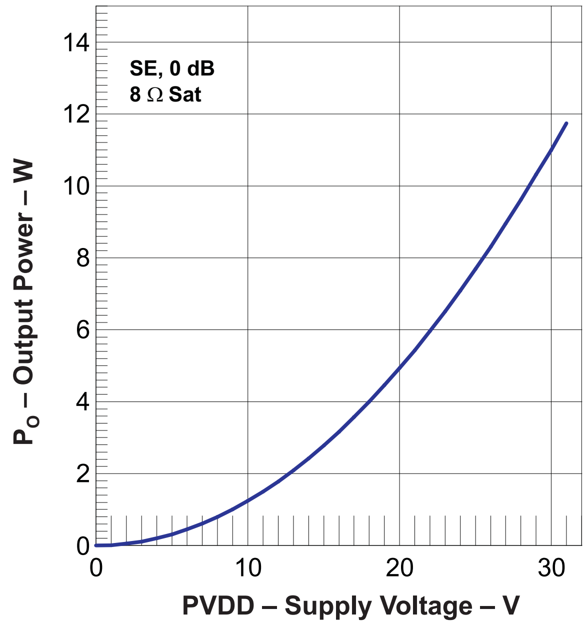


Figure 5.

OUTPUT POWER
vs
SUPPLY VOLTAGE

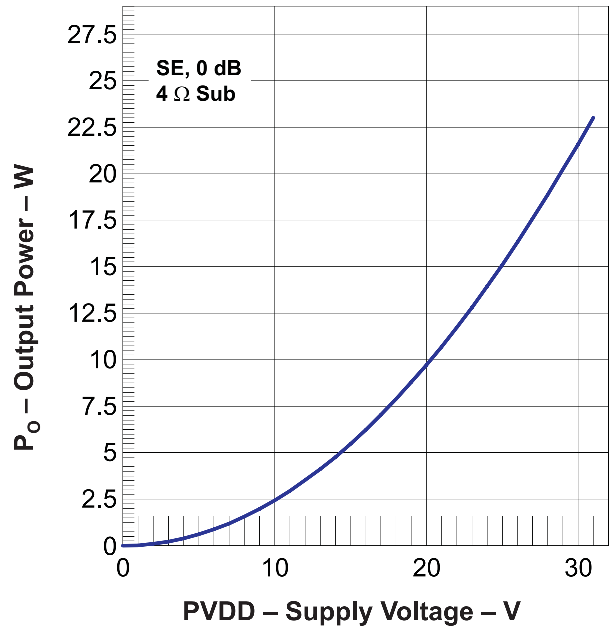


Figure 6.

SYSTEM EFFICIENCY
vs
TOTAL OUTPUT POWER

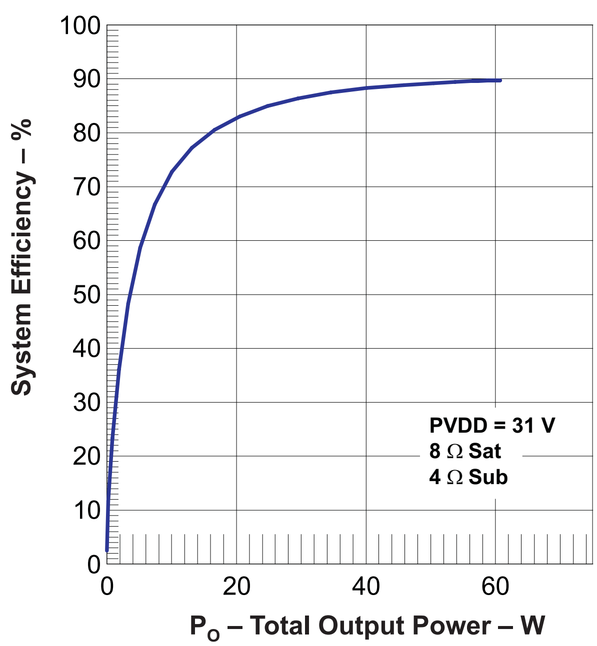


Figure 7.

SYSTEM POWER LOSS
vs
TOTAL OUTPUT POWER

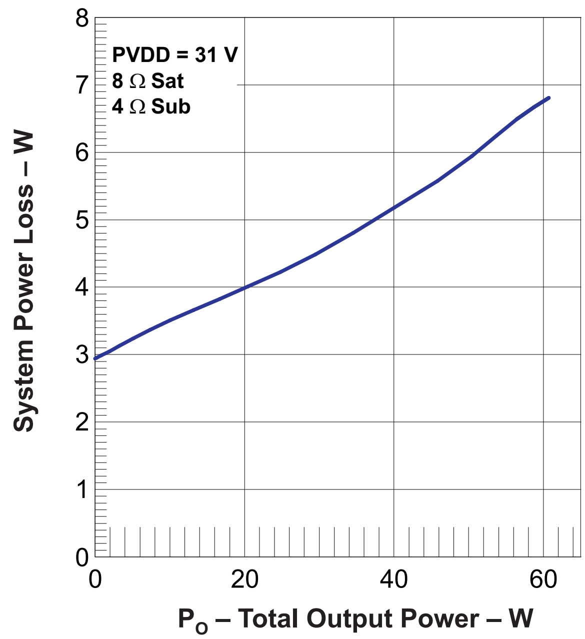


Figure 8.

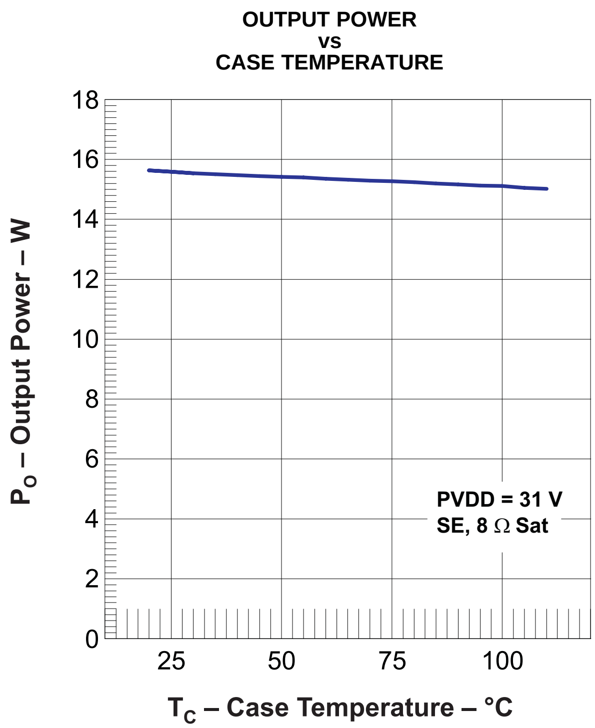


Figure 9.

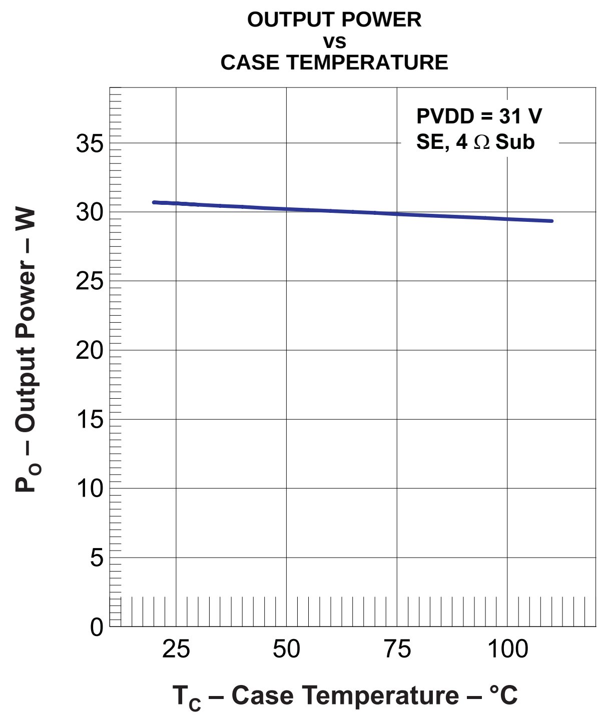


Figure 10.

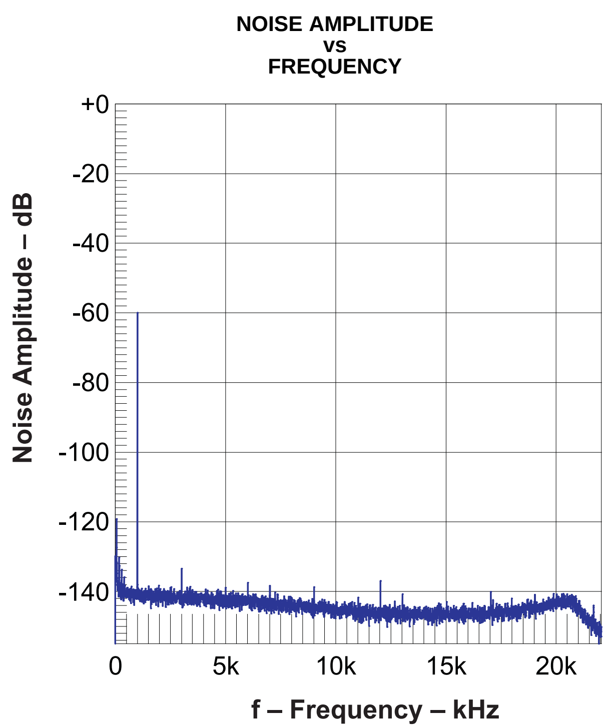


Figure 11.

TYPICAL CHARACTERISTICS, 3.0 BTL MODE

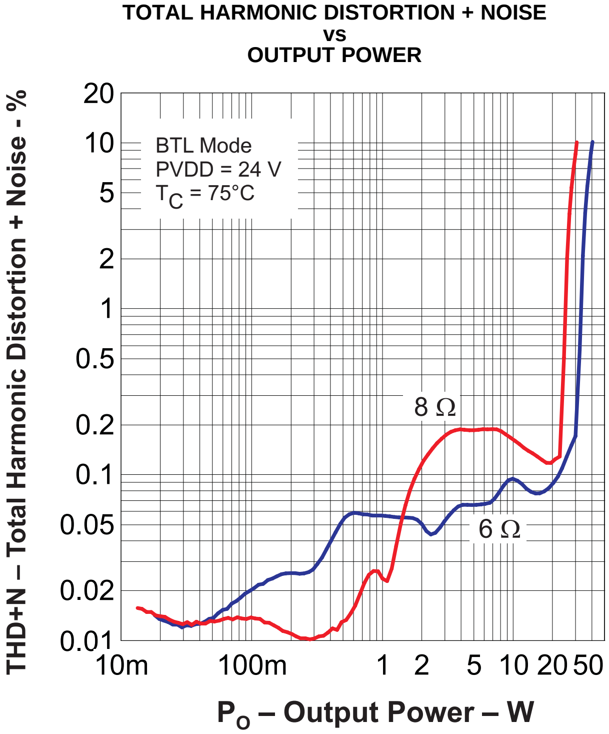


Figure 12.

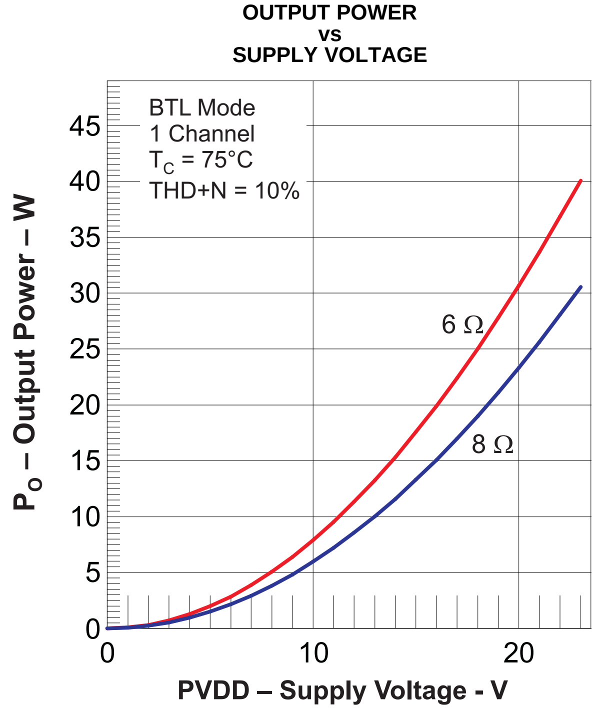


Figure 13.

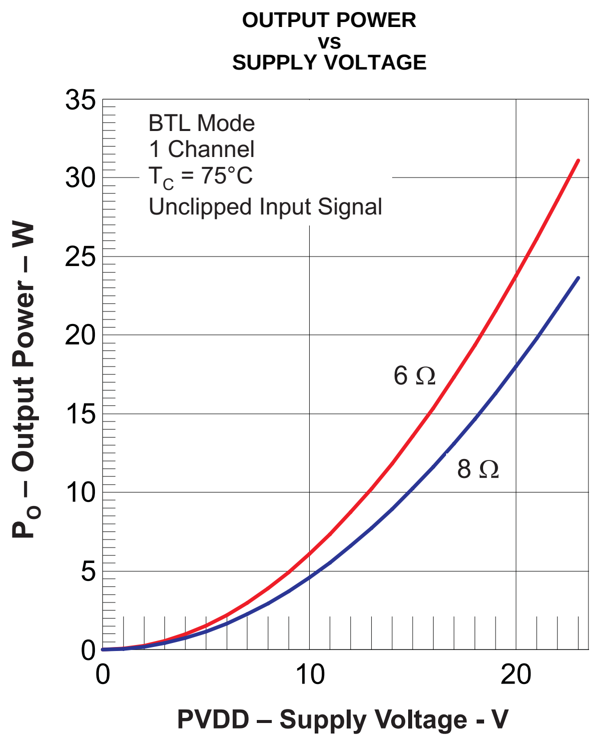


Figure 14.

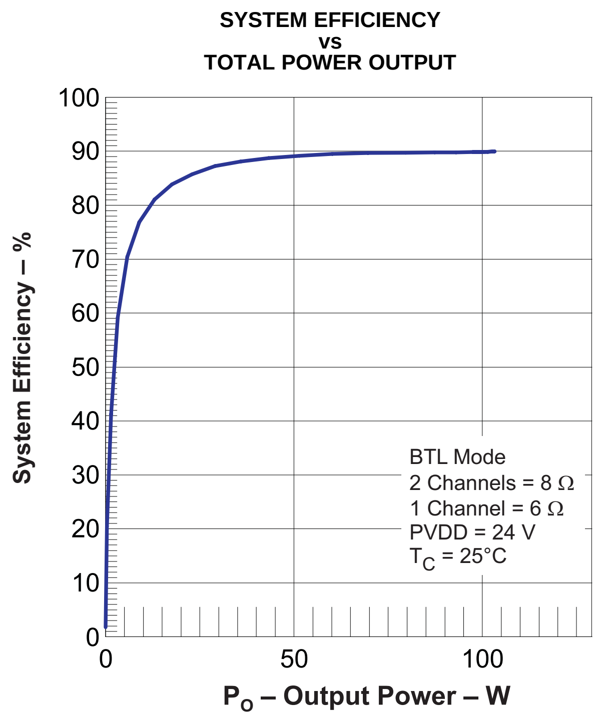


Figure 15.

SYSTEM POWER LOSS
vs
TOTAL OUTPUT POWER

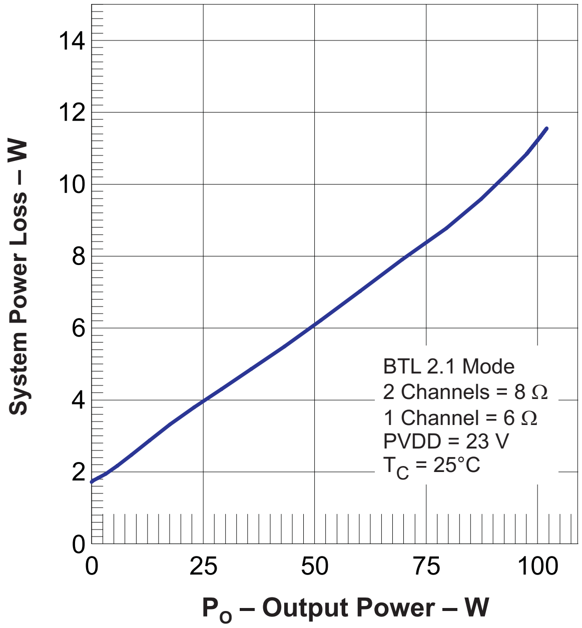


Figure 16.

OUTPUT POWER
vs
CASE TEMPERATURE

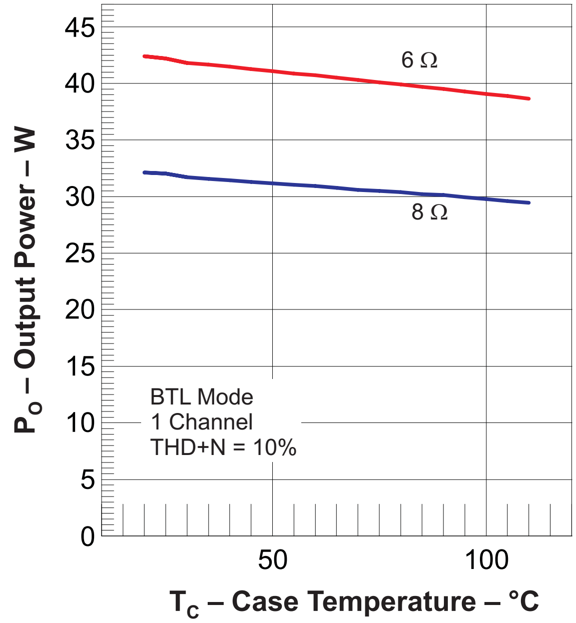


Figure 17.

NOISE AMPLITUDE
vs
FREQUENCY

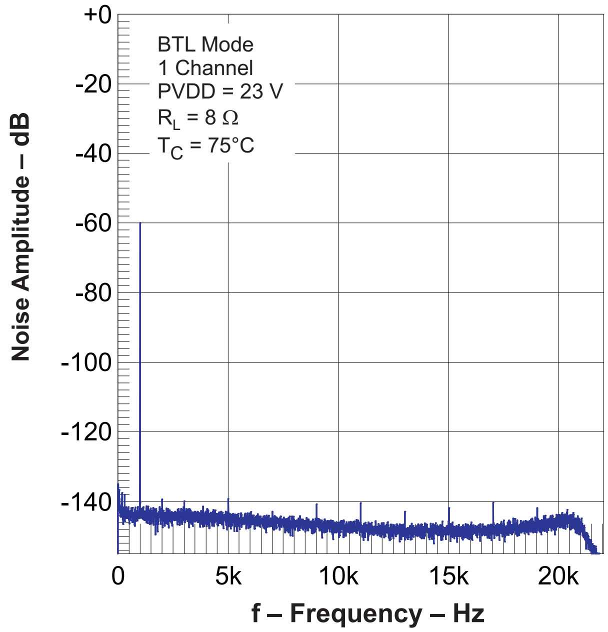


Figure 18.

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5176 needs only a 12-V supply in addition to a typical 31-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustic characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X) and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as power supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_X and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output voltage is high, the bootstrap capacitor voltage is shifted above the output voltage potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap capacitor. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully started during all of the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 250 kHz to 192 kHz, the bootstrap capacitor might need to be increased in value. Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin on the same side of the PCB as the TAS5176. It is recommended to follow the PCB layout and PowerPad layout of the TAS5176 reference design. For additional information on the recommended power supply and required components, see the application diagrams given in this data sheet. The 12-V supply should be powered from a low-noise, low-output-impedance voltage regulator. Likewise, the PVDD power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical due to the internal power-on-reset circuit. Moreover, the TAS5176 is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are typically noncritical.

SYSTEM POWER-UP/DOWN SEQUENCE

The TAS5176 does not require a power-up sequence. The outputs of the H-bridge remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device.

When the TAS5176 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET}}$ is required, provided that the chipset is configured as recommended.

Powering Down

The TAS5176 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) threshold level (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops and clicks

When the TAS5176 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET}}$ is required, provided that the chipset is configured as recommended.

Error Reporting

The $\overline{\text{SD}}$ and $\overline{\text{OTW}}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the SD pin going low. Likewise, OTW goes low when the device junction temperature exceeds 125°C (see the following table).

SD	OTW	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Overtemperature warning. Junction temperature higher than 125°C, typical
1	1	Normal operation. Junction temperature lower than 125°C, typical

It should be noted that asserting RESET low forces the SD and OTW signals high independently of faults being present. It is recommended to monitor the OTW signal using the system microcontroller and to respond to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device that would result in device shutdown (OTE). To reduce external component count, an internal pullup resistor to 3.3 V is provided on both the SD and OTW outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

Device Protection System

The TAS5176 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as safeguarding the device from permanent failure due to a wide range of fault conditions such as short circuit, overload, and undervoltage. The TAS5176 responds to a fault by immediately setting the power stage in a high-impedance state (Hi-Z) and asserting the SD pin low. In situations other than overload, the device automatically recovers when the fault condition has been removed, e.g., the supply voltage has increasedor the temperature has dropped. For highest possible reliability, recovering from an overload fault requires external reset of the device no sooner than 1 second after the shutdown (see the *Device Reset* section of this data sheet).

OVERCURRENT (OC) PROTECTION WITH CURRENT LIMITING AND OVERLOAD DETECTION

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing. I.e., it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load-impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND.

OC-Adjust Resistor Values (kΩ)	Maximum Current Before OC Occurs (A)
18K	4.5 (sat), 8.0 (sub)
27K	TBD

It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the speaker terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor.

- For the lowest-cost bill of materials in terms of component selection, the OC threshold current should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation filter inductor must retain at least 5 μH of inductance at twice the OC threshold setting.

Most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to inductor core losses and the dc resistance of the inductor copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues such as lack of output power and/or unexpected shutdowns due to sensitive overload detection.

In general, it is recommended to follow closely the external component selection and PCB layout as given in the application section.

OVERTEMPERATURE PROTECTION

The TAS5176 has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (typical), and If the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance state (Hi-Z) and SD being asserted low.

THERMAL CONSIDERATIONS

The TAS5176 device package (DDW) is designed with the PowerPad on the bottom of the device. It must be soldered to the ground plane on the printed circuit board (PCB). Under the PowerPad, there should be a pattern of vias to conduct heat through the PCB to the bottom layer ground plane. Using this technique alone, the device is capable of a total continuous power of 80 Watts.

Additional heatsinking is required for total continuous power of 100 Watts. An exposed area in the bottom layer soldermask can be created and then a aluminum bracket mechanically and thermally coupled (with heatsink paste) to the exposed area. The other end of the aluminum bracket can then be mechanically and thermally connected to the system chassis. This technique will allow the TAS5176 to run at higher ambient temperatures and/or deliver more power.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5176 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 10 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and SD being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, the output FETs in all half-bridges are forced into a high-impedance (Hi-Z) state.

Asserting the RESET input low removes any fault information to be signaled on the SD output, i.e., SD is forced high.

A rising-edge transition on the RESET input allows the device to resume operation after an overload fault.

ACTIVE-BIAS CONTROL (ABC)

Audible pop noises are often associated with single-rail, single-ended power stages at power-up or at the start of switching. This commonly known problem has been virtually eliminated by incorporating a proprietary active-bias control circuitry as part of the TAS5176 feature set. By the use of only a few passive external components (typically resistors), the ABC can pre-charge the dc-blocking element in the audio path, i.e., split-cap capacitors or series capacitor, to the desired potential before switching is started on the PWM outputs. (For recommended configuration, see the typical application schematic included in this data sheet).

The start-up sequence can be controlled through sequencing the M3 and RESET pins according to Table 2 and Table 3.

Table 2. 5.1 Mode—All Output Channels Active

M3	RESET	OUT_BIAS	OUT_A, _B, _C	OUT_D, _E, _F	COMMENT
0	0	Hi-Z	Hi-Z	Hi-Z	All outputs disabled, nothing is switching.
1	0	Active	Hi-Z	Hi-Z	OUT_BIAS enabled, all other outputs disabled
1	1	Hi-Z	Active	Active	OUT_BIAS disabled, all other outputs switching

Table 3. 2.1 Mode—Only Output Channels A, B, and C Active

M3	RESET	OUT_BIAS	OUT_A, _B, _C	OUT_D, _E, _F	COMMENT
0	0	Hi-Z	Hi-Z	Hi-Z	All outputs disabled, nothing is switching.
1	0	Active	Hi-Z	Hi-Z	OUT_BIAS enabled, all other outputs disabled
0	1	Hi-Z	Active	Hi-Z	OUT_BIAS disabled, all other outputs switching

Table 4. 3.0 Mode—Output Channels In BTL Mode

M3	$\overline{RESET}$	OUT_BIAS	OUT_A, _B, _C	OUT_D, _E, _F	COMMENT
0	0	Hi-Z	Hi-Z	Hi-Z	All outputs disabled, nothing is switching.
1	0	Active	Hi-Z	Hi-Z	OUT_BIAS enabled, all other outputs disabled
0	1	Hi-Z	Active	Hi-Z	OUT_BIAS disabled, all other outputs switching

When the TAS5176 is used with the TAS5086 PWM modulator, no special attention to start-up sequencing is required, provided that the chipset is configured as recommended.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TAS5176DDW	ACTIVE	HTSSOP	DDW	44	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5176DDWG4	ACTIVE	HTSSOP	DDW	44	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5176DDWR	ACTIVE	HTSSOP	DDW	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5176DDWRG4	ACTIVE	HTSSOP	DDW	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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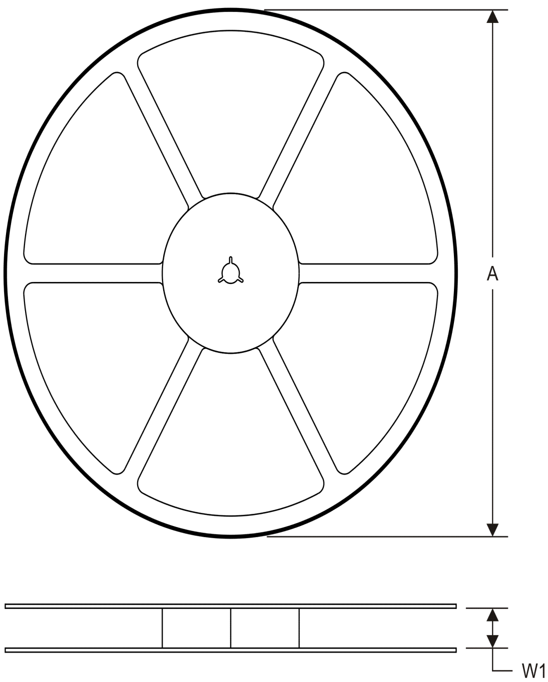
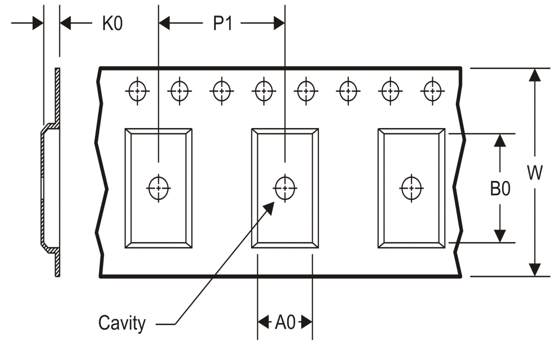
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



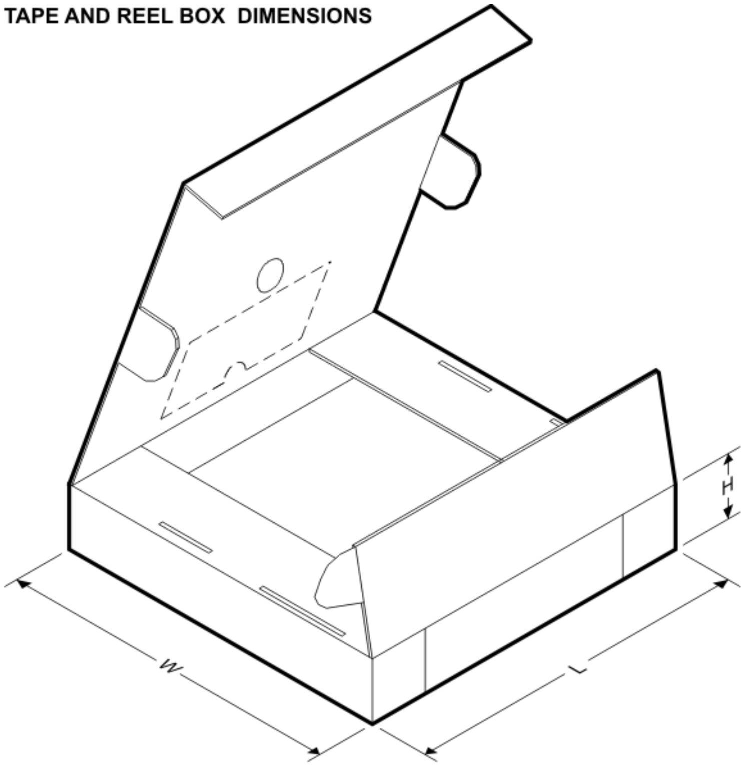
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5176DDWR	HTSSOP	DDW	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

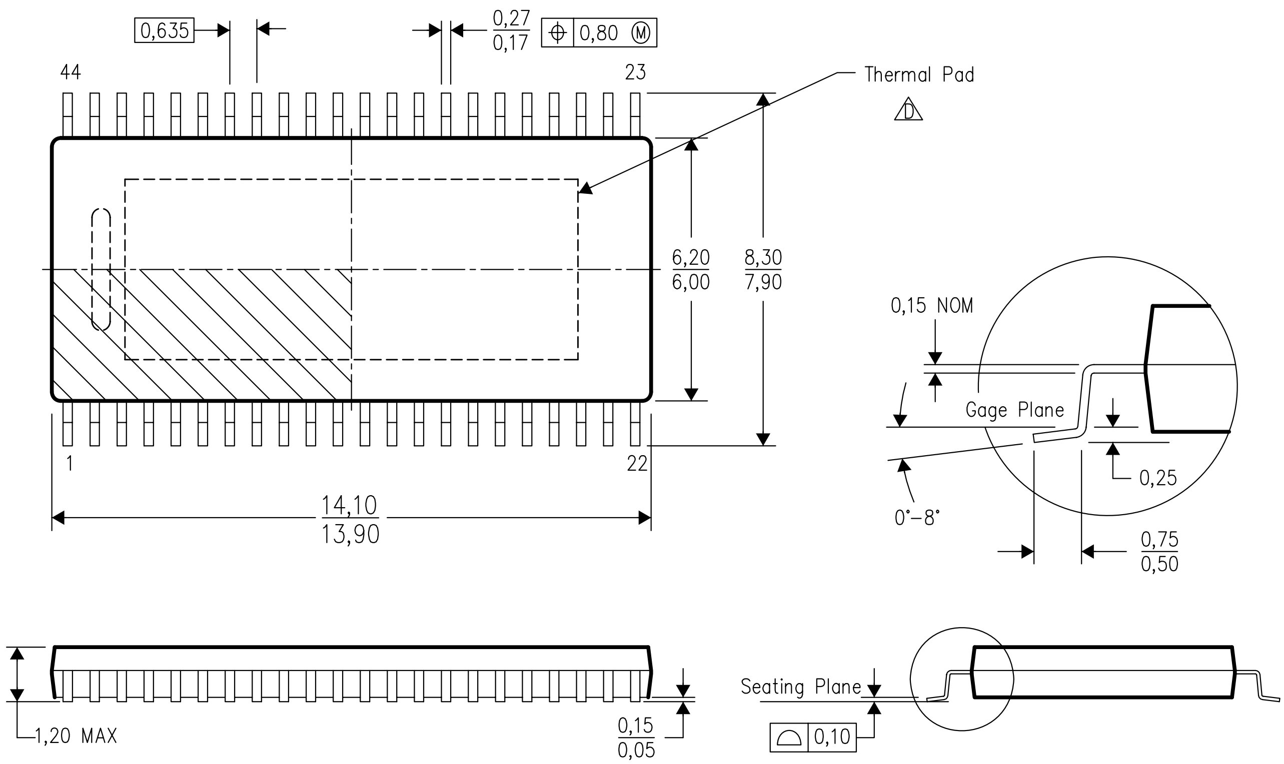
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5176DDWR	HTSSOP	DDW	44	2000	367.0	367.0	45.0

DDW (R-PDSO-G44) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE (PAD DOWN)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package thermal performance is optimized for conductive cooling with attachment to an external heat sink. See the product data sheet for details regarding the exposed thermal pad dimensions.

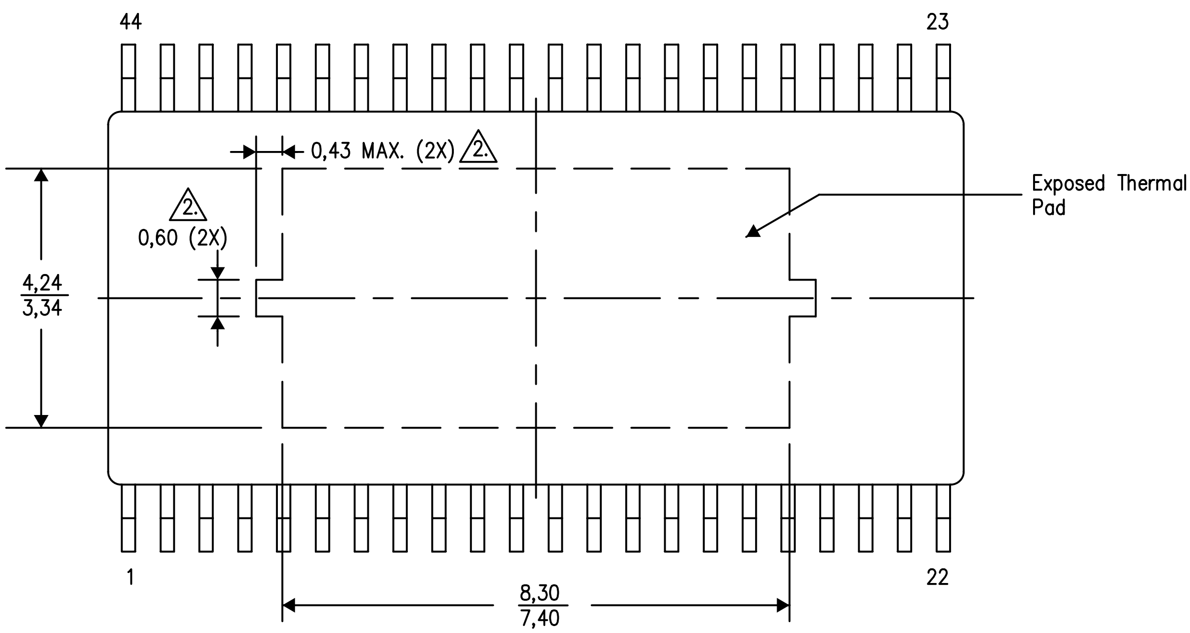
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

1. All linear dimensions are in millimeters
2. These features may not be present.

Exposed Thermal Pad Dimensions