

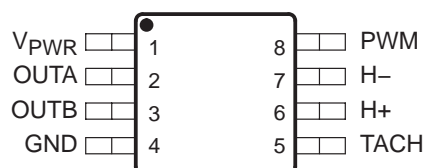
THMC45

5-V AND 3.3-V DC BRUSHLESS FAN MOTOR DRIVER WITH SINGLE WIRE CONTROL

SLIS101A – MAY 2001

- 5-V DC Fan Motor PWM Drive for Speed Control With No External Power Drive Stage Required
- High Efficiency H-Bridge Topology With Integrated Low $R_{DS(ON)}$ MOS Output Drivers to Drive Single Winding, Bipolar Wound, Two-Phase BLMs
- Digital PWM Input to Control Output PWM Frequency and Duty Cycle—Suited for Cooling Fan Applications Requiring Variable RPM Control to Reduce Noise/Increase MTBF
- Single Wire RPM Control, Tachometer Feedback Signal, and Locked Rotor Detect Feedback Signal
- Low Current Sleep State
- Tachometer Signal Valid Over Entire RPM Range
- Noise Immune Signal Conditioning to Allow Use of Low Cost Hall Effect Position Sensor
- Locked Rotor Protection With Auto Retry
- Thermal Shutdown Protection
- 8-Pin MSOP PowerPad™ Package Suited for Small Fan Circuit Board and Rotor Housing

DGN Package
(TOP VIEW)



description

The THMC45 is a dc brushless motor (BLM) driver and control device designed for use with low-voltage (5 V or 3.3 V) dc cooling fans having two-phase motors with a single-winding stator. The device includes a high-efficiency H-bridge pulse width modulation (PWM) drive topology with integrated MOS high-side and low-side drivers, plus a PWM control input stage to provide the industry's first efficient speed control solution *inside* low-voltage dc cooling fans. This solution eliminates the need for any power drive components on the main system board, reducing printed-circuit board (PCB) component count, PCB space, and assembly time. The device also offers two advantages over the other commonly used fan speed control methods, adjustable external dc supply voltage and adjustable external PWM drive duty cycle.

Unlike the external linear voltage regulation method, the THMC45 high-efficiency PWM drive method adjusts the level of motor winding power while all other circuitry inside the fan obtains a fixed dc voltage from the fan supply. This eliminates problems with loss of headroom to internal control circuitry at low fan supply voltage and the resulting limitation of low-speed operation of 40% that is typically associated with external dc voltage regulation. The high-efficiency PWM drive method employed by the THMC45 reduces fan supply power consumption and maximizes full-scale RPM speed over the external linear voltage regulation method, which has $V \times I$ power loss due to the voltage drop across the regulator.

The THMC45 includes a Hall sensor amplifier and signal conditioning, global thermal shutdown, and locked rotor protection with automatic restart after a locked rotor condition. The device provides a sleep state to eliminate the need for an external power component to disconnect the fan from the supply during a system sleep state. The device also has internal reverse blocking capability to prevent excessive reverse leakage current due to reversal of power line. The THMC45 is primarily designed for 5-V dc notebook PC cooling fan applications that require single-wire RPM speed control and tachometer feedback. However, with an open-drain tachometer output, the device is also suitable for applications that require two wires for RPM speed control and tachometer signal.



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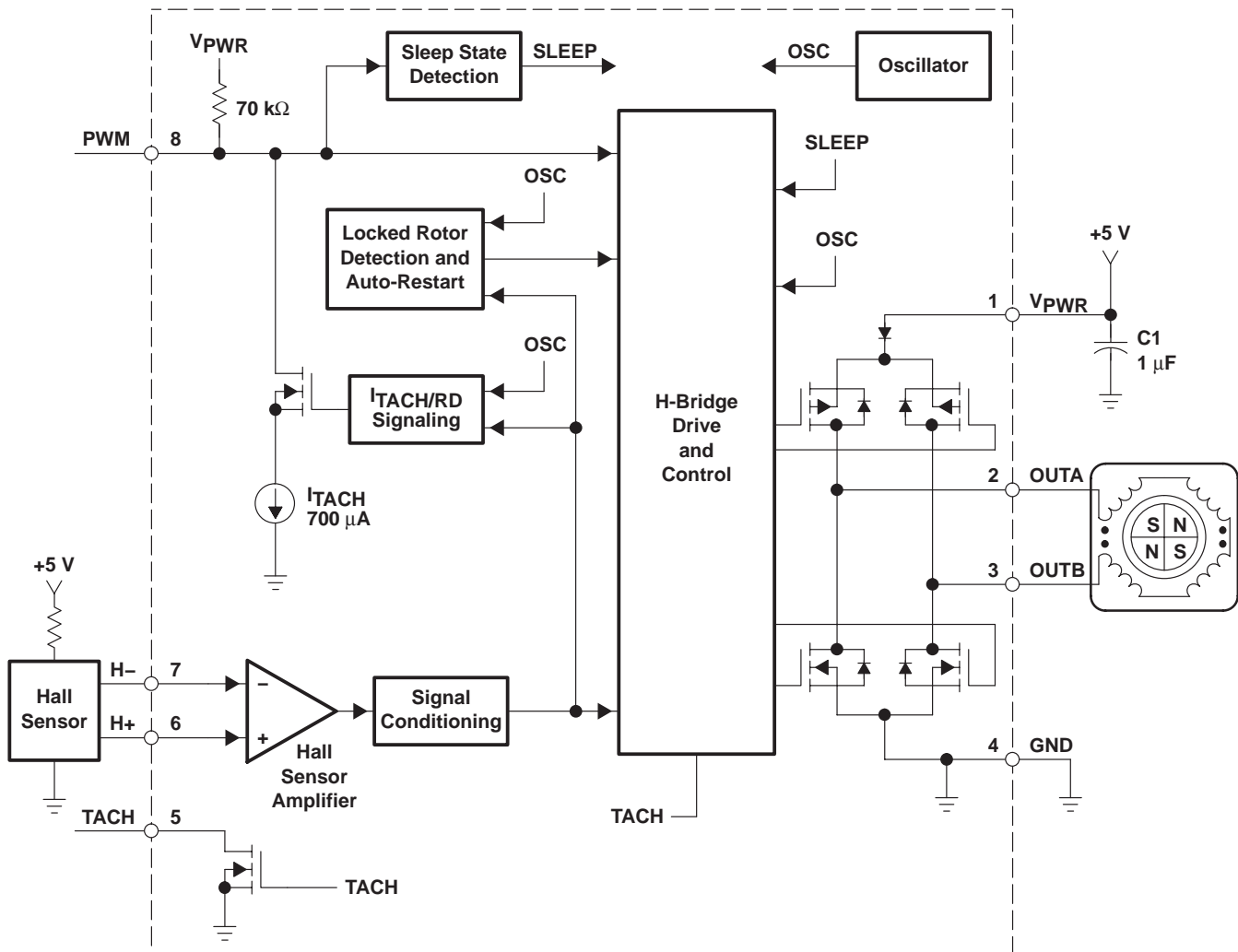


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THMC45 5-V AND 3.3-V DC BRUSHLESS FAN MOTOR DRIVER WITH SINGLE WIRE CONTROL

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functional block diagram



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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	4	I	Ground
H+	6	I	Hall sensor positive input
H-	7	I	Hall sensor negative input
OUTA	2	O	Motor winding drive output A
OUTB	3	O	Motor winding drive output B
PWM	8	I/O	PWM duty cycle control input and tachometer/locked rotor detect current sink output
TACH	5	O	Open drain tachometer output signal
V _{PWR}	1	I	5-V Supply voltage input

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage input, V _{PWR} (see Note 1)	6 V
Open-drain tachometer output voltage, V _{TACH} (see Note 1)	6 V
H-bridge output voltage, V _{OUTA} , V _{OUTB} (see Note 1)	6 V
Hall sensor amplifier input voltage, V _{H+} , V _{H-} (see Note 1)	6 V
Speed control voltage input and tachometer/locked rotor feedback, V _{PWM} (see Note 1)	6 V
Continuous H-bridge output current source/sink, I _{OUTA} , I _{OUTB} (see Note 2)	350 mA
Continuous H-bridge output current source/sink, I _{OUTA} , I _{OUTB} (see Note 3)	260 mA
Continuous power dissipation, P _D (see Note 4)	2.1 W
Operating case temperature range, T _C	–30°C to 80°C
Storage temperature range, T _{stg}	–55°C to 150°C
Maximum junction temperature, T _J	150°C
Lead temperature (soldering, 10 sec), T _{LEAD}	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values are with respect to GND.
 - Assumed package plus PCB system thermal impedance = 170°C/W, T_A = 25°C.
 - Assumed package plus PCB system thermal impedance = 170°C/W, T_A = 80°C.
 - In free air at T_A = 25°C, assumed 58.4°C/W and T_J = 150°C.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V _{PWR}	2.5	5	V
PWM high-level input voltage, V _{IH}	2		V
PWM low-level input voltage, V _{IL}		0.8	V
PWM input frequency, f _{PWM}	18	50	kHz
Operating case temperature, T _C	–30	80	°C



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dc electrical characteristics, $V_{PWR} = 5V$, $T_A = -30^{\circ}C$ to $80^{\circ}C$ (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PWR}	Supply voltage normal operation		4.5	5	5.5	V
	Supply voltage functional with derated performance		2.4		4.5	
V_{POR}	Power-on reset voltage threshold	Increase V_{PWR} until logic active		1.5		V
I_{VPWR}	V_{PWR} supply current	$I_L = 0 A$		0.5	1.5	mA
		Idle condition, in locked rotor detect		0.5	1.5	
I_{REV}	Reverse leakage	$V_{PWR} = -5 V$ at $T_A = 25^{\circ}C$		5		mA
I_{SLEEP}	Sleep-state current	$V_{PWM} = 0 V$ for $>2 ms$		75	300	μA

Hall sensor signal conditioning

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IB(HL)}$	Input bias current	See Note 5	-1		1	μA
$V_{ICR(HL)}$	ICR(HL) common mode input voltage range		1		3.5	V
V_{IO}	Hall amplifier input offset voltage		-20	0	20	mV

NOTE 5: Design target only. Not tested in production.

OUTA, OUTB phase winding driver outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	OUTA, OUTB output leakage current	$V_{PWM} = 0 V$ for $>2 ms$, sleep state, $V_{OUTx} = 5 V$	-1		1	μA
$R_{DSON(Low)}$	OUTA, OUTB low-side output ON resistance	$I_{OUTx} = 200 mA$, $T_A = 25^{\circ}C$		1.6	2.5	Ω
$R_{DSON(High)}$	OUTA, OUTB high-side output ON resistance	$I_{OUTx} = -200 mA$, $T_A = 25^{\circ}C$		1.9	2.5	Ω
R_{DSON}	OUTA, OUTB low-side output ON resistance	$I_{OUTx} = 100 mA$, $T_A = 25^{\circ}C$, $V_{PWR} = 2.4 V$		3	6	Ω
	OUTA, OUTB high-side output ON resistance	$I_{OUTx} = -100 mA$, $T_A = 25^{\circ}C$, $V_{PWR} = 2.4 V$		3.5	6	Ω

PWM input/TACH pulse output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	PWM high-level input voltage		2			V
V_{IL}	PWM low-level input voltage				0.8	V
I_{IH}	PWM high-level input current	$V_{PWM} = 5 V$	-1		1	μA
I_{IL}	PWM low-level input current	$V_{PWM} = 0 V$		75	200	μA
V_{OL}	PWM input tachometer pulse output low voltage	$I_{PWM} = 2 mA$			0.4	V

TACH open-drain output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	TACH output high leakage	$V_{TACH} = V_{PWR}$	-1		1	μA
V_{OL}	TACH output low voltage	$I_{TACH} = 5 mA$			400	mV



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ac electrical characteristics, $V_{PWR} = 5\text{ V}$, $T_A = -30^\circ\text{C}$ to 80°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		18	30	50	kHz
$t_{(SLEEP)}$	Time to enter sleep state after no transitions on PWM terminal	See Figure 5		2		ms
$t_{(PW)}$	Tachometer signal pulse width	See Figure 4		1		μs
t_d	Delay after rising edge of PWM input for TACH signal	See Figure 4		1		μs
t_{RD}	Locked rotor detect delay time	See Figure 6		1		s
t_{RETRY}	Auto-restart delay time	See Figure 6		8		s
$t_{(de-glitch)}$	Hall transition valid time for commutation to occur	See Figures 1 and 4		25		μs
$t_{(PWM_de-glitch)}$	De-glitch time for PWM input to prevent TACH current pulses from falsely triggering PWM	See Figure 5		25		μs
$t_f(\text{OUT})$	OUTA, OUTB output fall time	See Note 5		200		ns
$t_r(\text{OUT})$	OUTA, OUTB output rise time	See Note 5		200		ns

NOTE 5: Design target only. Not tested in production.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta J(\text{SYS})}$	Thermal resistance, in system	2 oz. copper traces, JEDEC low K board, 0 LFPM airflow		58.4	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal resistance, junction-to-case	Exposed back-side die mount		4.7	$^\circ\text{C/W}$

PRINCIPLES OF OPERATION

general overview

The THMC45 is a dc BLM driver and control device designed for use with low-voltage (5 V or 3.3 V) dc cooling fans having two-phase motors with a single winding, bipolar-wound stator. The device is intended primarily for low-voltage cooling fan applications requiring speed control with a tachometer feedback signal to ensure normal fan operation. The output drive PWM duty cycle and frequency are dependent on the input signal on the PWM terminal. The device has an internal Hall sensor amplifier and signal conditioning with drive commutation logic, a low power sleep-state mode, and locked rotor protection with automatic restart after a locked rotor condition. The PWM terminal is used to input PWM frequency and duty cycle, to output a tachometer current pulse feedback signal, and to provide a means for entering sleep and run states. The THMC45 provides a more effective drive solution to fan RPM control than either external linear voltage regulation or external PWM drive. The device is offered in an MSOP-8 miniature surface-mount package to meet the critical space constraints of PCB designs of small low-voltage fans typically found in notebook PCs.

supply voltage input (V_{PWR})

The V_{PWR} terminal serves as the voltage supply input to the THMC45. A 0.1- μF bypass capacitor should be placed as close to this terminal as layout permits.



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PRINCIPLES OF OPERATION

Hall sensor amplifier inputs (H+, H-)

The THMC45 has an internal Hall sensor amplifier with signal conditioning to allow the use of low-cost Hall sensors requiring no external components for noise filtering. The Hall signal conditioning block receives a low-level differential voltage from the Hall position sensor and implements a zero differential voltage crossing detection with a de-glitch time of 25 μ s (typical), $t_{(de-glitch)}$, to reject noise on the Hall signal inputs. Refer to Figure 1, the OUTA output changes from sourcing current to sinking current after the 25- μ s de-glitch time. Likewise, the OUTB output changes from sinking current to sourcing current after the 25- μ s de-glitch time. The Hall amplifier circuit has an input offset voltage, V_{IO} , not greater than ± 13 mV when V_{PWR} is between 4.5 V and 5.5 V. The common mode input voltage range is 1 V to 3.5 V when V_{PWR} is between 4.5 V and 5.5 V.

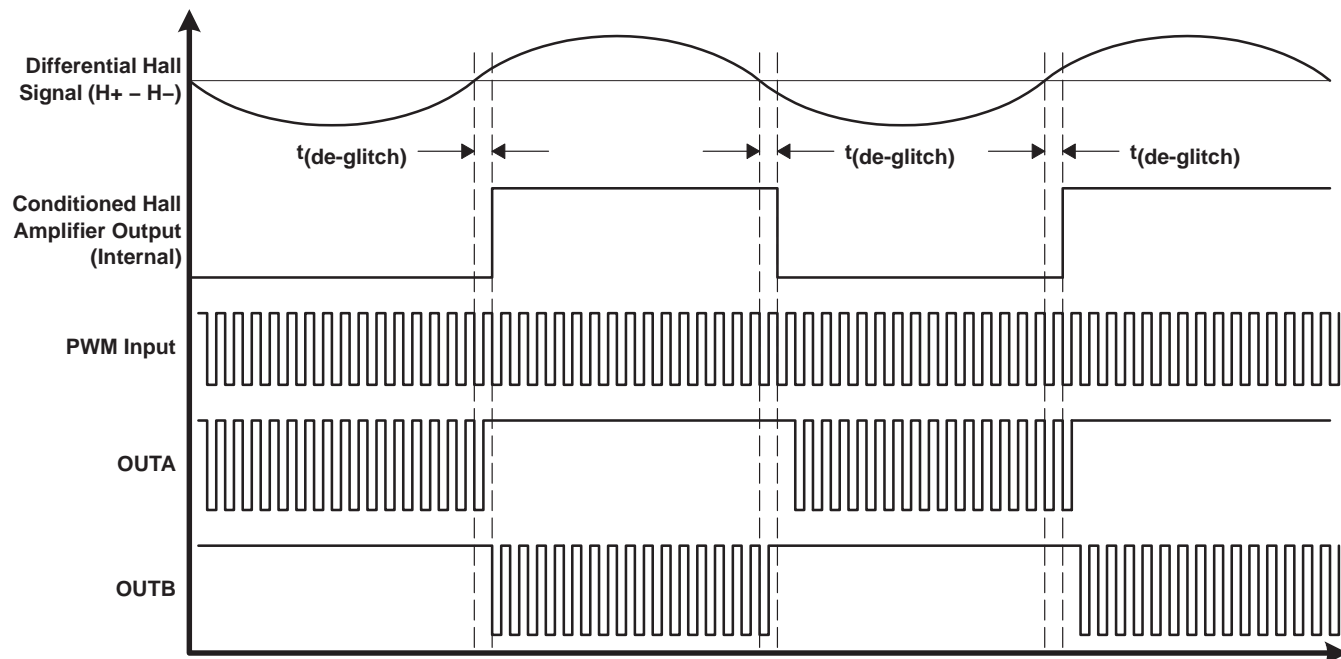


Figure 1. Hall Sensor Signal Conditioning Waveform and OUTA/OUTB Commutation

Illustrated in truth table format, Table 1 shows OUTA and OUTB commutation and PWM.

Table 1. OUTA and OUTB Low-Side Drive Commutation

H+	H-	OUTA	OUTB
H	L	H	PWM
L	H	PWM	H

H-bridge motor drive outputs (OUTA, OUTB)

Using an H-bridge to drive a bipolar wound, two-phase BLM provides several advantages for dc fans over the unipolar-wound motor commonly driven by two commutated low-side switches. A bipolar-wound motor has only two connections; hence, the H-bridge drive topology requires only two output terminals and two traces are needed on the fan PCB. A bipolar-wound stator has a single-wire winding which is simpler to manufacture, and thus increases reliability and reduces manufacturing time. All factors combine to allow a smaller diameter fan center hub, and thus higher blade area for increased airflow on a given fan frame size. Generally, an H-bridge drive method with bipolar-wound stator increases fan motor torque density over a typical unipolar drive method. The H-bridge drive method also eliminates the need for snubbing inductive energy at commutation transitions and allows for recirculation of winding current to maintain energy in the motor while PWM switching occurs.

PRINCIPLES OF OPERATION

H-bridge motor drive outputs (OUTA, OUTB) (continued)

Figures 2a and 2b show THMC45 H-bridge motor drive states with stator winding current being driven from OUTA to OUTB and from OUTB to OUTA, respectively, based on the Hall sensor commutation state. As shown during t_{ON} , PWM signal is high and the drive current is from V_{PWR} through the activated switches and motor to GND. PWM occurs on the low side, and the stator winding inductive current recirculates on the high side during t_{OFF} and PWM signal is low (see Figure 3 for motor current waveform). Recirculation of inductive current through the high-side switches during t_{OFF} , known as *synchronous rectification*, improves power conversion efficiency by maintaining energy in the stator winding and results in a continuous dc current level.

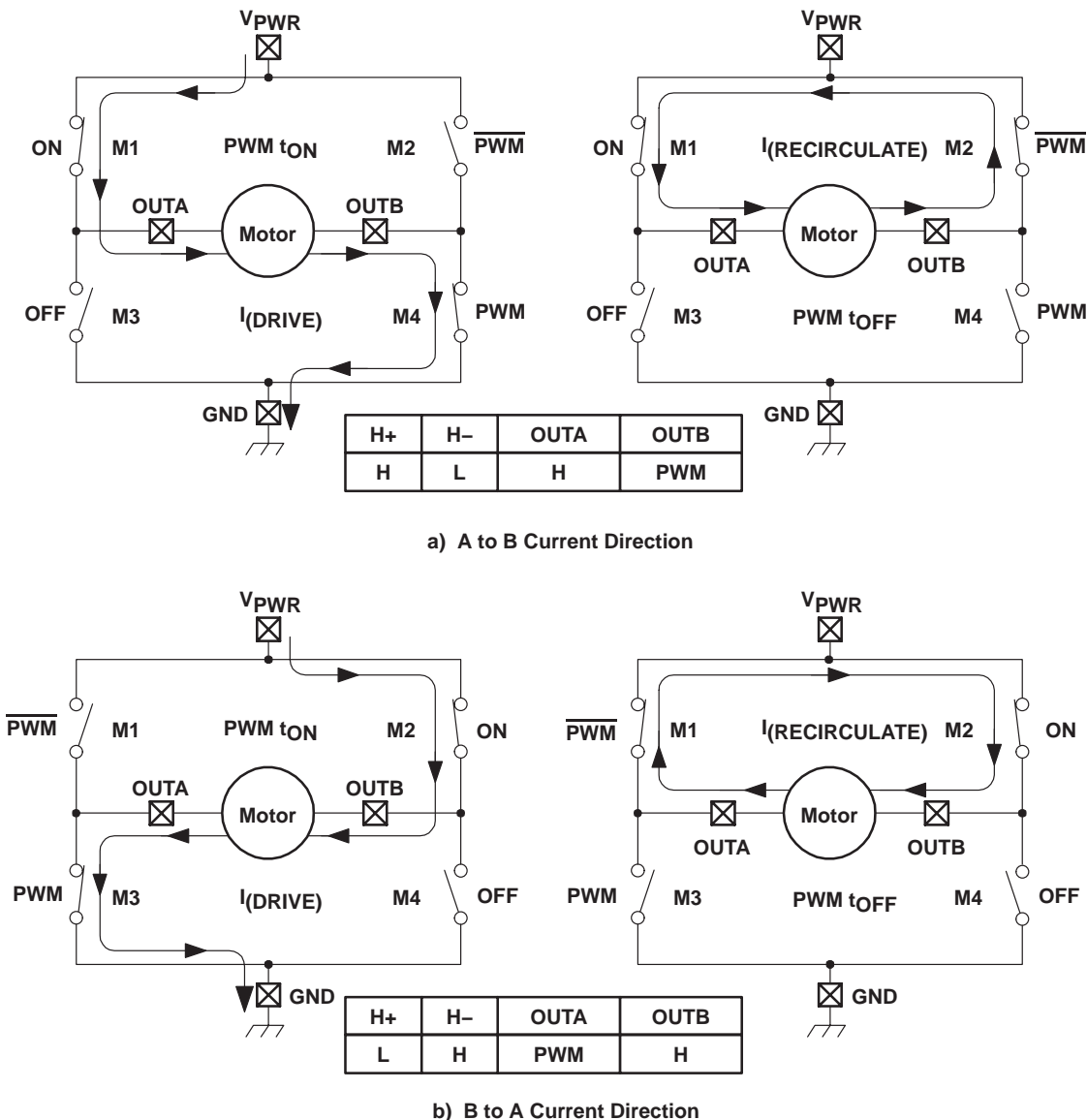


Figure 2. H-Bridge PWM Drive With Synchronous Rectification

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PRINCIPLES OF OPERATION

PWM input (PWM)

The PWM input provides several functions:

- Input for controlling H-bridge PWM drive frequency and duty cycle
- Output for a tachometer current sink pulse on the first rising edge of the PWM input signal after a commutation
- Initiating a low-current sleep state when the voltage maintained a logic low level for 2 ms (typical) or longer, and allowing the THMC45 to return to a normal run state on the next rising edge of the PWM input signal

The THMC45 requires a TTL level PWM input signal from another device, such as a Super I/O device. This signal, along with the Hall sensor input, is used to PWM the OUTA and OUTB outputs according to truth table, Table 1.

It is recommended that the frequency of the PWM input signal be between 18 kHz and 60 kHz. A PWM frequency of 18 kHz or higher, being above the audible range, ensures quiet fan operation. Frequencies above 18 kHz also promote efficient fan speed control by keeping the PWM period below the electrical L/R time constant of the motor. This allows continuous current in the fan windings (see Figure 3). Keeping the PWM frequency below 60 kHz minimizes switching losses. Switching losses, typically observed at higher frequencies, decreases overall efficiency.

The speed of the cooling fan can be varied by adjusting the duty cycle of the PWM input signal. The higher the duty cycle of the PWM input signal, the higher the current in the fan windings, and thus results in faster fan speed.

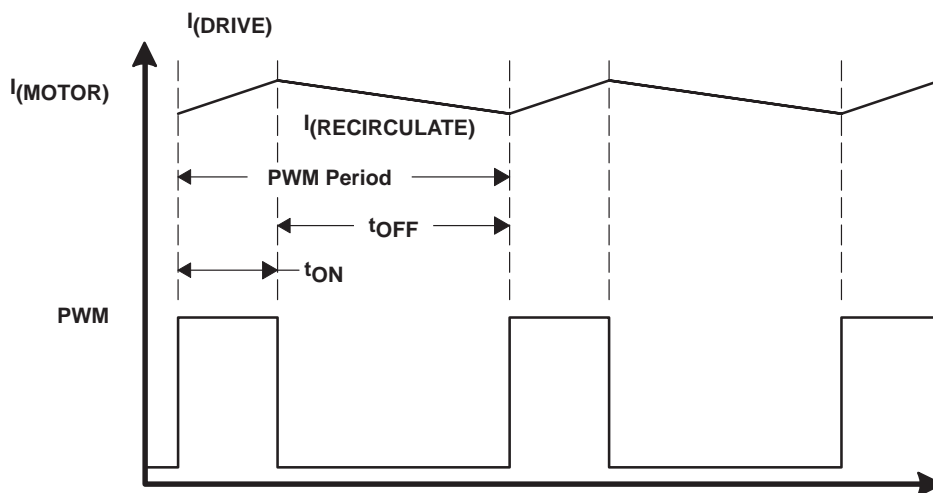


Figure 3. Motor Current Waveform

PRINCIPLES OF OPERATION

tachometer signaling on PWM input (PWM)

The PWM terminal of the THMC45 provides a 1- μ s (typical) current sink pulse, $t_{(PW)}$, following the next rising edge of the PWM input signal after the Hall sensor amplifier changes states (see Figure 4). Note that the THMC45 incorporates a blanking circuit that disregards transitions on the PWM terminal during the TACH current pulses. This ensures that the TACH pulses do not corrupt the output PWM signal. This current signal can be detected with external circuitry and can be sent to the TACH input of the hardware monitor portion of a Super I/O device.

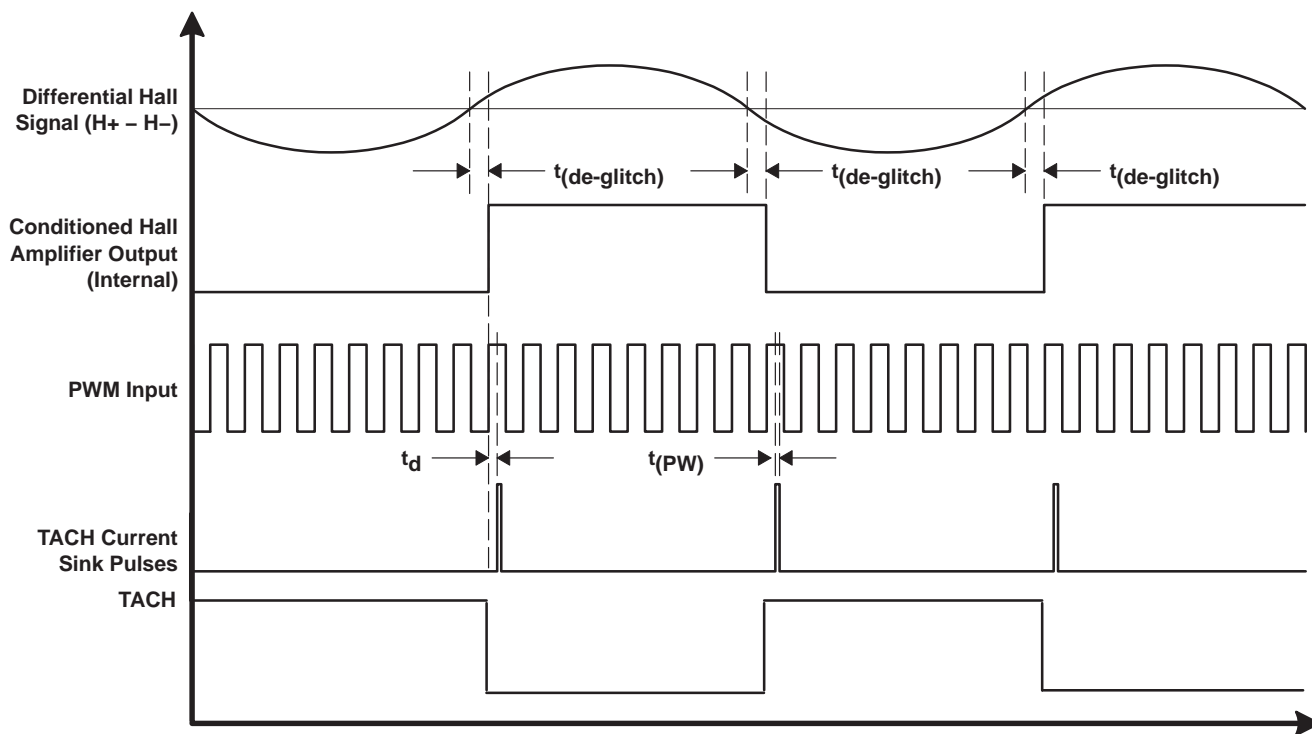


Figure 4. Tachometer Current Pulse Timing on PWM Input Pin

sleep/run states using PWM input (PWM)

The THMC45 enters a low-current sleep state when the PWM input maintains a logic low level for more than 2 ms (typical), $t_{(SLEEP)}$. In sleep state, the OUTA and OUTB outputs are in a high-impedance state. The THMC45 transitions from sleep state to run state on the first rising edge on the PWM input. Figure 5 shows the timing relationships between the PWM signal and sleep/run state.

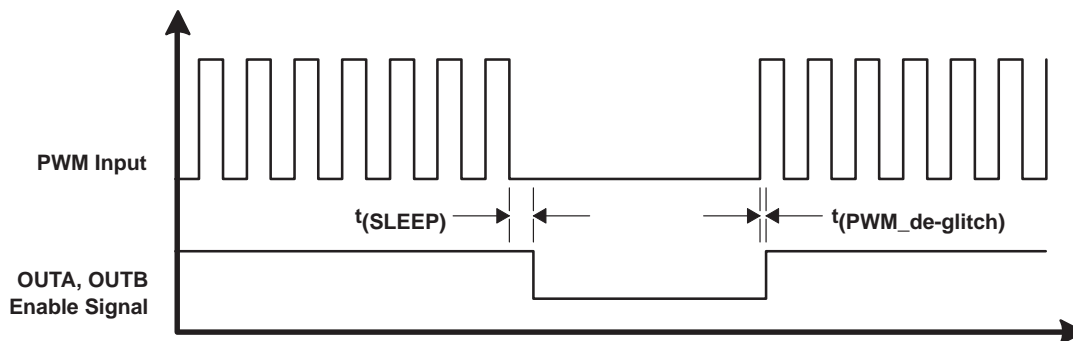


Figure 5. PWM Input Signal, Sleep State, and Run State Timing

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PRINCIPLES OF OPERATION

locked rotor protection

An internal digital timer is used to monitor the output of the Hall sensor amplifier. When change in commutation state is not observed via the Hall amplifier inputs within 1 second (typical), $t_{(RD)}$, the OUTA and OUTB outputs are disabled for 8 seconds (typical), $t_{(RETRY)}$. After this period, the THMC45 re-enables the OUTA and OUTB outputs to automatically restart the motor after a locked rotor condition. When the locked rotor condition continues to exist, the above process repeats itself until the locked condition is removed or the THMC45 is powered down (see Figure 6).

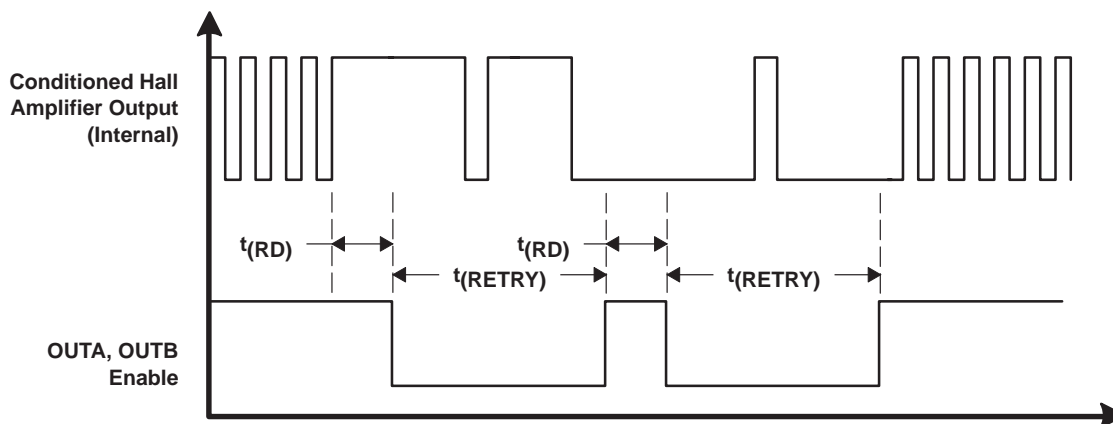


Figure 6. Typical Locked Rotor Protection Timing Waveforms

open-drain tachometer output (TACH)

The TACH output is an open-drain output that is activated by the output of the Hall sensor comparator output. When the output of the Hall sensor comparator is high, the TACH output floats high. When the output of the Hall sensor amplifier is low, the TACH output is pulled low. The resulting output signal has two pulses per revolution on a four-pole motor.

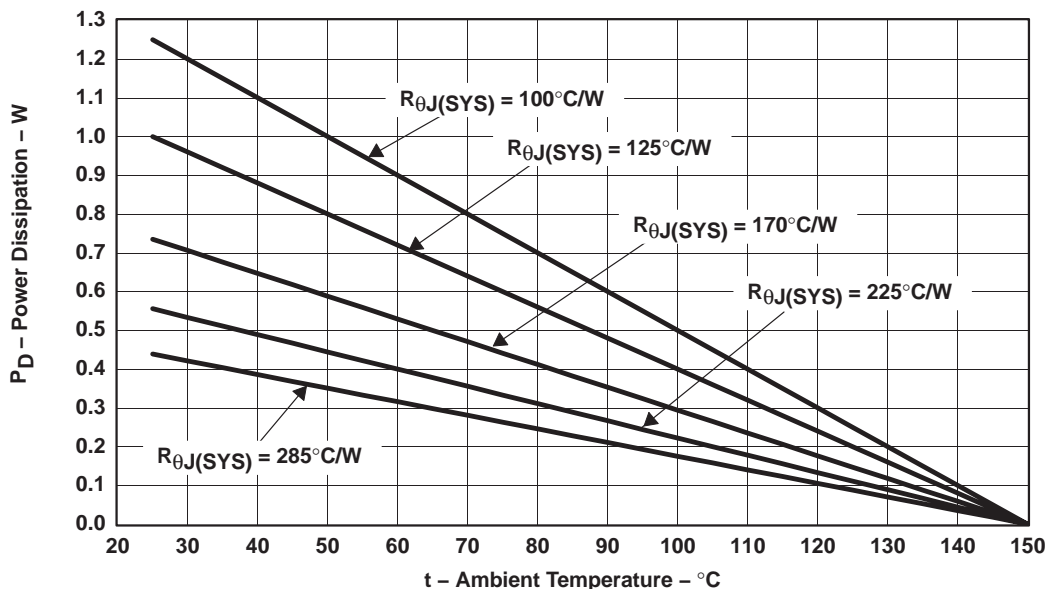
The TACH output can be used to monitor and measure actual fan speed. It may also be used as part of a closed-loop speed control system.

thermal shutdown

The THMC45 provides protection against excessive device temperature with a thermal sensor to monitor the die temperature. In the event that operating or abnormal condition causes the die temperature to exceed $t_{(SD)}$, the thermal shutdown threshold (175°C typical), all output drivers are turned off. When $t_{(SD)}$ has been exceeded, the die temperature must fall below a hysteresis temperature, $t_{(SD_HYS)}$ (15°C typical) before the output drivers are re-enabled.

THERMAL INFORMATION

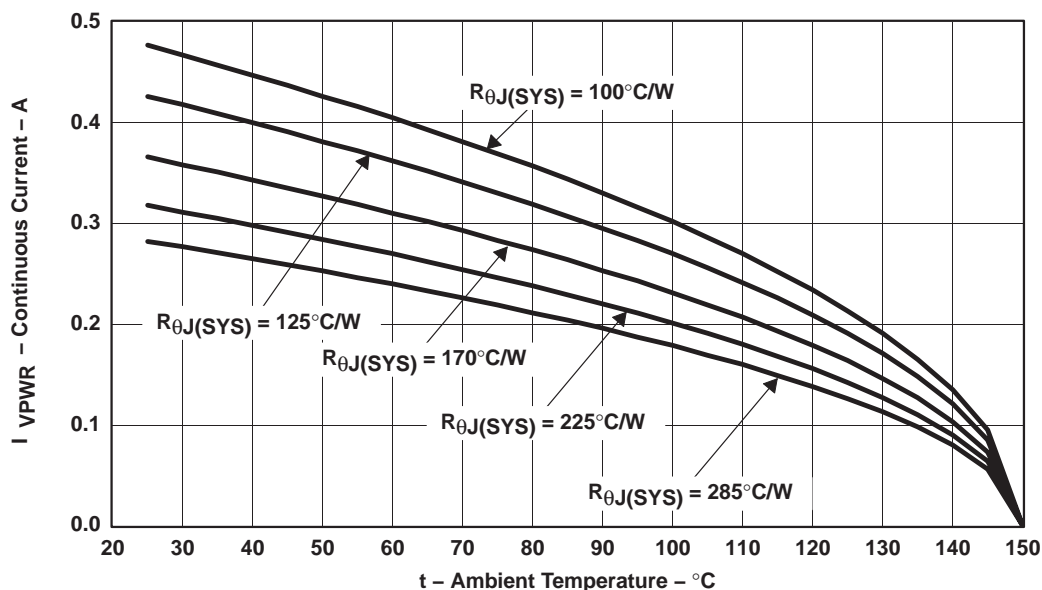
**POWER DISSIPATION
 vs
 AMBIENT TEMPERATURE**



Note: R_{θJ(SYS)} refers to composite thermal impedance provided by the IC package, PCB, and fan housing.

Figure 7

**CONTINUOUS CURRENT
 vs
 AMBIENT TEMPERATURE**



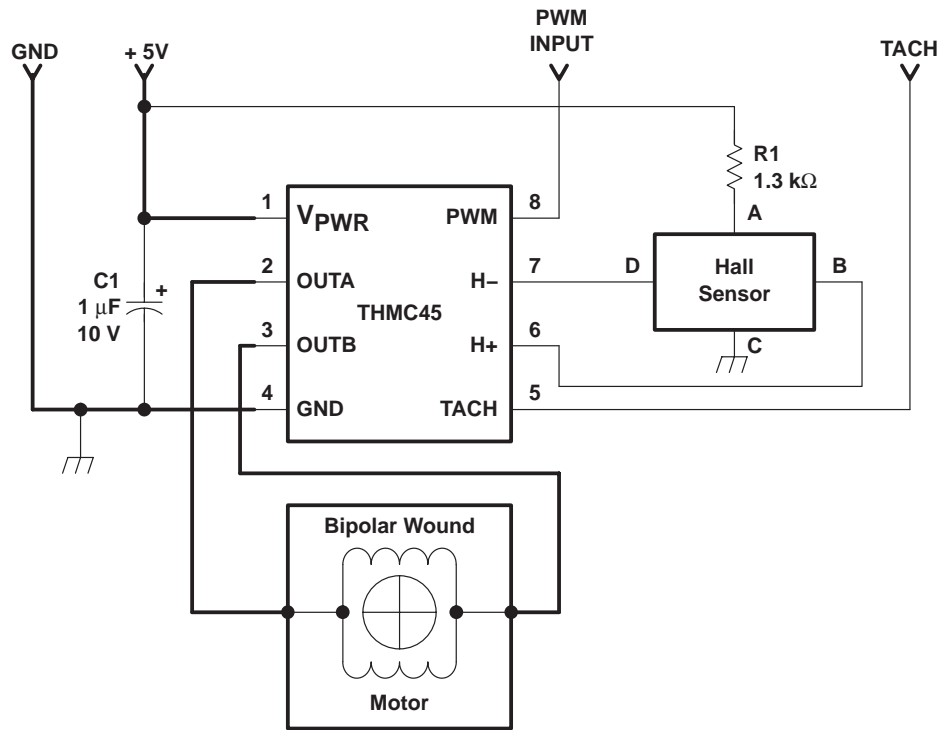
Note: R_{θJ(SYS)} refers to composite thermal impedance provided by the IC package, PCB, and fan housing. Analysis assumes combined high and low-side R_{DSon} = 5.5 Ω.

Figure 8

THMC45
5-V AND 3.3-V DC BRUSHLESS FAN MOTOR DRIVER
WITH SINGLE WIRE CONTROL

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APPLICATION INFORMATION



- NOTES: A. Traces in bold are high current traces.
 B. C1 should be placed as close as possible to terminals 1 and 4.

Figure 9. Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THMC45DGN	OBSOLETE	MSOP-PowerPAD	DGN	8		TBD	Call TI	Call TI	-30 to 80		
THMC45DGNR	OBSOLETE	MSOP-PowerPAD	DGN	8		TBD	Call TI	Call TI	-30 to 80		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

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