Integrated 1394a-2000 OHCI PHY/Link-Layer Controller

FEATURES

- **Fully compliant with *1394 Open Host Controller Interface Specification* (Release 1.1)**
- **Fully compliant with provisions of IEEE Std 1394-1995 for a high-performance serial bus[1] and IEEE Std 1394a-2000**
- **Fully interoperable with FireWire and i.LINK implementations of IEEE Std 1394**
- **Compliant with Intel *Mobile Power Guideline 2000***
- **Full IEEE Std 1394a-2000 support includes: connection debounce, arbitrated short reset, multispeed concatenation, arbitration acceleration, fly-by concatenation, and port disable/suspend/resume**
- **Power-down features to conserve energy in battery-powered applications include: automatic device power down during suspend, PCI power management for link-layer, and inactive ports powered down**
- **Ultralow-power sleep mode**
- **One IEEE Std 1394a-2000 fully compliant cable port at 100M bits/s, 200M bits/s, or 400M bits/**
- **Cable port monitors line conditions for active connection to remote node**
- **Cable power presence monitoring**
- **1.8-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments**
- **Physical write posting of up to three outstanding transactions**
- **PCI burst transfers and deep FIFOs to tolerate large host latency**
- **$\overline{\text{PCI\_CLKRUN}}$ protocol**
- **External cycle timer control for customized synchronization**
- **Extended resume signaling for compatibility with legacy DV components**
- **PHY-link logic performs system initialization and arbitration functions**
- **PHY-link encode and decode functions included for data-strobe bit level encoding**
- **PHY-link incoming data resynchronized to local clock**
- **Low-cost 24.576-MHz crystal provides transmit and receive data at 100M bits/s, 200M bits/s, or 400M bits/s**
- **Node power class information signaling for system power management**
- **Serial ROM interface supports 2-wire serial EEPROM devices**
- **Two general-purpose I/Os**
- **Register bits give software control of contender bit, power class bits, link active control bit, and IEEE Std 1394a-2000 features**
- **Fabricated in advanced low-power CMOS process**
- **PCI and CardBus register support**
- **Isochronous receive dual-buffer mode**
- **Out-of-order pipelining for asynchronous transmit requests**
- **Register access fail interrupt when the PHY SCLK is not active**
- **PCI power-management D0, D1, D2, and D3 power states**
- **Initial bandwidth available and initial channels available registers**
- **$\overline{\text{PME}}$ support per *1394 Open Host Controller Interface Specification***

NOTE: Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.

DESCRIPTION

The Texas Instruments TSB43AB21 device is an integrated 1394a-2000 OHCI PHY/link-layer controller (LLC) device that is fully compliant with the *PCI Local Bus Specification*, the *PCI Bus Power Management Interface Specification*(Revision 1.1), IEEE Std 1394-1995, IEEE Std 1394a-2000, and the *1394 Open Host Controller Interface Specification* (Release 1.1). It is capable of transferring data between the 33-MHz PCI bus and the 1394 bus at 100M bits/s, 200M bits/s, and 400M bits/s. The TSB43AB21 device provides one 1394 port. The TSB43AB21 device also supports the IEEE Std 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI, and it provides plug-and-play (PnP) compatibility. Furthermore, the TSB43AB21 device is compliant with the *PCI Bus Power Management Interface Specification* as specified by the *PC 2001 Design Guide* requirements. The TSB43AB21 device supports the D0, D1, D2, and D3 power states.

The TSB43AB21 design provides PCI bus master bursting, and it is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Because PCI latency can be large, deep FIFOs are provided to buffer the 1394 data.

The TSB43AB21 device provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The TSB43AB21 device also provides multiple isochronous contexts, multiple cacheline burst transfers, and advanced internal arbitration.

An advanced CMOS process achieves low power consumption and allows the TSB43AB21 device to operate at PCI clock rates up to 33 MHz.

The TSB43AB21 PHY-layer provides the digital and analog transceiver functions needed to implement a single-port node in a cable-based 1394 network. The cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB43AB21 PHY-layer requires only an external 24.576-MHz crystal as a reference for the cable ports. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals that control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the integrated LLC for synchronization and is used for resynchronization of the received data.

Data bits to be transmitted through the cable port are received from the integrated LLC and are latched internally in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304M, 196.608M, or 393.216M bits/s (referred to as S100, S200, or S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the twisted-pair B (TPB) cable pair, and the encoded strobe information is transmitted differentially on the twisted-pair A (TPA) cable pair.

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are resynchronized to the local 49.152-MHz system clock and sent to the integrated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB43AB21 device provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1.0 μF.

The line drivers in the TSB43AB21 device operate in a high-impedance current mode and are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. The network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current and other internal operating currents. This current-setting resistor has a value of 6.34 kΩ± 1%.

When the power supply of the TSB43AB21 device is off and the twisted-pair cables are connected, the TSB43AB21 transmitter and receiver circuitry present a high impedance to the cable and do not load the TPBIAS voltage at the other end of the cable.

When the device is in a low-power state (for example, D2 or D3) the TSB43AB21 device automatically enters a low-power mode if the port is inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB43AB21 device disables its internal clock generators and also disables various voltage and current reference circuits, depending on the state of the port (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the ultralow-power sleep mode) is attained when the port is either disconnected or disabled with the port interrupt enable bit cleared.

The TSB43AB21 device exits the low-power mode when bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h is set to 1 or when a port event occurs which requires that the TSB43AB21 device to become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, or a new connection is detected on a nondisabled port). When the TSB43AB21 device is in the low-power mode, the internal 49.153-MHz clock becomes active (and the integrated PHY layer becomes operative) within 2 ms after bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h is set to 1.

The TSB43AB21 device supports hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at OHCI offset A88h. The enhancements include automatic timestamp insertion for transmitted DV and MPEG-formatted streams and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization timestamp for both DV and MPEG CIP formats. The TSB43AB21 device supports modification of the synchronization timestamp field to ensure that the value inserted via software is not stale—that is, the value is less than the current cycle timer when the packet is transmitted.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSB43AB21PDT	NRND	TQFP	PDT	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TSB43AB21PDTG4	NRND	TQFP	PDT	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

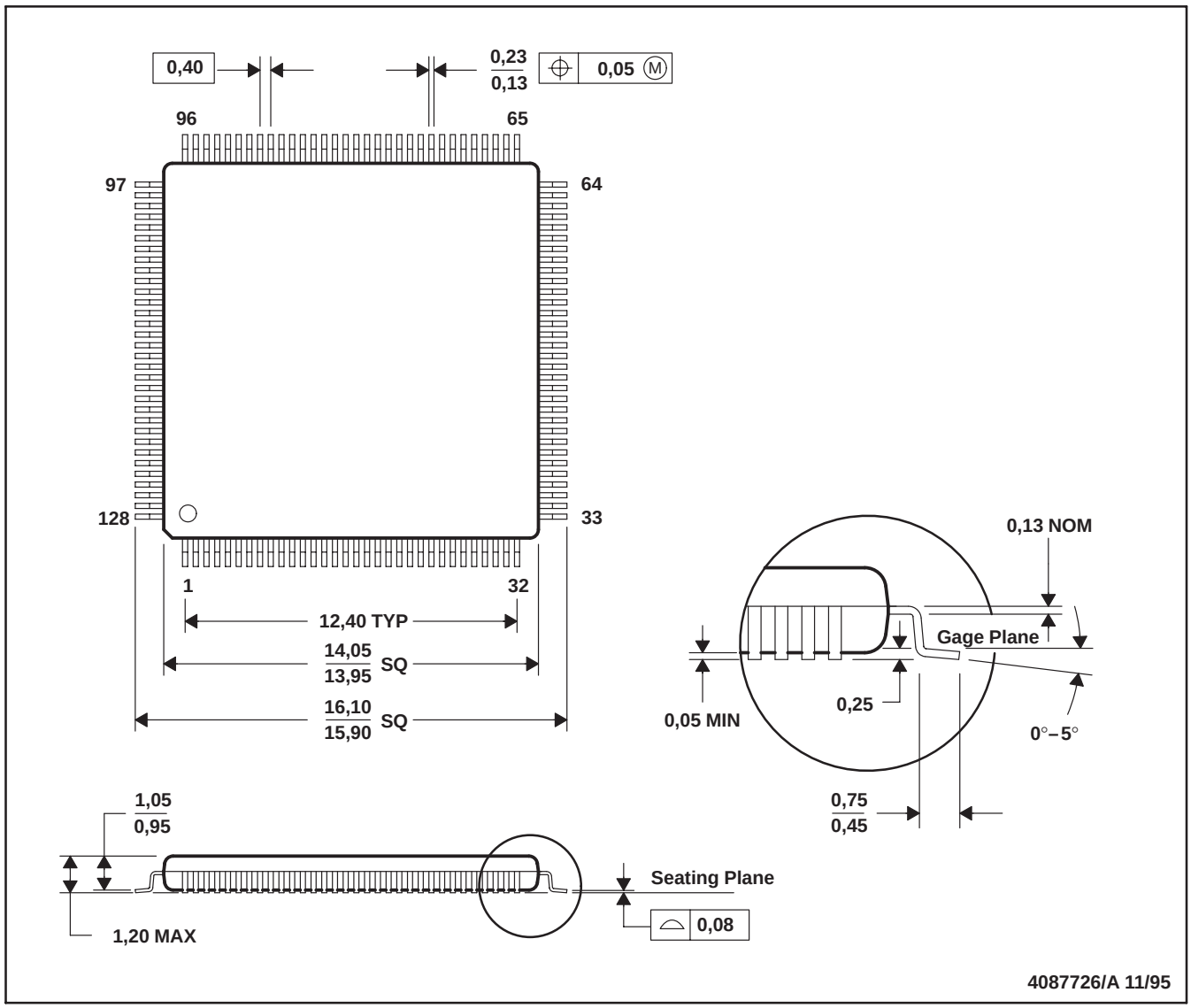
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPQF013 – NOVEMBER 1995

PDT (S-PQFP-G128) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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