OHCI-Lynx™ PCI-Based IEEE 1394 Host Controller

FEATURES

- **3.3-V and 5-V PCI bus signaling**
- **3.3-V supply (core voltage is internally regulated to 1.8 V)**
- **Serial bus data rates of 100M bits/s, 200M bits/s, and 400M bits/s**
- **Physical write posting of up to three outstanding transactions**
- **Serial ROM interface supports 2-wire devices**
- **External cycle timer control for customized synchronization**
- **PCI burst transfers and deep FIFOs to tolerate large host latency**
- **Two general-purpose I/Os**
- **Fabricated in advanced low-power CMOS process**
- **Packaged in 100-terminal LQFP (PZT)**
- **$\overline{\text{PCI_CLKRUN}}$ protocol**

DESCRIPTION

The Texas Instruments TSB12LV26 device is a PCI-to-1394 host controller compliant with the *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Std 1394-1995, and *1394 Open Host Controller Interface Specification*. The chip provides the IEEE 1394 link function and is compatible with 100M bits/s, 200M bits/s, and 400M bits/s serial bus data rates.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI and provides plug-and-play (PnP) compatibility. Furthermore, the TSB12LV26 device is compliant with the *PCI Bus Power Management Interface Specification*, per the *PC 99 Design Guide* requirements. TSB12LV26 device supports the D0, D2, and D3 power states.

The TSB12LV26 design provides PCI bus master bursting and is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Since PCI latency can be large, deep FIFOs are provided to buffer 1394 data.

The TSB12LV26 device provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The TSB12LV26 device also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus-holding buffers on the PHY/link interface.

An advanced CMOS process achieves low power consumption and allows the TSB12LV26 device to operate at PCI clock rates up to 33 MHz.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TSB12LV26PZT	ACTIVE	TQFP	PZT	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
TSB12LV26PZTG4	ACTIVE	TQFP	PZT	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TSB12LV26 :

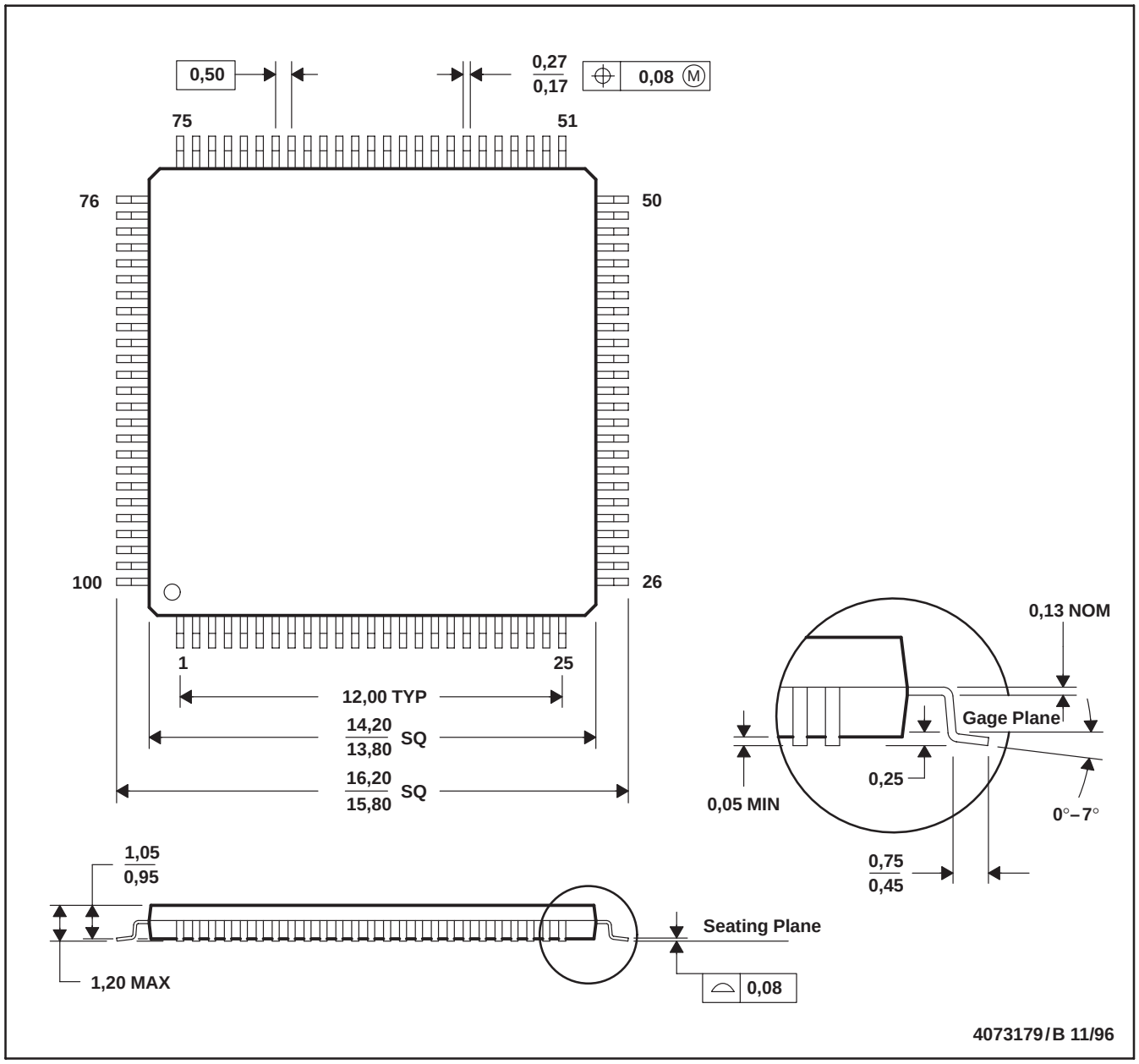
- Enhanced Product: TSB12LV26-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

MTQF012B – OCTOBER 1994 – REVISED DECEMBER 1996

PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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