TL16PNP200
STANDALONE PLUG-AND-PLAY (PnP) CONTROLLER

SLLS229A − NOVEMBER 1995 − REVISED APRIL 1996

- **PnP Card Autoconfiguration Sequence Compliant**
- **Satisfies All Requirements for Qualifying for the Windows 95™ Logo**
- **Supports up to Five Logical Devices**
- **24-Bit Memory Address Decoding and 16-Bit I/O Address Decoding With Programmable (1, 2, 4, 8, 16, 32, 64) I/O Block Size**
- **Device Interrupt Mapping to Any of the 11 Interrupt Request (IRQ) Signals on Industry Standard Architecture (ISA) Bus**
- **Direct Memory Access (DMA) Support For Two Logical Devices with Configurable DMA Channel Connection**
- **Configurable $\overline{\text{OEN}}$ Signals That Can Be Used to Enabled Logical Device Transceivers**
- **Simple 3-Terminal Interface to Serial EEPROM 2K/4K ST93C56/66 or Equivalent for Resource Data Storage and Power-Up Defaults, As Well As General Board-Specific Data**
- **Default Configuration Loading and Activation Upon Power-up for Non-PnP Systems**
- **Two Modes of Operation That Satisfy A Wide Range of Applications**
- **Direct Connection to ISA/AT Bus Without Need for Buffers**
- **5-V Power Supply Operation**
- **Available in 80-pin PQFP**

description

The TL16PNP200 is an ISA plug-and-play (PnP) controller that provides autoconfiguration capability to ISA cards according to the ISA PnP 1.0a specification. It interfaces to a serial EEPROM where card resource requirements and power-up defaults are stored. On power up, the controller loads the default configuration from the EEPROM making it ready for operation (non-PnP systems) or to be configured by the PnP configuration process (PnP-capable systems). During configuration mode, the PnP autoconfiguration process reads the card resource requirements, configures the card by writing to the TL16PNP200 configuration registers, activates the device, and removes it from the configuration mode. Thereafter, the TL16PNP200 routes all ISA transactions between the card and the ISA bus. The TL16PNP200 operates in one of two modes. In mode 0, the device supports two logical devices with memory, I/O, interrupt, and DMA resources for each device. In mode 1, the device supports five logical devices with I/O and interrupt resources for all logical devices and DMA resources for two of the five logical devices; there is no memory support in mode 1. The TL16PNP200 provides interface signals to allow on-board logic access to the serial EEPROM.

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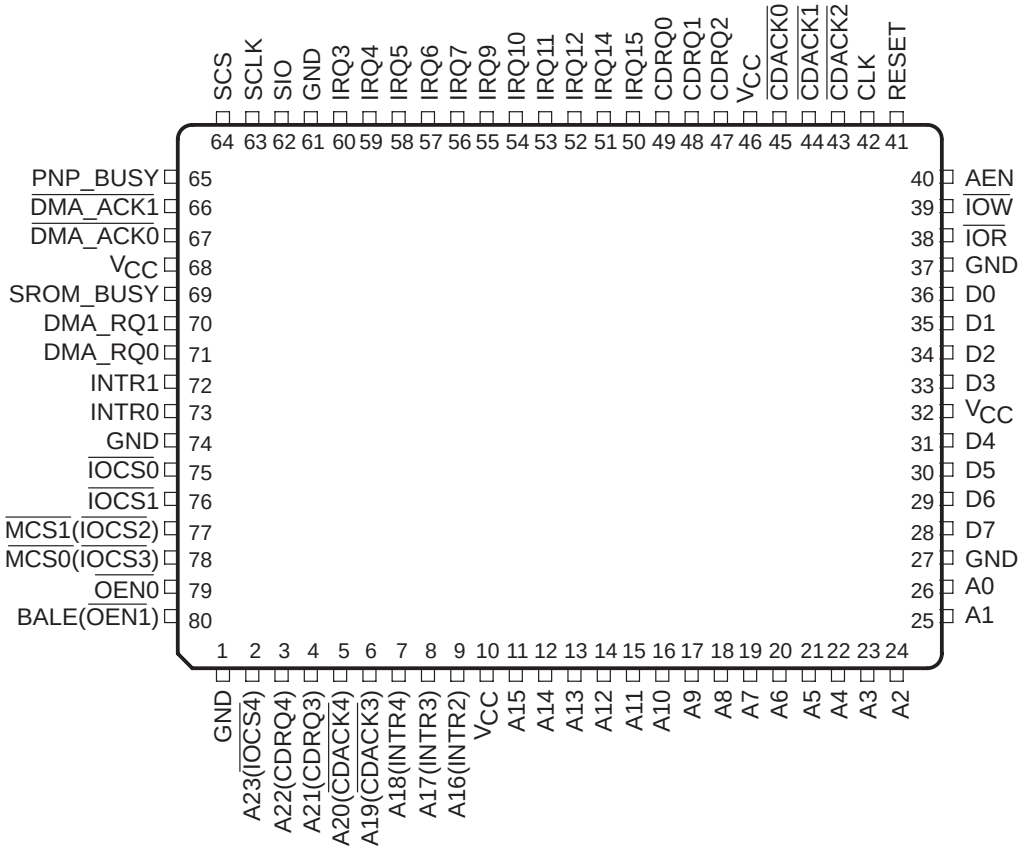
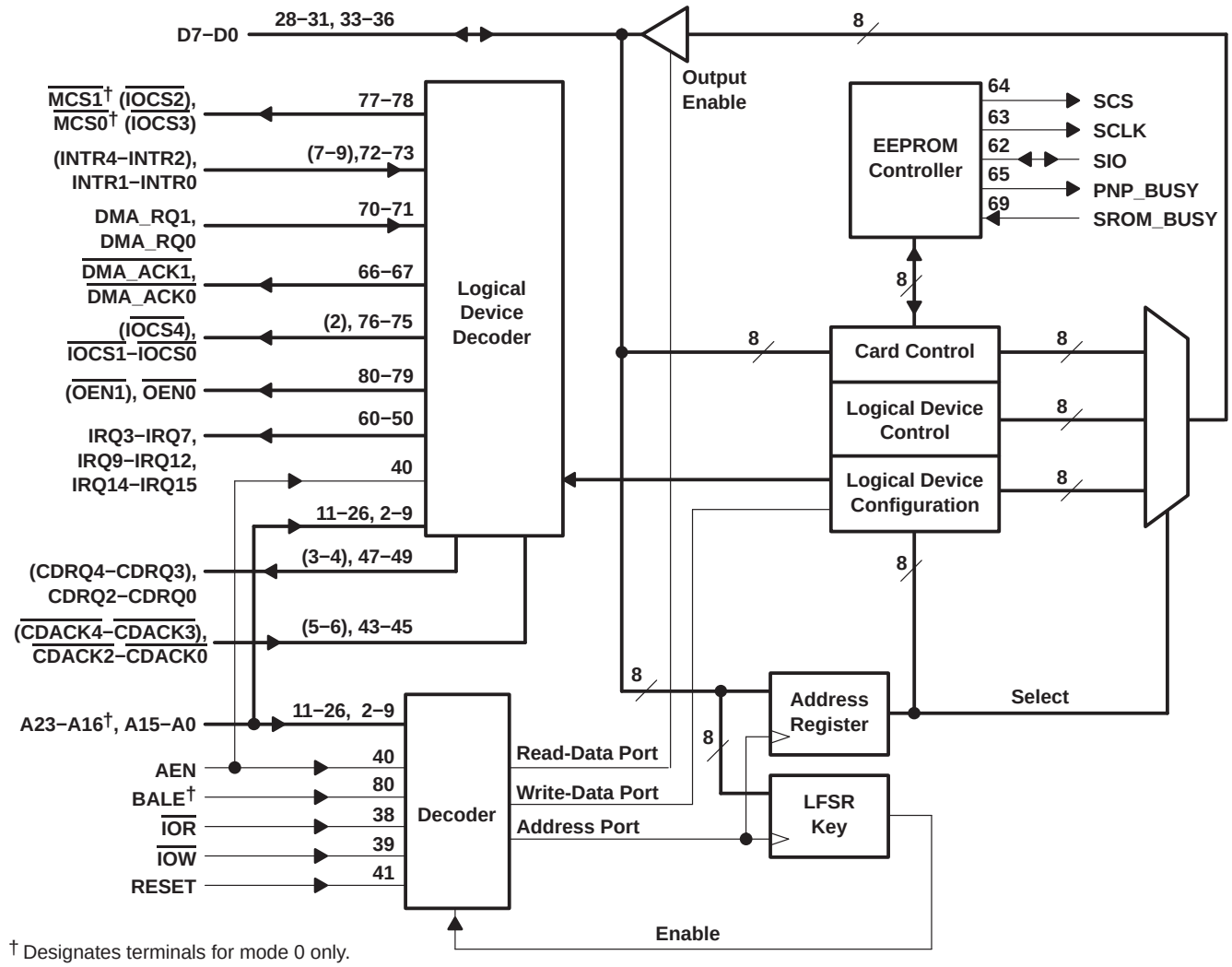
PH PACKAGE
(TOP VIEW)



functional block diagram



† Designates terminals for mode 0 only.

NOTE A: Terminals in parentheses are for mode 1 operation only.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A15-A0	11-26	I	Address. A15-A0 connects to ISA address bits SA15-SA0.
A16 (INTR2),† A17 (INTR3),† A18 (INTR4)†	9-7	I	Address (Interrupt). In Mode 0, A16−A18 should be connected to ISA address bits SA16, LA17, and LA18 respectively. In Mode 1, INTR2−INTR4 are interrupt requests from logical devices 2, 3, and 4 respectively.
A19 ($\overline{\text{CDACK3}}$),† A20 (CDACK4)†	6, 5	I	Address (DMA acknowledge). In Mode 0, A19−A20 should be connected to ISA address bits LA19 and LA20. In Mode 1, CDACK3 and CDACK4 are configurable data acknowledge signals and should be connected to the ISA DACK signals of the selected DMA channels as specified by DMA mapping in the power-up defaults.
A21 (CDRQ3),† A22 (CDRQ4)†	4, 3	I/O	Address (DMA request). In Mode 0, A21 and A22 are inputs that should be connected to ISA address bits LA21 and LA22. In Mode 1, CDRQ3 and CDRQ4 are configurable data request outputs and should be connected to the ISA DRQ signals of the selected DMA channels as specified by DMA mapping in the power-up defaults.
A23 ($\overline{\text{IOCS4}}$)†	2	I/O	Address (I/O chip select). In Mode 0, A23 is an input that should be connected to ISA address bit LA23. In Mode 1, $\overline{\text{IOCS4}}$ is a I/O chip select output for logical device 4.
AEN	40	I	ISA address enable. During DMA operation, AEN is an active signal that prevents the controller from generating an I/O chip select.
BALE ($\overline{\text{OEN1}}$)†	80	I/O	ISA bus address latch enable (output enable). In Mode 0, BALE is an ISA input which is used to latch the upper address. In Mode 1, $\overline{\text{OEN1}}$ is an output enable and can be configured to respond to I/O read operations to any logical device, which can use it to enable its transceivers.
$\overline{\text{CDACK0}}$, $\overline{\text{CDACK1}}$, $\overline{\text{CDACK2}}$	45-43	I	Configurable ISA DMA acknowledge. $\overline{\text{CDACK0}}$ − $\overline{\text{CDACK2}}$ should be connected to the ISA $\overline{\text{DACK}}$ signals of the selected DMA channels as specified by DMA mapping in the power-up defaults.
CDRQ0, CDRQ1, CDRQ2	49-47	O	Configurable ISA DMA data request. CDRQ0−CDRQ2 should be connected to the ISA DRQ signals of the selected DMA channels as specified by DMA mapping in the power-up defaults.
CLK	42	I	10-22 MHz clock. CLK is an input from the OSC signal on the ISA bus.
D0-D7	31-28, 36-33	I/O	8-bit ISA data
$\overline{\text{DMA\_ACK0}}$, $\overline{\text{DMA\_ACK1}}$	67, 66	O	DMA acknowledge. $\overline{\text{DMA\_ACK0}}$ and $\overline{\text{DMA\_ACK1}}$ are used for DMA acknowledge to logical devices 0 and 1.
DMA_RQ0, DMA_RQ1	71, 70	I	DMA requests. DMA_RQ0 and DMA_RQ1 are used for DMA requests from logical devices 0 and 1.
GND	1, 27, 37, 61, 74		Ground (0 V). All terminals must be tied to GND for proper operation.
INTR0, INTR1	73, 72	I	Interrupt requests. INTR0 and INTR1 generate interrupt requests from logical devices 0 and 1.
$\overline{\text{IOCS0}}$, $\overline{\text{IOCS1}}$	75, 76	O	I/O chip select outputs to logical devices 0 and 1. The address decoder decodes the full 16-bit I/O address and generates the I/O chip select signals based on the selected I/O block size.
$\overline{\text{IOR}}$	38	I	ISA I/O read.
$\overline{\text{IOW}}$	39	I	ISA I/O write.
IRQ3−IRQ7, IRQ9−IRQ12, IRQ14, IRQ15	50-60	O	ISA Interrupt request. These signals should be connected to the corresponding ISA IRQ signals.
$\overline{\text{MCS0}}$($\overline{\text{IOCS3}}$),† $\overline{\text{MCS1}}$($\overline{\text{IOCS2}}$)†	78, 77	O	Memory chip select (I/O chip select). In Mode 0, $\overline{\text{MCS0}}$ and $\overline{\text{MCS1}}$ are the memory chip select outputs for logical devices 0 and 1. A 24-bit memory address is decoded to generate the memory chip select signals based on the selected memory block size. In Mode 1, $\overline{\text{IOCS3}}$ and $\overline{\text{IOCS2}}$ are the I/O chip select outputs for logical devices 3 and 2.
$\overline{\text{OEN0}}$	79	O	Output enable. $\overline{\text{OEN0}}$ can be configured to respond to I/O read operations to any logical device, which can use it to enable its transceivers.

† Terminal names in parenthesis indicate when the device is in mode 1 operation.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PNP_BUSY	65	O	Plug-and-play busy. PNP_BUSY signal requests access to the EEPROM and is asserted during PNP configuration. On-board logic uses this signal to determine when it can access the EEPROM. This signal can also be used as a soft reset.
RESET	41	I	Reset. When active (high), RESET clears most logical device registers and puts the TL16PNP200 in the wait-for-key state. All configuration registers are loaded with their power-up defaults, and card select number (CSN) is reset to 0.
SCLK	63	O	Serial clock (3-state output path). SCLK controls the serial bus timing for address and data. A 100 µA pulldown transistor is connected internally to this terminal.
SCS	64	O	EEPROM chip select. SCS controls the activity of the EEPROM. A 100 mA pulldown transistor is connected internally to this terminal.
SIO	62	I/O	Serial input/output. SIO is a 3-state bidirectional EEPROM I/O data path. A 100 µA pulldown transistor is connected internally to this terminal .
SROM_BUSY	69	I	Serial EEPROM busy. SROM_BUSY is asserted by on-board logic during its access to the EEPROM.
V_{CC}	10,32, 46,68		5-V supply voltage.

detailed description

modes of operation

The TL16PNP200 operates in one of two modes: Mode 0 or Mode1. The mode is selected by setting the mode bit in the power-up defaults (see defaults format section).

Mode 0:

- Supports two logical devices
- Supports memory, I/O, IRQ, and DMA for each of the two logical devices
- Routes device DMA request to three DMA channels that can be connected to any three DMA channels on the ISA bus
- Has one configurable $\overline{\text{OEN}}$ signal

Mode 1:

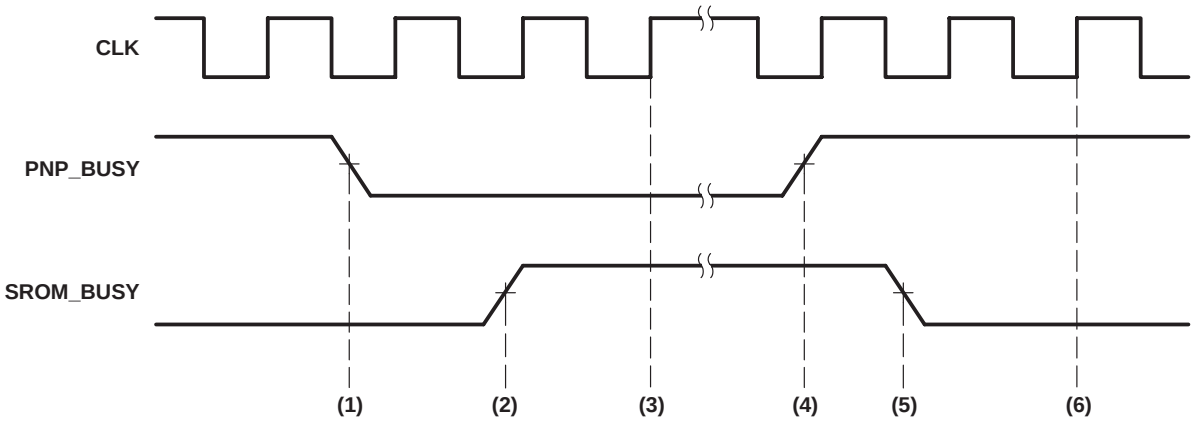
- Supports five logical devices
- Supports I/O and IRQ for the five logical devices and supports DMA for two logical devices
- Routes device DMA requests to five DMA channels that can be connected to any five DMA channels on the ISA bus
- Has two configurable $\overline{\text{OEN}}$ signals

EEPROM interface

This device interfaces to a SGS Thomson 2 kbit ST93C56, or 4 kbit ST93C66 compatible EEPROM. In addition to the three EEPROM signals (SCS, SCLK, and SIO), the two interface signals (PNP_BUSY and SROM_BUSY) are provided to allow optional on-board logic access to the EEPROM. On power-up or reset, the TL16PNP200 gains access to the EEPROM and asserts the PNP_BUSY output high indicating that the device is in the configuration mode and is accessing the EEPROM. After the configuration is complete, the device goes to the wait-for-key state, puts SIO, SCLK, and SCS outputs into a high impedance state (these signals are pulled down internally), and deasserts the PNP_BUSY signal. On-board logic can assert to the SROM_BUSY signal at any time to request access to the EEPROM, then SROM_BUSY can start accessing the EEPROM after 2 clock cycles when PNP_BUSY is deasserted; otherwise, SROM_BUSY must wait until PNP_BUSY is deasserted. In a similar manner, the device uses the PNP_BUSY signal to request access to the EEPROM. In that case on-board logic should stop accessing the EEPROM and deassert SROM_BUSY, after which the device starts accessing the EEPROM (see Figure 1). If on-board logic does not need to access the EEPROM, SROM_BUSY should be tied to ground and PNP_BUSY should be left unconnected. All unused inputs should be tied to the inactive state, and all unused outputs should be left open.

NOTE

If the TL16PNP200 enters the configuration mode again and leaves the wait-for-key state, the wake command generates a read transaction from address 0x0E, which is the beginning of the card resource data.



The following steps reflect the EEPROM interface:

(1) The device finishes accessing the EEPROM.
(2) On-board logic requests access to the EEPROM (can be any time).
(3) On-board logic starts accessing the EEPROM since PNP_BUSY is low.
(4) The device requests access to the EEPROM.
(5) On-board logic relinquishes the EEPROM.
(6) The device starts accessing the EEPROM.

Figure 1. EEPROM Interface Signals

default format

On power up or reset, the TL16PNP200 starts generating read operations to the EEPROM. Each read transaction consists of read opcode, address, and data cycles (see EEPROM section). The data cycle is comprised to 16-bits. EEPROM addresses 0x00 through 0x0D store the power-up defaults. These defaults include the PnP configuration register defaults, I/O block size, DMA mapping, and OEN configuration. Table 1 is a description of the format for storing the defaults in the EEPROM.

Table 1. Default Format

ADDRESS	DESCRIPTION
0x00	LD0 Memory base address bits 23-8 (Note 1)
0x01	LD1 Memory base address bits 23-8 (Note 1)
0x02	LD0 Memory upper address bits 23-8 (Note 1)
0x03	LD1 Memory upper address bits 23-8 (Note 1)
0x04	LD0 I/O Base address bits 15-0
0x05	LD1 I/O Base address bits 15-0
0x06	LD2 I/O Base address bits 15-0 (Note 2)
0x07	LD3 I/O Base address bits 15-0 (Note 2)
0x08	LD4 I/O Base address bits 15-0 (Note 2)
0x09	Bits 15-13: LD0 I/O block size, bits 12-10: LD1 I/O block size, bits 9-7: LD2 I/O block size, bits 6-4: LD3 I/O block size, bits 3-1: LD4 I/O block size (Note 3)
0x0A	Bits 15-12: LD0 IRQ level, bits 11-8: LD1 IRQ level, bits 7-4: LD2 IRQ level, bits 3-0: LD3 IRQ level (Note 4)
0x0B	Bits 15-12: LD4 IRQ level, bits 11-9 LD0: DMA channel, bits 8-6: LD1 DMA channel (Note 5)
0x0C	Bit 15: LD0 active, bit 14: LD1 active, bit 13: LD2 active, bit 12: LD3 active, bit 11: LD4 active, bits 10-8: $\overline{\text{OEN0}}$ configuration, bits 7-5: $\overline{\text{OEN1}}$ configuration, bit 4: mode (Note 6)
0x0D	Bits 14-12: DMA 4 mapping, bits 11-9: DMA 3 mapping, bits 8-6: DMA 2 mapping, bits 5-3: DMA 1 mapping, bits 2-0: DMA 0 mapping (Note 7)

NOTES: 1. In Mode 1, these fields are ignored.
2. In Mode 0, these fields are ignored.
3. Bit 0 is unused, and in Mode 0 bits 9-1 are ignored.
4. In Mode 0 bits 7-0 are ignored.
5. Bits 5-0 are unused, and in Mode 0 bits 15-12 are ignored.
6. Bits 3-0 are unused, and in Mode 0 bits 13-11 and bits 7-5 are ignored.
7. Bit 15 is unused, and in Mode 0 bits 14-9 are ignored.

default format (continued)

The formats for the coded fields are as follows:

Table 2. I/O Block Size

CODE	BLOCK SIZE	ADDRESS BITS DECODED
000	1 byte	15-0
001	2 bytes	15-1
010	4 bytes	15-2
011	8 bytes	15-3
100	16 bytes	15-4
101	32 bytes	15-5
110	64 bytes	15-6

Table 3. OEN0 Configuration - Mode 0

CODE	LOGICAL DEVICE
000	LD0
001	LD1
010	LD0 or LD1

Table 4. OEN0 and OEN1 Configuration - Mode 1

CODE	LOGICAL DEVICE
000	LD0
001	LD1
010	LD2
011	LD3
100	LD4

The IRQ level field is the IRQ level number (e.g. 0011 for IRQ3, 0100 for IRQ4, ... etc.), and the DMA channel field is the DMA channel number (e.g. 000 for DMA channel 0, 001 for DMA channel 1, ... etc.). The LDn Active bits should be set to 1 when device n is required to be active on power-up or after reset, otherwise it is cleared to 0. The mode bit should be 0 for Mode 0 operation and 1 for Mode 1 operation.

The DMA mapping fields tell the TL16PNP200 which ISA DMA channels are connected to the device. For example, in Mode 0 any three ISA DMA channels can be connected to the device. When DMA channels 0, 3, and 5 are connected to CDRQ0/$\overline{\text{CDACK0}}$, CDRQ1/$\overline{\text{CDACK1}}$, and CDRQ2/$\overline{\text{CDACK2}}$, respectively, then DMA 0 mapping field should be 000, DMA 1 mapping field should be 011, and DMA 2 mapping field should be 101.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (See Note 8) . . . . . −0.5 V to 6 V
Input voltage range, V_I: Standard . . . . . −0.5 V to V_{CC} +0.5 V
Fail safe . . . . . −0.5 V to 6.5 V
Output voltage range, V_O: Standard . . . . . −0.5 V to V_{CC} +0.5 V
Fail safe . . . . . −0.5 V to 6.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 9) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 8) . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 8. This applies for external output and bidirectional buffers. V_O > V_{CC} does not apply to fail-safe terminals.·
9. This applies for external input and bidirectional buffers. V_I > V_{CC} does not apply to fail-safe terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −4 mA (see Note 10)	V_{CC}−0.8			V
		I_{OH} = −12 mA (see Note 11)	V_{CC}−0.8			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA (see Note 10)			0.5	V
		I_{OL} = 12 mA (see Note 11)			0.5	
I_I	Input current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±1	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Pullup transistors and pulldown transistors are off			±10	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, All inputs toggle, No load on outputs, T_A = 25°C, f = 22 MHz,		25		mA
$C_{i(CLK)}$	Clock input capacitance			5		pF
f_{CLK}	Clock frequency		10		22	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 10. These parameters apply for all outputs except D7−D0, IRQ and CDRQ outputs.
11. These parameters only apply for D7−D0, IRQ , and CDRQ outputs.

serial EEPROM clock timing requirements over recommended ranges of supply voltage and operating free-air temperature

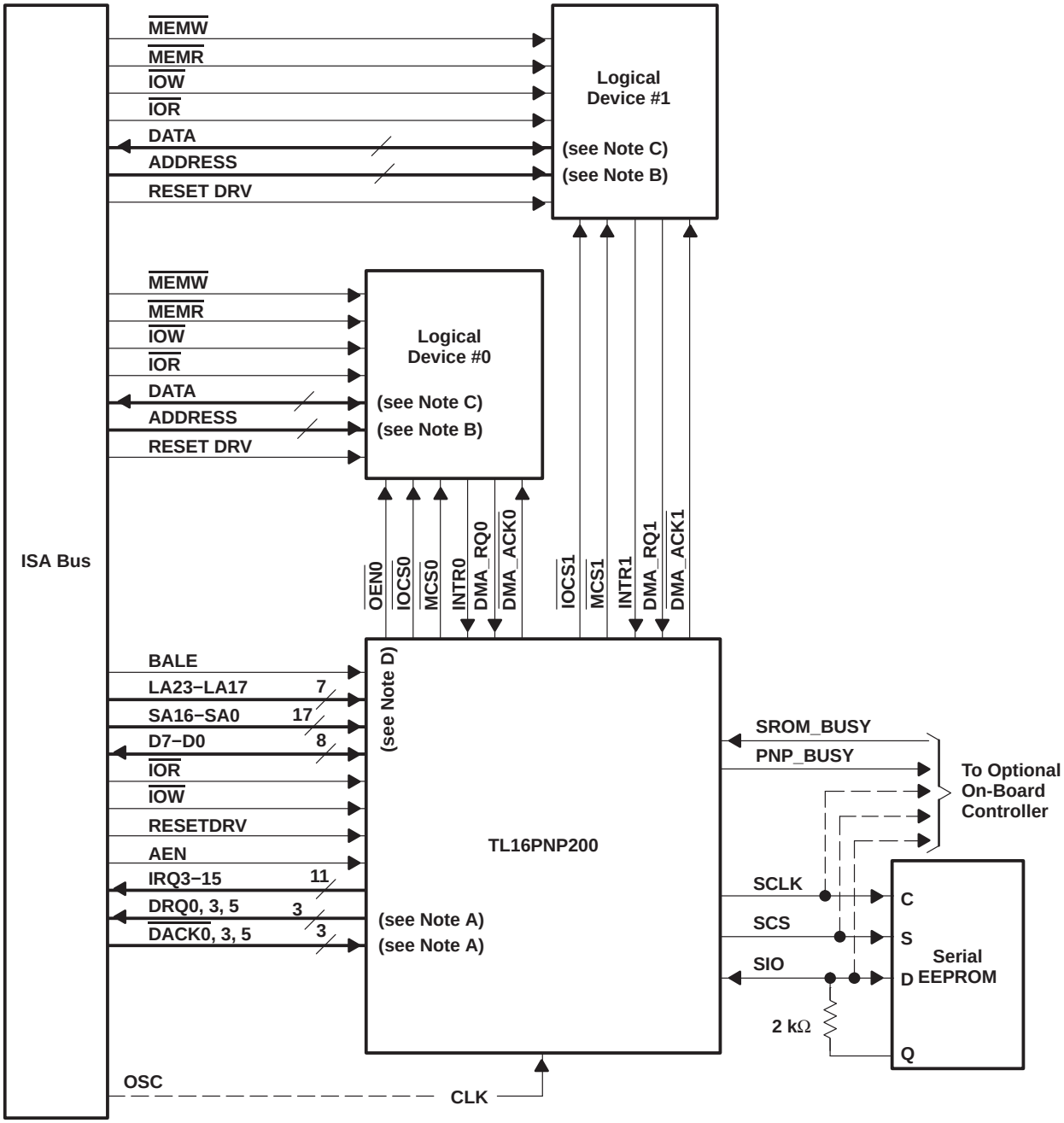
PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SCLKH)}$	Pulse duration, SCLK high to low (see Note 12)	t_{CHCL}	See Figure 9	250		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low to high (see Note 12)	t_{CLCH}		250		ns
f_{CLK}	SCLK clock frequency (see Note 13)			0.3	0.68	MHz
t_{d1}	Delay time, CS high to SCLK high	t_{SHCH}	See Figure 9	50		ns
t_{d2}	Delay time, SIO input valid to SCLK high	t_{DVCH}	See Figures 9 and 10	100		ns
t_{pd1}	Propagation delay time, SCLK high to input level transition	t_{CHDX}		100		ns
t_{pd2}	Propagation delay time, SCLK high to output valid	t_{CHQV}	See Figure 10		500	ns
t_{pd3}	Propagation delay time, SCLK low to CS transition	t_{CLSL}			2	clock period
t_{d3}	Delay time, CS low to output Hi-Z	t_{SLQZ}			100	ns

NOTES: 12. The ST93C56 chip select, S, must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles per the ST93C56 specification.
13. The SCLK signal is attained by dividing the internal CLK signal frequency by 32.

system timing requirements and switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, write strobe ($\overline{IOW}$)	t_{WR}	6		2		clock periods
t_{w2}	Pulse duration, read strobe ($\overline{IOR}$)	t_{RD}	5		3		clock periods
t_{w3}	Pulse duration, reset	t_{RST}			1		µs
t_{su1}	Setup time, data (D7-D0) valid before $\overline{IOW}$↑	t_{DS}	6		10		ns
t_{su2}	Setup time, address (A23-A0) valid before $\overline{IOW}$↑	t_{AS}	6		10		ns
t_{su3}	Setup time, address (A23-A0) valid before BALE↓	t_{BALE}	6		10		ns
t_{h1}	Hold time, data (D7-D0) valid after $\overline{IOW}$↑	t_{DH}	6		5		ns
t_{h2}	Hold time, address (A15-A0) valid after $\overline{IOW}$↑	t_{AH}	6		5		ns
t_{d4}	Delay time, address (A15-A0) valid to $\overline{IOCSn}$↓	t_{IOCSf}	5			18	ns
t_{d5}	Delay time, address (A15-A0) invalid to $\overline{IOCSn}$↑	t_{IOCSr}	5			14	ns
t_{d6}	Delay time, address (A23-A0) valid to $\overline{MCSn}$↓	t_{MCSf}	6			18	ns
t_{d7}	Delay time, address (A23-A0) invalid to $\overline{MCSn}$↑	t_{MCSr}	6			14	ns
t_{d8}	Delay time, $\overline{IOR}$↓ to $\overline{OENn}$↓	t_{OENf}	5			15	ns
t_{d9}	Delay time, $\overline{IOR}$↑ to $\overline{OENn}$↑	t_{OENr}	5			10	ns
t_{d10}	Delay time, $\overline{IOR}$↓ to data (D7-D0) valid	t_{VD}	5	After 2-1/2 clock periods		25	ns
t_{d11}	Delay time, $\overline{IOR}$↑ to data (D7-D0) floating	t_{HZD}	5			20	ns
t_{d12}	Delay time, INTRn↑ to IRQm↑	t_{IRQr}	7			12	ns
t_{d13}	Delay time, INTRn↓ to IRQm↓	t_{IRQf}	7			14	ns
t_{d14}	Delay time, DMA_RQn↑ to CDRQm↑	t_{DRQr}	8			9	ns
t_{d15}	Delay time, DMA_RQn↓ to CDRQm↓	t_{DRQf}	8			10	ns
t_{d16}	Delay time, $\overline{CDACKm}$↓ to $\overline{DMA\_ACKn}$↓	t_{DACKf}	8			16	ns
t_{d17}	Delay time, $\overline{CDACKm}$↑ to $\overline{DMA\_ACKn}$↑	t_{DACKr}	8			12	ns

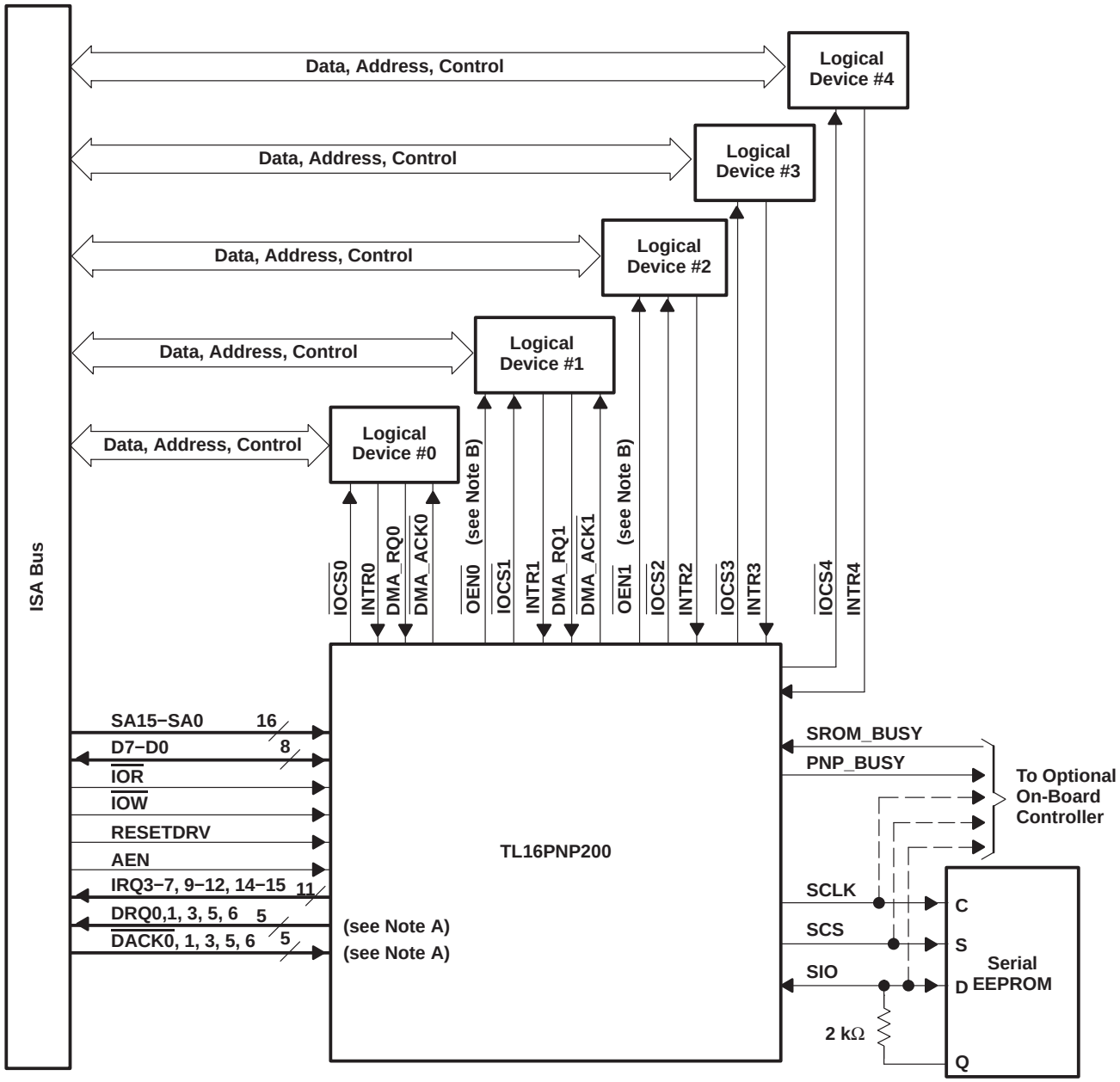
APPLICATION INFORMATION



NOTES: A. Any three DMA channels can be used.
B. Number of address lines depends on the programmed I/O and memory block sizes.
C. Number of data lines is logical device dependent.
D. $\overline{\text{OEN0}}$ can be used with either logical device.

Figure 2. TL16PNP200 Application − Mode 0

APPLICATION INFORMATION



NOTES: A. Any five DMA channels can be used.
B. $\overline{\text{OEN0}}$ and $\overline{\text{OEN1}}$ can be used with any two logical devices.

Figure 3. Typical Application − Mode 1

APPLICATION INFORMATION

on-board EEPROM programming

This section describes a simple approach to programming the resource EEPROM in an expansion board that uses the TL16PNP200. This approach involves utilizing a readily available standard EEPROM programmer and a ribbon cable in addition to minor additions to the expansion board.

A connector is needed on the expansion board to provide access to the EEPROM signals as shown in Figure 4. Two jumper wires are used to isolate the EEPROM during programming. Power to the board must be removed before programming. To isolate the V_{CC} of the EEPROM from the board V_{CC}, Jumper 2 should be disconnected. This disables the PnP controller and prevents it from driving the EEPROM inputs. Jumper 1 should also be taken off during programming to isolate the D input and Q output. The PnP controller uses a single pin for the EEPROM data input and output.

The ribbon cable plugs into the on-board connector on one end, and the other end has a DIP connector that plugs into the EEPROM programmer.

Programming the EEPROM is achieved by connecting the unpowered board to the programmer using the ribbon cable, removing the jumper wires, and then using the software supplied with the programmer. After programming is complete, the jumper wires are reattached and the board is now ready for testing.

hardware required for programming an expansion board EEPROM

The hardware required for programming an expansion board EEPROM is listed in the following bulleted list and shown in Figure 4.

- EEPROM programmer
- Ribbon cable with connectors
- On-board connector and two jumper wires

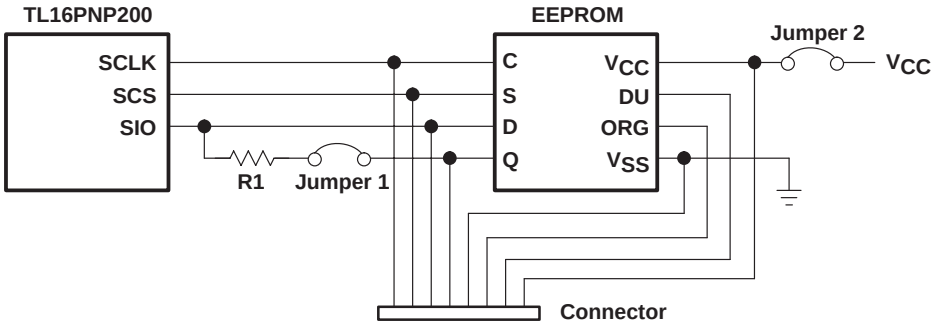


Figure 4. Programming an Expansion Board EEPROM

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PARAMETER MEASUREMENT INFORMATION

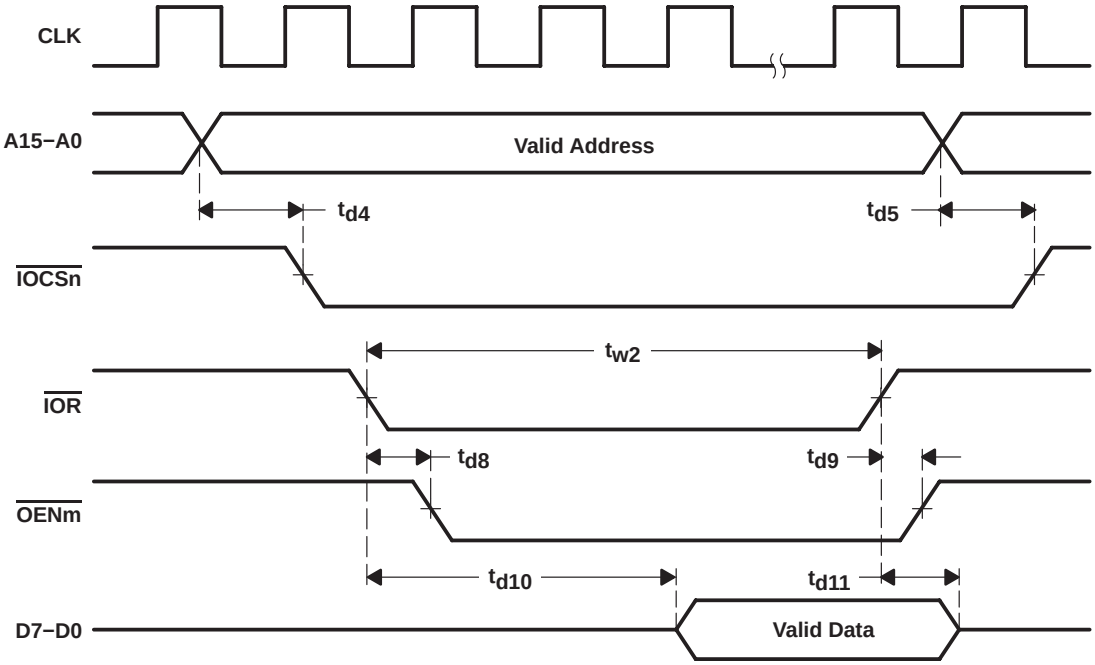


Figure 5. Read Cycle and I/O Chip Select Timing

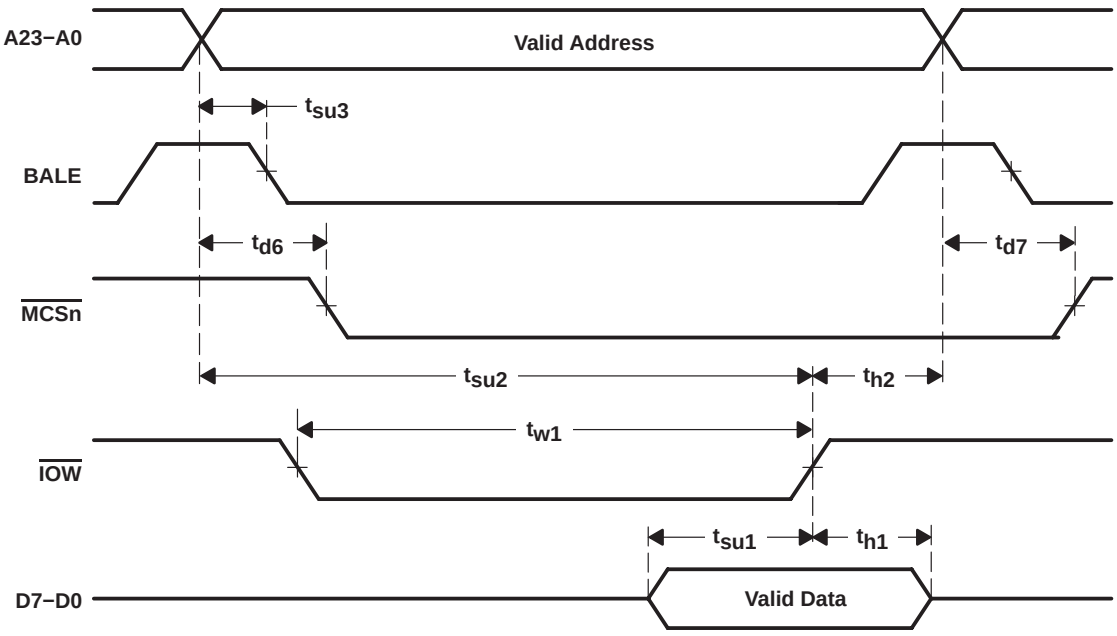


Figure 6. Write Cycle and Memory Chip Select Timing

PARAMETER MEASUREMENT INFORMATION

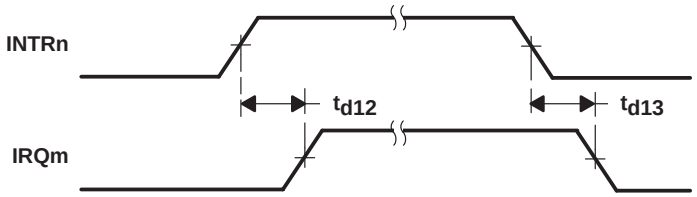


Figure 7. Interrupt Timing

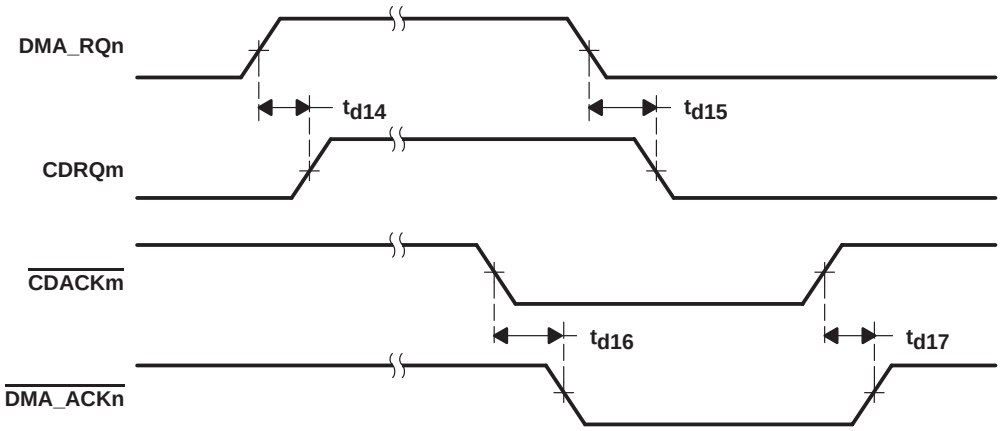


Figure 8. DMA Signal Timing

PRINCIPLES OF OPERATION

PnP card configuration sequence

The PnP logic is quiescent on power up and must be enabled by software.

1. The initiation key places the PnP logic into configuration mode through a series of predefined writes to the ADDRESS port (see autoconfiguration ports section).
2. A serial identifier is accessed in bit-sequence and used to isolate the ISA cards. Seventy-two READ_DATA port reads are required to isolate each card.
3. Once isolated, a card is assigned a CSN that is later used to select the card. This assignment is accomplished by programming the CSN register.
4. The PnP software then reads the resource-data structure on each card. When all resource capabilities and demands are known, a process of resource arbitration is invoked to determine resource allocation for each card.
5. All PnP cards are then activated and removed from the configuration mode. This activation is accomplished by programming the ACTIVE register.

PnP autoconfiguration ports

Three 8-bit ports (see Table 5) are used by the software to access the configuration space on each PnP ISA card. These registers are used by the PnP software to issue commands, check status, access the resource data information, and configure the PnP hardware.

The ports have been chosen so as to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 5. Autoconfiguration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0×0279 (printer status port)	Write only
WRITE_DATA	0×0A79 (printer status port + 0×0800)	Write only
READ_DATA	Relocatable in range 0×0203 to 0×03FF	Read only

The PnP registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. Once addressed, the desired register may be accessed multiple times through the WRITE_DATA or READ_DATA ports.

The ADDRESS port is also the destination of the initiation key writes (see PnP ISA specification).

The address of the READ_DATA port is set by programming the SET RD_DATA PORT register. When a card cannot be isolated for a given READ_DATA port address, the READ_DATA port address is in conflict. The READ_DATA port address must then be relocated and the isolation process begun again. The entire range between 0×0203 and 0×3FF is available; however, in practice it is expected that only a few address locations are necessary before the software determines that PnP cards are not present.

PRINCIPLES OF OPERATION

PnP registers

PnP card standard registers are divided into three parts: card control, logical device control, and logical device configuration. There is one of each card control register on each ISA card. Card control registers are used for global functions that control the entire card. Logical device control registers and logical device configuration registers are repeated for each logical device. All unimplemented configuration registers are reset to 0 when read.

PnP card control registers

The PnP card control registers are listed in Table 6. All registers are cleared to 0 on power-up.

Table 6. PnP Card Control Registers

ADDRESS PORT	REGISTER NAME	ACCESSIBILITY
0×00	SET RD_DATA PORT	Write only
	Writing to this register modifies the address port used for reading from the PnP ISA card. Writing to this register is only allowed when the card is in the isolation state. Bit [7-0] These bits become I/O port address bits 9-2.	
0×01	SERIAL ISOLATION	Read only
	Reading from this register causes a card in the isolation state to compare one bit of the board ID.	
0×02	CONFIGURATION CONTROL	Write only
	This 3-bit register consists of three independent commands, which are activated by writing a 1 to their corresponding register bits. These bits are automatically reset to 0 by the hardware after the commands execute. Bit [2] Writing a 1 to this bit causes the card to reset its CSN and RD-DATA port to zero. Bit [1] Writing a 1 to this bit causes the card to enter the wait-for-key state, but the card CSN is preserved and the logical device is unaffected. Bit [0] Writing a 1 to this bit resets the logical device's configuration registers to their default state, and the CSN is preserved.	
0×03	WAKE[CSN]	Write only
	Writing to this register, when the write data [7-0] matches the card CSN, causes the card to go from the sleep state either to the isolation state when the write data for this command is zero, or to the configuration state when the write data is not zero. The pointer to the SERIAL IDENTIFIER is reset. This register is write only.	
0×04	RESOURCE DATA	Read only
	Reading from this register reads the next byte of resource information from the EEPROM. The STATUS register must be polled until its bit 0 is set before this register may be read.	
0×05	STATUS	Read only
	Bit [0] A one-bit register that, when set, indicates that it is okay to read the next data byte from the RESOURCE DATA register.	
0×06	CARD-SELECT NUMBER	Read/write
	Writing to this register sets the CSN of a card, which is uniquely assigned to a card after the serial identification process. This allows each card to be individually selected during a Wake[CSN] command.	
0×07	LOGICAL DEVICE NUMBER	Read/write
	This register specifies which logical device is being configured.	

PRINCIPLES OF OPERATION

PnP logical device control registers

The registers in Table 7 are repeated for each logical device. These registers control device functions, such as enabling the device onto the ISA bus.

Table 7. PnP Logical Device Control Registers

ADDRESS PORT	REGISTER NAME	ACCESSIBILITY
0×30	ACTIVE	Read/write
	This register controls whether the logical device is active on the bus. Bit [7-1] These bits are reserved and must be set to 0. Bit [0] If set, this bit activates the logical device. An inactive device does not respond to nor drive any ISA bus signals. Before a logical device is activated, I/O range check must be disabled.	
0×31	I/O RANGE CHECK	Read/write
	This register is used to perform a conflict check on the I/O port range programmed for use by the logical device. Bit [7-2] This bit is reserved and must be set to 0. Bit [1] If bit is set, the I/O range check is enabled. I/O range check is only valid when the logical device is inactive. Bit [0] If bit 0 is set, the logical device responds to I/O and reads to its assigned I/O range with a 0×55. If bit 0 is clear, the logical device responds with a 0×AA.	

PnP logical device configuration registers

The registers in Table 8 program the device ISA bus resource use and are repeated for each logical device. Registers in the ISA PnP specification that are not implemented in the TL16PNP200 are reset to 0 when read, except for the unimplemented DMA channel select descriptor 1 (0x75) which returns a 4 when read.

Table 8. PnP Logical Device Configuration Registers

ADDRESS PORT	REGISTER NAME	ACCESSIBILITY
0×40	MEMORY BASE ADDRESS [23-16]	Read/write
	This register indicates the selected memory base address of bits 23-16.	
0×41	MEMORY BASE ADDRESS [15-8]	Read/write
	This register indicates the selected memory base address of bits 15-8.	
0×42	MEMORY CONTROL	Read/write
	Bit 1 specifies 8 by 16-bit control. When set bit 1 indicates 16-bit memory, and cleared to indicate 8-bit memory. Bit 0 is read-only. It is internally set to 1 indicating that the next field is the upper limit for the address. TL16PNP200 supports memory upper limit, not range length.	
0×43	MEMORY UPPER LIMIT ADDRESS [23−16]	Read/write
	This register indicates the selected memory upper limit address of bits 23-16.	
0×44	MEMORY UPPER LIMIT ADDRESS [15-8]	Read/write
	This register indicates the selected memory upper limit address of bits 15-8.	
0×60	I/O PORT BASE ADDRESS [15-8]	Read/write
	This register indicates bits 15-8 of the base address that are to be used for the selected I/O address range.	
0×61	I/O PORT BASE ADDRESS [7-0]	Read/write
	This register indicates bits 7-0 of the base address that are to be used for the selected I/O address range.	

PRINCIPLES OF OPERATION

Table 9. PnP Logical Device Configuration Registers (continued)

ADDRESS PORT	REGISTER NAME	ACCESSIBILITY
0×70	INTERRUPT REQUEST LEVEL SELECT	Read/write
	This register indicates the selected interrupt level. Bits [3-0] select which interrupt level is used. The TL16PNP200 supports all 11 interrupts available on the ISA bus.	
0×71	INTERRUPT REQUEST TYPE SELECT	Read/write
	This register indicates which type of interrupt is used for the selected IRQ. Bit[1] : Level, 1 = high, 0 = low Bit[0] : Type, 1 = level, 0 = edge Note that at the IRQ outputs of the TL16PNP200, the interrupt type is the same as the type at the INTR inputs, regardless of the programmed type.	
0×74	DMA CHANNEL SELECT	Read/write
	This register indicates the selected DMA channel. Bits 2-0 select which DMA channel is in use: 000 selects DMA channel 0, 111 select DMA channel 7. DMA channel 4, the cascade channel indicates no DMA channel is active. The TL16PNP200 supports three DMA channels to select from in Mode 0 and five in Mode 1. The DMA mapping register, loaded on power-up, tells the device which DMA channels are connected to it (see the defaults description section).	

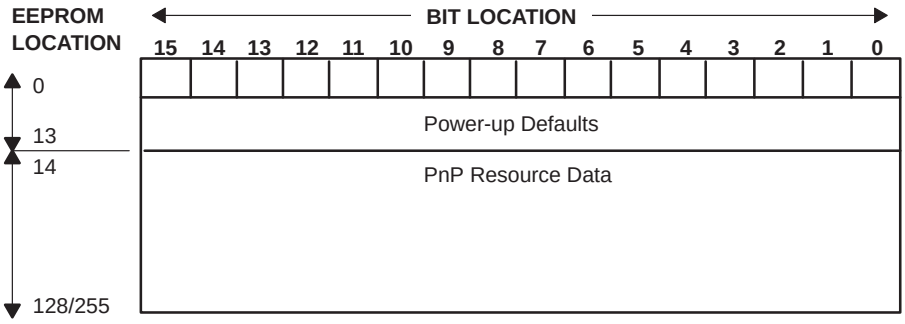
EEPROM

The TL16PNP200 interfaces to the SGS Thomson EEPROM ST93C56/66 or an equivalent. The EEPROM provides the PnP resource data and power-up defaults.

memory organization

The EEPROM should be organized as 128/255 words multiplied by 16 bits, therefore, its ORG terminal should be connected to V_{CC} or left unconnected. The memory organization for the EEPROM is shown in Table 10.

Table 10. EEPROM Memory Organization



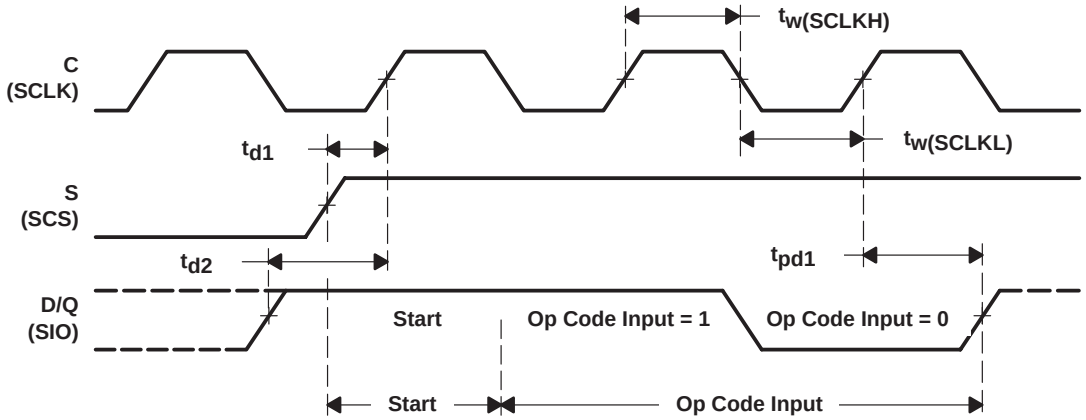
EEPROM READ (see Figure 9 and 10)

This device only supports read transactions. The READ op code instruction (10) must be sent into the EEPROM. The op code is then followed by an 8-bit-long address for the 16-bit word. The READ op code with accompanying address directs the EEPROM to output serial data on the EEPROM data terminals D and Q, which is connected to the TL16PNP200 bidirectional serial data bus (SIO). Specifically, when a READ op code and address are received, the instruction and address are decoded and the addressed EEPROM data is transferred into an output shift register in the EEPROM. Each read transaction consists of a start bit, 2-bit op code (10), 8-bit address, and 16-bit data. The TL16PNP200 does not accommodate the auto-address next word feature of the EEPROM.

PRINCIPLES OF OPERATION

READ op code transfer (see Figure 9)

Initially, the chip select signal,S, of the EEPROM, which connects to the TL16PNP200 EEPROM chip select (SCS), is raised. The data D and Q of the EEPROM then sample the TL16PNP200 (SIO) line on the following rising edges of the TL16PNP200 clock SCLK, until a 1 is sampled and decoded by the EEPROM as a start bit. The SCLK signal of the TL16PNP200 connects to the EEPROM clock C. The READ op code (10) is then sampled on the next two rising edges of SCLK. The TL16PNP200 sources the op code at the falling edges of SCLK.

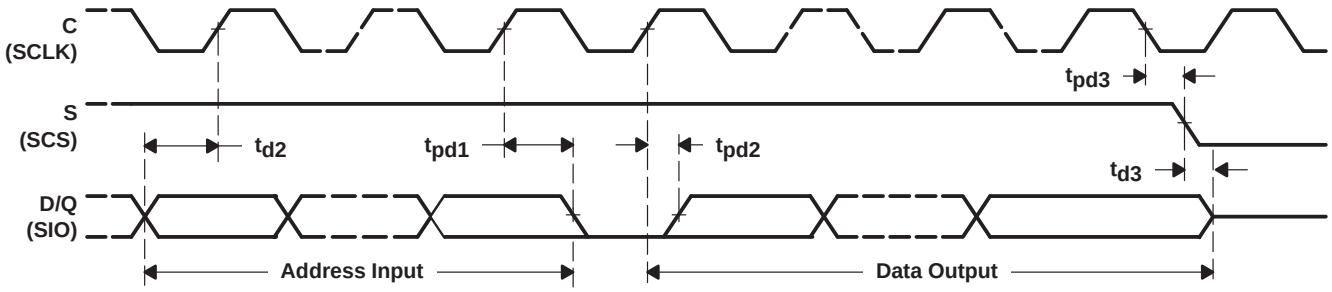


NOTE A: The corresponding TL16PNP200 terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together with a 2-kΩ resistor.

Figure 9. READ Op Code Transfer

READ address and data transfer (see Figure 10)

After receiving the READ op code, the EEPROM samples the READ address on the next eight rising edges of SCLK. The device sources the address at the falling edge of SCLK. The EEPROM then sends out a dummy bit 0 on the D/Q line, which is followed by the 16-bit data word with the MSB first. Output data changes are triggered by the rising edges of SCLK. The data is also read by the TL16PNP200 on the rising edges of SCLK.

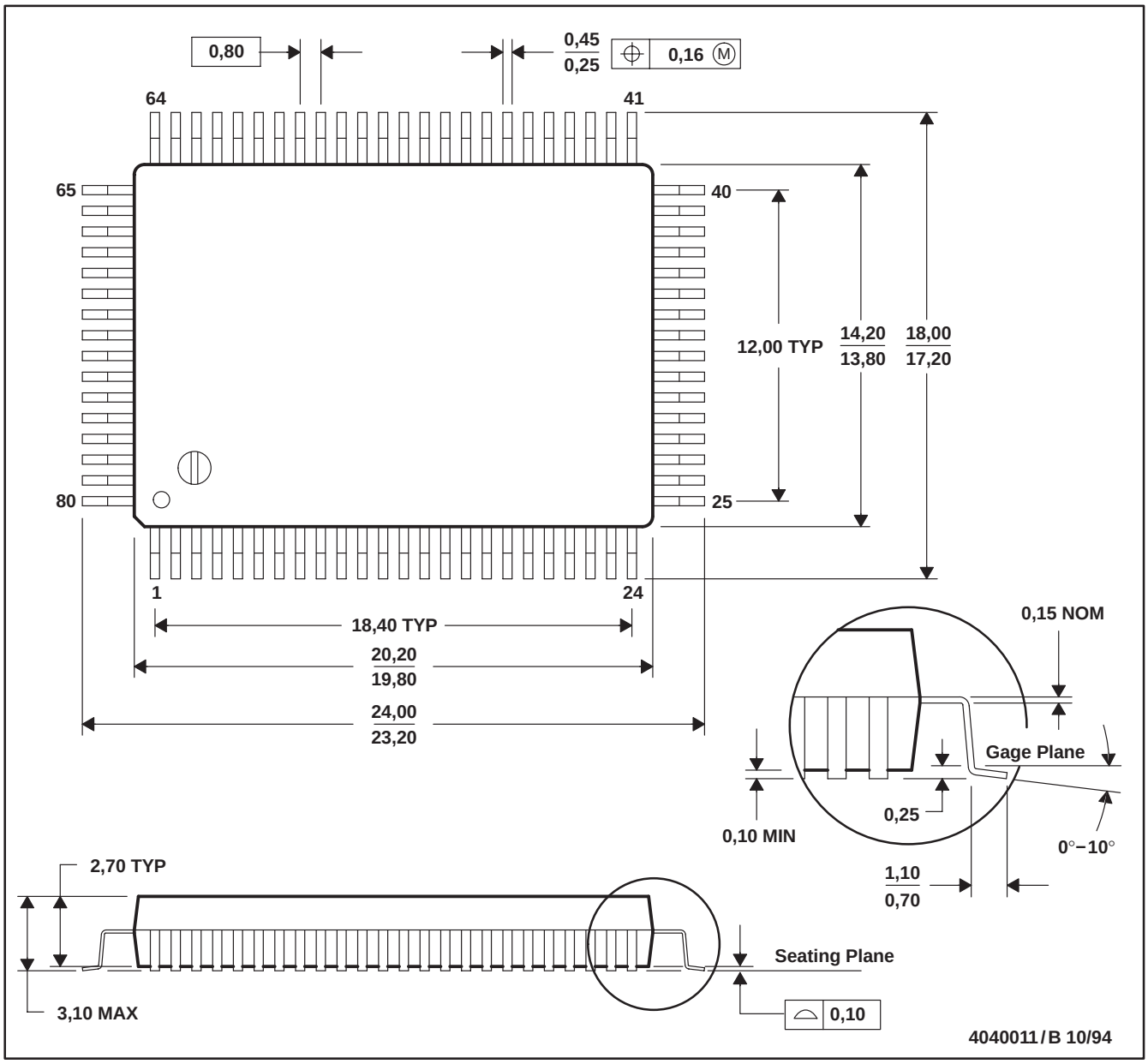


NOTE A: The corresponding TL16PNP200 terminal names are provided in parentheses. D/Q indicates that D and Q terminals in the EEPROMs are tied together with a 2-kΩ resistor.

Figure 10. READ Address and Data Transfer

MECHANICAL INFORMATION

PH (R-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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