

SLLS259I - NOVEMBER 1996-REVISED APRIL 2011

FlatLink[™] RECEIVER

Check for Samples: SN75LVDS82

FEATURES	DGG PA	CKAGE
 4:28 Data Channel Expansion at up to 238 Mbytes/s Throughput 		/IEW)
 Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI 	D22 [1 D23 [2 D24 [3	56
 Four Data Channels and Clock Low-Voltage Differential Channels In and 28 Data and Clock Low-Voltage TTL Channels Out 	GND [] 4 D25 [] 5 D26 [] 6 D27 [] 7	53] D19 52] GND 51] D18
 Operates From a Single 3.3-V Supply With 250 mW (Typ) 	D27 [] 7 LVDSGND [] 8 A0M [] 9	50] D17 49] D16 48] V _{CC}
5-V Tolerant SHTDN Input	A0P 10	47 D15
 Falling Clock-Edge-Triggered Outputs 	A1M 🛛 11	46 D14
 Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch 	A1P [12 LVDSV _{CC} [13	45 013 44 GND
Consumes Less Than 1 mW When Disabled	LVDSGND [14	43 D12
 Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz 	A2M [15 A2P [16	42 D11 41 D10
 No External Components Required for PLL 		40 V _{CC}
 Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard 	CLKINP [] 18 A3M [] 19 A3P [] 20	39] D9 38] D8 37] D7
Improved Replacement for the		36 GND
National™ DS90C582	PLLGND 22	35 D6
DESCRIPTION	PLLV _{CC} [23 PLLGND [24	34] D5 33] D4
The SN75LVDS82 FlatLink™ receiver contains four	SHTDN 25	32 D3
serial-in, 7-bit parallel-out shift registers, a 7× clock		31 V _{CC}
synthesizer, and five low-voltage differential signaling (LVDS) line receivers in a single integrated circuit.	D0 [27 GND [28	30] D2 29] D1

These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, over five balanced-pair conductors, and expansion to 28 bits of single-ended low-voltage TTL (LVTTL) synchronous data at a lower transfer rate. The SN75LVDS82 can also be used with the SN75LVDS84 or SN75LVDS85 for 21-bit transfers.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate of seven times (7×) the LVDS input clock (CLKIN). The data is then unloaded to a 28-bit-wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop (PLL) clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS82 presents valid data on the falling edge of the output clock (CLKOUT).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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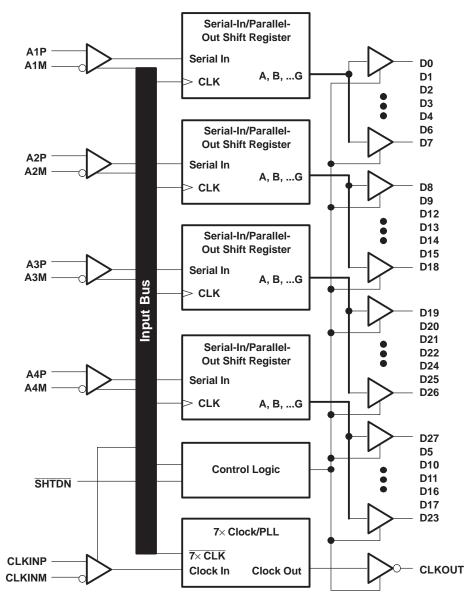
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The SN75LVDS82 requires only five line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only possible user intervention is the use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low-level on SHTDN clears all internal registers to a low level and places the CMOS outputs in a high-impedance state.

The SN75LVDS82 is characterized for operation over ambient air temperatures of 0°C to 70°C.



FUNCTIONAL BLOCK DIAGRAM



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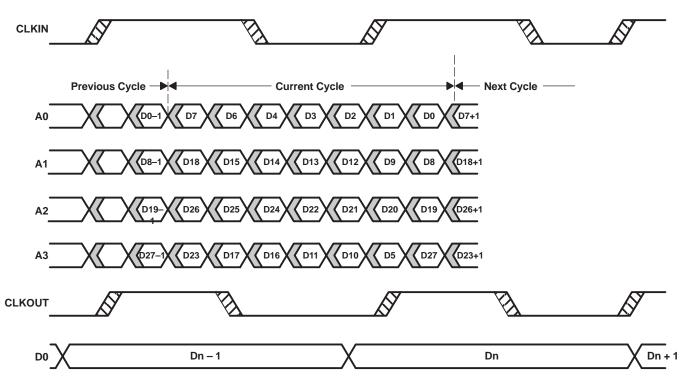
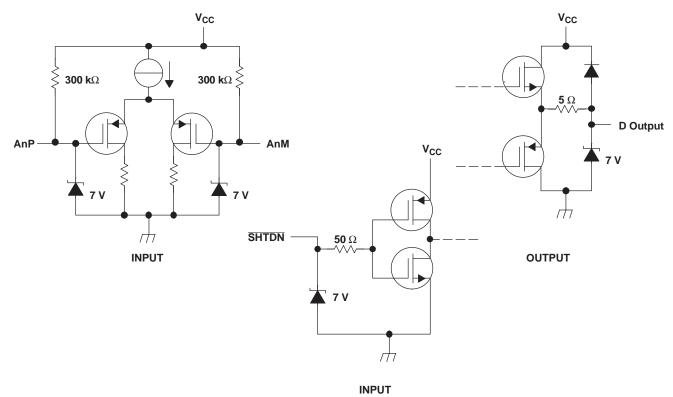


Figure 1. SN75LVDS82 Load and Shift Timing Sequences

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			UNIT
V _{CC}	Supply voltage range ⁽²⁾		–0.5 V to 4 V
Vo	Output voltage range (Dxx terminals)		–0.5 V to V _{CC} + 0.5 V
V		Any terminal except SHTDN	-0.5 V to V _{CC} + 0.5 V
VI	Input voltage range	SHTDN	–0.5 V to 5.5 V
	Continuous total power dissipation	See Dissipation Rating Table	
T _A	Operating temperature range		0°C to 70°C
T _{stg}	Storage temperature range	–65°C to 150°C	
	Lead temperature 1,6 mm (1/16 in) from case	260°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR ⁽¹⁾	T _A = 70°C
	POWER RATING	ABOVE $T_A = 25^{\circ}C$	POWER RATING
DGG	1377 mW	11.0 mW/°C	822 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
VIH	High-level input voltage (SHTDN)	2			V
V _{IL}	Low-level input voltage (SHTDN)			0.8	V
V _{ID}	Differential input voltage	0.1		0.6	V
V _{IC}	Common-mode input voltage (see Figure 2 and Figure 3)	$\frac{ V_{ID} }{2}$		$\frac{ V_{\text{ID}} }{2}$ $V_{\text{CC}} - 0.8$	V
T _A	Operating free-air temperature	0		70	°C

TIMING REQUIREMENTS

		MIN	MAX	UNIT
t _c	Cycle time, input clock ⁽¹⁾	14.7	32.3	ns
t _{su1}	Setup time, input (see Figure 7)	600		ps
t _{h1}	Hold time, input (see Figure 7)	600		ps

(1) Parameter t_c is defined as the mean duration of a minimum of 32000 clock cycles.



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ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input threshold voltage				100	mV
V _{IT-}	Negative-going differential input threshold voltage ⁽²⁾		-100			mV
V _{ОН}	High-level output voltage	$I_{OH} = -4 \text{ mA}$	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA			0.4	V
		Disabled, All inputs open			280	μA
		Enabled, AnP = 1 V, AnM = 1.4 V, $t_c = 15.38$ ns		60	74	
I _{CC}	Quiescent current (average)	Enabled, $C_L = 8 \text{ pF}$, Grayscale pattern (see Figure 4), $t_c = 15.38 \text{ ns}$		74		mA
		Enabled, $C_L = 8 \text{ pF}$, Worst-case pattern (see Figure 5), $t_c = 15.38 \text{ ns}$		107		
I _{IH}	High-level input current (SHTDN)	$V_{IH} = V_{CC}$			±20	μA
I _{IL}	Low-level input current (SHTDN)	$V_{IL} = 0$			±20	μA
I _{IN}	Input current (LVDS input terminals A and CLKIN)	$0 \le V_1 \le 2.4 V$			±20	μA
l _{oz}	High-impedance output current	$V_{O} = 0$ or V_{CC}			±10	μA

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (1)

The algebraic convention, in which the less-positive (more-negative) limit is designed minimum, is used in this data sheet for the (2)negative-going input voltage threshold only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{su2}	Setup time, D0–D27 valid to CLKOUT \downarrow	C _L = 8 pF, See Figure 6	5			ns
t _{h2}	Hold time, CLKOUT↓ to D0–D27 valid	$C_L = 8 \text{ pF}$, See Figure 6	5			ns
t _{RSKM}	Receiver input skew margin ⁽²⁾ (see Figure 7)	t _c = 15.38 ns (± 0.2%), Input clock jitter < 50 ps ⁽³⁾	490			ps
t _d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	t _c = 15.38 ns (± 0.2%), C _L = 8 pF		3.7		ns
A.L	Cuele time, change in output cleak period ⁽⁴⁾	t_c = 15.38 + 0.75 sin (2π500E3t) ± 0.05 ns, See Figure 8		±80		20
∆t _{c(o)}	Cycle time, change in output clock period ⁽⁴⁾	t_c = 15.38 + 0.75 sin (2π3E6t) ± 0.05 ns, See Figure 8		±300	ps	
t _{en}	Enable time, SHTDN↑ to Dn valid	See Figure 9		1		ms
t _{dis}	Disable time, SHTDN↓ to off state	See Figure 10		400		ns
t _t	Transition time, output (10% to 90% t_r or t_f)	C _L = 8 pF		3		ns
tw	Pulse duration, output clock			0.43 t _c		ns

 All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
 The parameter t_(RSKM) is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $t_c/14 - t_{su1}/t_{h1}$. |Input clock jitter| is the magnitude of the change in input clock period.

(3)

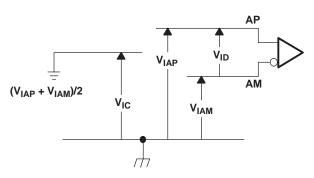
(4) $\Delta t_{c(o)}$ is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

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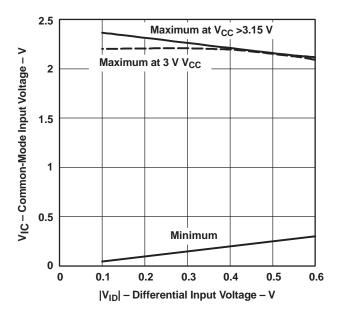
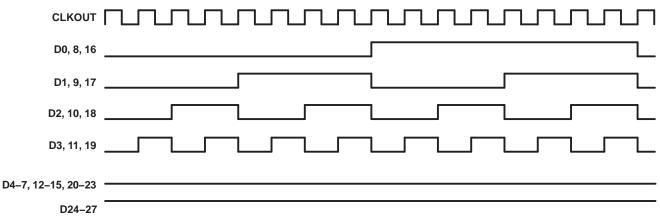


Figure 3. Common-Mode Input Voltage vs Differential Input Voltage



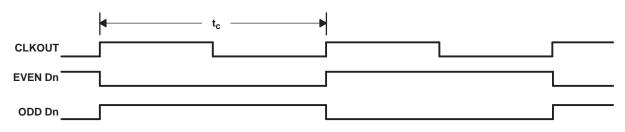
NOTE A: The 16-grayscale test-pattern tests device power consumption for a typical display pattern.





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PARAMETER MEASUREMENT INFORMATION (continued)



NOTE A: The worst-case test pattern produces the maximum switching frequency for all of the outputs.

Figure 5. Worst-Case Test-Pattern Waveforms

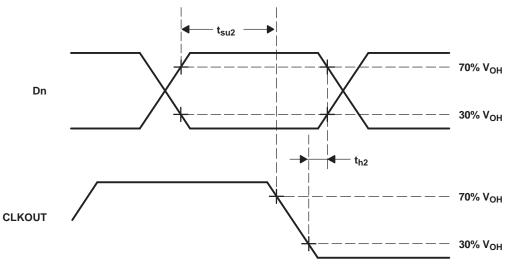


Figure 6. Setup and Hold Time Waveforms



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PARAMETER MEASUREMENT INFORMATION (continued)

F0FFFFF and 0F00000) CLKIN CLKOUT

A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The magnitude of the advance or delay is t_(RSKM).

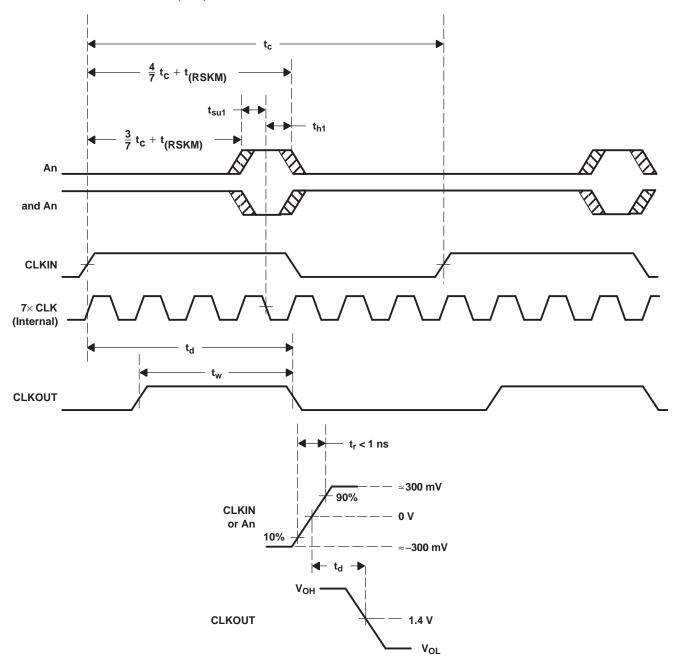


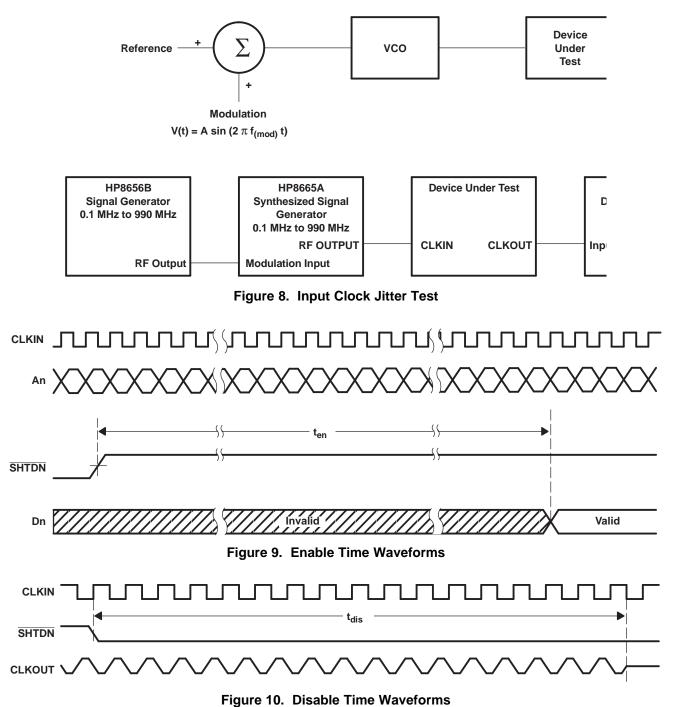
Figure 7. Receiver Input Skew Margin and Delay Timing Waveforms





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TYPICAL CHARACTERISTICS

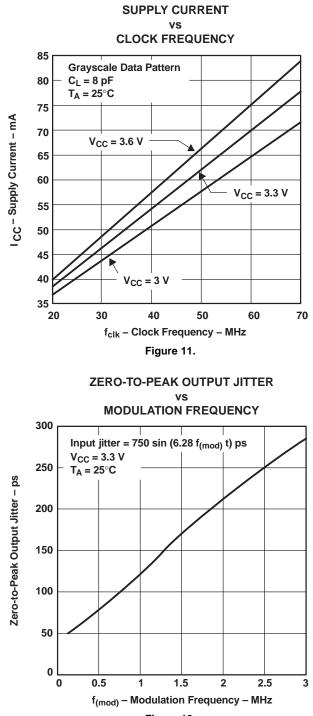


Figure 12.



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APPLICATION INFORMATION

9 100 Ω 10 10 11 11 100 Ω 12 15	SN75L A0M A0P A1M A1P	VDS82 D0 D1 D2 D3 D4 D6 D27 D5 D7 D5 D7 D8 D9 D12 D13	27 29 30 32 33 35 7 34 37 38 39 43	12-BIT RED0 RED1 RED2 RED3 RSVD RSVD NA NA GREEN0 GREEN1 GREEN2	ohic Control <u>18-BIT</u> RED0 RED1 RED2 RED3 RED4 RED5 NA NA GREEN0 GREEN1 GREEN2	24-BIT RED0 RED1 RED2 RED3 RED4 RED5 RED6 RED7 GREEN0 GREEN0 GREEN1 GREEN2
100 Ω 10 10 10 11 11 100 Ω 12 15	A0M A0P A1M A1P	D0 D1 D2 D3 D4 D6 D27 D5 D7 D8 D9 D12	29 30 32 33 35 7 34 37 38 39 43	RED0 RED1 RED2 RSVD RSVD NA NA GREEN0 GREEN1 GREEN2	RED0 RED1 RED2 RED3 RED4 RED5 NA NA GREEN0 GREEN1 GREEN2	RED0 RED1 RED2 RED3 RED4 RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
100 Ω 10 10 10 11 11 100 Ω 12 15	- A0P - A1M - A1P	D1 D2 D3 D4 D6 D27 D5 D7 D8 D9 D12	29 30 32 33 35 7 34 37 38 39 43	RED1 RED2 RSVD RSVD NA NA GREEN0 GREEN1 GREEN2	RED1 RED2 RED3 RED4 RED5 NA NA GREEN0 GREEN1 GREEN2	RED1 RED2 RED3 RED4 RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
10 11 100 Ω 12 15	- A1M - A1P	D2 D3 D4 D6 D27 D5 D7 D8 D9 D12	30 32 33 35 7 34 37 38 39 43	RED2 RED3 RSVD RSVD NA GREEN0 GREEN1 GREEN2	RED2 RED3 RED4 RED5 NA NA GREEN0 GREEN1 GREEN2	RED2 RED3 RED4 RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
10 11 100 Ω 12 15	- A1M - A1P	D3 D4 D6 D27 D5 D7 D8 D9 D12	32 33 35 7 34 37 38 39 43	RED3 RSVD RSVD NA GREEN0 GREEN1 GREEN2	RED3 RED4 RED5 NA GREEN0 GREEN1 GREEN2	RED3 RED4 RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
11 100 Ω 12 15	- A1M - A1P	D4 D6 D27 D5 D7 D8 D9 D12	33 35 7 34 37 38 39 43	RSVD RSVD NA GREEN0 GREEN1 GREEN2	RED4 RED5 NA GREEN0 GREEN1 GREEN2	RED4 RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
100 Ω 12 15	- A1M - A1P	D6 D27 D5 D7 D8 D9 D12	35 7 34 37 38 39 43	RSVD NA NA GREEN0 GREEN1 GREEN2	RED5 NA NA GREEN0 GREEN1 GREEN2	RED5 RED6 RED7 GREEN0 GREEN1 GREEN2
100 Ω 12 15	A1P	D27 D5 D7 D8 D9 D12	7 34 37 38 39 43	NA NA GREEN0 GREEN1 GREEN2	NA NA GREEN0 GREEN1 GREEN2	RED6 RED7 GREEN0 GREEN1 GREEN2
100 Ω 12 15	A1P	D5 D7 D8 D9 D12	34 37 38 39 43	NA GREEN0 GREEN1 GREEN2	NA GREEN0 GREEN1 GREEN2	RED7 GREEN0 GREEN1 GREEN2
	A1P	D5 D7 D8 D9 D12	37 38 39 43	GREEN0 GREEN1 GREEN2	GREEN0 GREEN1 GREEN2	GREEN0 GREEN1 GREEN2
		D8 D9 D12	38 39 43	GREEN1 GREEN2	GREEN1 GREEN2	GREEN0 GREEN1 GREEN2
		D8 D9 D12	39 43	GREEN2	GREEN2	GREEN1 GREEN2
		D9 D12	43	GREEN2	GREEN2	GREEN2
	A2M	D12				
	A2M			GREEN3	GREEN3	GREEN3
			45	RSVD	GREEN4	GREEN4
		D14	46	RSVD	GREEN5	GREEN5
100 Ω ≷		D10	41	- NA	NA	GREEN6
16		D10	42	- NA	NA	GREEN7
	A2P	D15	47	BLUE0	BLUE0	BLUE0
		D13	51	BLUE1	BLUE1	BLUE1
19		D10	53	BLUE2	BLUE2	BLUE2
	A3M	D19	54	BLUE2	BLUE2	BLUE2 BLUE3
Ι 100 Ω ≷		D20 D21	55	RSVD	BLUE3	BLUE3
20			1			
· · · · · · · · · · · · · · · · · · ·	A3P	D22	49	RSVD	BLUE5	BLUE5
			50			BLUE6
İ						BLUE7
				-		H_SYNC
17			6	_	—	V_SYNC
			2			ENABLE
1'00 Ω <						RSVD
		CLKOUT			CLOCK	CLOCK
18			1			
÷	17 100 Ω 18	17 100 Ω 18	ASF D16 D17 D24 17 D25 100 Ω 18 18 CLKOUT	17 CLKINM D16 49 100 Ω 17 CLKINM D26 2 100 Ω CLKINM D26 2 26	ASP D16 49 NA D17 D24 50 NA 17 D24 5 V_SYNC 17 CLKINM D26 6 ENABLE 100 Ω 18 CLKOUT 26 CLOCK	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

A. The five 100- Ω terminating resistors are recommended to be 0603 types.

B. NA — not applicable, these unused inputs should be left open.

Figure 13. 24-Bit Color Host to 24-Bit LCD Flat Panel Display Application

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Host		Cable	Flat F	Panel Display					
SN75LVDS84/85				SN75LV	0582	ן ו	Grap	hic Contro	ller
SIN7 JLV D304/03			-		0302		<u>12-BIT</u>	<u>18-BIT</u>	<u>24-BIT</u>
YOM	41		9	АОМ	D0	27	RED0	RED0	RED0
		r A	Ţ		D1	29	RED1	RED1	RED1
		100 Ω	\$		D2	30	RED2	RED2	RED2
YOP	40 📉] 10	AOP	D3	32	RED3	RED3	RED3
TUP			•	AUP	D4	33	RSVD	RED4	RED4
					D6	35	RSVD	RED5	RED5
Y1M	39		11	A1M	D27	7	NA	NA	RED6
		ľ ľ	Ţ		D5	34	NA	NA	RED7
		100 Ω	3		D7	37	GREEN0	GREEN0	GREEN0
Y1P	38 🗸		12	A1P	D8	38	GREEN1	GREEN1	GREEN1
TIP	4	r 1	•		D9	39	GREEN2	GREEN2	GREEN2
					D12	43	GREEN3	GREEN3	GREEN3
Y2M	35		15	A2M	D13	45	RSVD	GREEN4	GREEN4
		r x	Ţ		D14	46	RSVD	GREEN5	GREEN5
		100 Ω			D10	41	NA	NA	GREEN6
Y2P	34		16	A2P	D11	42	NA	NA	GREEN7
126			•		D15	47	BLUE0	BLUE0	BLUE0
					D18	51	BLUE1	BLUE1	BLUE1
		i 1	19	АЗМ	D19	53	BLUE2	BLUE2	BLUE2
		i í			D20	54	BLUE3	BLUE3	BLUE3
		İİ			D21	55	RSVD	BLUE4	BLUE4
		∣ ∖	20	A3P	D22	1	RSVD	BLUE5	BLUE5
		l í			D16	49	NA	NA	BLUE6
					D17	50	NA	NA	BLUE7
					D24	3	H_SYNC	H_SYNC	H_SYNC
	40		17		D25	5	V_SYNC	V_SYNC	V_SYNC
CLKOUTM			•	CLKINM	D26	6	ENABLE	ENABLE	ENABLE
		΄1 100 Ω	Ş		D23	2	NA	NA	RSVD
	39 🗸		18		CLKOUT	26	CLOCK	CLOCK	CLOCK
CLKOUTP	39	\rightarrow	• 10	CLKINP					
L				L		1			
	1	I I							

A. The four 100- Ω terminating resistors are recommended to be 0603 types.

B. NA — not applicable, these unused inputs should be left open.

Figure 14. 18-Bit Color Host to 24-Bit Color LCD Panel Display Application

TEXAS INSTRUMENTS

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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing		Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
SN75LVDS82DGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	_
GINIGEVEDODZEDOG	AOINE	10001	200	50	55	& no Sb/Br)		LEVEL 2000 T TEAK	01070	01473272002	Samples
SN75LVDS82DGGG4	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples
SN75LVDS82DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples
SN75LVDS82DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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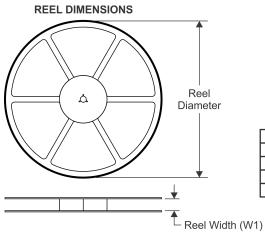
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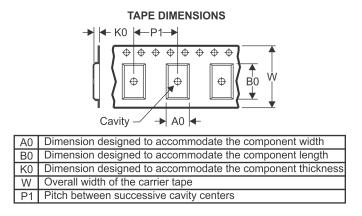
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS82DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS82DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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