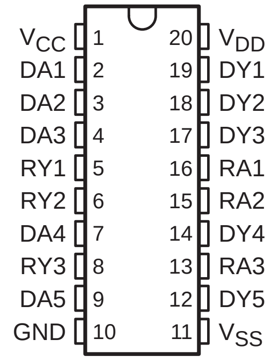
SLLS294A – APRIL 1998 – REVISED JUNE 1999

- **Single-Chip RS-232 Interface for an External Modem or Other Computer Peripheral Serial Port**
- **Designed to Transmit and Receive 4-μs Pulses (Equivalent to 256 kbit/s)**
- **Wide Driver Supply-Voltage Range: 4.75 V to 15 V**
- **Driver Output Slew Rates Are Controlled Internally to 30 V/μs Maximum**
- **Receiver Input Hysteresis . . . 1000 mV Typical**
- **RS-232 Bus-Pin ESD Protection Exceeds 15 kV Using Human-Body Model (HBM)**
- **Five Drivers and Three Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Complements the SN75LP1185**
- **Designed to Replace the Industry-Standard SN75196 With the Same Flow-Through Pinout**
- **Package Options Include Plastic Small Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Dual-in-Line (N) Packages**

DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The SN75LP196 is a low-power bipolar device containing five drivers and three receivers, with 15 kV of ESD protection on the bus pins with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75196 and allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatibles. This device provides a rugged, low-cost solution for this function with the combination of bipolar processing and 15-kV ESD protection.

The SN75LP196 has internal slew-rate control to provide a maximum rate of change in the output signal of 30 V/μs. The driver output swing is clamped nominally at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. Even though the driver outputs are clamped, they can handle voltages up to ±15 V without damage. All the logic inputs can accept 3.3-V or 5-V input signals.

The SN75LP196 complies with the requirements of the TIA/EIA-232-F and the ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75LP196 support rates up to 256 kbit/s with lower capacitive loads (shorter cables).

The SN75LP196 is characterized for operation from 0°C to 70°C.

Function Tables

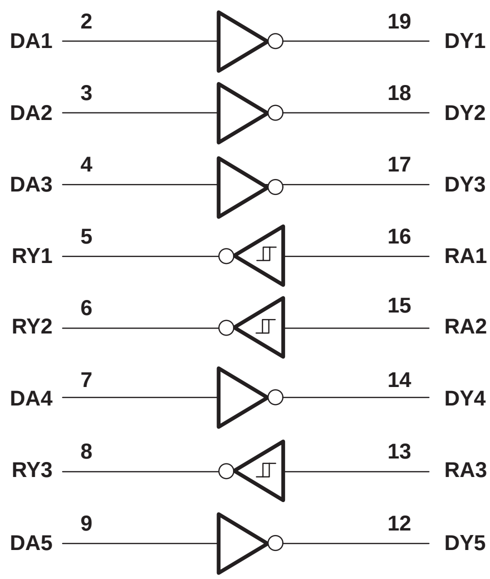
DRIVER

INPUT DA	OUTPUT DY
H	L
L	H
Open	L

RECEIVER

INPUT RA	OUTPUT RY
H	L
L	H
Open	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply-voltage range (see Note 1): V_{CC} . . . . –0.5 V to 7 V
V_{DD} (see Note 1) . . . . –0.5 V to 15 V
Negative supply-voltage range, V_{SS} (see Note 1) . . . . 0.5 V to –15 V
Input-voltage range, V_I: Receiver (RA) . . . . –30 V to 30 V
Driver (DA) . . . . –0.5 V to V_{CC}+0.4 V
Output-voltage range, V_O: Receiver (RY) . . . . –0.5 V to 6 V
Driver (DY) . . . . –15 V to 15 V
Electrostatic discharge: Bus pins (human-body model) (see Note 2) . . . . Class 3, A: 15 kV
All pins (human-body model) (see Note 2) . . . . Class 3, A: 5 kV
All pins (machine model) . . . . 200 V
Package thermal impedance, θ_{JA} (see Notes 3 and 4): DB package . . . . 115°C/W
DW package . . . . 97°C/W
N package . . . . 67°C/W
PW package . . . . 128°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Storage temperature range, T_{stg} . . . . 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal, unless otherwise noted.
2. Per MIL-STD-883 Method 3015.7
3. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 5)		4.75	5	5.25	V
V_{DD}	Supply voltage (see Note 6)		9	12	15	V
V_{SS}	Supply voltage (see Note 6)		–9	–12	–15	V
V_{IH}	High-level input voltage	DA	2			V
V_{IL}	Low-level input voltage	DA			0.8	V
V_I	Receiver input voltage	RA	–25		25	V
I_{OH}	High-level output current	RY			–1	mA
I_{OL}	Low-level output current	RY			2	mA
T_A	Operating free-air temperature		0		70	°C

NOTES: 5. V_{CC} cannot be greater than V_{DD}.
6. The device operates down to $V_{DD} = V_{CC}$ and $|V_{SS}| = V_{CC}$, but supply currents increase and other parameters may vary slightly from the data-sheet limits.

supply currents over the recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply current for V_{CC}, I_{CC}	No load, All inputs at minimum V_{OH} or maximum V_{OL}	V_{DD} = 9 V, V_{SS} = –9 V			1000	µA
		V_{DD} = 12 V, V_{SS} = –12 V			1000	
Supply current for V_{DD}, I_{DD}		V_{DD} = 9 V, V_{SS} = –9 V			800	µA
		V_{DD} = 12 V, V_{SS} = –12 V			800	
Supply current for V_{SS}, I_{SS}		V_{DD} = 9 V, V_{SS} = –9 V			–800	µA
		V_{DD} = 12 V, V_{SS} = –12 V			–800	

driver electrical characteristics over the recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 9 V, V_{SS} = –9 V, See Note 7	5	5.8	6.6	V
			V_{DD} = 12 V, V_{SS} = –12 V, See Note 8	5	5.8	6.6	
V_{OL}	Low-level output voltage	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 9 V, V_{SS} = –9 V, See Note 7	–5	–5.8	–6.9	V
			V_{DD} = 12 V, V_{SS} = –12 V, See Note 8	–5	–5.8	–6.9	
I_{IH}	High-level input current	V_I at V_{CC}				1	µA
I_{IL}	Low-level input current	V_I at GND				–1	µA
$I_{OS(H)}$	Short-circuit high-level output current	V_O = GND or V_{SS},	See Figure 2 and Note 9		–30	–55	mA
$I_{OS(L)}$	Short-circuit low-level output current	V_O = GND or V_{DD},	See Figure 2 and Note 9		30	55	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,	V_O = –2 V to 2 V	300			Ω

NOTES: 7. Minimum RS-232 driver output voltages are not attained with ±5-V supplies. With V_{DD} less than V_{CC} + 2 V, the supply currents may increase. For RS-232 compliant output swings and minimum power consumption, $V_{DD} \geq V_{CC}$ + 2 V.

8. Maximum output swing is nominally clamped at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. The driver outputs may slightly exceed the maximum output voltage over the full V_{CC} and temperature ranges.

9. Not more than one output should be shorted at one time.

driver switching characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1		300	800	1600	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1		300	800	1600	ns
t_{TLH}	Transition time, low- to high-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 10	Using V_{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF	375		2240	ns
			Using V_{TR} = ±3 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using V_{TR} = ±3 V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
t_{THL}	Transition time, high- to low-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 10	Using V_{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF	375		2240	ns
			Using V_{TR} = ±3 V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using V_{TR} = ±3 V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
SR	Output slew rate	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V,	Using V_{TR} = ±3 V transition region, Driver speed = 0 to 250 kbit/s, C_L = 15 pF	4	20	30	V/µs

NOTE 10: Maximum output swing is limited to ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions.

receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

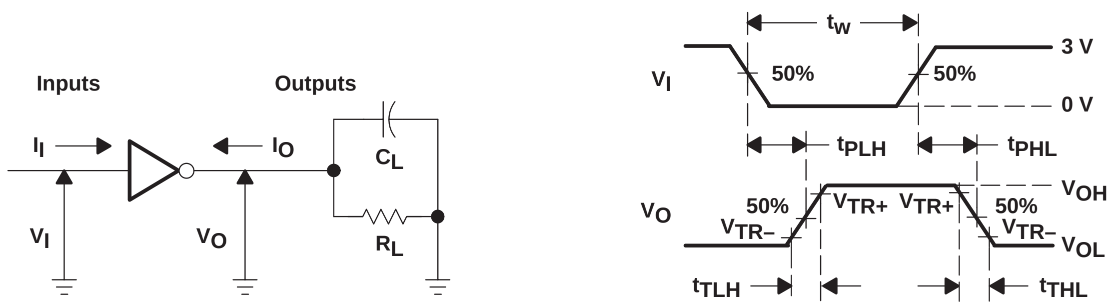
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 3	1.6	2	2.55	V
$V_{IT–}$	Negative-going input threshold voltage	See Figure 3	0.6	1	1.45	V
V_{HYS}	Input hysteresis, V_{IT+} $V_{IT–}$	See Figure 3	750	1000		mV
V_{OH}	High-level output voltage	I_{OH} = –1 mA	2.5	3.9		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.33	0.5	V
I_{IH}	High-level input current	V_I = 3 V	0.43	0.6	1	mA
		V_I = 25 V	3.6	5.1	8.3	
I_{IL}	Low-level input current	V_I = 3 V	–0.43	–0.6	–1	mA
		V_I = 25 V	–3.6	–5.1	–8.3	
$I_{OS(H)}$	Short-circuit high-level output current	V_O = 0, See Figure 5 and Note 9			–20	mA
$I_{OS(L)}$	Short-circuit low-level output current	V_O = V_{CC}, See Figure 5 and Note 9			20	mA
R_{IN}	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

NOTE 9: Not more than one output should be shorted at one time.

receiver switching characteristics over operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output		400	900	ns
t_{PLH}	Propagation delay time, low- to high-level output		400	900	
t_{TLH}	Transition time, low- to high-level output		200	450	ns
t_{THL}	Transition time, high- to low-level output		200	400	
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$		200	425	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:
For C_L < 1000 pF: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
For C_L = 2500 pF: t_W = 8 µs, PRR = 125 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform

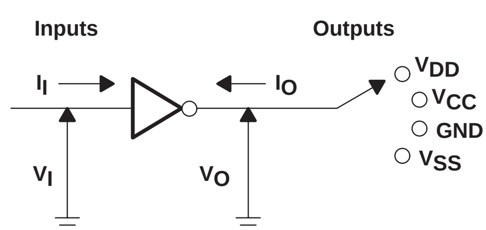


Figure 2. Driver I_{OS} Test

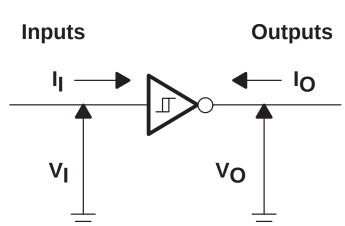
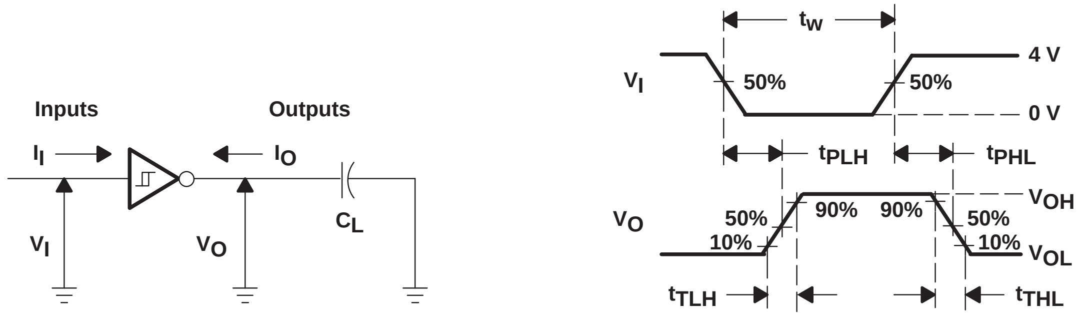


Figure 3. Receiver V_{IT} Test

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Parameter Test Circuit and Waveform

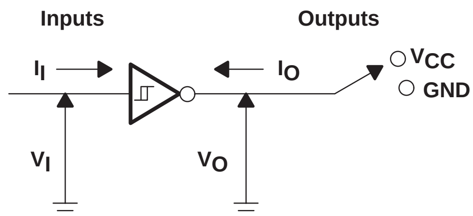


Figure 5. Receiver I_{OS} Test

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75LP196 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground (see Figure 6).

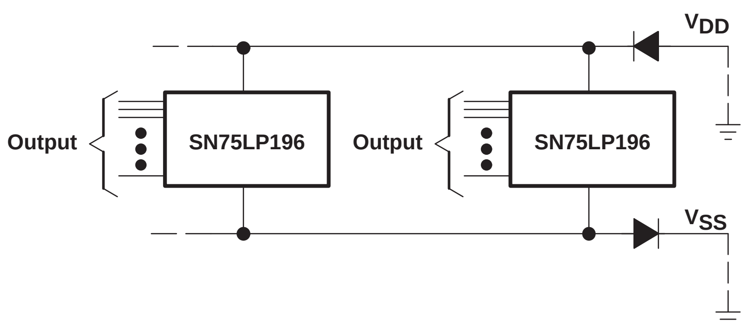


Figure 6. Power-Supply Protection to Meet Power-Off Fault Conditions of EIA/TIA-232-F

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN75LP196DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LP196DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75LP196DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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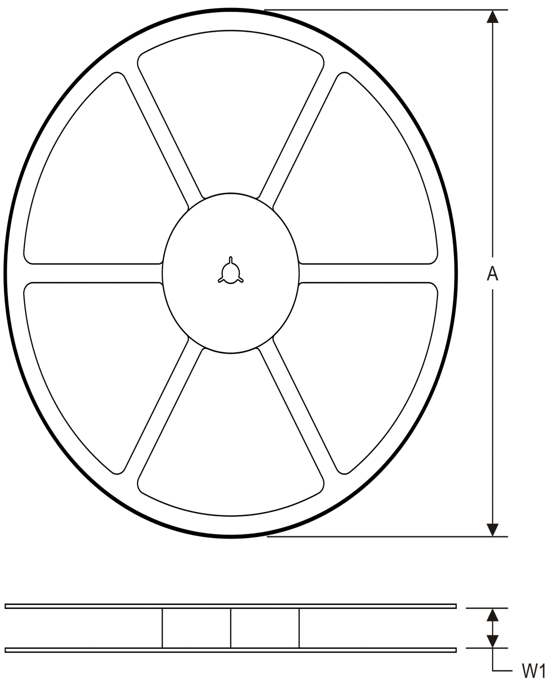
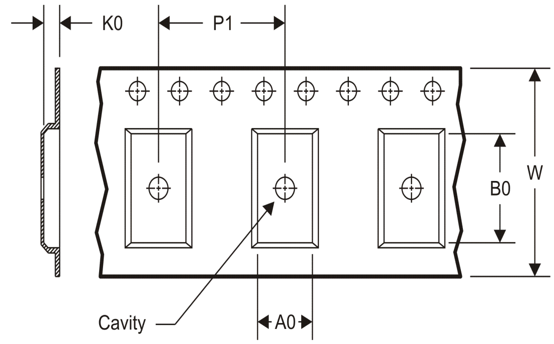
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



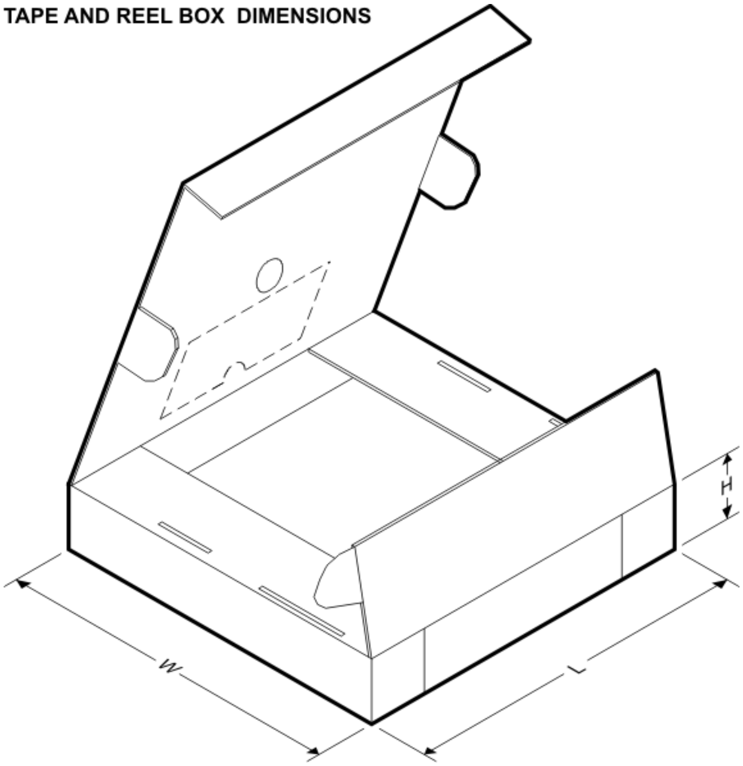
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LP196DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

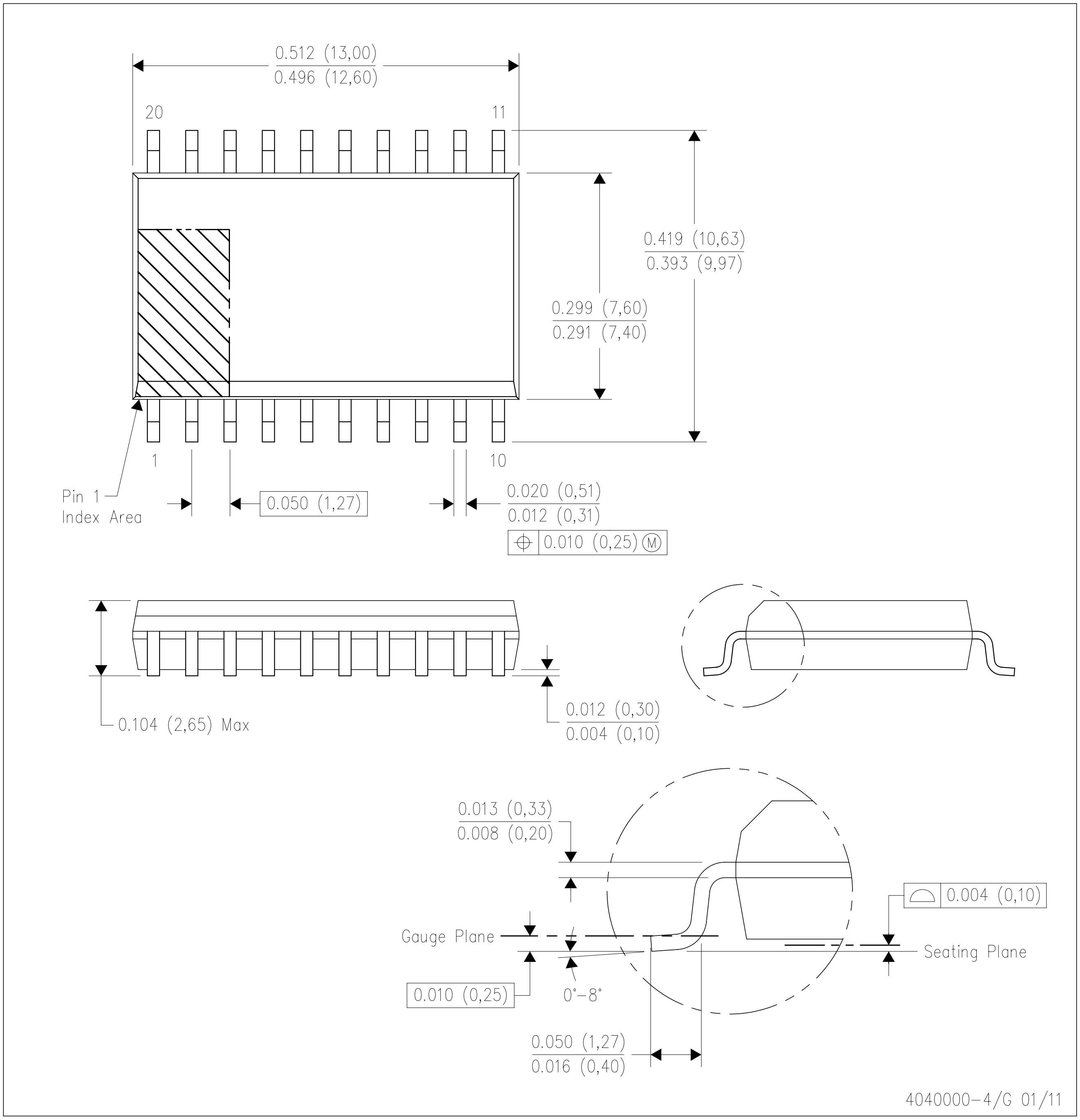
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

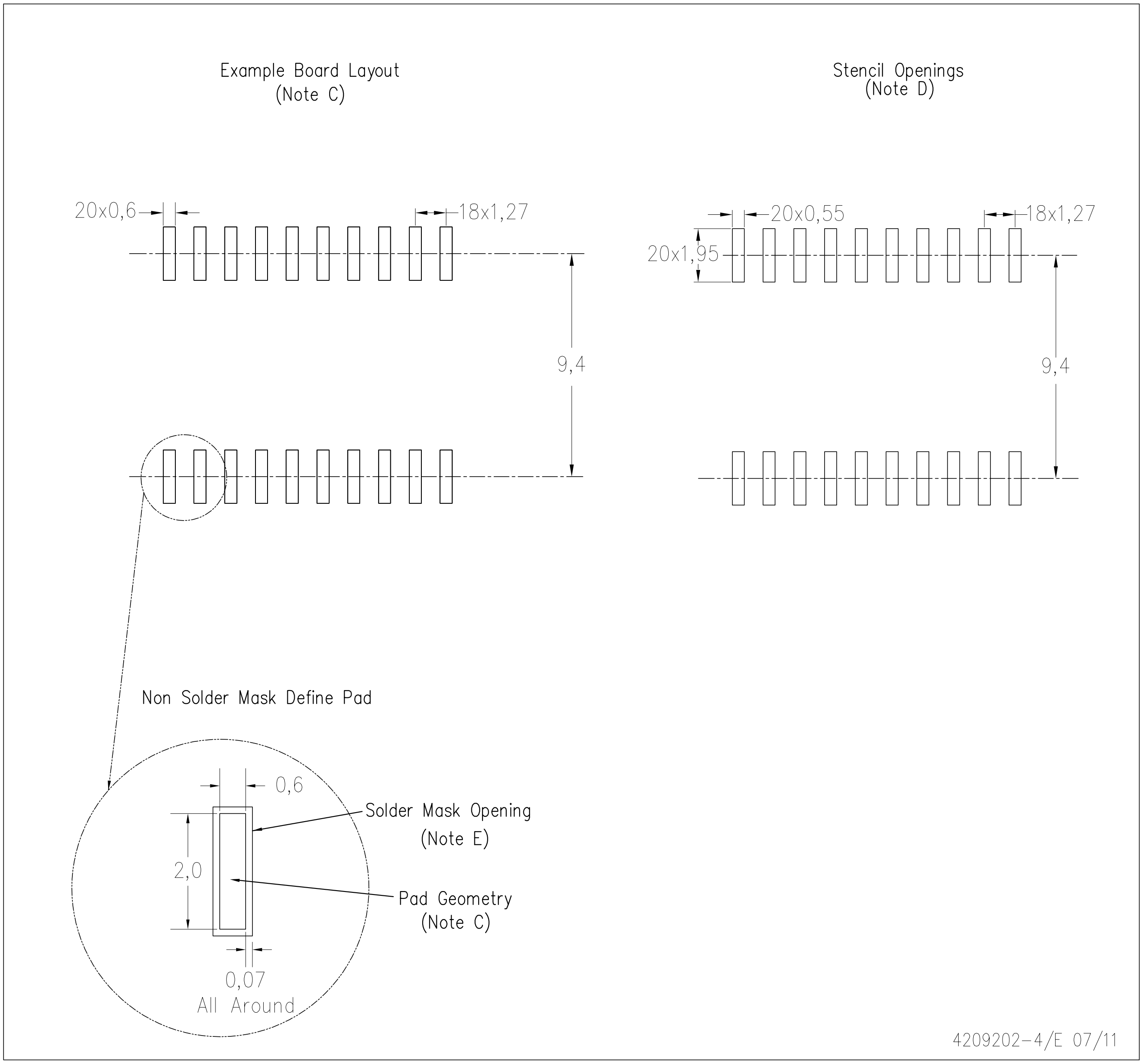
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LP196DWR	SOIC	DW	20	2000	367.0	367.0	45.0

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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