

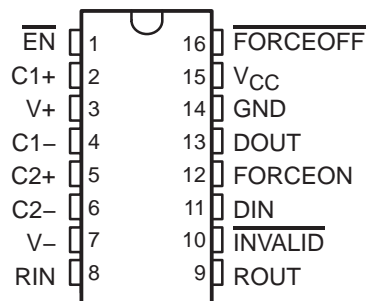
# MAX3221

## 3-V TO 5.5-V SINGLE-CHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

SLLS348M – JUNE 1999 – REVISED MARCH 2004

- **RS-232 Bus-Pin ESD Protection Exceeds  $\pm 15$  kV Using Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V  $V_{CC}$  Supply**
- **Operates Up To 250 kbit/s**
- **One Driver and One Receiver**
- **Low Standby Current . . . 1  $\mu$ A Typical**
- **External Capacitors . . .  $4 \times 0.1 \mu$ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Alternative High-Speed Pin-Compatible Device (1 Mbit/s)**
  - SNx5C3221
- **Auto-Powerdown Feature Automatically Disables Drivers for Power Savings**
- **Applications**
  - Battery-Powered, Hand-Held, and Portable Equipment
  - PDAs and Palmtop PCs
  - Notebooks, Subnotebooks, and Laptops
  - Digital Cameras
  - Mobile Phones and Wireless Devices

DB OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

The MAX3221 consists of one line driver, one line receiver, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SSOP (DB)	Tube of 80	MAX3221CDB
		Reel of 2000	MAX3221CDBR
	TSSOP (PW)	Tube of 90	MAX3221CPW
		Reel of 2000	MAX3221CPWR
–40°C to 85°C	SSOP (DB)	Tube of 80	MAX3221IDB
		Reel of 2000	MAX3221IDBR
	TSSOP (PW)	Tube of 90	MAX3221IPW
		Reel of 2000	MAX3221IPWR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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# MAX3221

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### description/ordering information (continued)

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and  $\overline{\text{FORCEOFF}}$  is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If  $\overline{\text{FORCEOFF}}$  is set low and  $\overline{\text{EN}}$  is high, both the driver and receiver are shut off, and the supply current is reduced to 1  $\mu\text{A}$ . Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and  $\overline{\text{FORCEOFF}}$  are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The  $\overline{\text{INVALID}}$  output notifies the user if an RS-232 signal is present at the receiver input.  $\overline{\text{INVALID}}$  is high (valid data) if the receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30  $\mu\text{s}$ .  $\overline{\text{INVALID}}$  is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30  $\mu\text{s}$ . Refer to Figure 5 for receiver input levels.

### Function Tables

EACH DRIVER

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

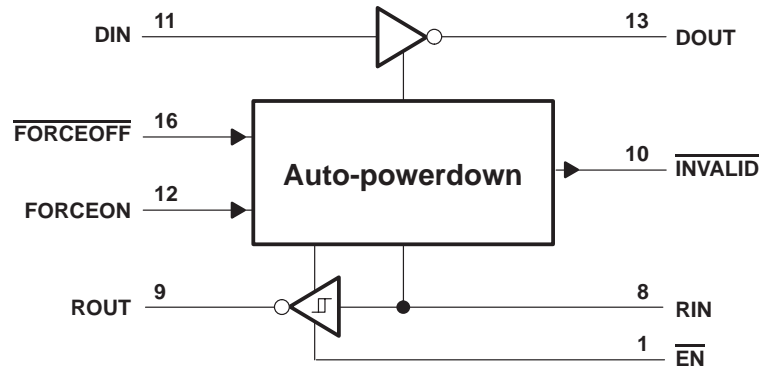
INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, $V_I$ : Driver ( $\overline{\text{FORCEOFF}}$ , $\text{FORCEON}$ , $\overline{\text{EN}}$ )	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, $V_O$ : Driver	–13.2 V to 13.2 V
Receiver ( $\overline{\text{INVALID}}$ )	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DB package	82°C/W
PW package	108°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 4 and Figure 6)**

		MIN	NOM	MAX	UNIT	
Supply voltage		$V_{CC} = 3.3$ V	3	3.3	3.6	V
		$V_{CC} = 5$ V	4.5	5	5.5	
$V_{IH}$ Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$ , $\text{FORCEON}$ , $\overline{\text{EN}}$	$V_{CC} = 3.3$ V	2		V	
		$V_{CC} = 5$ V	2.4			
$V_{IL}$ Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$ , $\text{FORCEON}$ , $\overline{\text{EN}}$			0.8	V	
$V_I$ Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$ , $\text{FORCEON}$	0			5.5	V
$V_I$ Receiver input voltage		–25			25	V
$T_A$ Operating free-air temperature	MAX3221C	0			70	°C
	MAX3221I	–40			85	

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3$  V  $\pm$  0.3 V; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5$  V  $\pm$  0.5 V.



# MAX3221

## 3-V TO 5.5-V SINGLE-CHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$I_I$	Input leakage current	FORCEOFF, FORCEON, EN		±0.01		±1	μA
$I_{CC}$	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at $V_{CC}$	0.3		1	mA
		Powered off	No load, FORCEOFF at GND		1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at $V_{CC}$ , FORCEON at GND, All RIN are open or grounded		1	10	

† All typical values are at  $V_{CC} = 3.3$  V or  $V_{CC} = 5$  V, and  $T_A = 25^\circ\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1 μF at  $V_{CC} = 3.3$  V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at  $V_{CC} = 5$  V ± 0.5 V.

### DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3$ kΩ to GND, DIN = GND		5	5.4		V
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3$ kΩ to GND, DIN = $V_{CC}$		–5	–5.4		V
$I_{IH}$	High-level input current	$V_I = V_{CC}$		±0.01		±1	μA
$I_{IL}$	Low-level input current	$V_I$ at GND		±0.01		±1	μA
$I_{OS}$	Short-circuit output current‡	$V_{CC} = 3.6$ V, $V_O = 0$ V		±35		±60	mA
		$V_{CC} = 5.5$ V, $V_O = 0$ V		±35		±60	
$r_o$	Output resistance	$V_{CC}$ , $V_+$ , and $V_- = 0$ V, $V_O = \pm 2$ V		300	10M		Ω
$I_{off}$	Output leakage current	FORCEOFF = GND	$V_O = \pm 12$ V, $V_{CC} = 3$ V to 3.6 V			±25	μA
			$V_O = \pm 10$ V, $V_{CC} = 4.5$ V to 5.5 V			±25	

† All typical values are at  $V_{CC} = 3.3$  V or  $V_{CC} = 5$  V, and  $T_A = 25^\circ\text{C}$ .

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at  $V_{CC} = 3.3$  V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at  $V_{CC} = 5$  V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate	$C_L = 1000$ pF, $R_L = 3$ kΩ, See Figure 1		150	250		kbit/s
$t_{sk(p)}$	Pulse skew§	$C_L = 150$ pF to 2500 pF, $R_L = 3$ kΩ to 7 kΩ, See Figure 2			100		ns
SR(tr)	Slew rate, transition region (see Figure 1)	$V_{CC} = 3.3$ V, $R_L = 3$ kΩ to 7 kΩ	$C_L = 150$ pF to 1000 pF	6		30	V/μs
			$C_L = 150$ pF to 2500 pF	4		30	

† All typical values are at  $V_{CC} = 3.3$  V or  $V_{CC} = 5$  V, and  $T_A = 25^\circ\text{C}$ .

§ Pulse skew is defined as  $|t_{pLH} - t_{pHL}|$  of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at  $V_{CC} = 3.3$  V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at  $V_{CC} = 5$  V ± 0.5 V.



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**ESD protection**

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
DOUT	13	HBM	±15	kV

**RECEIVER SECTION**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> -0.6	V <sub>CC</sub> -0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>off</sub>	Output leakage current	FORCEOFF = 0 V		±0.05	±10	µA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See Figure 3		150		ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See Figure 3		150		ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4		200		ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4		200		ns
t <sub>sk(p)</sub>	Pulse skew‡	See Figure 3		50		ns

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

‡ Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

**ESD protection**

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
RIN	8	HBM	±15	kV



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**AUTO-POWERDOWN SECTION****electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V <sub>T+(valid)</sub>	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
V <sub>T-(valid)</sub>	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
V <sub>T(invalid)</sub>	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V <sub>OH</sub>	$\overline{\text{INVALID}}$ high-level output voltage	I <sub>OH</sub> = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	V <sub>CC</sub> -0.6		V
V <sub>OL</sub>	$\overline{\text{INVALID}}$ low-level output voltage	I <sub>OL</sub> = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		0.4	V

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)**

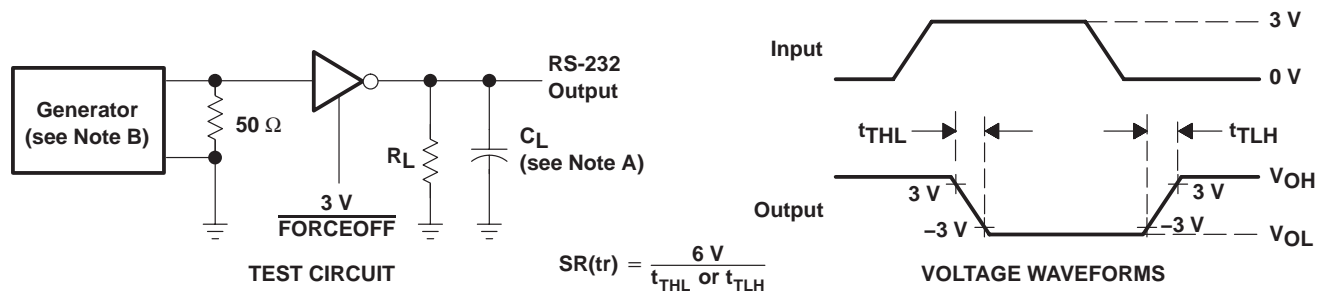
PARAMETER		MIN	TYP†	MAX	UNIT
t <sub>valid</sub>	Propagation delay time, low- to high-level output		1		μs
t <sub>invalid</sub>	Propagation delay time, high- to low-level output		30		μs
t <sub>en</sub>	Supply enable time		100		μs

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

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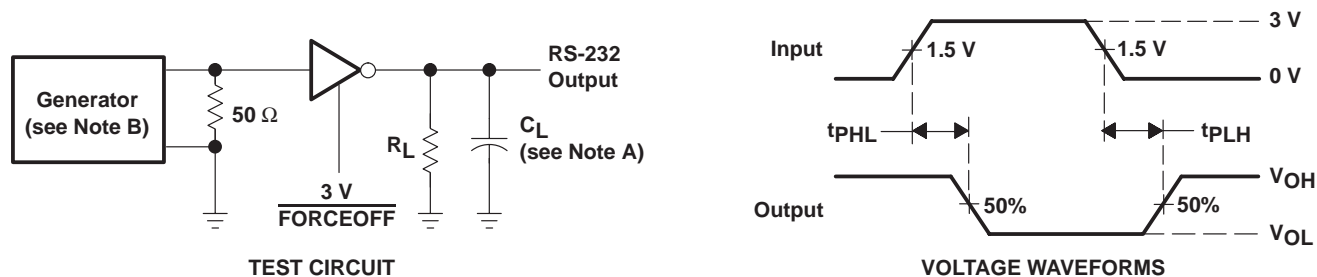
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**PARAMETER MEASUREMENT INFORMATION**



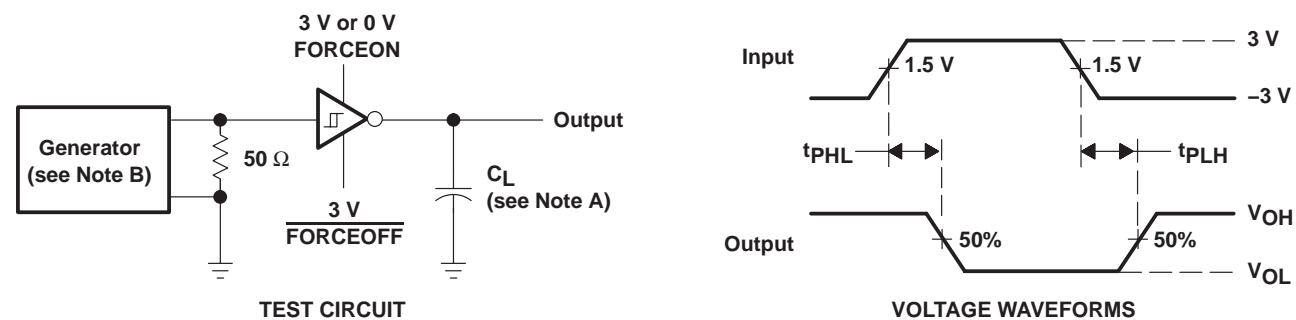
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 1. Driver Slew Rate**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 2. Driver Pulse Skew**



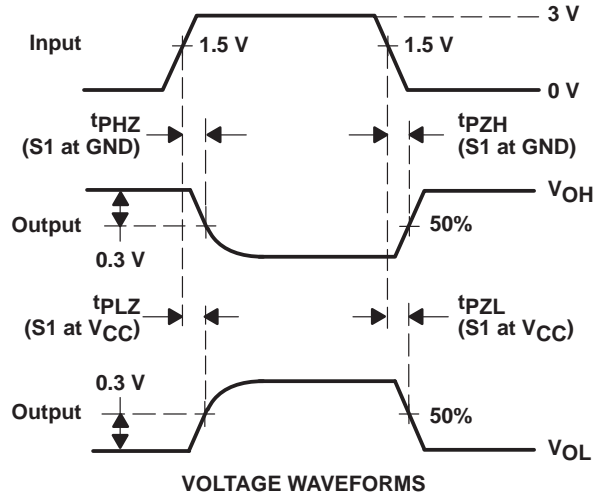
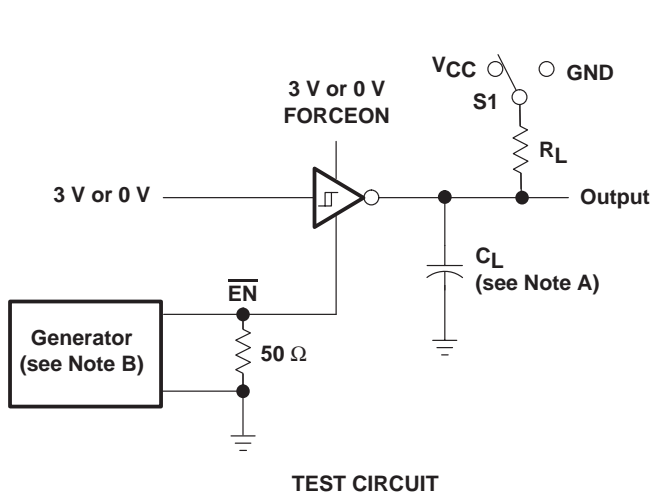
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 3. Receiver Propagation Delay Times**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .  
 C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

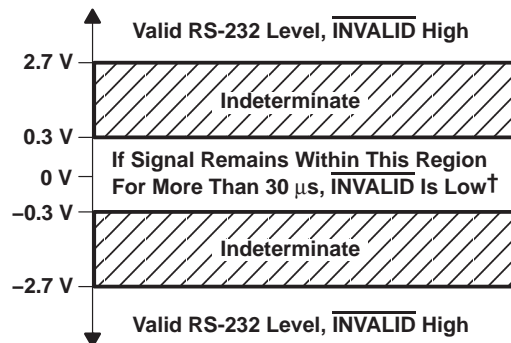
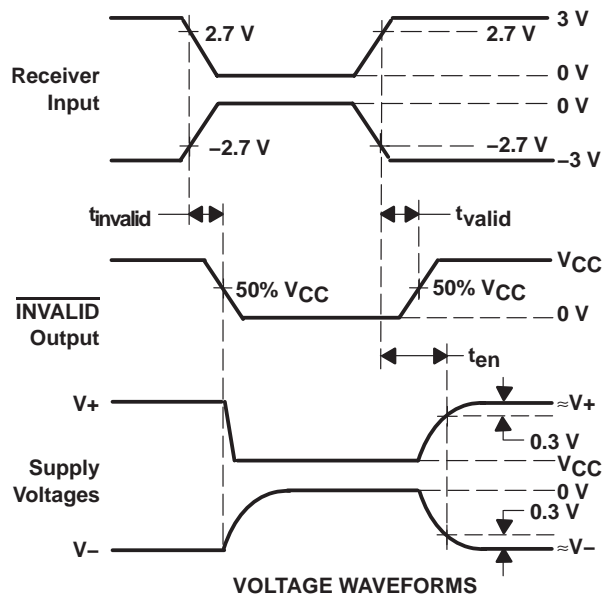
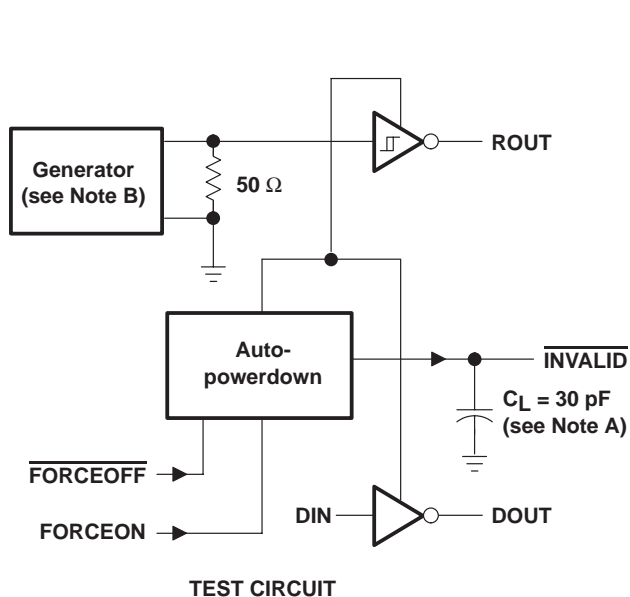
**Figure 4. Receiver Enable and Disable Times**



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**PARAMETER MEASUREMENT INFORMATION**



† Auto-powerdown disables drivers and reduces supply current to 1  $\mu$ A.

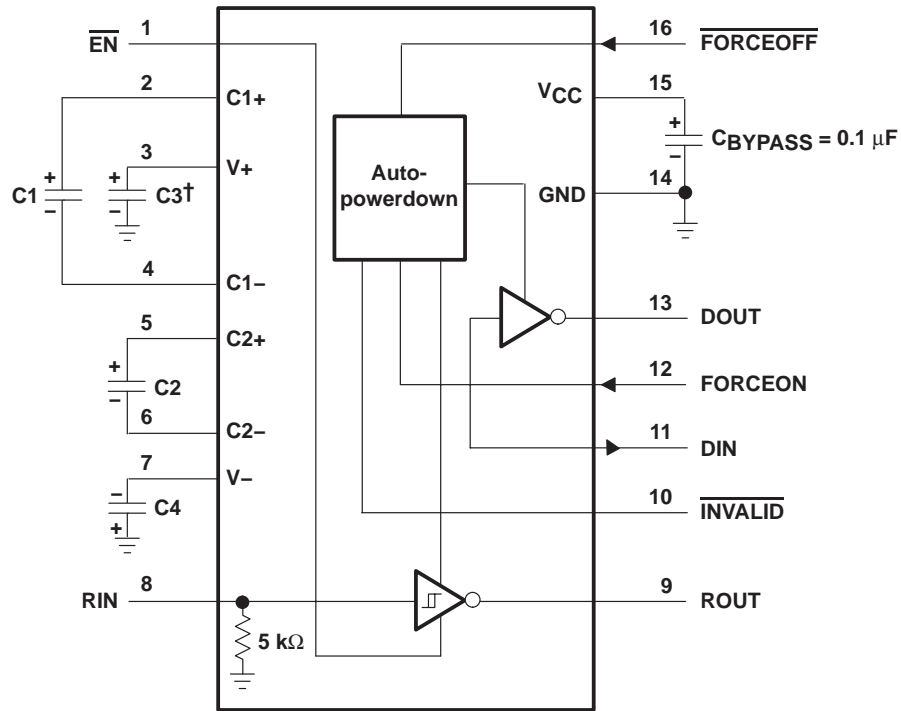
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

**Figure 5.  $\overline{\text{INVALID}}$  Propagation Delay Times and Driver Enabling Time**

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**APPLICATION INFORMATION**



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**V<sub>CC</sub> vs CAPACITOR VALUES**

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

**Figure 6. Typical Operating Circuit and Capacitor Values**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MAX3221CDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	<a href="#">Samples</a>
MAX3221IDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MAX3221IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>
MAX3221IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF MAX3221 :**

- Enhanced Product: [MAX3221-EP](#)

**NOTE: Qualified Version Definitions:**

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3221CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

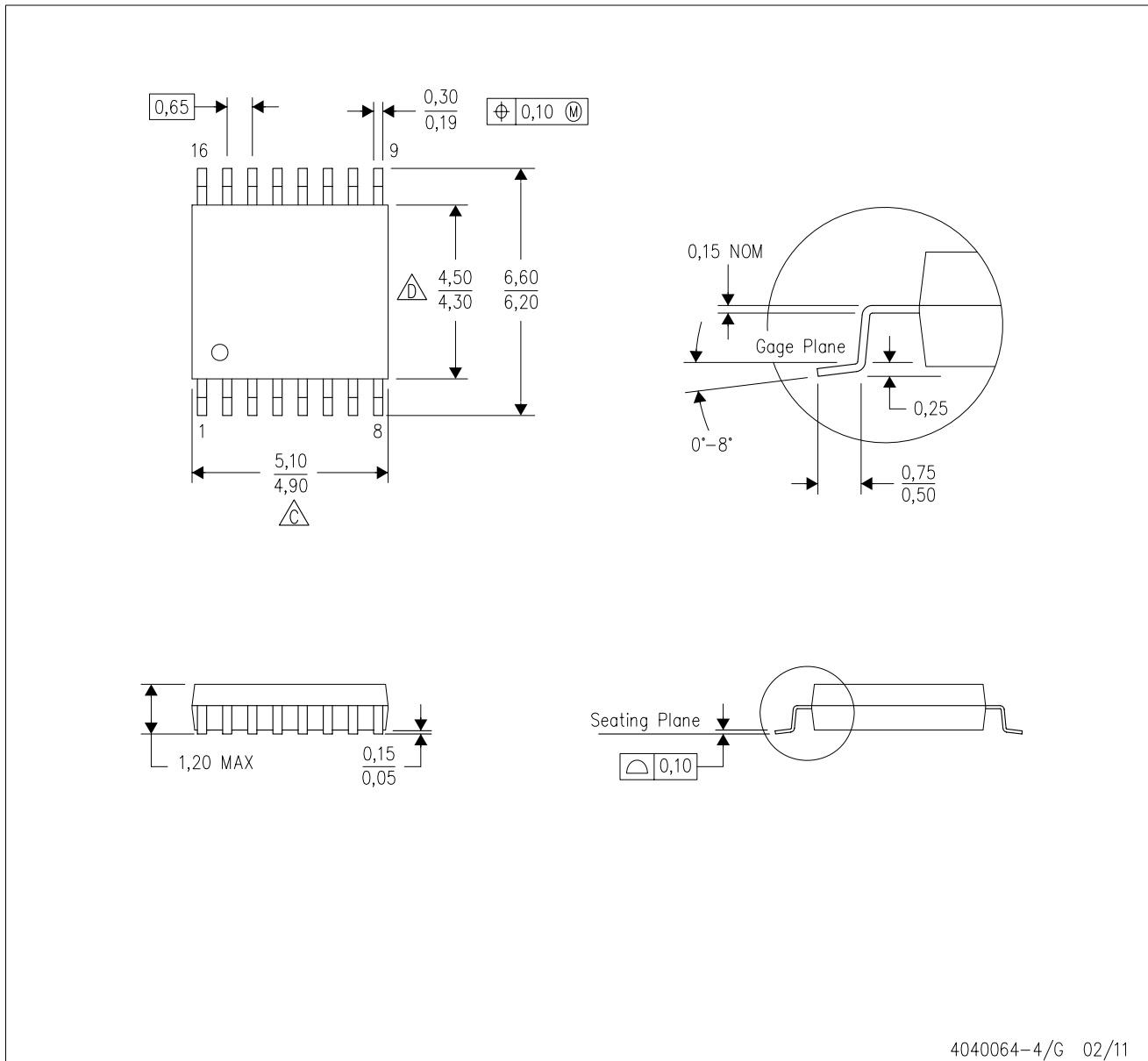
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3221CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3221IDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3221IPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX3221IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3221IPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



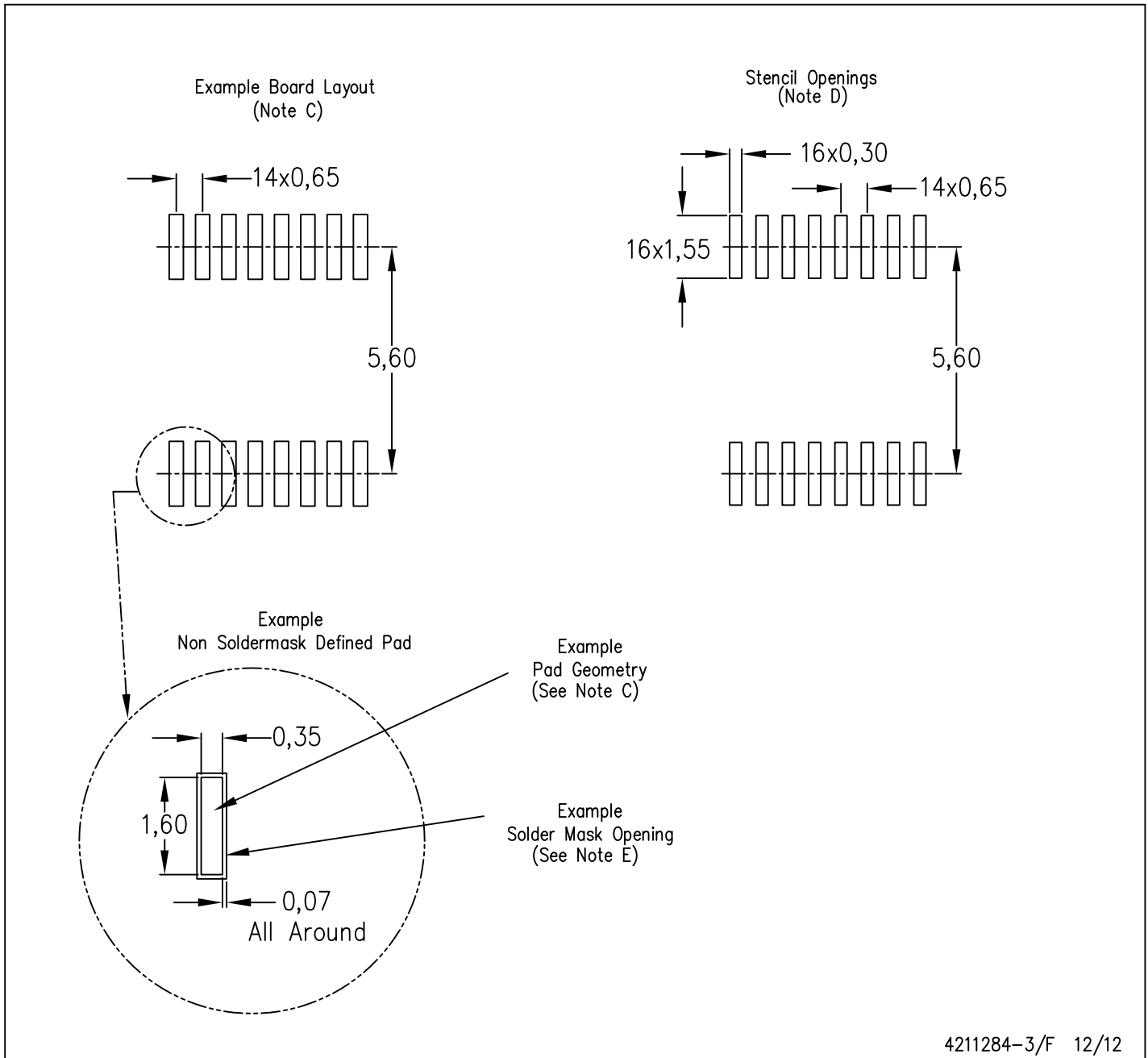
4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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