

### features

- Multi-Rate Operation from 155 Mbps Up To 2.5 Gbps
- Ultralow Power Consumption
- Input Offset Cancellation
- High Input Dynamic Range
- Output Disable
- Output Polarity Select
- CML Data Outputs

- Single 3.3-V Supply
- Surface Mount Small Footprint 3 mm × 3 mm 16-Pin QFN Package

### applications

- SONET/SDH Transmission Systems at OC3, OC12, OC24, OC48
- 1.0625-Gbps and 2.125-Gbps Fibre Channel Receivers
- Gigabit Ethernet Receivers

### description

The ONET2511PA is a versatile high-speed limiting amplifier for multiple fiber optic applications with data rates up to 2.5 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV<sub>p-p</sub>.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1800 mV<sub>p-p</sub>.

The ONET2511PA is available in a small footprint 3 mm × 3 mm 16-pin QFN package. The circuit requires a single 3.3-V supply.

This power efficient limiting amplifier is characterized for operation from –40°C to 85°C.



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# ONET2511PA 155-Mbps TO 2.5-Gbps LIMITING AMPLIFIER

SLLS604C – MARCH 2004 – REVISED OCTOBER 2005

## block diagram

A simplified block diagram of the ONET2511PA is shown in Figure 1.

This compact, low power 2.5-Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

The limiting amplifier requires a single 3.3-V supply voltage. All circuit parts are described in detail below.

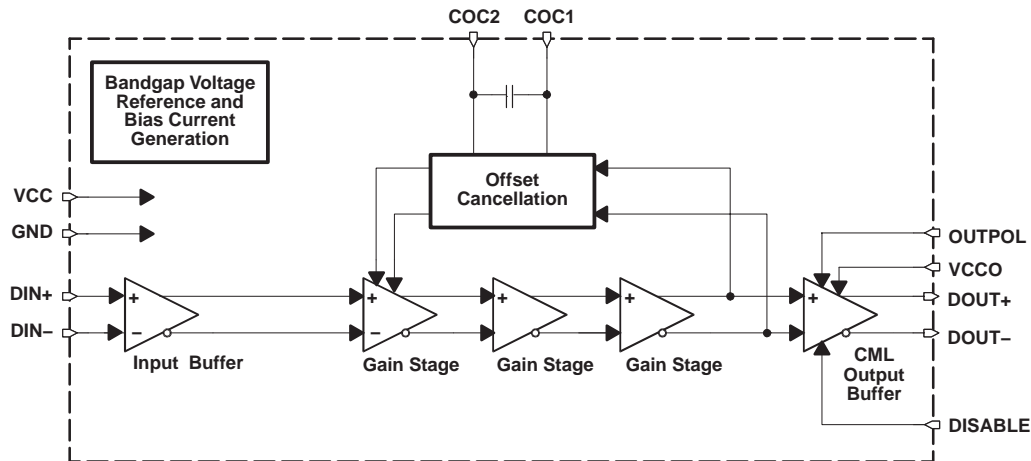


Figure 1. Block Diagram

## high-speed data path

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN-. The data path consists of the input stage with  $2 \times 50\text{-}\Omega$  on-chip line termination to VCC, three gain stages which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT-, which provide  $2 \times 50\text{-}\Omega$  back-termination to VCCO. The output stage also includes a data polarity switching function, which is controlled by the OUTPUTPOL input and a disable function, controlled by the signal applied to the DISABLE input pin.

An offset cancellation compensates inevitable internal offset voltages and thus ensures proper operation even for small input data signals.

The low frequency cutoff is as low as 45 kHz with the built-in filter capacitor.

For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

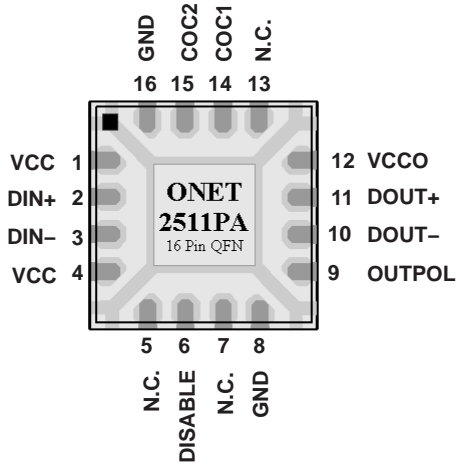
## bandgap voltage and bias generation

The ONET2511PA limiting amplifier is supplied by a single  $3.3\text{-V} \pm 10\%$  supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

**package**

For the ONET2511PA a small footprint 3 mm × 3 mm 16-pin QFN package is used, with a lead pitch of 0,5 mm. The pinout is shown in Figure 2.



**Figure 2. Pinout of ONET2511PA in a 3 mm × 3 mm 16-Pin QFN Package (Top View)**

**terminal functions**

The following table shows a pin description for the ONET2511PA in a 3 mm x 3 mm 16-pin QFN package.

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4	Supply	3.3-V ±10% supply voltage
DIN+	2	Analog in	Noninverted data input. On-chip 50-Ω terminated to VCC
DIN-	3	Analog in	Inverted data input. On-chip 50-Ω terminated to VCC
N.C.	5, 7, 13		Not connected
DISABLE	6	CMOS in	Disables CML output stage when set to high level
GND	8, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
OUTPUTPOL	9	CMOS in	Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.
DOUT-	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCCO
DOUT+	11	CML out	Noninverted data output. On-chip 50-Ω back-terminated to VCCO
VCCO	12	Supply	3.3-V ±10% supply voltage for output stage
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

# ONET2511PA

## 155-Mbps TO 2.5-Gbps LIMITING AMPLIFIER

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### absolute maximum ratings

over operating free-air temperature range unless otherwise noted†

		VALUE	UNIT
V <sub>CC</sub> , V <sub>CCO</sub>	Supply voltage, See Note 1	-0.3 to 4	V
V <sub>DIN+</sub> , V <sub>DIN-</sub>	Voltage at DIN+, DIN-, See Note 1	0.5 to 4	V
V <sub>DISABLE</sub> , V <sub>OUTPOL</sub> , V <sub>DOUT+</sub> , V <sub>DOUT-</sub> , V <sub>COC1</sub> , V <sub>COC2</sub>	Voltage at TH, DISABLE, OUTPOL, DOUT+, DOUT-, COC1, and COC2, See Note 1	-0.3 to 4	V
V <sub>COC_DIFF</sub>	Differential voltage between COC1 and COC2	±1	V
V <sub>DIN_DIFF</sub>	Differential voltage between DIN+ and DIN-	±2.5	V
I <sub>DIN+</sub> , I <sub>DIN-</sub> , I <sub>DOUT+</sub> , I <sub>DOUT-</sub>	Continuous current at inputs and outputs	-25 to 25	mA
ESD	ESD rating at all pins except V <sub>CCO</sub>	3	kV (HBM)
	ESD rating at V <sub>CCO</sub>	1.1	
T <sub>J(max)</sub>	Maximum junction temperature	125	°C
T <sub>stg</sub>	Storage temperature range	-65 to 85	°C
T <sub>A</sub>	Characterized free-air operating temperature range	-40 to 85	°C
T <sub>L</sub>	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

### recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V <sub>CC</sub> , V <sub>CCO</sub>	3	3.3	3.6	V
Operating free-air temperature, T <sub>A</sub>	-40		85	°C

### dc electrical characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub> , V <sub>CCO</sub>	Supply voltage	3	3.3	3.6	V
I <sub>VCC</sub>	Supply current		22	28	mA
V <sub>OD</sub>	Differential data output voltage swing		0.25	10	mV <sub>p-p</sub>
		DISABLE = high	600	780	1200
R <sub>IN</sub> , R <sub>OUT</sub>	Data input/output resistance		50		Ω
V <sub>IN,MIN</sub>	Data input sensitivity		3	5	mV <sub>p-p</sub>
V <sub>IN,MAX</sub>	Data input overload	1800			mV <sub>p-p</sub>
	CMOS input high voltage	2.1			V
	CMOS input low voltage			0.6	V



**ac electrical characteristics**

over recommended operating conditions (unless otherwise noted), typical operating condition is at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$

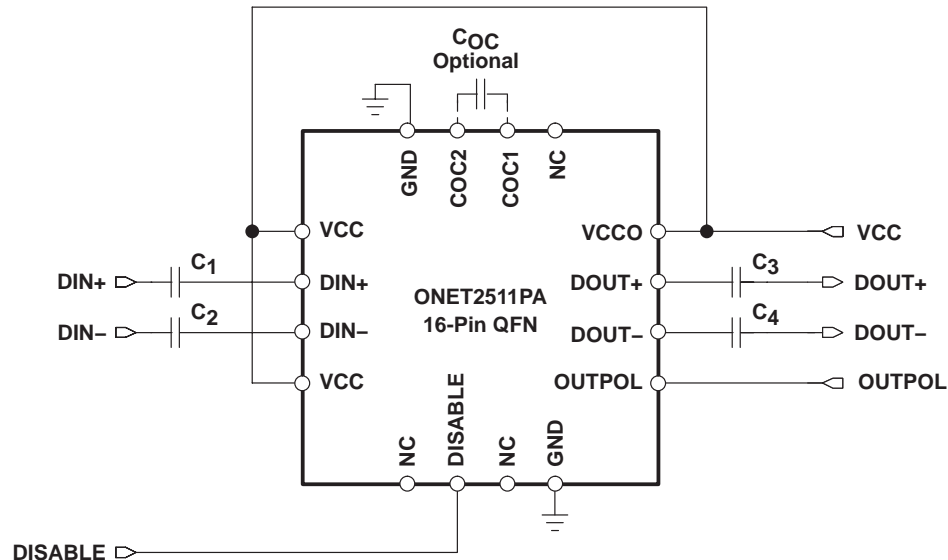
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency -3-dB bandwidth	$C_{OC} = \text{open}$		45	70	kHz
	$C_{OC} = 100\text{ nF}$		0.8		
Data rate		2.5			Gb/s
VNI Input referred noise				300	$\mu\text{VRMS}$
DJ Deterministic jitter, See Note 2	K28.5 pattern at 2.5 Gbps		8.5	25	$\text{ps}_{\text{p-p}}$
	$2^{23}-1$ PRBS equivalent pattern at 2.5 Gbps		9.3	30	
	$2^{23}-1$ PRBS equivalent pattern at 155 Mbps		25	50	
RJ Random jitter	Input = 5 mVpp		6.5		$\text{ps}_{\text{RMS}}$
	Input = 10 mVpp		3		
$t_r$ Output rise time	20% to 80%		60	85	ps
$t_f$ Output fall time	20% to 80%		60	85	ps
PSNR Power supply noise rejection	$f < 2\text{ MHz}$	26			dB
$t_{DIS}$ Disable response time			20		ns

NOTE 2: Deterministic jitter does not include pulse-width distortion due to residual small output offset voltage.

**APPLICATION INFORMATION**

Figure 3 shows the ONET2511PA connected with an ac-coupled interface to the data signal source as well as to the output load.

The ac-coupling capacitors  $C_1$  through  $C_4$  in the input and output data signal lines are the only required external components. In addition, an optional external filter capacitor ( $C_{OC}$ ) may be used if a lower cutoff frequency is desired.

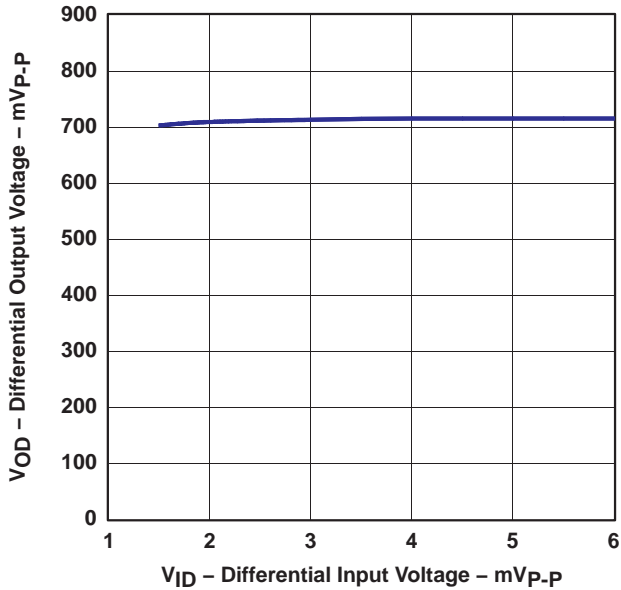


**Figure 3. Basic Application Circuit With AC-Coupled I/Os**

**TYPICAL CHARACTERISTICS**

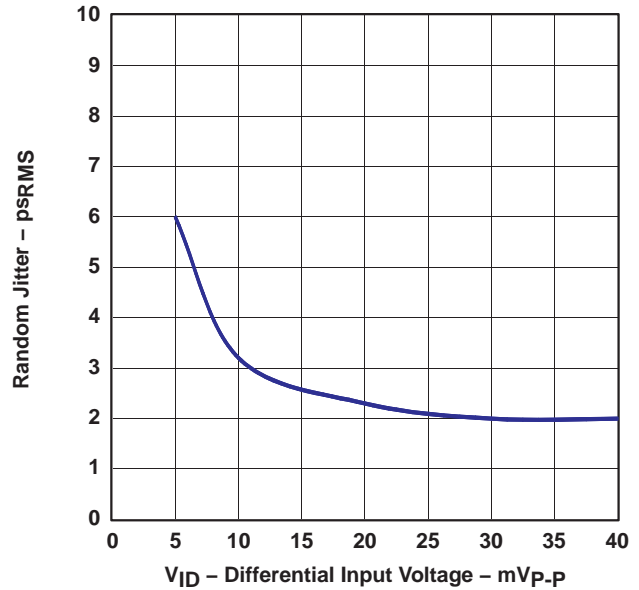
Typical operating condition is at  $V_{CC} = V_{CCO} = +3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

**DIFFERENTIAL OUTPUT VOLTAGE**  
**vs**  
**DIFFERENTIAL INPUT VOLTAGE**



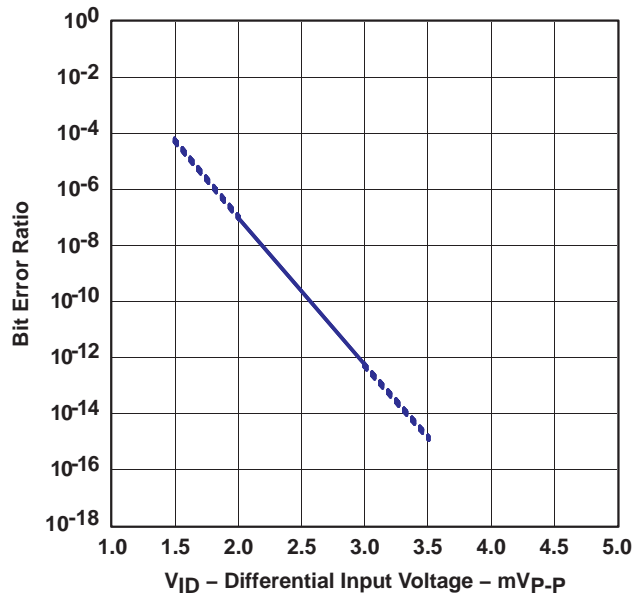
**Figure 4**

**RANDOM JITTER**  
**vs**  
**DIFFERENTIAL INPUT VOLTAGE**



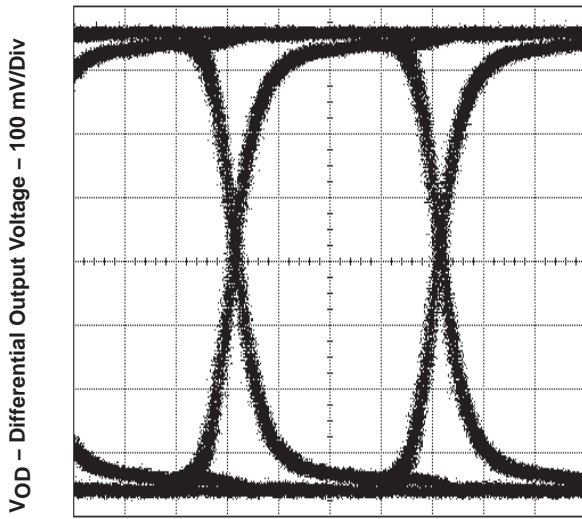
**Figure 5**

**BIT ERROR RATIO**  
**vs**  
**DIFFERENTIAL INPUT VOLTAGE**



**Figure 6**

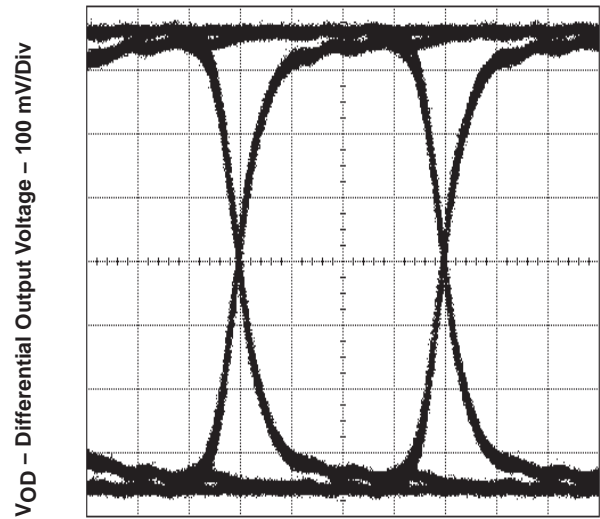
**OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND  
 MINIMUM INPUT VOLTAGE (5 mV<sub>p-p</sub>)**



t – Time – 100 ps/Div

**Figure 7**

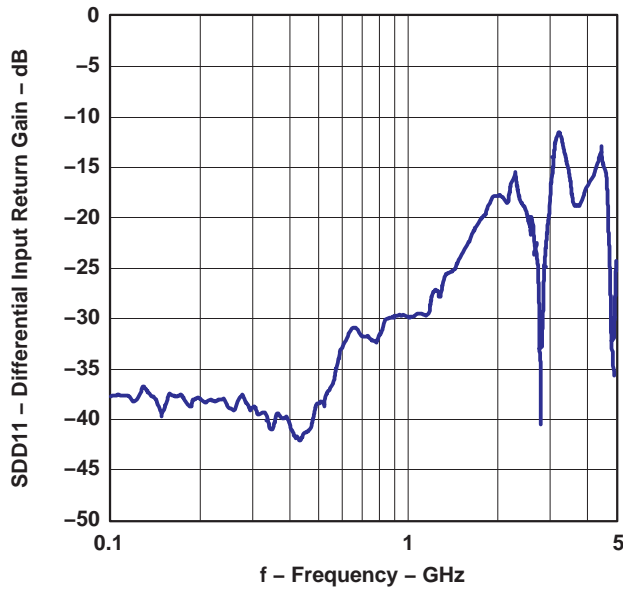
**OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND  
 MAXIMUM INPUT VOLTAGE (1800 mV<sub>p-p</sub>)**



t – Time – 100 ps/Div

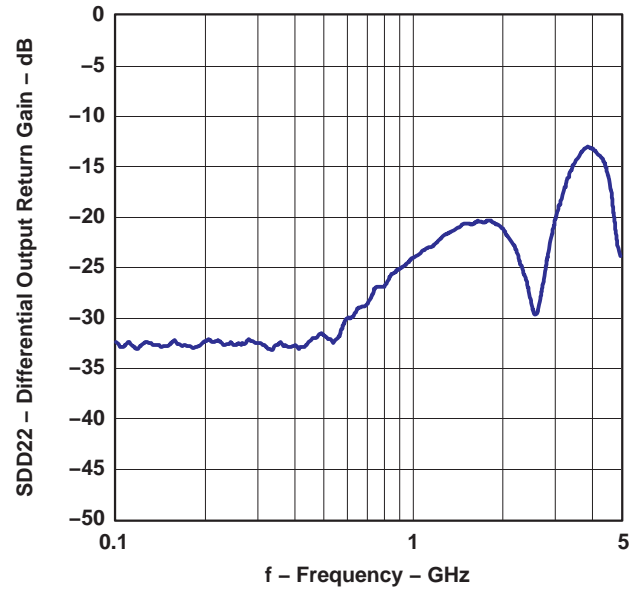
**Figure 8**

**DIFFERENTIAL INPUT RETURN GAIN  
 VS  
 FREQUENCY**



**Figure 9**

**DIFFERENTIAL OUTPUT RETURN GAIN  
 VS  
 FREQUENCY**



**Figure 10**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ONET2511PARGTR	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85	251P	
ONET2511PARGTRG4	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85		
ONET2511PARGTT	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85	251P	
ONET2511PARGTTG4	OBSOLETE	QFN	RGT	16		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

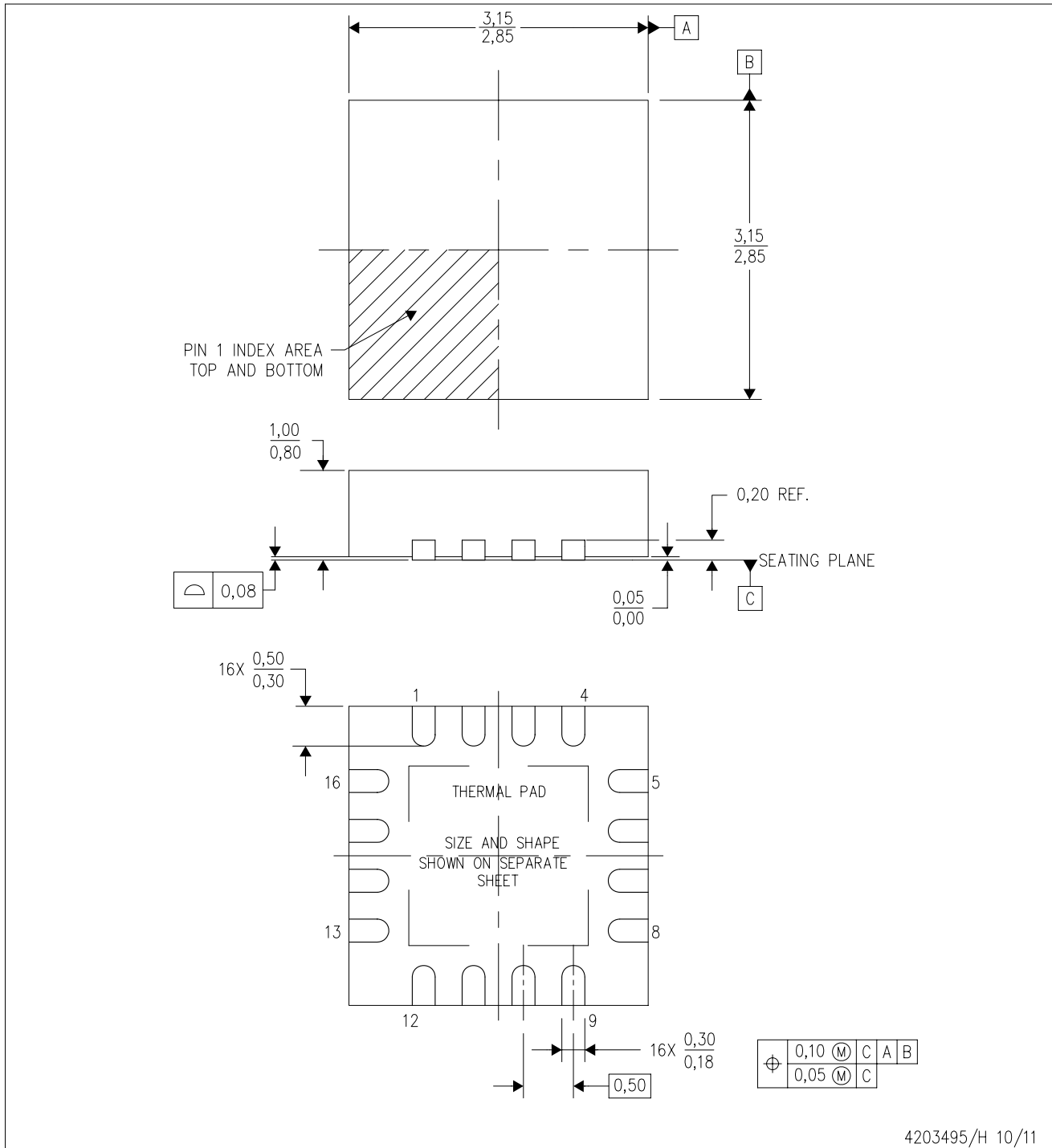
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RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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