

155-Mbps to 4.25-Gbps LASER DRIVER

Check for Samples: [ONET4201LD](#)

FEATURES

- **Multirate Operation From 155 Mbps up to 4.25 Gbps**
- **Bias Current Programmable From 1 mA to 100 mA**
- **Modulation Current Programmable From 5 mA to 85 mA**
- **APC and Fault Detection**
- **Fault Mode Selection**
- **Bias and Photodiode Current Monitors**
- **CML Data Inputs**
- **Temperature Compensation of Modulation Current**
- **Single 3.3-V Supply**
- **Active Back-Termination at the Output**
- **Surface-Mount, Small-Footprint, 4-mm × 4-mm, 24-Lead QFN Package**

APPLICATIONS

- **SONET/SDH Transmission Systems**
- **Fibre Channel Optical Modules**
- **Fiber Optic Data Links**
- **Digital Cross-Connects**
- **Optical Transmitters**

DESCRIPTION

The ONET4201LD is a laser driver for multiple fiber optic applications up to 4.25 Gbps. The device accepts CML input data and provides bias and modulation currents for driving a laser diode. Also provided are automatic power control (APC), temperature compensation of modulation current, fault detection, and current monitor features.

The device is available in a small-footprint, 4-mm × 4-mm, 24-pin, QFN package. The circuit requires a single 3.3-V supply.

This power-efficient laser driver is characterized for operation from –40°C to 85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DETAILED DESCRIPTION

BLOCK DIAGRAM

A simplified block diagram of the ONET4201LD is shown in Figure 1.

This compact, low-power, 4.25-Gbps laser driver circuit consists of a high-speed data path and a bias and control block.

The function of the data path is to buffer the input data and then modulate the laser diode current according to the input data stream.

The bias and control block generates the laser diode bias current, contains automatic power control (APC) to maintain constant optical output power, generates a modulation current that can be temperature compensated and controls power-on during start-up and shutdown after failure detection. The circuit design is optimized for high-speed and low-voltage operation (3.3 V).

The main circuit blocks are described in detail below.

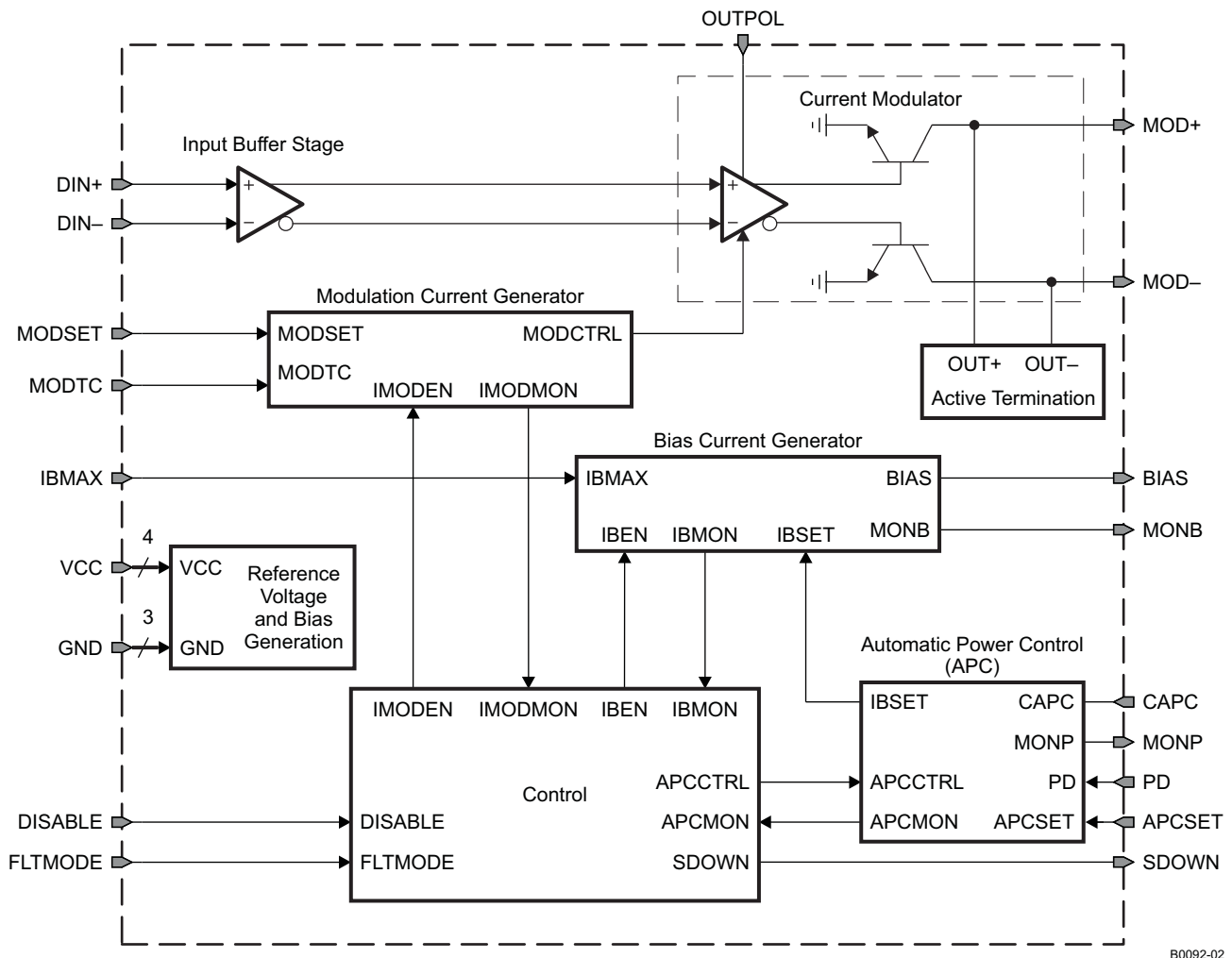


Figure 1. Simplified Block Diagram of the ONET4201LD

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HIGH-SPEED DATA PATH

The high-speed data path consists of an input buffer stage and a current modulator.

The input buffer stage takes CML compatible differential signals. It provides on-chip 50-Ω termination to VCC. AC-coupling may be used at the DIN+ and DIN– inputs.

The laser diode current modulator mainly consists of two common-emitter output transistors and the required driver circuitry. Depending on the input data stream, the modulation current is sunk at the MOD+ or the MOD– pin.

Modulation current setting is performed by means of the modulation current generator block, which is supervised by the control circuit block.

The laser diode can be either ac- or dc-coupled. In both cases, the maximum modulation current is 85 mA. The modulation output is optimized for driving a 20-Ω load.

For optimum performance when driving a laser diode over a 20-Ω transmission line, the ONET4201LD provides active 20-Ω back-termination, which minimizes jitter caused by reflections.

BIAS AND CONTROL

The bias and control circuitry consists of the bandgap voltage and bias generation block, the bias current generator, the automatic power control block and the supervising control circuitry.

BANDGAP VOLTAGE AND BIAS GENERATION

The bandgap voltage reference provides process and temperature-independent reference voltages needed to set bias current, modulation current, and photodiode reference current. Additionally, this block provides the biasing for all internal circuits.

AUTOMATIC POWER CONTROL

The ONET4201LD laser driver incorporates an APC loop to compensate for the changes in laser threshold current over temperature and lifetime. The internal APC is enabled when resistors are connected to the IBMAX and APCSET pins. A back-facet photodiode mounted in the laser package is used to detect the average laser output power. The photodiode current I_{PD} , which is proportional to the average laser power, can be calculated by using the laser-to-monitor transfer ratio, ρ_{MON} , and the average power, P_{AVG} :

$$I_{PD} [A] = P_{AVG} [W] \times \rho_{MON} [A/W] \quad (1)$$

In closed-loop operation, the APC modifies the laser diode bias current by comparing I_{PD} with a reference current I_{APCSET} and generates a bias compensation current. I_{PD} can be programmed by selecting the external resistor R_{APCSET} according to:

$$R_{APCSET} [\Omega] = \frac{4.69 V}{I_{PD} [A]} = \frac{4.69 V}{P_{AVG} [W] \times \rho_{MON} [A/W]} \quad (2)$$

The bias compensation current subtracts from the maximum bias current to maintain the monitor photodiode current. The maximum bias current is programmed by the resistor connected to IBMAX:

$$I_{BIASMAX} [A] = \frac{343 V}{R_{BIASMAX} [\Omega]} \quad (3)$$

This current limit establishes the maximum bias current available in closed loop mode, as well as in transient fault conditions such as shorts at the PD pin to ground or delayed laser power up.

An external pin MONB is provided as a bias current monitor output. A fraction of the bias current (1/68) is mirrored and develops a voltage drop across an external resistor to ground, R_{MONB} . The voltage at MONB is given as:

$$V_{MONB} [V] = \frac{R_{MONB} [\Omega] \times I_{BIAS} [A]}{68} \quad (4)$$

If the voltage at MONB is greater than the programmed threshold, a fault mode occurs.

The MONP is also provided as a photocurrent monitor output. The photodiode current, I_{PD} , is mirrored and develops a voltage across an external resistor to ground, R_{MONP} . The voltage at MONP is given as:

$$V_{MONP}[V] = R_{MONP}[\Omega] \times I_{PD}[A] \quad (5)$$

If the voltage at MONP is greater than the programmed threshold, a fault mode occurs.

As with any negative-feedback system design, care must be taken to assure stability of the loop. The loop bandwidth must not be too high in order to minimize pattern-dependent jitter. The dominant pole is determined by the capacitor C_{APC} . The recommended value for C_{APC} is 200 nF. The capacitance of the monitor photodiode C_{PD} adds another pole to the system, and thus it must be small enough to maintain stability. The recommended value for this capacitance is $C_{PD} \leq 50$ pF.

The internal APC loop can be disabled by connecting a 100-k Ω resistor from APCSET to VCC and leaving PD open. In open-loop operation, the laser diode current is set by $I_{BIASMAX}$ and I_{MODSET} .

MODULATION-CURRENT GENERATOR

The modulation-current generator defines the tail current of the modulator, which is sunk from either MOD+ or MOD–, depending on the data pattern. The modulation current consists of a modulation current I_{MOD0} at a reference temperature $T_0 = 60^\circ\text{C}$ (set by the resistor R_{MODSET}) and a temperature-dependent modulation current defined by the resistor R_{MODTC} . The modulation current can be estimated as follows:

$$I_{MOD}[A] = \frac{265 \text{ V}}{R_{MODSET}[\Omega]} \times \left(1 + \left(\frac{24 \Omega}{R_{MODTC}[\Omega]} + 630 \text{ ppm} \right) \times (T[^\circ\text{C}] - T_0[^\circ\text{C}]) \right) \quad (6)$$

Note that the reference temperature, T_0 , and the temperature compensation set by R_{MODTC} vary from part to part. To reduce the variation, I_{MOD} can be calibrated over temperature and set with a microcontroller DAC or digital potentiometer.

CONTROL

The functions of this block are to control the start-up sequence, detect faults, detect tracking failure of the APC loop, and provide disable control. The laser driver has a controlled start-up sequence, which helps prevent transient glitches from being applied to the laser during power on. At start-up, the laser diode is off, SDOWN is low, and the APC loop is open. Once V_{CC} reaches ~ 2.8 V, the laser diode bias generator and modulation current generator circuitry are activated (if DISABLE is low). The slow-start circuitry gradually brings up the current delivered to the laser diode. From the time that V_{CC} reaches ~ 2.8 V until the modulation current and bias current reach 95% of their steady state value, is considered the initialization time. If DISABLE is asserted during power on, the slow-start circuitry does not activate until DISABLE is negated.

FAULT DETECTION

The fault-detection circuitry monitors the operation of the ONET4201LD. If FLTMODE is set to a low level, (hard-fault mode) this circuitry disables the bias and modulation circuits and latches the SDOWN output on detection of a fault. The fault mode is reset by toggling DISABLE (for a minimum time of T_{RES}) or by toggling V_{CC} .

Once DISABLE is toggled, SDOWN is set low and the circuit is re-initialized.

If FLTMODE is set to a high level (soft-fault mode), a fault is indicated at the SDOWN output; however, the bias and modulation circuits are not disabled. The SDOWN output is reset once the fault causing condition disappears. Toggling DISABLE or V_{CC} is not required.

A functional representation of the fault detection circuitry is shown in [Figure 2](#).

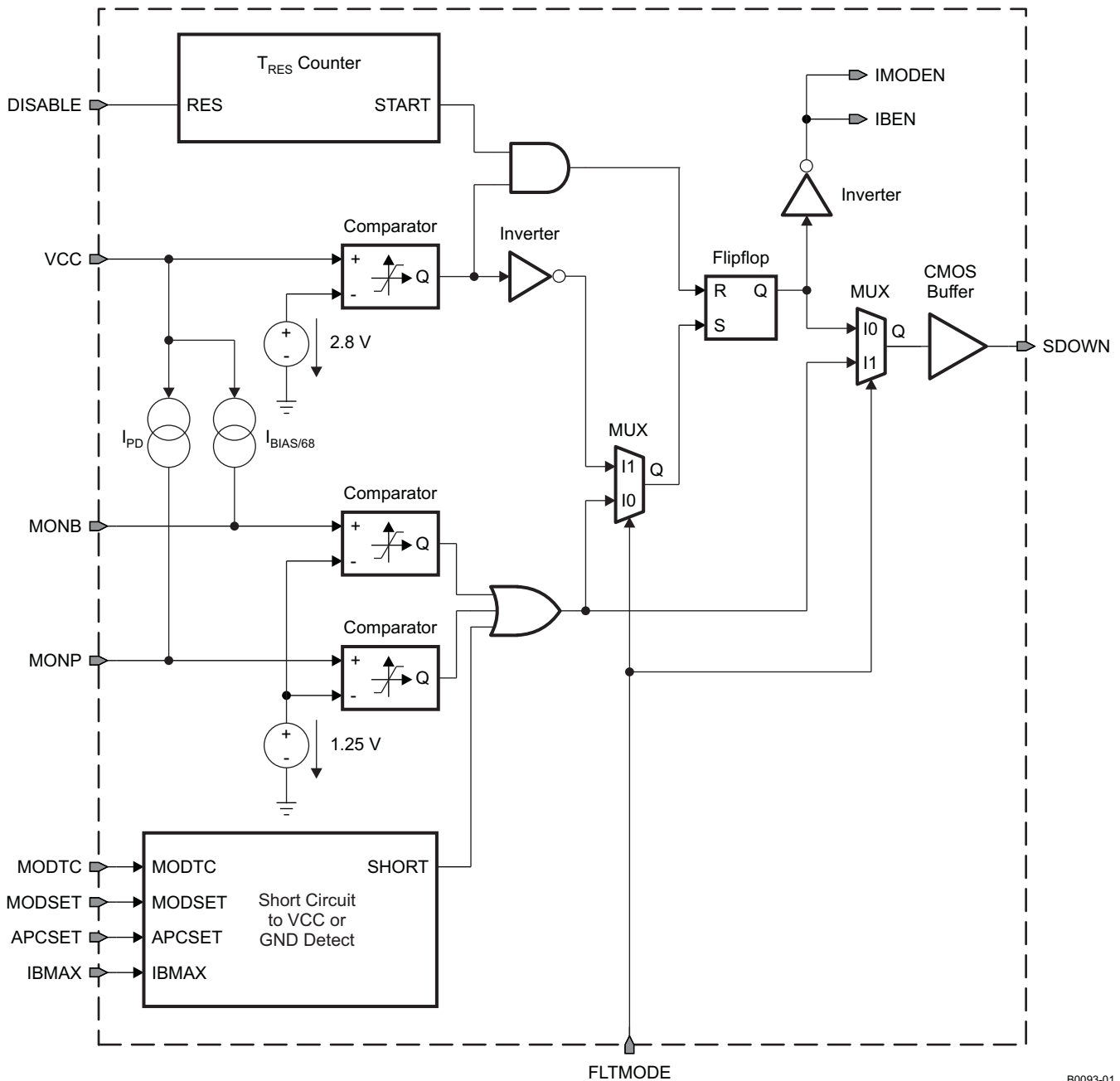


Figure 2. Functional Representation of the Fault Detection Circuitry

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A fault mode is produced if the laser cathode is grounded and the photocurrent causes MONP to exceed its programmed threshold. Another fault mode can be produced if the laser diode end-of-life condition causes excessive bias current and photodiode current that results in monitor voltages (MONP, MONB) being greater than their programmed threshold. Other fault modes can occur if there are any I/O pin single-point failures (short to V_{CC} or GND) and the monitor voltages exceed their programmed threshold (see [Table 1](#)).

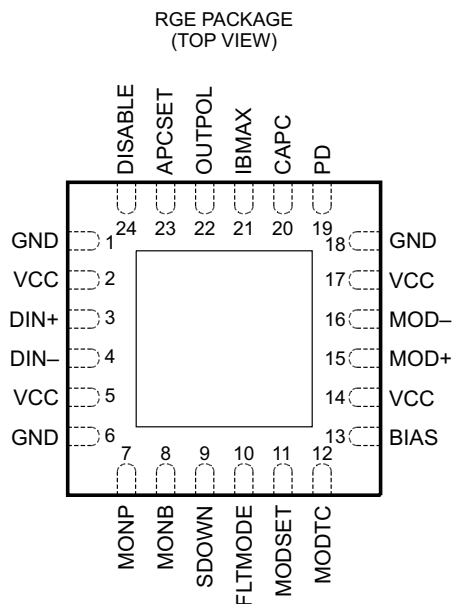
Table 1. Response to I/O-Pin Shorts to VCC or GND

| PIN | FLTMODE = LOW | | FLTMODE = HIGH | |
|---------|---|---|---|---|
| | Response to Short to GND | Response to Short to V _{CC} | Response to Short to GND | Response to Short to V _{CC} |
| APCSET | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault, I _{MOD} unaffected | SDOWN high, I _{BIAS} and I _{MOD} unaffected | No fault |
| BIAS | SDOWN latched high, I _{MOD} disabled | No fault, I _{BIAS} goes to zero | SDOWN high, I _{MOD} unaffected | No fault, I _{MOD} unaffected |
| CAPC | No fault | No fault, I _{BIAS} goes to zero | No fault, I _{MOD} unaffected | No fault, I _{BIAS} goes to zero |
| DIN+ | No fault, I _{MOD} disabled | No fault | No fault, I _{MOD} disabled | No fault |
| DIN- | No fault, I _{MOD} disabled | No fault | No fault, I _{MOD} disabled | No fault |
| DISABLE | Normal circuit operation | Normal circuit operation | Normal circuit operation | Normal circuit operation |
| IBMAX | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | SDOWN high, I _{MOD} unaffected | SDOWN high, I _{MOD} unaffected |
| MOD+ | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault | SDOWN high, I _{BIAS} unaffected | No fault |
| MOD- | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault | SDOWN high, I _{BIAS} unaffected | No fault |
| MODSET | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault, disables I _{MOD} | SDOWN high, I _{BIAS} unaffected | No fault, disables I _{MOD} |
| MODTC | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault | SDOWN high, I _{BIAS} and I _{MOD} unaffected | No fault |
| MONB | No fault | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault | SDOWN high, I _{BIAS} and I _{MOD} unaffected |
| MONP | No fault | SDOWN latched high, I _{BIAS} and I _{MOD} disabled | No fault | SDOWN high, I _{BIAS} and I _{MOD} unaffected |
| OUTPOL | No fault, polarity reverses | No fault | No fault, polarity reverses | No fault |
| PD | No fault, I _{MOD} unaffected | No fault, I _{BIAS} goes to zero | No fault, I _{MOD} unaffected | No fault, I _{BIAS} goes to zero |
| SDOWN | No fault | No fault | No fault | No fault |

PACKAGE

For the ONET4201LD, a small-footprint, 4-mm x 4-mm, 24-lead QFN package is used, with a lead pitch of 0,5 mm. The pinout is shown in [Figure 3](#).

In order to achieve the required low thermal resistance of about 38 K/W, which keeps the maximum junction temperature below 115°C, a good thermal connection of the exposed die pad is mandatory.



P0024-03

Figure 3. Pinout of the ONET4201LD in a 4-mm x 4-mm, 24-Lead QFN Package (Top View)

TERMINAL FUNCTIONS

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---------------|--------------|------------|--|
| APCSET | 23 | Analog-in | Set photodiode reference current with resistor to GND. |
| BIAS | 13 | Analog-out | Laser diode bias current sink. Connect to laser cathode. |
| CAPC | 20 | Analog | APC loop capacitor |
| DIN+ | 3 | CML-in | Noninverted data input. On-chip, 50-Ω terminated to VCC. |
| DIN- | 4 | CML-in | Inverted data input. On-chip, 50-Ω terminated to VCC. |
| DISABLE | 24 | LVTTL-in | Disable modulation and bias current outputs. |
| FLTMODE | 10 | CMOS-in | Fault mode selection input. If a low level is applied to this pin, any fault event is latched and the bias and modulation currents are disabled in a fault condition. Toggling of DISABLE or VCC resets the fault condition. If pin is set to a high level, fault events are flagged at the SDOWN output but not latched. The bias and modulation currents are not disabled. SDOWN is reset once the fault condition disappears. |
| GND | 1, 6, 18, EP | Supply | Circuit ground. The exposed die pad (EP) must be grounded. |
| IBMAX | 21 | Analog-in | Set maximum laser diode current with resistor to GND. |
| MOD+ | 15 | Analog-out | Laser modulation current output. Connect to laser cathode. Avoid usage of vias on board. |
| MOD- | 16 | Analog-out | Complementary laser modulation current output. Connect to VCC adjacent to anode of laser diode. Avoid usage of vias on board. |
| MODSET | 11 | Analog-in | Set temperature-independent modulation current with resistor to GND. |
| MODTC | 12 | Analog-in | Set modulation-current temperature compensation with resistor to GND. |
| MONB | 8 | Analog-out | Bias current monitor sources 1/68 of the bias current |
| MONP | 7 | Analog-out | Photodiode current monitor sources a current identical to the photodiode current |
| OUTPOL | 22 | LVTTL-in | Alters modulation current output polarity. Open or high: normal polarity, low: inverted polarity. OUTPOL is pulled up internally. Normal polarity: when DIN+ is high, current is sunk into MOD+. |
| PD | 19 | Analog-in | Monitor photodiode input. Connect to photodiode anode for APC. Sinks the photodiode current to GND. |
| SDOWN | 9 | LVTTL-out | Fault detection flag |
| VCC | 2, 5, 14, 17 | Supply | 3.3 V ±10% supply voltage |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | UNIT |
|--|---|-----------------------------|----------|
| V _{CC} | Supply voltage ⁽²⁾ | –0.3 to 4 | V |
| I _{BIAS} | Current into BIAS | –20 to 120 | mA |
| I _{IMOD+} , I _{IMOD–} | Current into MOD+, MOD– | –20 to 120 | mA |
| I _{PD} | Current into PD | –5 to 5 | mA |
| V _{DIN+} , V _{DIN–} , V _{DISABLE} , V _{MONB} , V _{MONP} , V _{FLTMODE} , V _{SDOWN} | Voltage at DIN+, DIN–, DISABLE, MONB, MONP, FLTMODE, SDOWN ⁽²⁾ | –0.3 to 4 | V |
| V _{CAPC} , V _{IBMAX} , V _{MODSET} , V _{APCSET} , V _{MODTC} | Voltage at CAPC, IBMAX, MODSET, APCSET, MODTC ⁽²⁾ | –0.3 to 3 | V |
| V _{MOD+} , V _{MOD–} | Voltage at MOD+, MOD– ⁽²⁾ | 0.6 to V _{CC} +1.5 | V |
| V _{BIAS} | Voltage at BIAS ⁽²⁾ | 1 to 3.5 | V |
| ESD | ESD rating at all pins except MOD+, MOD– | 2 | kV (HBM) |
| | ESD rating at MOD+, MOD– | 1 | |
| T _{J,max} | Maximum junction temperature | 150 | °C |
| T _{stg} | Storage temperature range | –65 to 150 | °C |
| T _A | Characterized free-air operating temperature range | –40 to 85 | °C |
| T _{LEAD} | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V _{CC} | Supply voltage | 3 | 3.3 | 3.6 | V |
| T _A | Operating free-air temperature | –40 | | 85 | °C |

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|------|------|--------|--------|
| V _{CC} | Supply voltage | | 3 | 3.3 | 3.6 | V |
| I _{VCC} | Supply current | I _{MOD} = 30 mA, I _{BIAS} = 20 mA (excluding I _{MOD} , I _{BIAS}) | 32 | | | mA |
| | | I _{MOD} = 60 mA, I _{BIAS} = 100 mA (excluding I _{MOD} , I _{BIAS}) | 55 | | | mA |
| I _{BIAS} | Bias current range | | 100 | | | mA |
| I _{BIAS-OFF} | Bias off-current | DISABLE = high or hard-fault mode; V _{BIAS} ≤ 3.5 V | 25 | | | μA |
| | Bias overshoot | During module hot plugging. V _{CC} turn on time must be ≤ 0.8 s | 10% | | | |
| | Bias current temperature stability | APC open loop | -480 | 480 | | ppm/°C |
| | Bias current absolute accuracy ⁽¹⁾ | I _{BIAS} ≥ 1 mA | -15% | 15% | | |
| | | I _{BIAS} = 1 mA, T _A = 25°C | ±15% | | | |
| | Bias current monitor gain | I _{BIAS} /I _{MONB} | 68 | | mA/ mA | |
| | MONB and MONP threshold range | A fault is never detected for V _{MONB/P} ≤ 1 V and a fault always occurs for V _{MONB/P} ≥ 1.35 V | 1 | 1.25 | 1.35 | V |
| | PD current monitor gain | I _{PD} /I _{MONP} | 1 | | mA/mA | |
| V _{ID} | Differential input signal | | 200 | 1600 | | mVp-p |
| | SDOWN output high voltage | I _{OH} = 100 μA sourcing | 2.4 | | V | |
| | SDOWN output low voltage | I _{OL} = 1 mA sinking | 0.4 | | V | |
| | DISABLE input impedance | | 4.7 | 7.4 | 10 | kΩ |
| | DISABLE input high voltage | | 2 | | V | |
| | DISABLE input low voltage | | 0.8 | | V | |
| V _{PD} | Monitor diode voltage | | 1.6 | | V | |
| | Monitor diode dc current range | | 18 | 1500 | | μA |

(1) Absolute accuracy refers to part-to-part variation.

AC ELECTRICAL CHARACTERISTICS

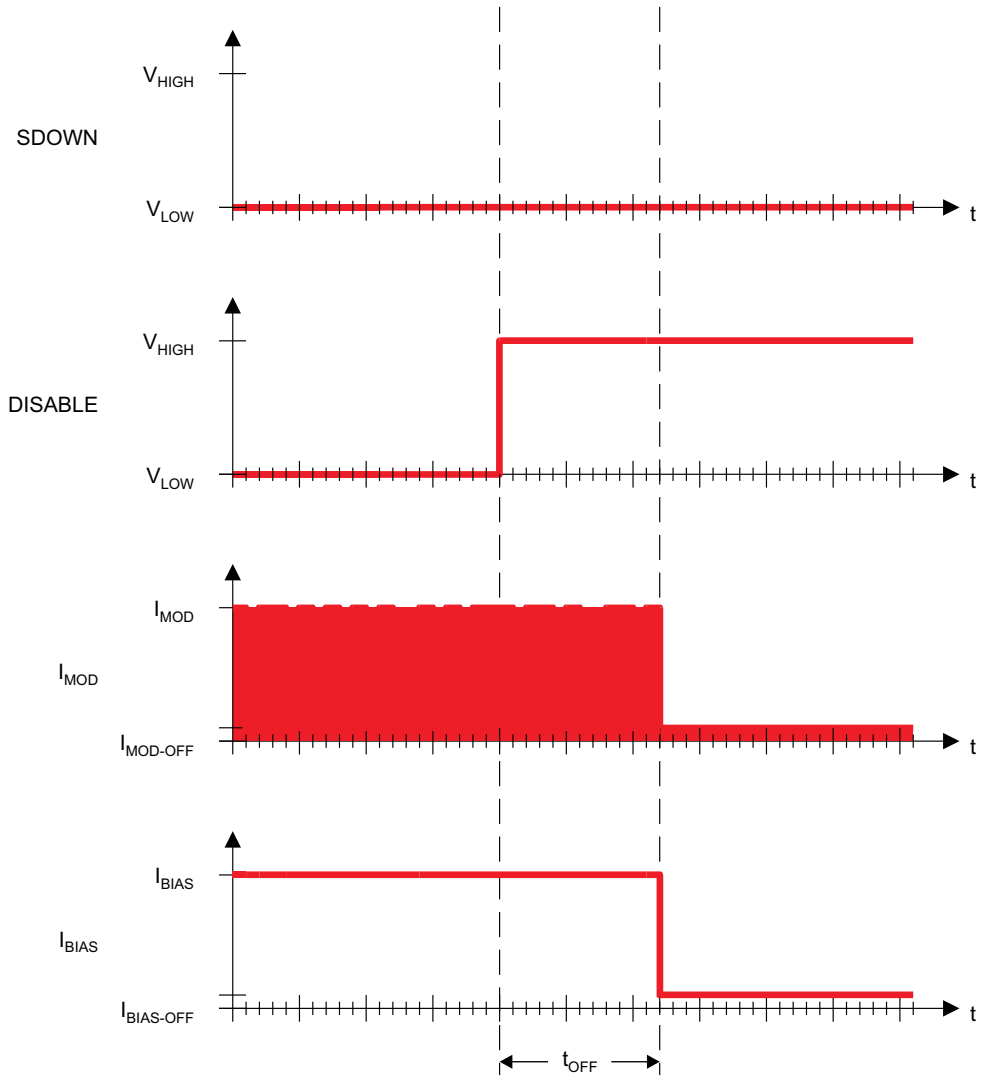
Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $I_{MOD} = 30\text{ mA}$, $I_{BIAS} = 20\text{ mA}$ and $T_A = 25^\circ\text{C}$, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--|--|--------|------------|-------|-----------------------|
| | Data Rate | | 4.25 | | | Gbps |
| I_{MOD} | Modulation current range | Current into MOD+/MOD- pin; $V_{MOD+}, V_{MOD-} \geq 0.6\text{ V}$ | 5 | | 85 | mA |
| $I_{MOD-OFF}$ | Modulation off-current | DISABLE = high or hard-fault occurred | | | 25 | μA |
| | Modulation current stability | | -600 | | 600 | ppm/ $^\circ\text{C}$ |
| | Modulation current absolute accuracy ⁽¹⁾ | $I_{MOD} = 10\text{ mA}$ | | $\pm 40\%$ | | |
| | | $I_{MOD} = 50\text{ mA}$ | | $\pm 25\%$ | | |
| | | $I_{MOD} = 80\text{ mA}$ | | $\pm 20\%$ | | |
| | Modulation current temperature compensation ⁽²⁾ | $R_{MODTC} = 3.125\text{ k}\Omega$ | | 8300 | | ppm/ $^\circ\text{C}$ |
| | | $R_{MODTC} = \text{Open}$ | | 630 | | |
| t_r | Output rise time (20% to 80%) | $V_{MOD+} \geq 1\text{ V}$, $V_{MOD-} \geq 1\text{ V}$, $I_{MOD} = 30\text{ mA}$ | | 55 | 75 | ps |
| t_f | Output fall time (20% to 80%) | $V_{MOD+} \geq 1\text{ V}$, $V_{MOD-} \geq 1\text{ V}$, $I_{MOD} = 30\text{ mA}$ | | 55 | 75 | ps |
| t_{OFF} | Disable assert time (see Figure 4) | Time from rising edge of DISABLE to when output currents fall below the maximum limits of $I_{MOD-OFF}$ and $I_{BIAS-OFF}$ | | 0.06 | 5 | μs |
| t_{ON} | Disable negate time (see Figure 5) | Time from falling edge of DISABLE to when output is 90% of nominal | | 80 | | μs |
| t_{INIT} | Time to initialize | From power on or negation of SDOWN using DISABLE | | 80 | | μs |
| t_{FAULT} | Fault assert time | Time from fault to SDOWN rising edge | | 3.3 | 50 | μs |
| t_{RESET} | DISABLE reset (see Figure 6) | Maximum spike pulse length at DISABLE being ignored | | | 0.8 | μs |
| | | Time DISABLE must be high to reset SDOWN | | | 6 | μs |
| | Output overshoot/undershoot | | -13.5% | | 13.5% | |
| | Random jitter | $I_{MOD} = 60\text{ mA}$ | | 0.6 | 0.9 | ps _{RMS} |
| DJ | Deterministic jitter ⁽³⁾ | $10\text{ mA} \leq I_{MOD} \leq 60\text{ mA}$, with K28.5 pattern at 4.25 Gbps | | 15 | 30 | ps _{p-p} |
| | | $10\text{ mA} \leq I_{MOD} \leq 60\text{ mA}$, with $2^{23} - 1$ PRBS or equivalent pattern at 2.67 Gbps | | 13 | 32 | ps _{p-p} |
| | | K28.5 pattern at 1.06 Gbps | | 5 | | ps _{p-p} |
| | | $2^{23} - 1$ PRBS or equivalent pattern at 155 Mbps | | 10 | | ps _{p-p} |

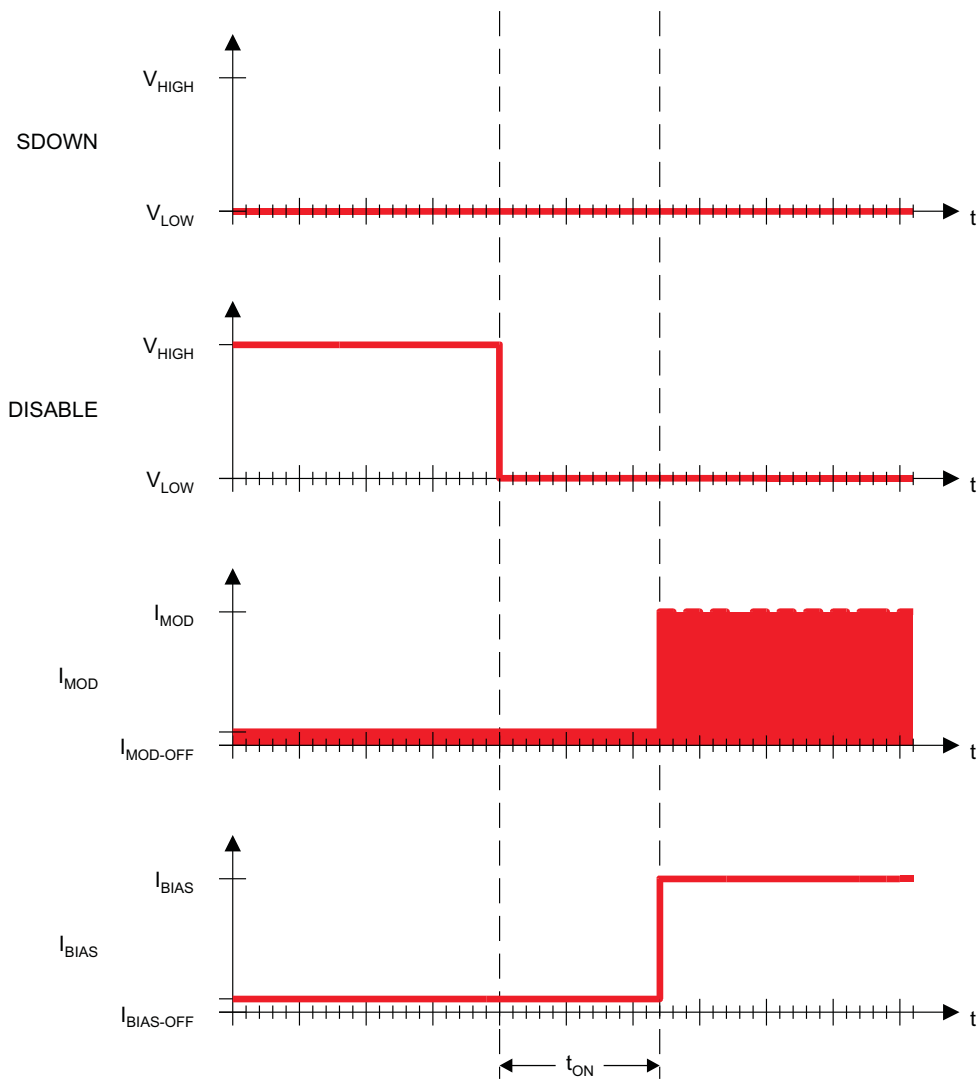
(1) Absolute accuracy refers to part-to-part variation.

(2) For a given external resistor connected to the MODTC pin, the modulation current temperature compensation will vary due to part-to-part variations.

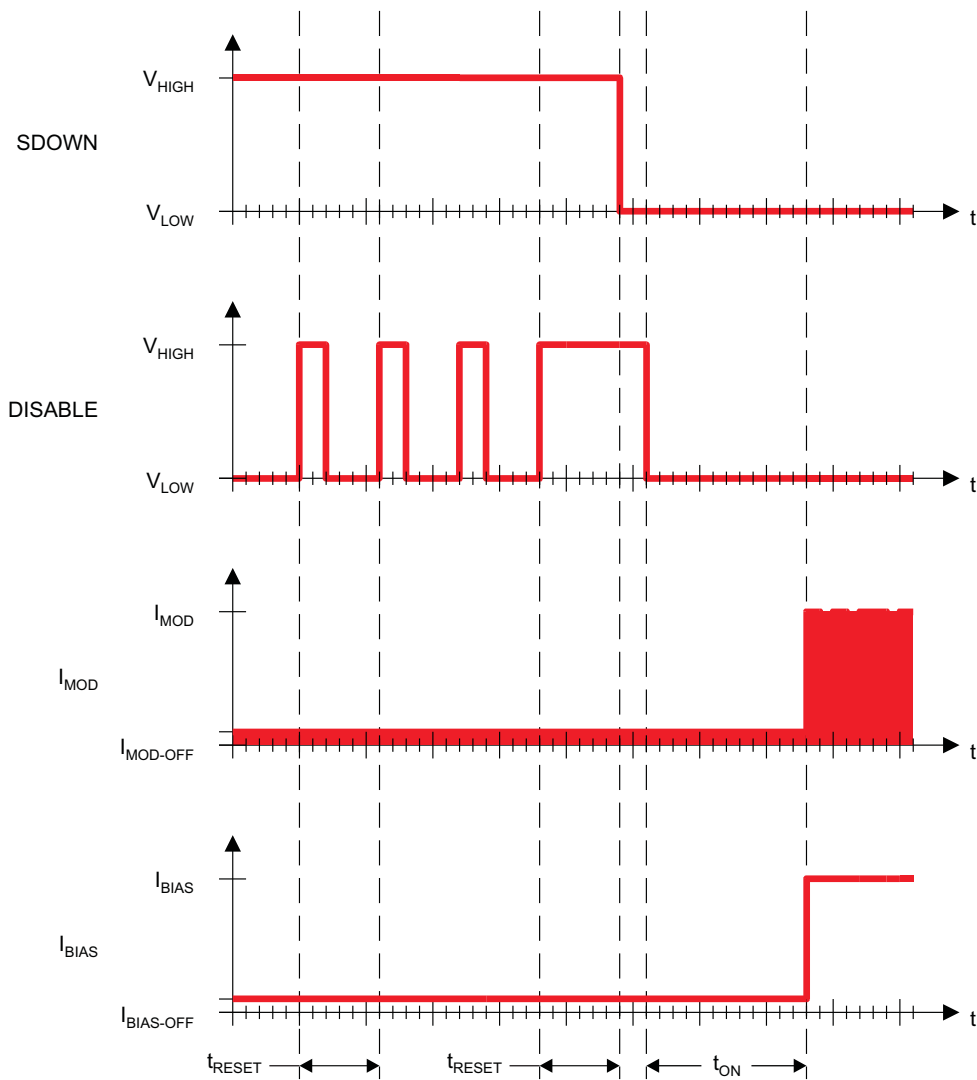
(3) Jitter measured at positive edge and negative edge crossing of eye diagram.



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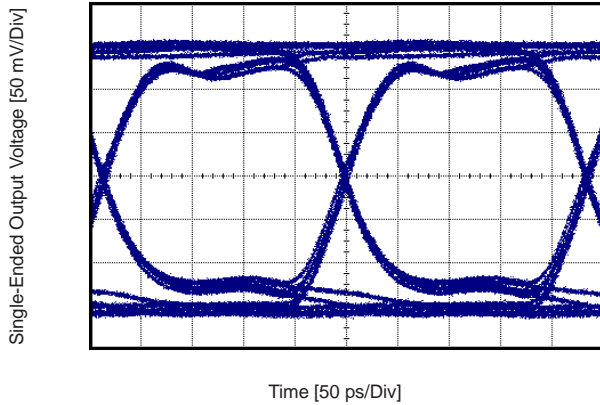


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TYPICAL CHARACTERISTICS

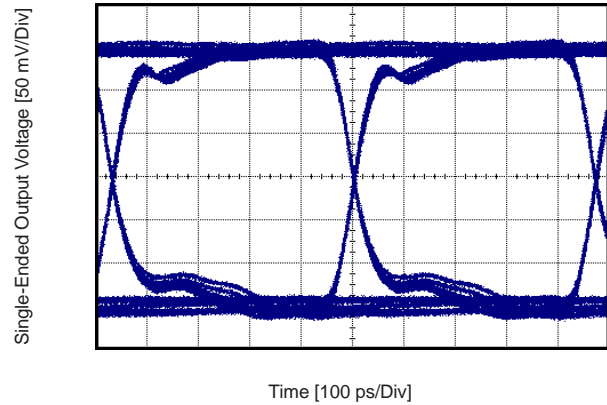
Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $I_{MOD} = 30\text{ mA}$, $I_{BIAS} = 20\text{ mA}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

**ELECTRICAL EYE-DIAGRAM AT 4.25 Gbps
WITH K28.5 PATTERN, $I_{MOD} = 30\text{ mA}$**



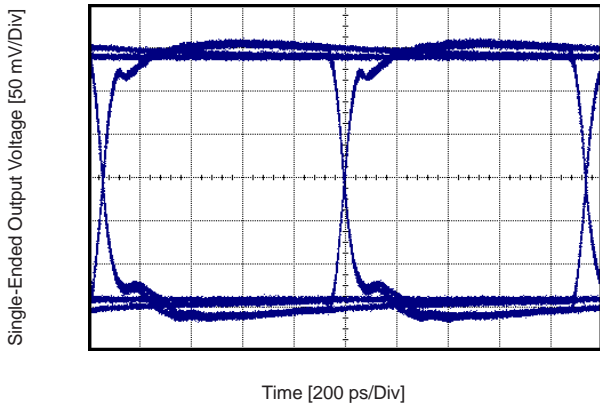
Time [50 ps/Div] G001
Figure 7.

**ELECTRICAL EYE-DIAGRAM AT 2.125 Gbps
WITH K28.5 PATTERN, $I_{MOD} = 30\text{ mA}$**



Time [100 ps/Div] G002
Figure 8.

**ELECTRICAL EYE-DIAGRAM AT 1.0625 Gbps
WITH K28.5 PATTERN, $I_{MOD} = 30\text{ mA}$**



Time [200 ps/Div] G003
Figure 9.

**DETERMINISTIC JITTER
vs
MODULATION CURRENT**

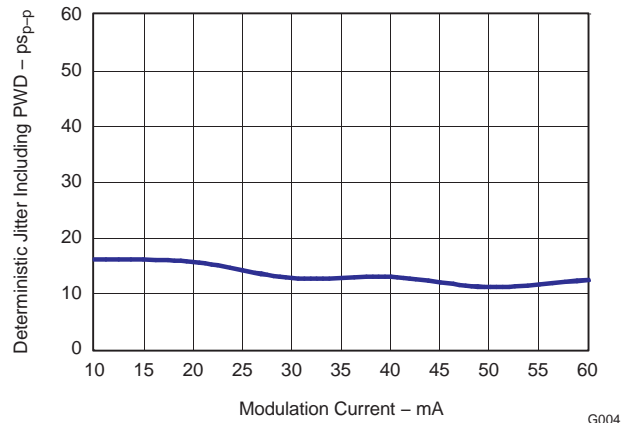


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $I_{MOD} = 30\text{ mA}$, $I_{BIAS} = 20\text{ mA}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

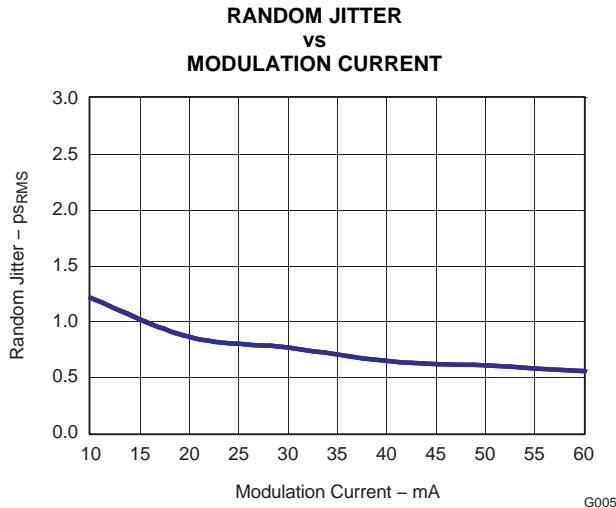


Figure 11.

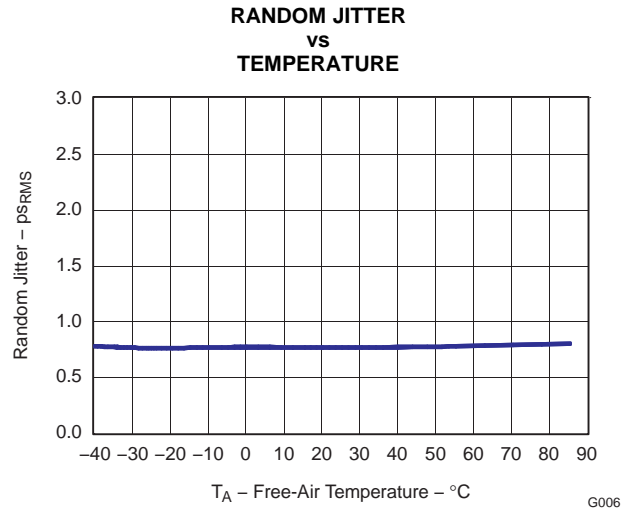


Figure 12.

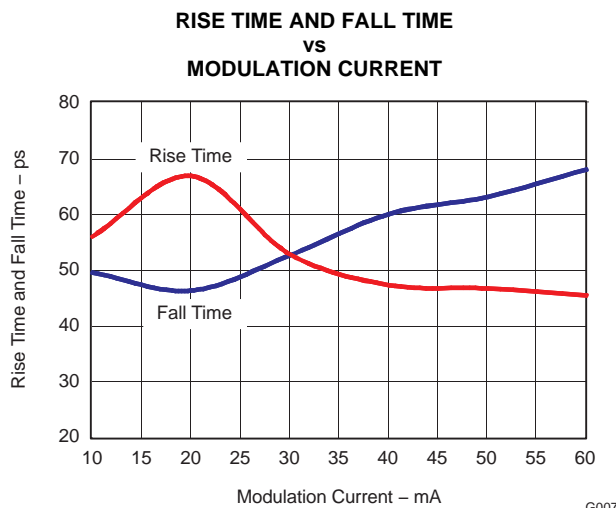


Figure 13.

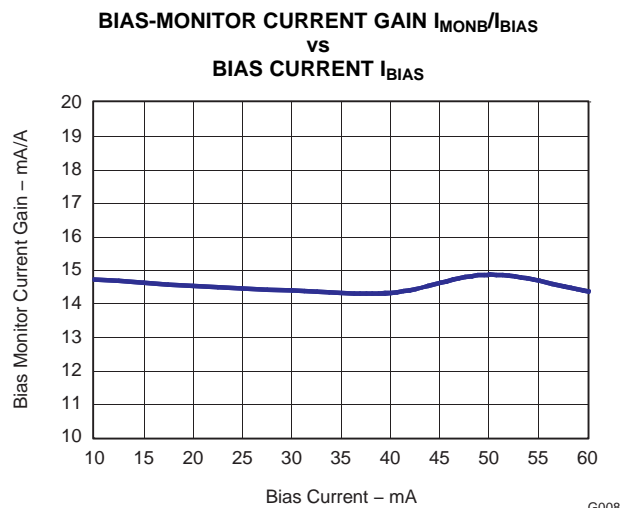


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $I_{MOD} = 30\text{ mA}$, $I_{BIAS} = 20\text{ mA}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

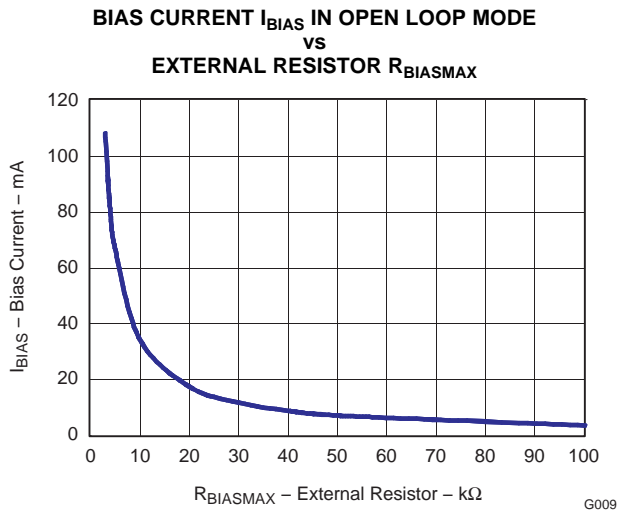


Figure 15.

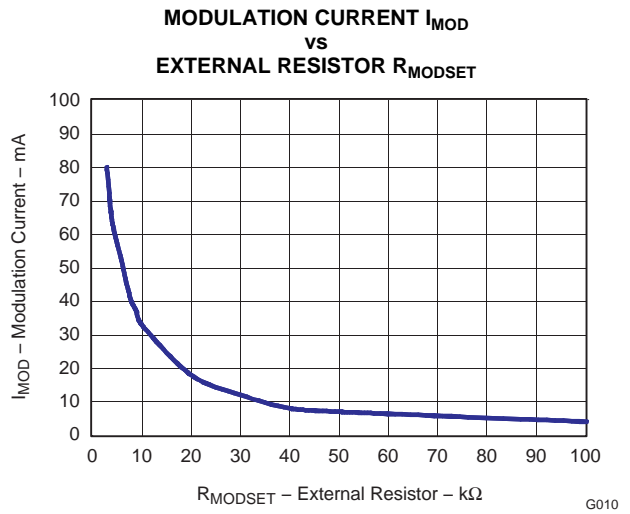


Figure 16.

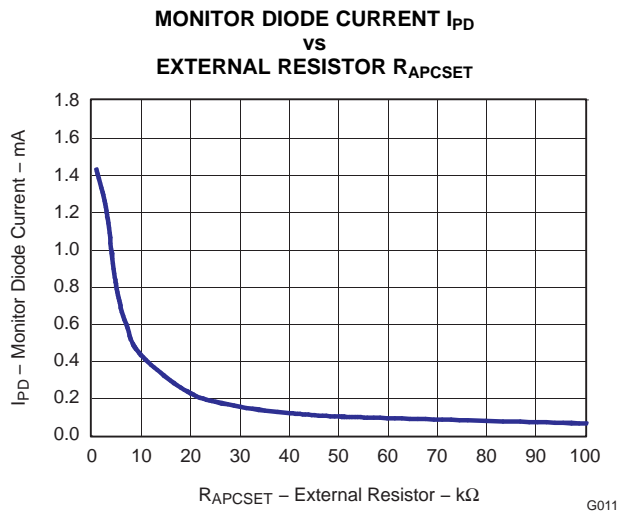


Figure 17.

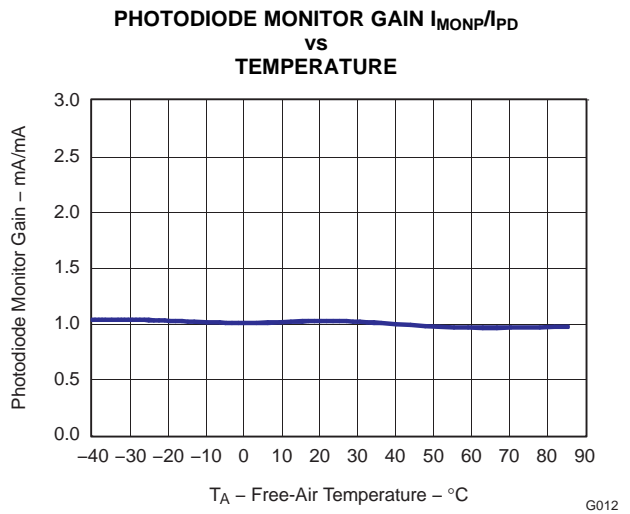


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $I_{MOD} = 30\text{ mA}$, $I_{BIAS} = 20\text{ mA}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

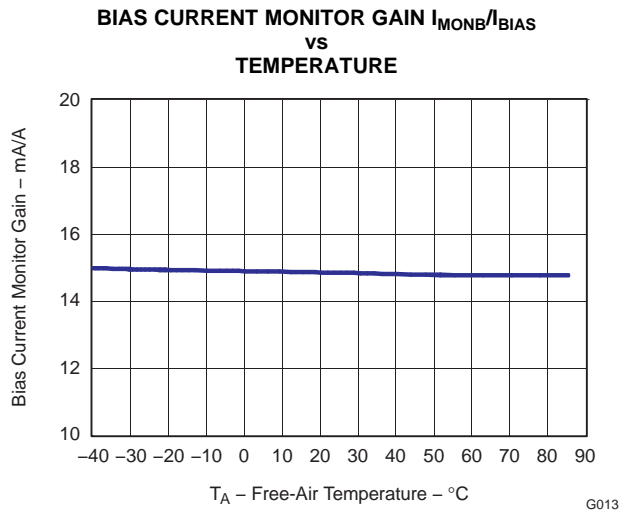


Figure 19.

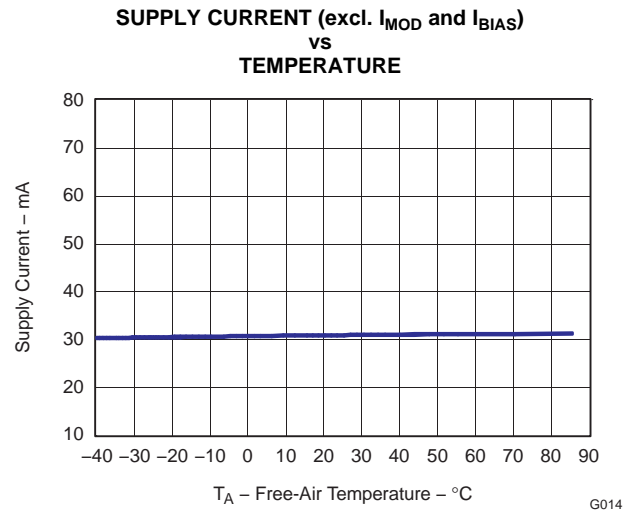


Figure 20.

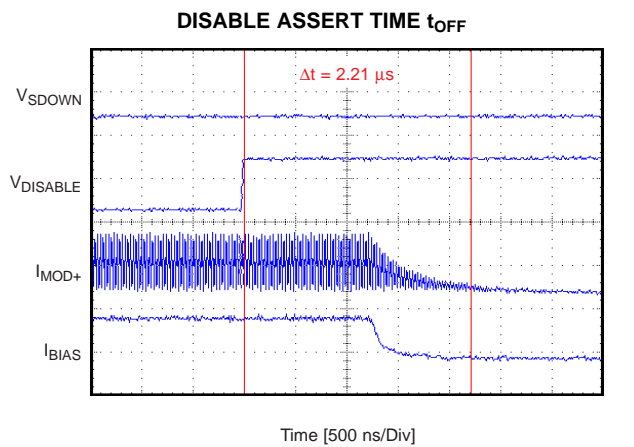


Figure 21.

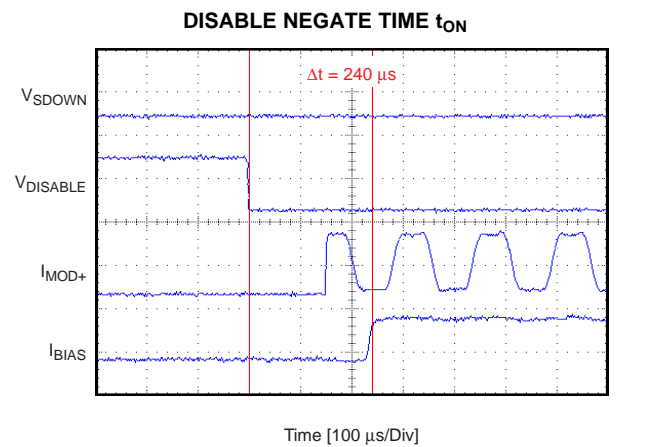


Figure 22.

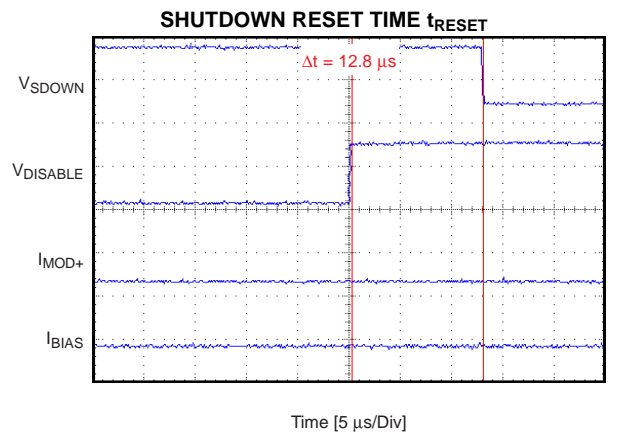
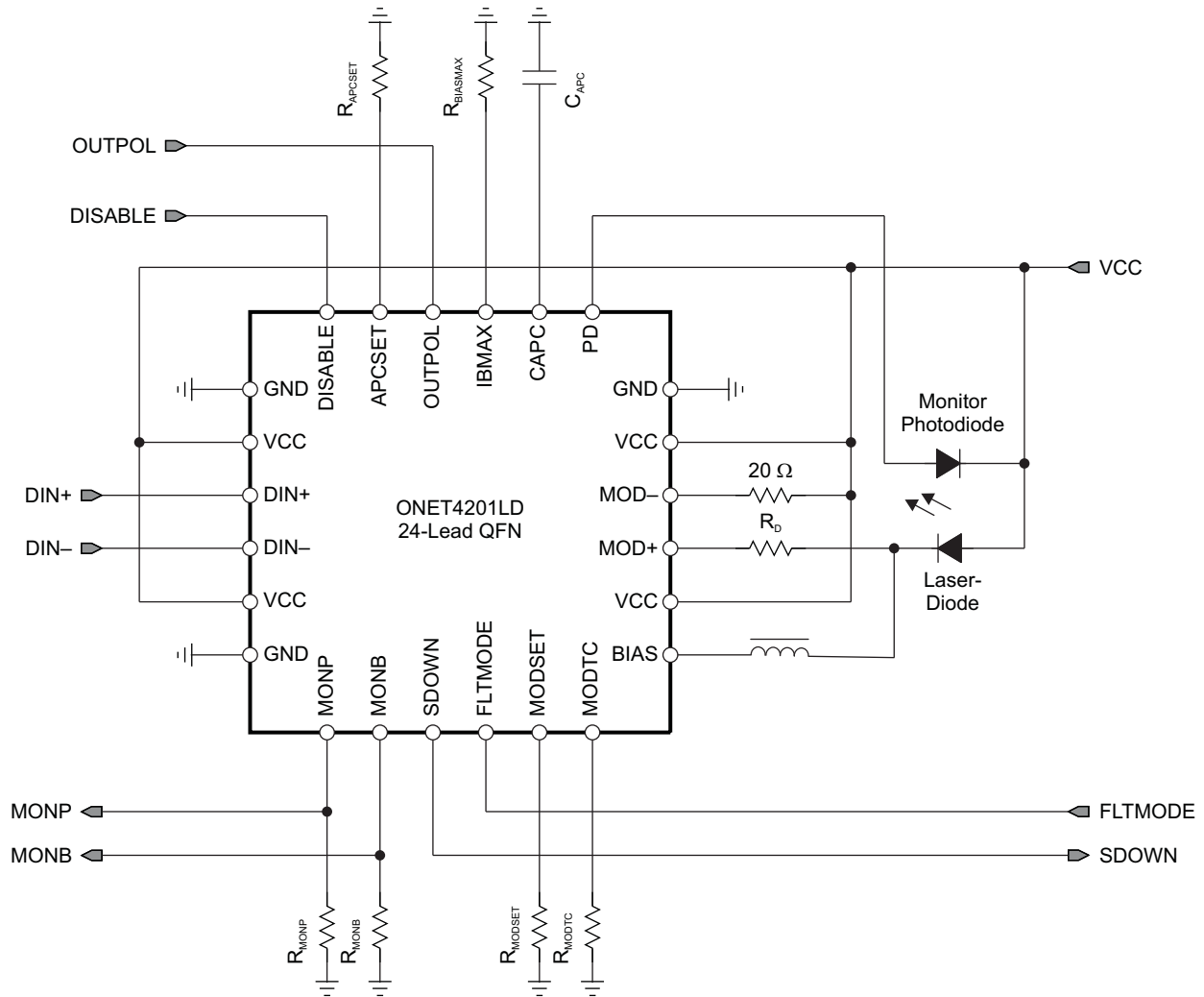


Figure 23.

APPLICATION INFORMATION

Figure 24 shows the ONET4201LD connected with a dc-coupled interface to the laser diode, alternatively the ONET4201LD laser driver can be ac-coupled.



S0154-02

Figure 24. Basic Application Circuit With DC-Coupled Interface Between the ONET4201LD and the Laser Diode

APC loop instability may occur with large inductive loading on the BIAS pin. To ensure loop stability in this case, it is recommended to connect a 1-nF capacitor to ground at the BIAS pin.

SELECT A LASER

In the design example according to [Figure 24](#), the ONET4201LD is dc coupled to a typical communication-grade laser diode capable of operating at 4.25 Gbps with the specifications shown in [Table 2](#).

Table 2. Laser Diode Specifications

| PARAMETER | | VALUE | UNITS |
|--------------|------------------------------|-------|-------|
| λ | Wavelength | 1310 | nm |
| P_{AVG} | Average optical output power | 5 | mW |
| I_{TH} | Threshold current | 10 | mA |
| ρ_{MON} | Laser-to-monitor transfer | 0.05 | mA/mW |
| η | Laser slope efficiency | 0.2 | mW/mA |

SELECT APCSET RESISTOR

When the APC loop is activated, the desired average optical output power P_{AVG} is defined by characteristics of the monitor diode and by the APCSET resistor R_{APCSET} . The relation between the monitor photodiode current I_{PD} and the average optical output power P_{AVG} is given by [Equation 7](#):

$$I_{PD} [A] = P_{AVG} [W] \times \rho_{MON} [A/W] \quad (7)$$

The R_{APCSET} resistor is calculated by [Equation 8](#):

$$R_{APCSET} [\Omega] = \frac{4.69 \text{ V}}{I_{PD} [A]} = \frac{4.69 \text{ V}}{P_{AVG} [W] \times \rho_{MON} [A/W]} \quad (8)$$

For the laser diode specified in [Table 2](#) and the desired average optical output power of 5 mW, R_{APCSET} is calculated as seen in [Equation 9](#):

$$R_{APCSET} [\Omega] = \frac{4.69 \text{ V}}{P_{AVG} [W] \times \rho_{MON} [A/W]} = \frac{4.69 \text{ V}}{5 \text{ mW} \times 0.05 \text{ mA/mW}} = 18.75 \text{ k}\Omega \quad (9)$$

Note that the monitor photodiode current I_{PD} must not exceed 1.5 mA corresponding to a minimum APCSET resistor $R_{APCSET,MIN} = 3.1 \text{ k}\Omega$.

SELECT MODSET RESISTOR

Modulation current I_{MOD} is dependent on the required optical output peak-to-peak power P_{p-p} or the average optical power P_{AVG} . I_{MOD} can be calculated using the laser slope efficiency η and the desired extinction ratio r_e :

$$I_{MOD} [A] = \frac{P_{p-p} [W]}{\eta [W/A]} = \frac{2 \times P_{AVG} [W] \times \frac{r_e - 1}{r_e + 1}}{\eta [W/A]} \quad (10)$$

Using the laser diode parameters from [Table 2](#) and assuming an extinction ratio $r_e = 8 \text{ dB}$ (6.3) for an average optical power $P_{AVG} = 5 \text{ mW}$ the required modulation current results as:

$$I_{MOD} = \frac{2 \times 5 \text{ mW} \times \frac{6.3 - 1}{6.3 + 1}}{0.2 \text{ mW/mA}} = 36.3 \text{ mA} \quad (11)$$

The modulation current is adjustable with a selectable temperature coefficient TC according to the relation:

$$I_{MOD} [A] = I_{MOD0} [A] \times \left(1 + TC \times (T [^\circ\text{C}] - T_0 [^\circ\text{C}]) \right) \quad (12)$$

where T is the ambient temperature in $^\circ\text{C}$ and T_0 is the reference temperature ($T_0 = 60^\circ\text{C}$).

The temperature coefficient of the modulation current TC is typically adjustable between 630 ppm/ $^\circ\text{C}$ and 8300 ppm/ $^\circ\text{C}$.

For calculation of the required external resistor R_{MODSET} for a given modulation current and a given temperature, the formula can be modified as follows:

$$R_{\text{MODSET}}[\Omega] = \frac{265 \text{ V}}{I_{\text{MOD}}[\text{A}]} \times \left(1 + \text{TC} \times (T[\text{°C}] - T_0[\text{°C}]) \right) \quad (13)$$

If 4000 ppm/°C is the desired temperature coefficient and the modulation current from the example above, 36.3 mA, is required at a temperature of 25°C, the MODSET resistor R_{MODSET} is given by [Equation 14](#).

$$R_{\text{MODSET}}[\Omega] = \frac{265 \text{ V}}{36.3 \text{ mA}} \times \left(1 + \frac{4000 \text{ ppm}}{\text{°C}} \times (25\text{°C} - 60\text{°C}) \right) = 6.3 \text{ k}\Omega \quad (14)$$

Note that the modulation current I_{MOD} must not exceed 85 mA over the complete temperature range, corresponding to a minimum MODSET resistor $R_{\text{MODSET,MIN}} = 3.1 \text{ k}\Omega$.

SELECT MODTC RESISTOR

The R_{MODTC} resistor is used to program a modulation temperature coefficient that can be used to compensate for the decreased slope efficiency of the laser at a higher temperature. The temperature coefficient TC_{LD} of the laser can be calculated using the slope efficiency η_1 at temperature T_1 and η_2 at temperature T_2 as shown in [Equation 15](#):

$$\text{TC}_{\text{LD}} \left[\frac{1}{\text{°C}} \right] = \frac{\eta_2[\text{W/A}] - \eta_1[\text{W/A}]}{\eta_1[\text{W/A}] \times (T_2[\text{°C}] - T_1[\text{°C}])} \times 10^6 \quad (15)$$

As an example, for the laser in [Table 2](#), the slope efficiency at temperature $T_1 = 25\text{°C}$ is $\eta_1 = 0.2 \text{ mW/mA}$. At temperature $T_2 = 85\text{°C}$ the slope efficiency is $\eta_2 = 0.15 \text{ mW/mA}$. The corresponding temperature coefficient TC_{LD} laser can be calculated:

$$\text{TC}_{\text{LD}} = \frac{0.15 \text{ mW/mA} - 0.2 \text{ mW/mA}}{0.2 \text{ mW/mA} \times (85\text{°C} - 25\text{°C})} \times 10^6 = -4167 \frac{1}{\text{°C}} \quad (16)$$

The MODTC resistor R_{MODTC} can be used to compensate the laser temperature coefficient TC_{LD} in order to maintain the same optical output swing within a range of 630 ppm up to 8300 ppm. For this, R_{MODTC} may be programmed as follows:

$$R_{\text{MODTC}} = \frac{24 \Omega}{(\text{TC} - 630 \text{ ppm}) \left[\frac{1}{\text{°C}} \right] \times \text{°C}} \quad (17)$$

To compensate for the decreased slope efficiency of the laser in [Table 2](#), T_C must be 4167 ppm/°C.

This leads to the following MODTC resistor R_{MODTC} :

$$R_{\text{MODTC}} = \frac{24 \Omega}{\frac{4167 \text{ ppm} - 630 \text{ ppm}}{\text{°C}} \times \text{°C}} = 6.8 \text{ k}\Omega \quad (18)$$

SELECT BIASMAX RESISTOR

The BIASMAX resistor R_{BIASMAX} is used to limit the bias current applied to the laser diode.

To calculate R_{BIASMAX} , the maximum threshold current at 85°C and end of life must be determined. The maximum bias current for the dc-coupled interface can be approximated by [Equation 19](#).

$$I_{\text{BIASMAX}}[\text{A}] = I_{\text{THMAX}}[\text{A}] \quad (19)$$

R_{BIASMAX} can be set by [Equation 20](#).

$$R_{\text{BIASMAX}}[\Omega] = \frac{343 \text{ V}}{I_{\text{BIASMAX}}[\text{A}]} = \frac{343 \text{ V}}{I_{\text{THMAX}}[\text{A}]} \quad (20)$$

For the example laser diode, the maximum threshold current is 40 mA at 85°C. Therefore, R_{BIASMAX} can be approximated by [Equation 21](#).

$$R_{\text{BIASMAX}} = \frac{343 \text{ V}}{40 \text{ mA}} = 8.6 \text{ k}\Omega \quad (21)$$

SELECT V_{MONB} AND V_{MONP} RANGE

Monitoring the bias current is achieved by taking the fractional (1/68) bias current and developing a voltage across an external resistor to ground. [Equation 22](#) provides the value for V_{MONB} for a resistor value equal to 768 Ω .

$$V_{\text{MONB}}[\text{V}] = \frac{R_{\text{MONB}}[\Omega] \times I_{\text{BIAS}}[\text{A}]}{68} = \frac{768 \Omega \times I_{\text{BIAS}}[\text{A}]}{68} = 11.29 \Omega \times I_{\text{BIAS}}[\text{A}] \quad (22)$$

Monitoring of the photodiode current is achieved by taking a mirror of I_{PD} and developing a voltage across an external resistor to ground. [Equation 23](#) provides the value for V_{MONP} for a resistor equal to 200 Ω .

$$V_{\text{MONP}}[\text{V}] = R_{\text{MONP}}[\Omega] \times I_{\text{PD}}[\text{A}] = 200 \Omega \times I_{\text{PD}}[\text{A}] \quad (23)$$





LASER DIODE INTERFACE

The output stage of the ONET4201LD is optimized for driving a 20- Ω load. The combination of a damping resistor, R_{D} , along with the resistance of the laser diode must be 20 Ω for impedance matching. The suggested typical value for R_{D} is 6 Ω to 15 Ω . A bypass capacitor of 10 nF placed close to the laser anode also helps to optimize performance.

REVISION HISTORY

| Changes from Original (November 2005) to Revision A | Page |
|---|------|
| • Changed 200us to 80us for typ value of t_{ON} | 10 |
| • Changed 200us to 80us for typ value of t_{INIT} | 10 |
| • Changed 10us to 0.8us for max value of t_{RESET} max spike | 10 |
| • Changed 20us min to 6us max value of t_{RESET} time DISABLE | 10 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---|
| ONET4201LDRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ONET 4201L |  |
| ONET4201LDRGERG4 | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ONET 4201L |  |
| ONET4201LDRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ONET 4201L |  |
| ONET4201LDRGETG4 | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ONET 4201L |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ONET4201LDRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| ONET4201LDRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |

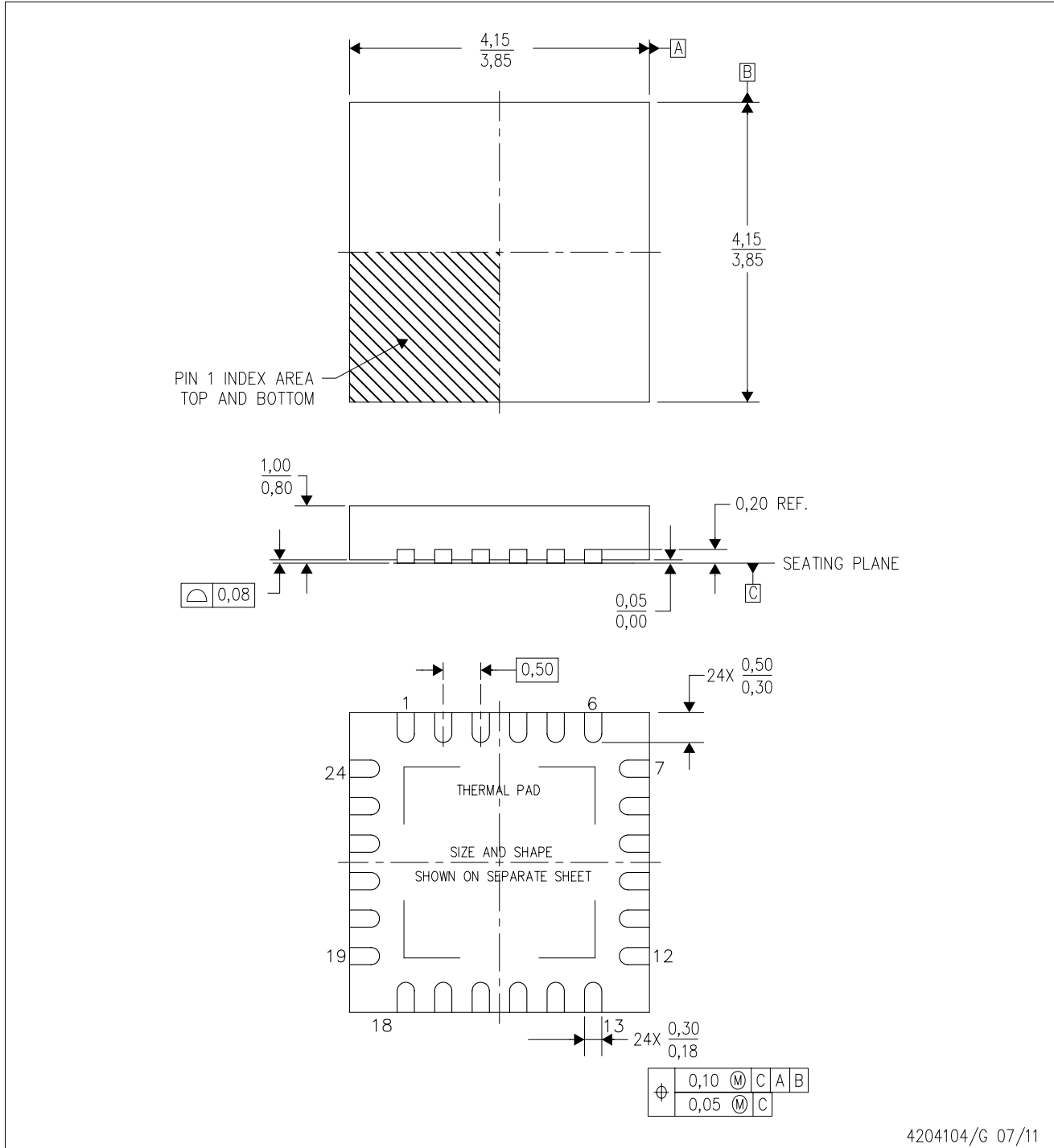
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ONET4201LDRGER | VQFN | RGE | 24 | 3000 | 338.1 | 338.1 | 20.6 |
| ONET4201LDRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

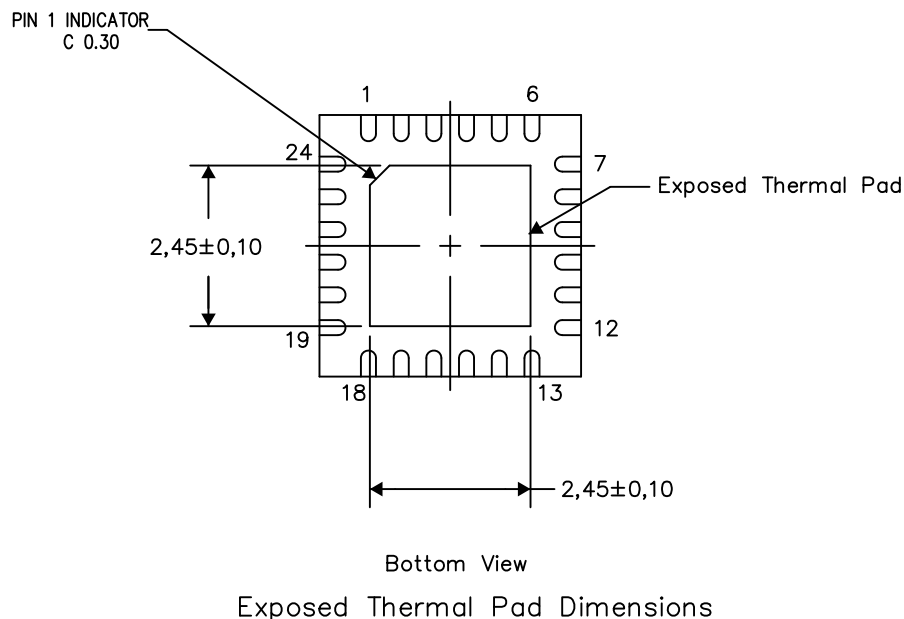
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

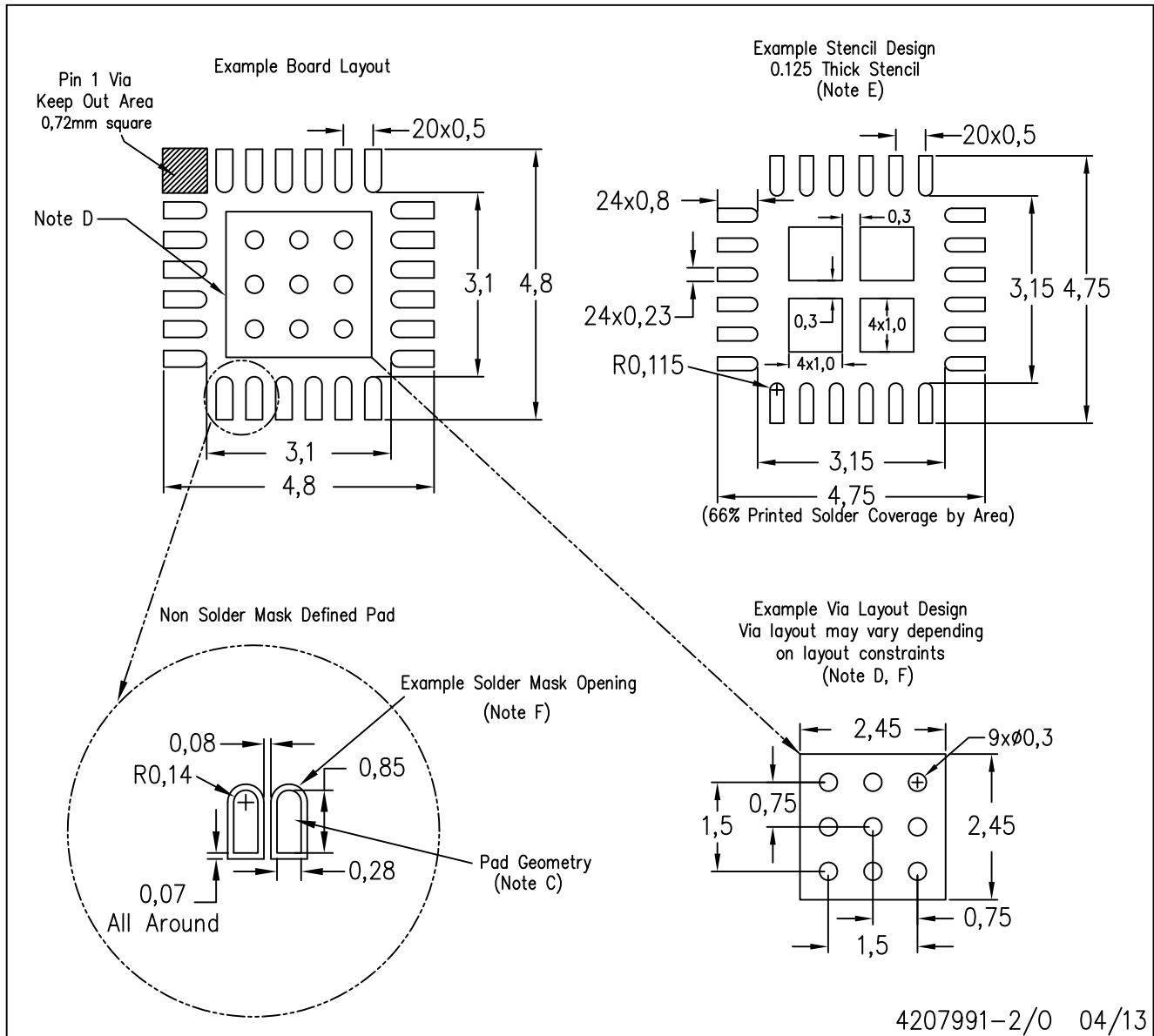


4206344-3/AC 03/13

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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