

## DisplayPort to TMDS Translator

Check for Samples: [SN75DP139](#)

### FEATURES

- DisplayPort Physical Layer Input Port to TMDS Physical Layer Output Port
- Integrated TMDS Level Translator With Receiver Equalization
- Supports Data Rates up to 3.4Gbps
- Achieves HDMI 1.4b Compliance
- 3D HDMI Support With TMDS Clock Rates up to 340MHz
- 4k x 2k Operation (30Hz, 24bpp)
- Deep Color Supporting 36bpp
- Integrated I<sup>2</sup>C Logic Block for DVI/HDMI Connector Recognition
- Integrated Active I<sup>2</sup>C Buffer
- Enhanced ESD: 10kV on All Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 48 Pin 7 x 7 QFN (RGZ) Package
- 40 Pin 5 x 5 QFN (RSB) Package

### APPLICATIONS

- Personal Computer Market
  - DP/TMDS Dongle
  - Desktop PC
  - Notebook PC
  - Docking Station
  - Standalone Video Card

### DESCRIPTION

The SN75DP139 is a Dual-Mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output. The TMDS output has a built in level translator supporting Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.4b standards. The SN75DP139 is specified up to a maximum data rate of 3.4Gbps, supporting resolutions greater than 1920x1200 or HDTV 12 bit color depth at 1080p (progressive scan). SN75DP139 is compliant with the HDMI 1.4b specifications and supports optional protocol enhancements such as 3D graphics at resolutions demanding a pixel rate up to 340MHz.

An integrated Active I<sup>2</sup>C buffer isolates the capacitive loading of the source system from that of the sink and interconnecting cable. This isolation improves overall signal integrity of the system and allows for considerable design margin within the source system for DVI / HDMI compliance testing.

A logic block was designed into the SN75DP139 in order to assist with TMDS connector identification. Through the use of the I<sup>2</sup>C\_EN pin, this logic block can be enabled to indicate the translated port is an HDMI port; therefore legally supporting HDMI content.

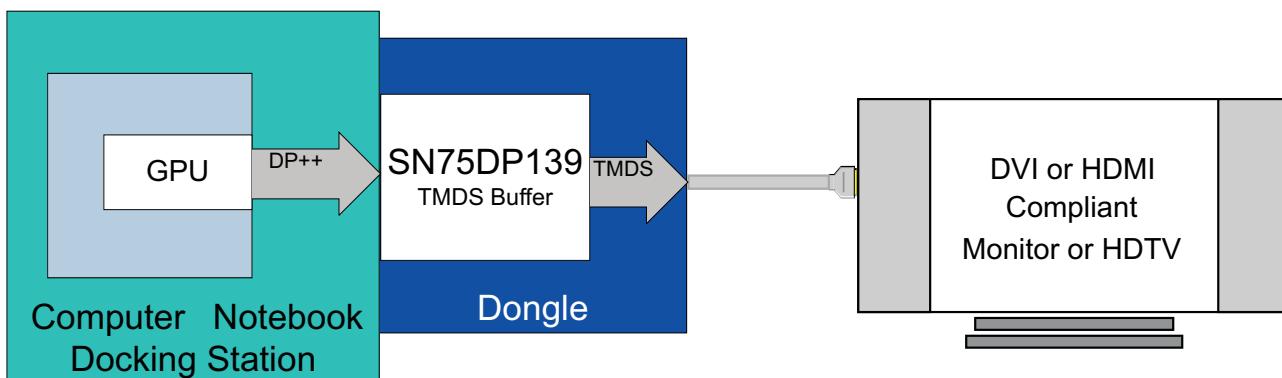


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## TYPICAL APPLICATION



GPU - Graphics Processing Unit

DP++ - Dual-Mode DisplayPort

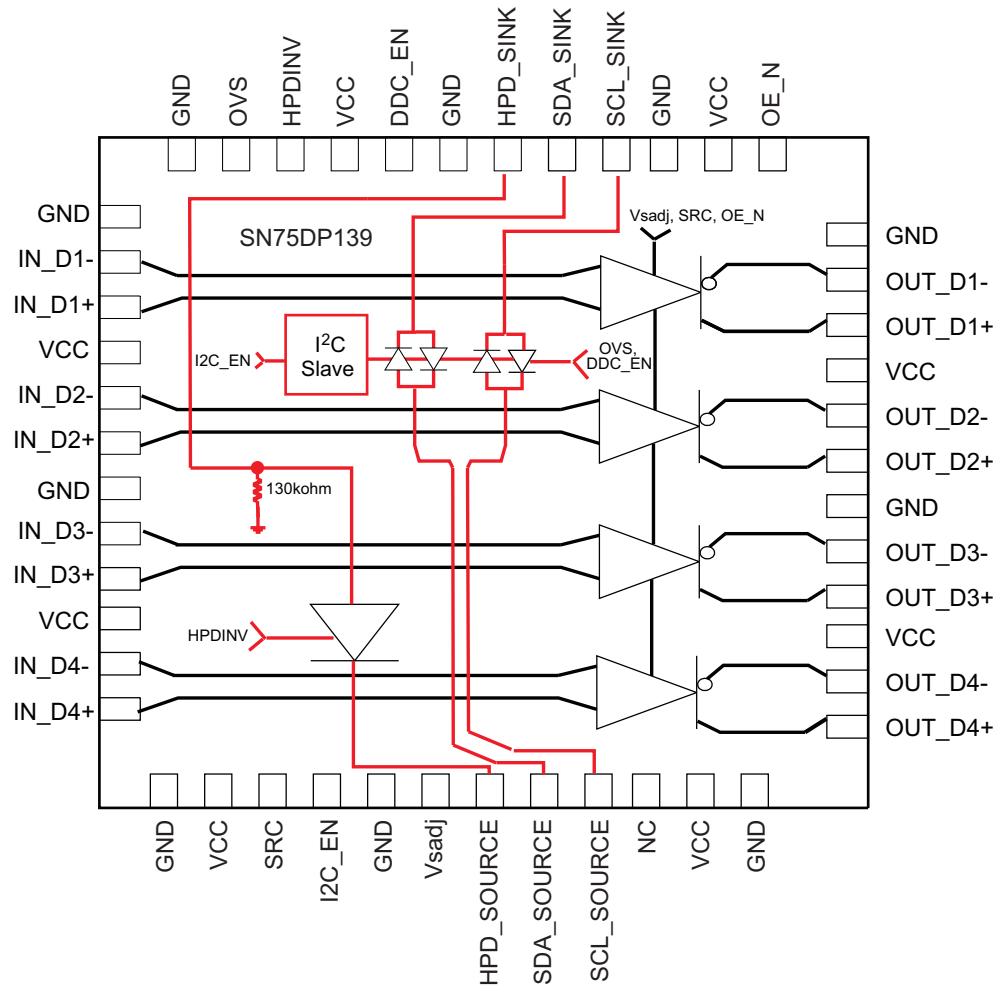
TMDS - Transition-Minimized Differential Signaling

DVI - Digital Visual Interface

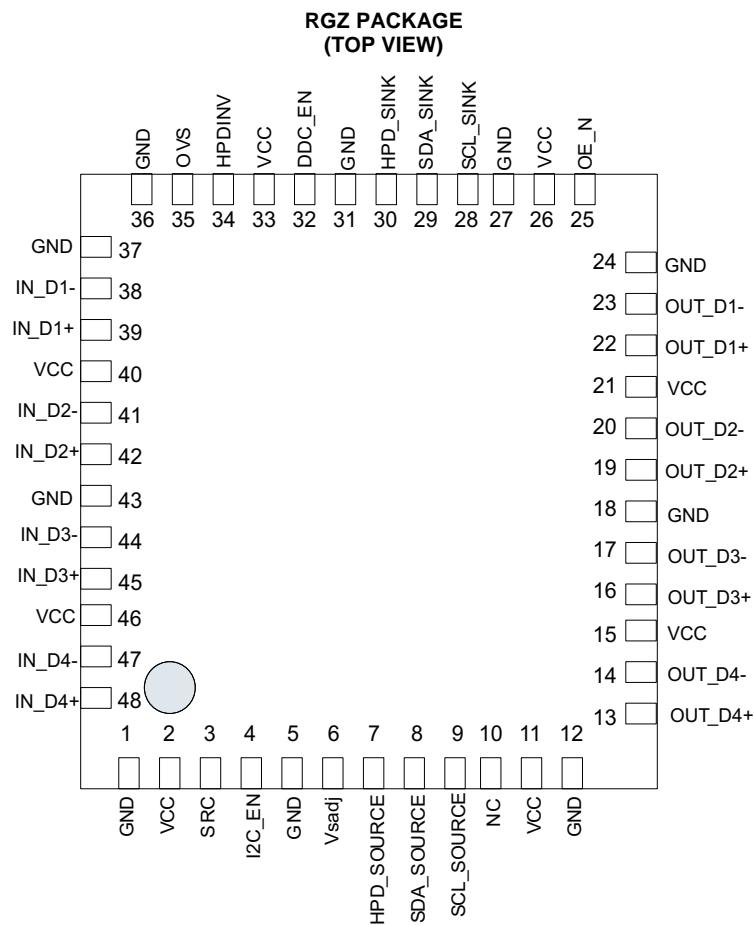
HDMI - High Definition Multimedia Interface

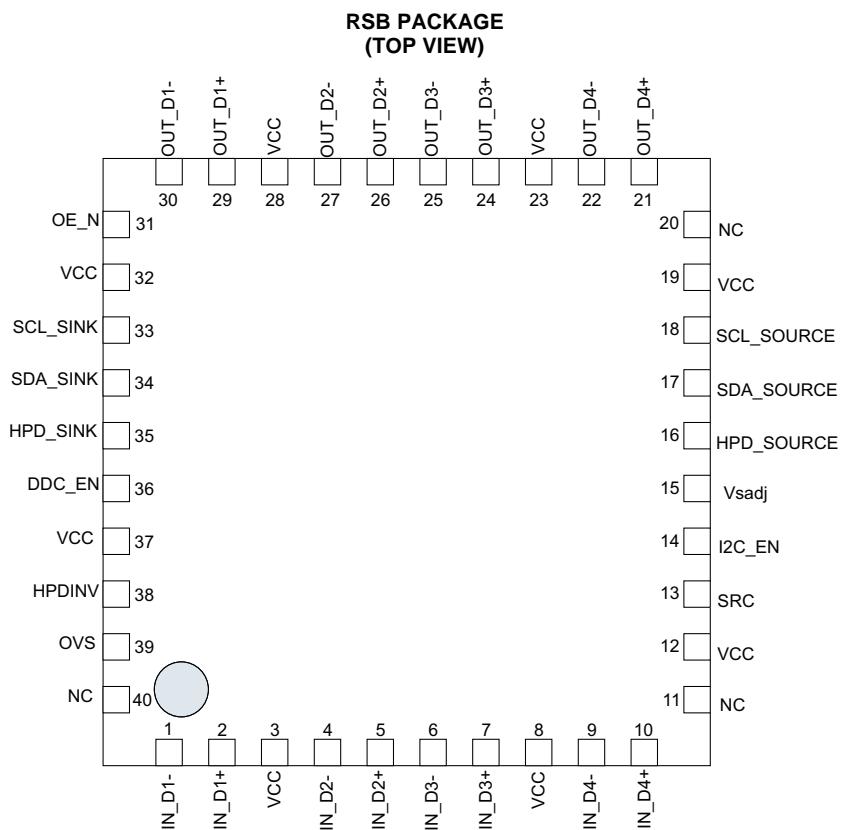
GPU	Graphics Processing Unit
DP++	Dual-Mode DisplayPort
TMDS	Transition-Minimized Differential Signaling
DVI	Digital Visual Interface
HDMI	High Definition Multimedia Interface

# DATA FLOW BLOCK DIAGRAM



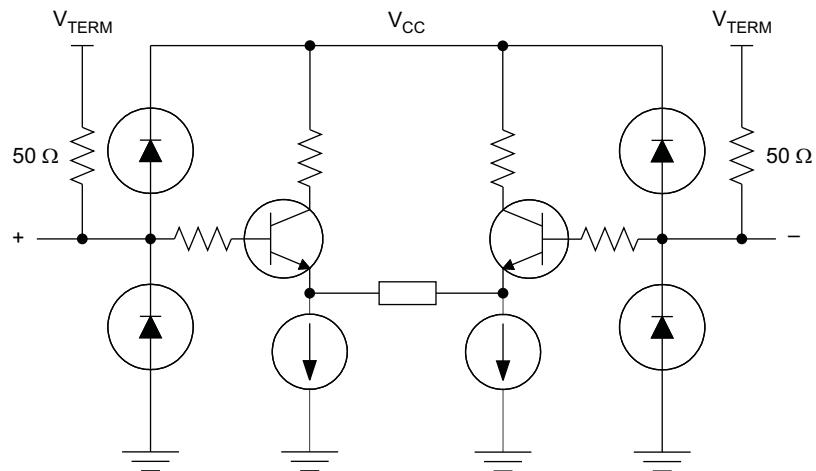
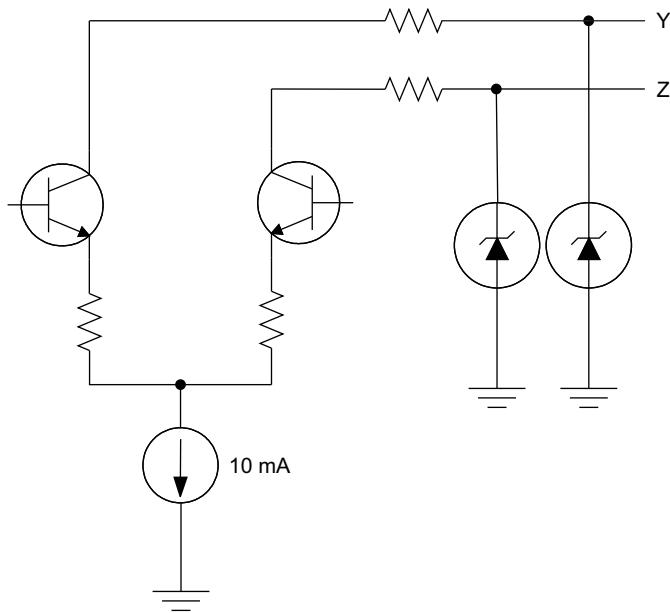
## DEVICE INFORMATION





## PIN FUNCTIONS

PIN		I/O	DESCRIPTION			
SIGNAL	NO.					
	RGZ	RSB				
<b>MAIN LINK INPUT PINS</b>						
IN_D1	38, 39	1, 2	I	DisplayPort Main Link Channel 0 Differential Input		
IN_D2	41, 42	4, 5	I	DisplayPort Main Link Channel 1 Differential Input		
IN_D3	44, 45	6, 7	I	DisplayPort Main Link Channel 2 Differential Input		
IN_D4	47, 48	9, 10	I	DisplayPort Main Link Channel 3 Differential Input		
<b>MAIN LINK PORT B OUTPUT PINS</b>						
OUT_D1	23, 22	30, 29	O	TMDS Data 2 Differential Output		
OUT_D2	20, 19	27, 26	O	TMDS Data 1 Differential Output		
OUT_D3	17, 16	25, 24	O	TMDS Data 0 Differential Output		
OUT_D4	14, 13	22, 21	O	TMDS Data Clock Differential Output		
<b>HOT PLUG DETECT PINS</b>						
HPD_SOURCE	7	16	O	Hot Plug Detect Output		
HPD_SINK	30	35	I	Hot Plug Detect Input		
<b>AUXILIARY DATA PINS</b>						
SDA_SOURCE, SCL_SOURCE	8, 9	17, 18	I/O	Source Side Bidirectional DisplayPort Auxiliary Data Line		
SDA_SINK, SCL_SINK	29, 28	34, 33	I/O	TMDS Port Bidirectional DDC Data Lines		
<b>CONTROL PINS</b>						
OE_N	25	31	I	Output Enable and power saving function for High Speed Differential level shifter path.		
NC	10	11, 20, 40		No Connect		
OVS	35	39	I	DDC I2C buffer offset select		
DDC_EN	32	36	I	Enables or Disables the DDC I2C buffer		
HPDINV	34	38	I	HPD_SOURCE Logic and Level Select		
VSadj	6	15	I	TMDS Compliant Voltage Swing Control		
SRC	3	13	I	TMDS outputs rise and fall time select		
I2C_EN	4	14	I	Internal I <sup>2</sup> C register enable, used for HDMI / DVI connector differentiation		
<b>SUPPLY AND GROUND PINS</b>						
VCC	2, 11, 15, 21, 26, 33, 40, 46	3, 8, 12, 19, 23 28, 32, 37		3.3V Supply		
GND	1, 5, 12, 18, 24, 27, 31, 36, 37, 43	Thermal Pad		Ground		

**Input/Output Equivalent Circuits**

**Figure 1. DisplayPort Input Stage**

**Figure 2. TMDS Output Stage**

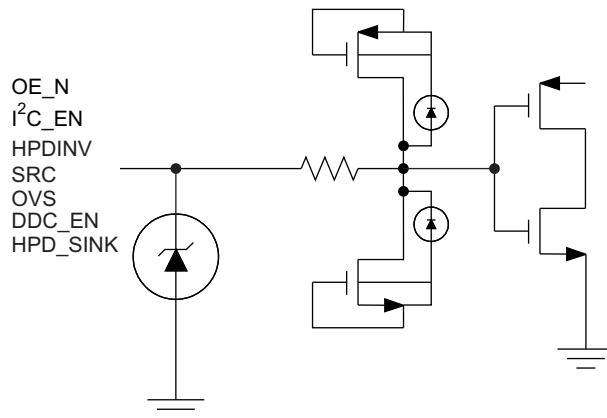


Figure 3. HPD and Control Input Stage

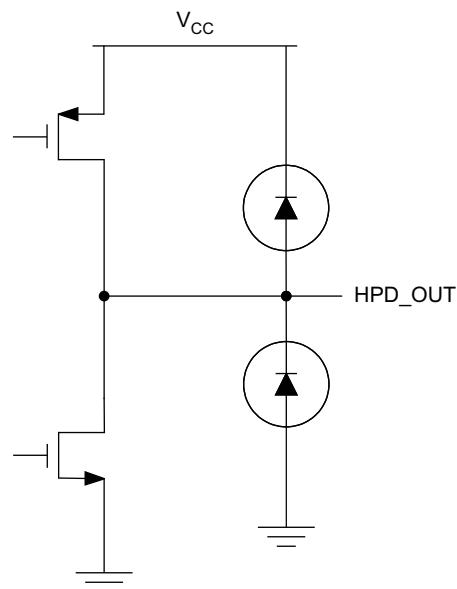


Figure 4. HPD Output Stage

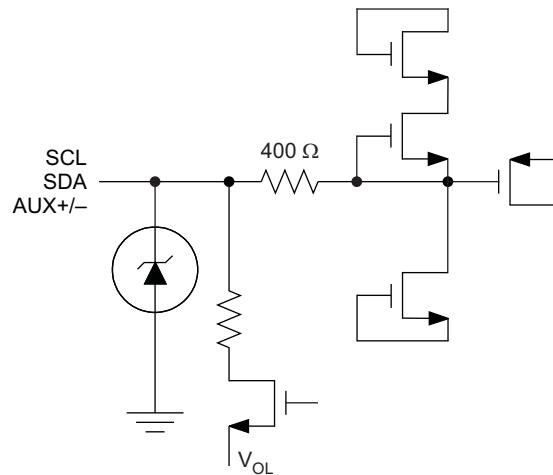


Figure 5. I<sup>2</sup>C Input and Output Stage

**Table 1. Control Pin Lookup Table**

SIGNAL	LEVEL <sup>(1)</sup>	STATE	DESCRIPTION
OE_N	H	Power Saving Mode	Main Link is disabled. IN_Dx termination = 50 Ω with common mode voltage set to 0V. OUT_Dx outputs = high impedance
	L	Normal Mode	IN_Dx termination = 50 Ω OUT_Dx outputs = active
I <sup>2</sup> C_EN	H	HDMI	The Internal I <sup>2</sup> C register is active and readable when the TMDS port is selected indicating that the connector being used is HDMI. This mode selects the fastest rise and fall time for the TMDS differential output signals
	L	DVI	The Internal I <sup>2</sup> C register is disabled and not readable when the TMDS port is selected indicating that the connector being used is DVI. This mode selects a slower rise and fall time for the TMDS differential output signals See <a href="#">DVI Application Section</a> .
VSadj	4.02 kΩ ±5%	Output Voltage Swing Control	Driver output voltage swing precision control to aid with system compliance
HPDINV	H	HPD Inversion	HPD_SOURCE VOH =0.9V (typical) and HPD logic is inverted
	L	HPD non-inversion	HPD_SOURCE VOH =3.2V (typical) and HPD logic is non-inverted
SRC	H	Edge Rate: Slowest	SRC helps to slow down the rise and fall time. SRC =High adds ~60ps to the rise and fall time of the TMDS differential output signals in addition to the I <sup>2</sup> C_EN pin selection (recommended setting)
	L	Edge Rate: Slow	SRC helps to slow down the rise and fall time. SRC =Low adds ~30ps to the rise and fall time of the TMDS differential output signals in addition to the I <sup>2</sup> C_EN pin selection
	Hi-Z	Edge Rate	Leaving the SRC pin High Z, will keep the default rise and fall time of the TMDS differential output signals as selected by the I <sup>2</sup> C_EN pin. It is recommended that an external resistor-divider (less than 100 kΩ) is used so that voltage on this pin = VCC/2, if Hi-Z logic level is intended on this pin.
OVS	H	Offset 1	DDC source side VOL and VIL offset range 1
	L	Offset 2	DDC source side VOL and VIL offset range 2
	Hi-Z	Offset 3	DDC source side VOL and VIL offset range 3 It is recommended that an external resistor-divider (less than 100 kΩ) is used so that voltage on this pin = VCC/2, if Hi-Z logic level is intended on this pin.
DDC_EN	H	DDC Buffer enabled	DDC Buffer is enabled
	L	DDC buffer disabled	DDC Buffer is disabled

(1) (H) Logic High; (L) Logic Low; (Z) High Z

ORDERING INFORMATION<sup>(1)</sup>

PART NUMBER	PART MARKING	PACKAGE
SN75DP139RGZR	DP139	48-pin QFN Reel (large)
SN75DP139RGZT	DP139	48-pin QFN Reel (small)
SN75DP139RSBR	DP139	40-pin QFN Reel (large)
SN75DP139RSBT	DP139	40-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT
Supply voltage range <sup>(2)</sup>	VCC	–0.3 to 3.6	V
Voltage range	Main Link Input (IN_Dx) differential voltage	–0.3 to VCC + 0.3	
	TMDS Outputs (OUT_Dx)	–0.3 to VCC + 0.3	
	HPD_SOURCE, SDA_SOURCE, SCL_SOURCE, OVS, DDC_EN, VSadj, SRC, I <sup>2</sup> C_EN	–0.3 to VCC + 0.3	
	HPD_SINK, SDA_SINK, SCL_SINK, OE_EN, HPDINV	–0.3 to 5.5	
Electrostatic discharge	Human body model <sup>(3)</sup>	±10000	V
	Charged-device model <sup>(4)</sup>	±1500	
	Machine model <sup>(5)</sup>	±200	
Continuous power dissipation	See Dissipation Rating Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A

(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX <sup>(1)</sup>	UNIT
$\theta_{JB}$ Junction-to-board thermal resistance	RGZ package	10.9			°C/W
	RSB package	10.8			
$\theta_{JCT}$ Junction-to-case-top thermal resistance	RGZ package	22.5			°C/W
	RSB package	24.4			
$\Psi_{JB}$ Junction-to-board thermal resistance metric	High-K board <sup>(2)</sup>	RGZ package	10.9		°C/W
		RSB package	10.8		
$\Psi_{JT}$ Junction-to-top thermal resistance metric	High-K board <sup>(2)</sup>	RGZ package	0.5		°C/W
		RSB package	0.4		
$P_{D1}$ Device power dissipation <sup>(3)</sup>	<b>HDMI Mode:</b> OE_N = 0V, DDC_EN = 3.6V, V <sub>CC</sub> = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: V <sub>I</sub> = 3.3V, 100 kHz PRBS <b>HPD:</b> HPD_SINK = 5V, I2C_EN = 3.6V, SRC = Hi-Z	270+146	396+146		mW
$P_{D2}$ Device power dissipation <sup>(3)</sup>	<b>DVI Mode:</b> OE_N = 0V, DDC_EN = 3.6V, V <sub>CC</sub> = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: V <sub>I</sub> = 3.3V, 100 kHz PRBS <b>HPD:</b> HPD_SINK= 5V, I2C_EN = 0V, SRC = Hi-Z	214+146	306+146		mW
$P_{SD1}$ Device power dissipation under low power with HPDINV = LOW	OE_N = 5V, DDC_EN = 0V, HPDINV = 0V, HPD_SINK = 0V	18	54		μW
$P_{SD2}$ Device power dissipation under low power with HPDINV = HIGH	OE_N = 5V, DDC_EN = 0V, HPDINV = 5V	1.7	3		mW
$P_{SD3}$ Device power dissipation under low power with DDC enabled with HPDINV = HIGH	OE_N = 5V, DDC_EN = 3.6V, HPDINV = 5V	16.5	29		mW
$P_{SD4}$ Device power dissipation under low power with DDC enabled with HPDINV = LOW	OE_N = 5V, DDC_EN = 3.6V, HPDINV = 0V	15	26		mW

(1) The maximum rating is simulated under 3.6V V<sub>CC</sub> unless otherwise noted.

(2) Test conditions for  $\psi_{JB}$  and  $\psi_{JT}$  are clarified in TI document [SPRA953](#), IC Package Thermal Metrics.

(3) Power dissipation is the sum of the power consumption from the VCC pins, plus the 146 mW of power from the AVCC (HDMI/DVI Receiver Termination Supply).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply Voltage	3	3.3	3.6	V
T <sub>A</sub>	Operating free-air temperature	0	85		°C
<b>MAIN LINK DIFFERENTIAL INPUT PINS</b>					
V <sub>ID_PP</sub>	Peak-to-peak AC input differential voltage	0.15	1.2		V
d <sub>R</sub>	Data rate	RGZ package	0.25	3.4	Gbps
		RSB package	0.25	3.4	
t <sub>rise fall time</sub>	Input Signal Rise and Fall time (20%-80%)	75			ps
V <sub>PRE</sub>	Pre-emphasis on the Input Signal at IN_Dx pins	0	0	0	db
<b>TMDS DIFFERENTIAL OUTPUT PINS</b>					
AV <sub>CC</sub>	TMDS output termination voltage	3	3.3	3.6	V
d <sub>R</sub>	Data rate	RGZ package	0.25	3.4	Gbps
		RSB package	0.25	3.4	
R <sub>T</sub>	Termination resistance	45	50	55	Ω
R <sub>Vsadj</sub>	TMDS output swing voltage bias resistor <sup>(1)</sup>	3.65	4.02		kΩ

(1) R<sub>Vsadj</sub> resistor controls the SN75DP139 Driver output voltage swing and thus helps in meeting system compliance. It is recommended that R<sub>Vsadj</sub> resistor should be above the MIN value as indicated in the RECOMMENDED OPERATING CONDITIONS table, however for NOM and MAX value, [Figure 24](#) could be used as reference. It is important to note that system level losses, AV<sub>CC</sub> and R<sub>T</sub> variation affect R<sub>Vsadj</sub> resistor selection. Worse case variation on system level losses, AV<sub>CC</sub>, R<sub>T</sub> could make R<sub>Vsadj</sub> resistor value of 4.02 kΩ ±5% result in non-compliant TMDS output voltage swing. In such cases [Figure 24](#) could be used as reference.

## RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
<b>AUXILIARY AND I2C PINS</b>					
V <sub>I</sub>	Input voltage	SDA_SINK, SCL_SINK	0	5.5	V
		SDA_SOURCE, SCL_SOURCE		3.6	
d <sub>R(I2C)</sub>	I <sup>2</sup> C data rate			100	kHz
<b>HPD_SINK, HPDINV, OE_N</b>					
V <sub>IH</sub>	High-level input voltage			2	5.5
V <sub>IL</sub>	Low-level input voltage			0	0.8
<b>DDC_EN, I2C_EN</b>					
V <sub>IH</sub>	High-level input voltage			2	3.6
V <sub>IL</sub>	Low-level input voltage			0	0.8
<b>SRC, OVS</b>					
V <sub>IH_SRC_OVS</sub>	High-level input voltage			3	3.6
V <sub>IL_SRC_OVS</sub>	Low-level input voltage			0	0.5

## DEVICE POWER

The SN75DP139 is designed to operate off of one supply voltage VCC.

The SN75DP139 offers features to enable or disable different functionality based on the status of the output enable (OE\_N) and DDC Enable (DDC\_EN) inputs.

- OE\_N affects only the High Speed Differential channels (Main Link/TMDS link). OE\_N has no influence on the HPD\_SINK input, HPD\_SOURCE output, or the DDC buffer.
- DDC\_EN affects only the DDC channel. The DDC\_EN should never change state during the I2C operation. Disabling DDC\_EN during a bus operation will hang the bus, while enabling the DDC\_EN during bus traffic will corrupt the I2C bus operation. DDC\_EN should only be toggled while the bus is idle.
- TMDS output edge rate control has impact on the SN75DP139 Active power. See [Figure 20](#). TMDS output edge rate can be controlled by SRC pin. Slower output Edge Rate Setting helps in reducing the Active power consumption.

HPD_SINK	HPDINV	OE_N	DDC_EN	IN_Dx	OUT_Dx	DDC	HPD_SOURCE	MODE
Input = H or L	L	L	L	50 Ω termination active	Enabled	High-impedance	Output = non inverted, follows HPD_SINK	Active
Input = H or L	L	L	H	50 Ω termination active	Enabled	enabled	Output = non inverted, follows HPD_SINK	Active
Input = H or L	L	H	L	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	High-impedance	Output = non inverted, follows HPD_SINK	Low Power
Input = H or L	L	H	H	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	enabled	Output = non inverted, follows HPD_SINK	Low Power with DDC channel enabled
Input = H or L	H	L	L	50 Ω termination active	Enabled	High-impedance	Output = inverted, follows HPD_SINK	Active
Input = H or L	H	L	H	50 Ω termination active	Enabled	enabled	Output = inverted, follows HPD_SINK	Active

HPD_SINK	HPDINV	OE_N	DDC_EN	IN_Dx	OUT_Dx	DDC	HPD_SOURCE	MODE
Input = H or L	H	H	L	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	High-impedance	Output = inverted, follows HPD_SINK	Low Power
Input = H or L	H	H	H	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	enabled	Output = inverted, follows HPD_SINK	Low Power with DDC channel enabled
L = LOW, H = HIGH								

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$		<b>HDMI Mode:</b> OE_N = 0V, DDC_EN = 3.6V, $V_{CC}$ = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: $V_I$ = 3.3V, 100 kHz PRBS HPD: HPD_SINK = 5V, I2C_EN = 3.6V, SRC = Hi-Z		82	110	mA
$I_{CC2}$		<b>DVI Mode:</b> OE_N = 0V, DDC_EN = 3.6V, $V_{CC}$ = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: $V_I$ = 3.3V, 100 kHz PRBS HPD: HPD_SINK = 5V, I2C_EN = 0V, SRC = Hi-Z		65	85	mA
$I_{SD1}$		OE_N = 5V, DDC_EN = 0V, HPDINV = 0V, HPD_SINK = 0V		5.5	15	μA
$I_{SD2}$		OE_N = 5V, DDC_EN = 0V, HPDINV = 5V		0.5	0.8	mA
$I_{SD3}$		OE_N = 5V, DDC_EN = 3.6V, HPDINV = 5V		5	8	mA
$I_{SD4}$		OE_N = 5V, DDC_EN = 3.6V, HPDINV = 0V		4.5	7.2	mA

## Hot Plug Detect

The SN75DP139 has a built in level shifter for the HPD outputs. The output voltage level of the HPD pin is defined by the voltage level of the VCC pin. The HPD input or HPD\_SINK side has 130kohm of pull down resistor integrated.

The logic of the HPD\_SOURCE output always follows the logic state of the HPD\_SINK input based on the HPDINV pin logic, regardless of whether the device is in Active or Low Power Mode

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH3.3}$		$I_{OH} = -100 \mu A$ , $V_{CC} = 3.3 V \pm 10\%$ , HPDINV = LOW		2.8	3.6	V
$V_{OH1.1}$		$I_{OH} = -100 \mu A$ , $V_{CC} = 3.3 V \pm 10\%$ , HPDINV = HIGH		0.8	1.1	V
$V_{OL}$		$I_{OH} = 100 \mu A$		0	0.1	V
$I_{IH}$		$V_{IH} = 2.0 V$ , $V_{CC} = 3.6 V$		-30	30	μA
$I_{IL}$		$V_{IL} = 0.8 V$ , $V_{CC} = 3.6 V$		-30	30	μA
$R_{INTHPD}$		Input pull down on HPD_SINK (HPD Input)		110	130	kΩ

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$ Propagation delay	$V_{CC} = 3.6$ V	2		30	ns

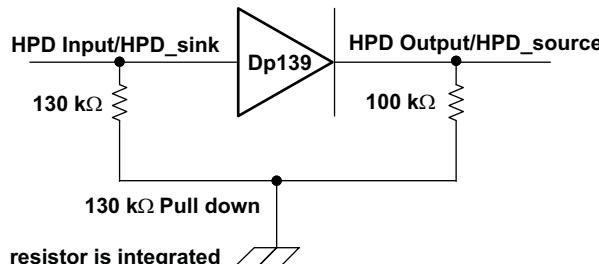


Figure 6. HPD Test Circuit (HPDINV = LOW)

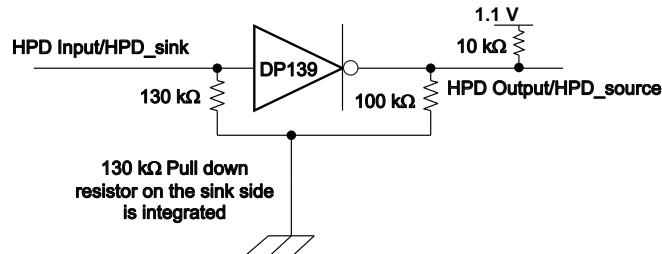


Figure 7. HPD Test Circuit (VOH = 1.1),  
HPDINV=HIGH

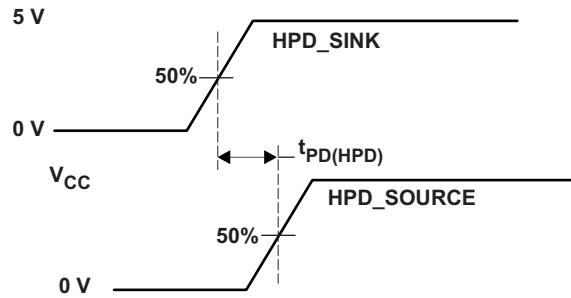


Figure 8. HPD Timing Diagram (HPDINV = LOW)

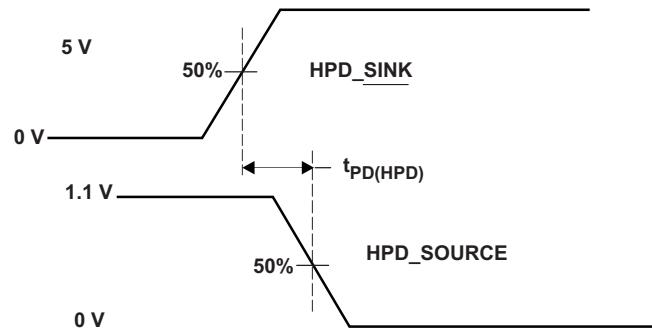


Figure 9. HPD Timing Diagram (HPDINV = HIGH)

## AUX / I<sup>2</sup>C pins

The SN75DP139 utilizes an active I<sup>2</sup>C repeater. The repeater is designed to isolate the parasitic effects of the system in order to aid with system level compliance.

In addition to the I<sup>2</sup>C repeater, the SN75DP139 also supports the connector detection I<sup>2</sup>C register. This register is enabled via the I<sup>2</sup>C\_EN pin. When active an internal memory register is readable via the AUX\_I<sup>2</sup>C I/O. The functionality of this register block is described in the APPLICATION INFORMATION section.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>L</sub>	Low input current	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 V	-10	10	10	µA
I <sub>lk</sub> <sub>g</sub> (AUX)	Input leakage current	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	-10	10	10	µA
C <sub>IO</sub> (AUX)	Input/Output capacitance	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	DC bias = 1.65 V, AC = 2.1Vp-p, f = 100 kHz		15	pF
V <sub>IH</sub> (AUX)	High-level input voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)		1.6	3.6	V
V <sub>IL1</sub> (AUX)	Low-level input voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	OVS = HIGH	-0.2	0.36	V
V <sub>OL1</sub> (AUX)	Low-level output voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	I <sub>O</sub> = 3 mA, OVS = HIGH	0.6	0.7	V
V <sub>IL2</sub> (AUX)	Low-level input voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	OVS = Hi-Z	-0.2	0.36	V
V <sub>OL2</sub> (AUX)	Low-level output voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	I <sub>O</sub> = 3 mA, OVS = Hi-Z	0.5	0.6	V
V <sub>IL3</sub> (AUX)	Low-level input voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	OVS = Low	-0.2	0.27	V
V <sub>OL3</sub> (AUX)	Low-level output voltage	AUX_I <sup>2</sup> C pins (SCL_SOURCE, SDA_SOURCE)	I <sub>O</sub> = 3 mA, OVS = Low	0.4	0.5	V
I <sub>lk</sub> <sub>g</sub> (I <sup>2</sup> C)	Input leakage current	I <sup>2</sup> C SDA/SCL pins (SCL_SINK, SDA_SINK)	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 4.95 V	-10	10	µA
C <sub>IO</sub> (I <sup>2</sup> C)	Input/Output capacitance	I <sup>2</sup> C SDA/SCL pins (SCL_SINK, SDA_SINK)	DC bias = 2.5 V, AC = 3.5Vp-p, f = 100 kHz		15	pF
V <sub>IH</sub> (I <sup>2</sup> C)	High-level input voltage	I <sup>2</sup> C SDA/SCL pins (SCL_SINK, SDA_SINK)		2.1	5.5	V
V <sub>IL</sub> (I <sup>2</sup> C)	Low-level input voltage	I <sup>2</sup> C SDA/SCL pins (SCL_SINK, SDA_SINK)		-0.2	1.5	V
V <sub>OL</sub> (I <sup>2</sup> C)	Low-level output voltage	I <sup>2</sup> C SDA/SCL pins (SCL_SINK, SDA_SINK)	I <sub>O</sub> = 3mA		0.2	V

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$	Propagation delay time, low to high	204	600	ns	
$t_{PHL1}$	Propagation delay time, high to low	35	200	ns	
$t_{PLH2}$	Propagation delay time, low to high	80	251	ns	
$t_{PHL2}$	Propagation delay time, high to low	35	200	ns	
$t_{f1}$	Output signal fall time	20	72	ns	
$t_{f2}$	Output signal fall time	20	72	ns	
$f_{SCL}$	SCL clock frequency for internal register		100	kHz	
$t_{W(L)}$	Clock LOW period for I <sup>2</sup> C register	Source Side	4.7		μs
$t_{W(H)}$	Clock HIGH period for internal register	Source Side	4.0		μs
$t_{SU1}$	Internal register setup time, SDA to SCL	Source Side	250	ns	
$t_{h(1)}$	Internal register hold time, SCL to SDA	Source Side	0		μs
$T_{(buf)}$	Internal register bus free time between STOP and START	Source Side	4.7		μs
$t_{su(2)}$	Internal register setup time, SCL to START	Source Side	4.7		μs
$t_{h(2)}$	Internal register hold time, START to SCL	Source Side	4.0		μs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Source Side	4.0		μs

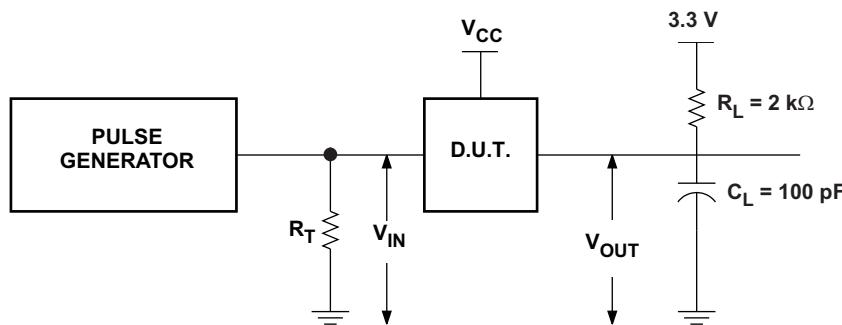


Figure 10. Source Side Test Circuit (SCL\_SOURCE, SDA\_SOURCE)

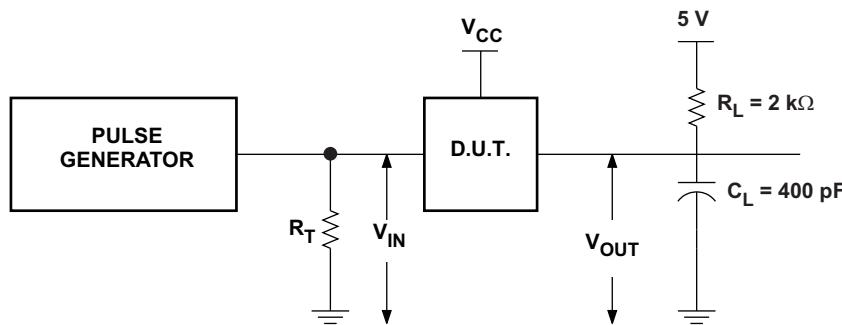
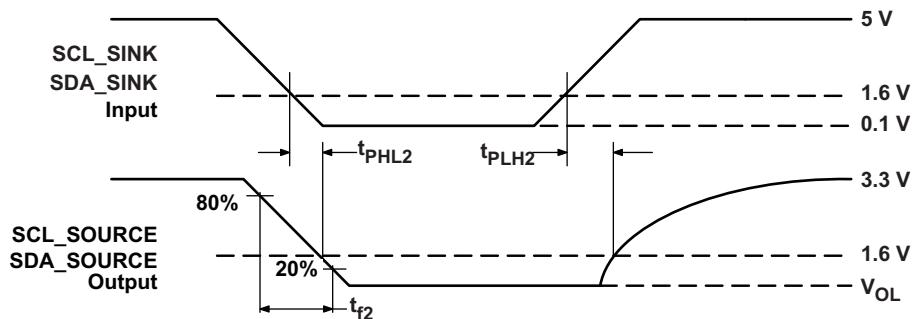
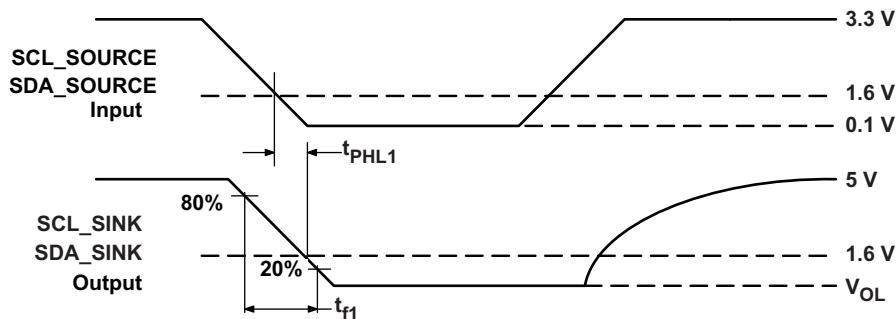


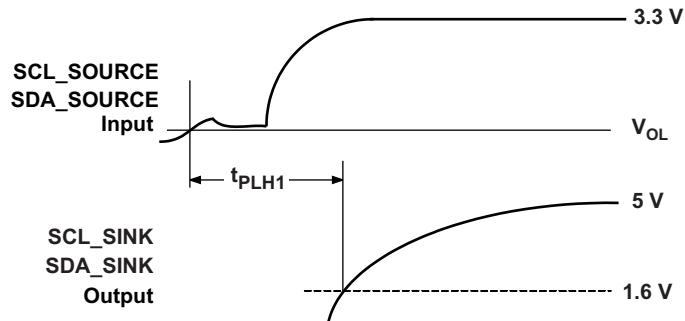
Figure 11. Sink Side Test Circuit (SCL\_SINK, SDA\_SINK)



**Figure 12. Source Side Output AC Measurements**



**Figure 13. Sink Side Output AC Measurements**



**Figure 14. Sink Side Output AC Measurements Continued**

### TMDS and Main link pins

The main link inputs are designed to support DisplayPort 1.1 specification. The TMDS outputs of the SN75DP139 are designed to support the Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.4b specifications. The differential output voltage swing can be fine tuned with the  $R_{V_{Sadj}}$  resistor.

The DP++ (dual-mode) input of the SN75DP139 is designed to accommodate the standard DP level ac coupled signal with no pre-emphasis with up to 16 inches of trace (4 mil 100  $\Omega$  differential stripline).

## ELECTRICAL CHARACTERISTICS

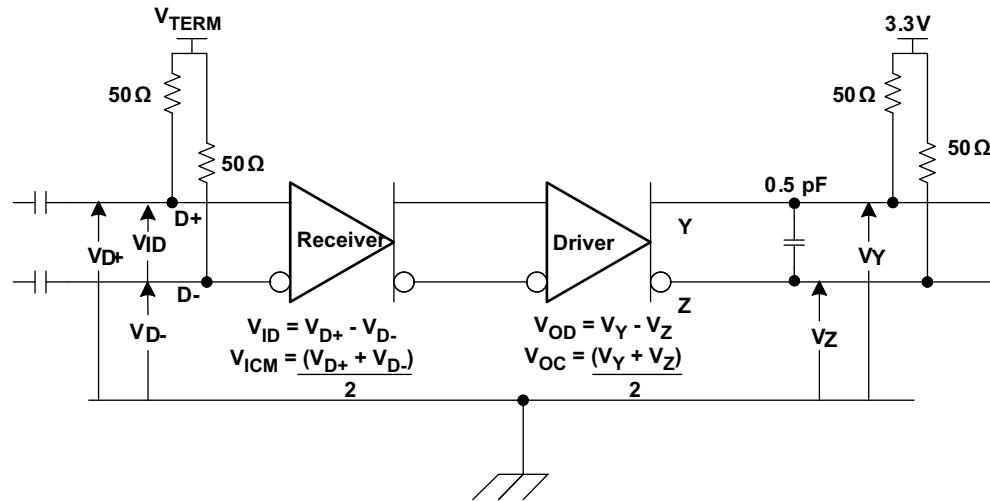
over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	Single-ended HIGH level output voltage AVCC = 3.3 V, $R_T$ = 50 $\Omega$ ,	AVCC–10	AVCC+10		mV
$V_{OL}$		AVCC–600	AVCC–400		mV
$V_{SWING}$		400	600		mV
$V_{OC(ss)}$		–5	5		mV
$V_{OD(PP)}$		800	1200		mV
$V_{(O)SBY}$	Single-ended standby output voltage AVCC = 3.3 V, $R_T$ = 50 $\Omega$ , OE_N = High	AVCC–10	AVCC+10		mV
$I_{(O)OFF}$	Single-ended power down output current 0V $\leq$ VCC $\leq$ 1.5 V, AVCC = 3.3 V, $R_T$ = 50 $\Omega$	–10	10		$\mu$ A
$I_{os}$	Short circuit output current See <a href="#">Figure 19</a>	–15	15		mA
$R_{INT}$	Input termination impedance	40	50	60	$\Omega$
$V_{term}$	Input termination voltage	1	2		V

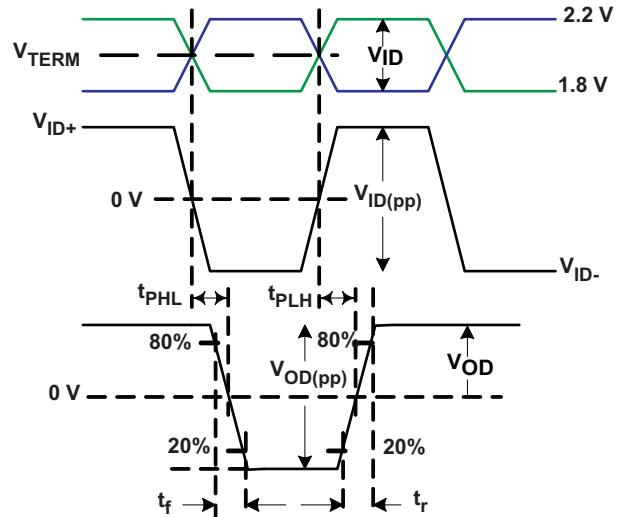
## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

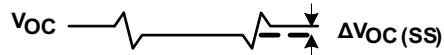
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time	250	350	600	ps
$t_{PHL}$	Propagation delay time	250	350	600	ps
$t_{R1}$	Rise Time (I <sub>2</sub> C_EN = HI, SRC = Hi-Z)	60	85	120	ps
$t_{F1}$	Fall Time (I <sub>2</sub> C_EN = HI, SRC = Hi-Z)	60	85	120	ps
$t_{R2}$	Rise Time (I <sub>2</sub> C_EN = Low, SRC = Hi-Z)	115	150		ps
$t_{F2}$	Fall Time (I <sub>2</sub> C_EN = Low, SRC = Hi-Z)	115	150		ps
$t_{R3}$	Rise Time (I <sub>2</sub> C_EN = HI, SRC = HI)	150	180		ps
$t_{F3}$	Fall Time (I <sub>2</sub> C_EN = HI, SRC = HI)	150	180		ps
$t_{R4}$	Rise Time (I <sub>2</sub> C_EN = HI, SRC = Low)	115	150		ps
$t_{F4}$	Fall Time (I <sub>2</sub> C_EN = HI, SRC = Low)	115	150		ps
$t_{R5}$	Rise Time (I <sub>2</sub> C_EN = Low, SRC = HI)	175	220		ps
$t_{F5}$	Fall Time (I <sub>2</sub> C_EN = Low, SRC = HI)	175	220		ps
$t_{R6}$	Rise Time (I <sub>2</sub> C_EN = Low, SRC = Low)	150	180		ps
$t_{F6}$	Fall Time (I <sub>2</sub> C_EN = Low, SRC = Low)	150	180		ps
$t_{SK(P)}$	Pulse skew	8	15		ps
$t_{SK(D)}$	Intra-pair skew	20	65		ps
$t_{SK(O)}$	Inter-pair skew	20	100		ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter AVCC = 3.3 V, $R_T$ = 50 $\Omega$ , dR = 3 Gbps, TMDS output slew rate (default). $R_{Vadj}$ = 4.02 k $\Omega$ (refer to <a href="#">Figure 18</a> )	14	50		ps
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter AVCC = 3.3 V, $R_T$ = 50 $\Omega$ , f = 300 MHz TMDS output slew rate (default). $R_{Vadj}$ = 4.02 k $\Omega$ (refer to <a href="#">Figure 18</a> )	8	30		ps



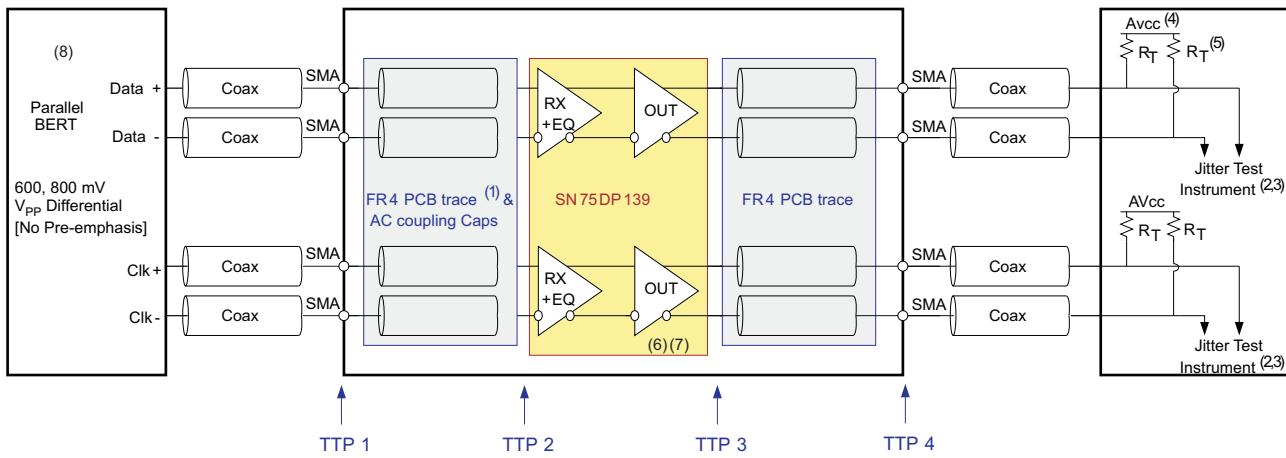
**Figure 15. TMDS Main Link Test Circuit**



**Figure 16. TMDS Main Link Timing Measurements**

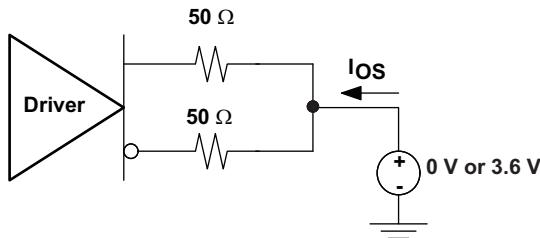


**Figure 17. TMDS Main Link Common Mode Measurements**



1. The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling cap, connector and another 1-8" of FR4. Trace width - 4 mils.
2. All Jitter is measured at a BER of  $10^{-9}$
3. Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1
4. AVCC = 3.3V
5. RT = 50Ω,
6. Jitter data is taken with SN75DP139 configured in the fastest slew rate setting(default)
7. Rvsadj = 4.02kΩ
8. The input signal from parallel BERT does not have any pre-emphasis. Refer to recommended operating conditions

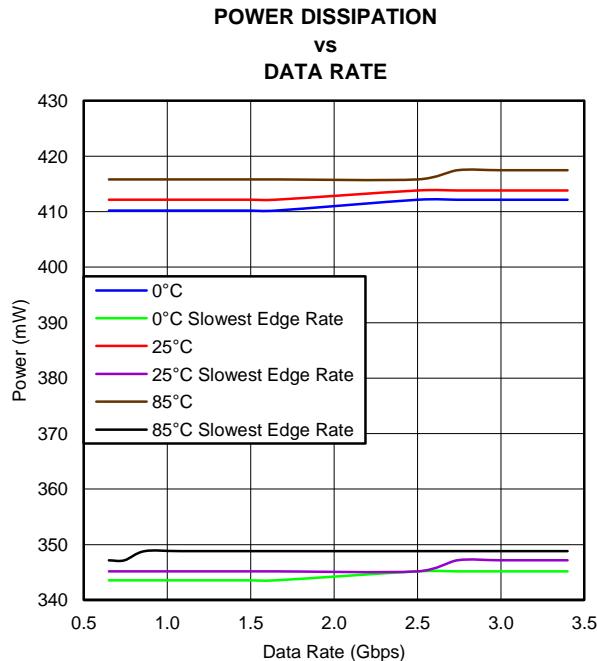
**Figure 18. TMDS Jitter Measurements**



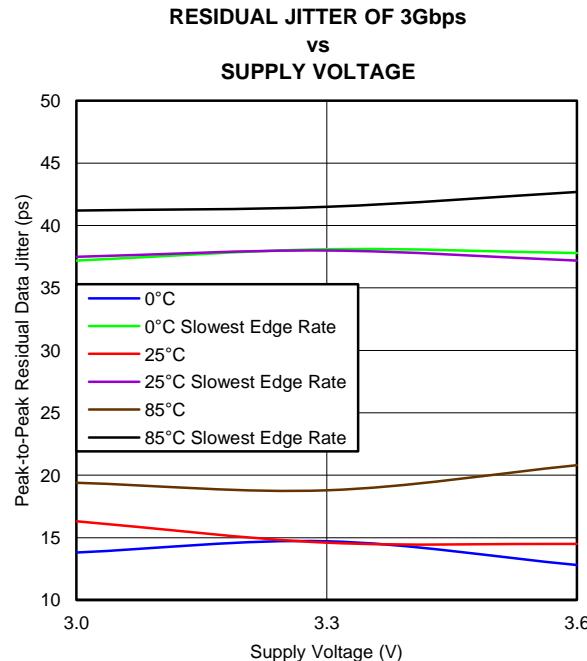
**Figure 19. TMDS Main Link Short Circuit Output Circuit**

## TYPICAL CHARACTERISTICS

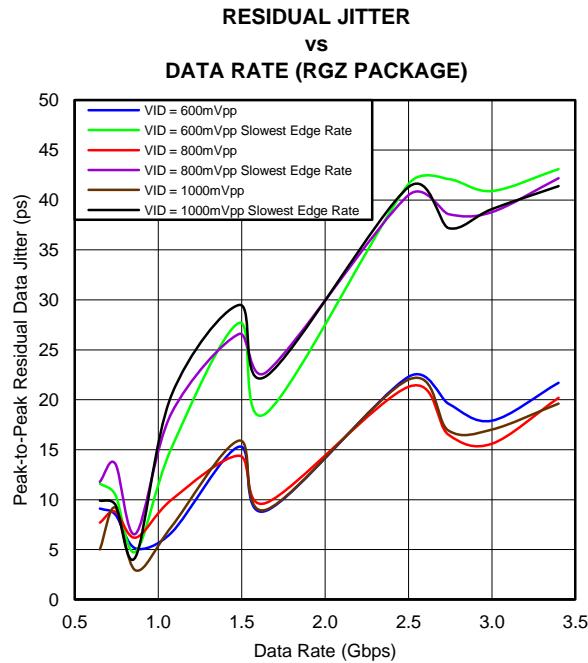
AVCC = 3.3 V,  $R_T$  = 50Ω



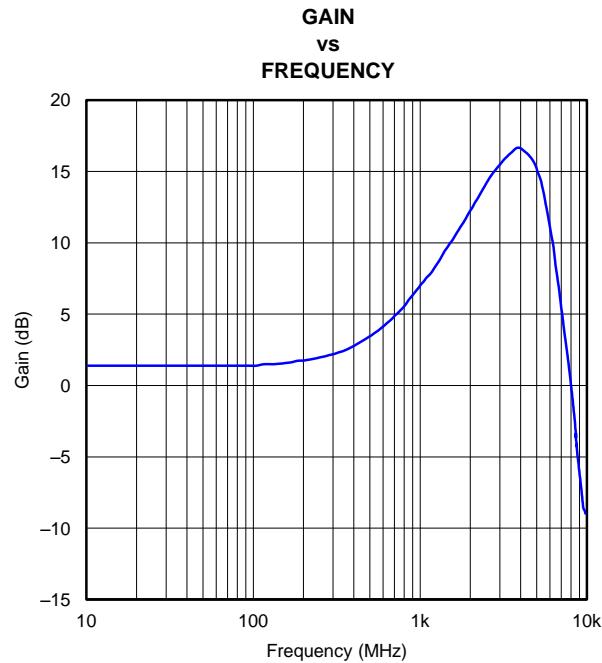
**Figure 20.**



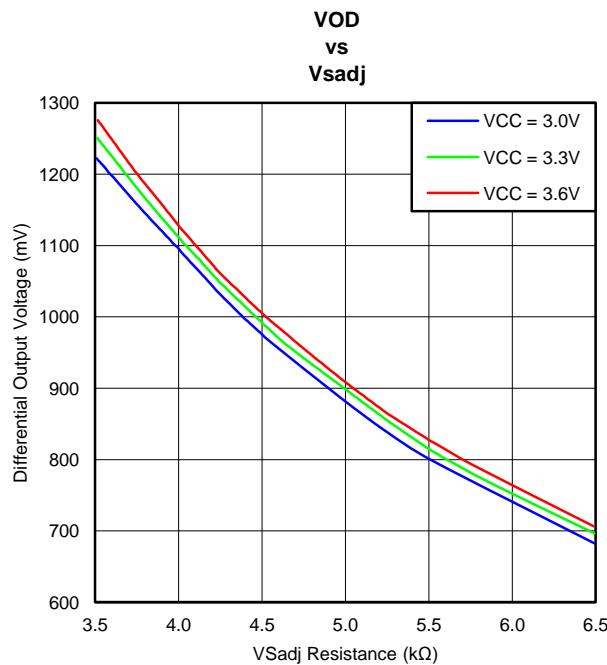
**Figure 21.**



**Figure 22.**



**Figure 23.**

**TYPICAL CHARACTERISTICS (continued)**AVCC = 3.3 V,  $R_T$  = 50 $\Omega$ **Figure 24.**

## APPLICATION INFORMATION

### DVI APPLICATION

In DVI application case, it is recommended that between the SN75DP139 TMDS outputs (OUT\_Dx) and a through hole DVI connector a series resistor placeholder is incorporated. This could help in case if there are signal integrity issues as well as help pass system level compliance.

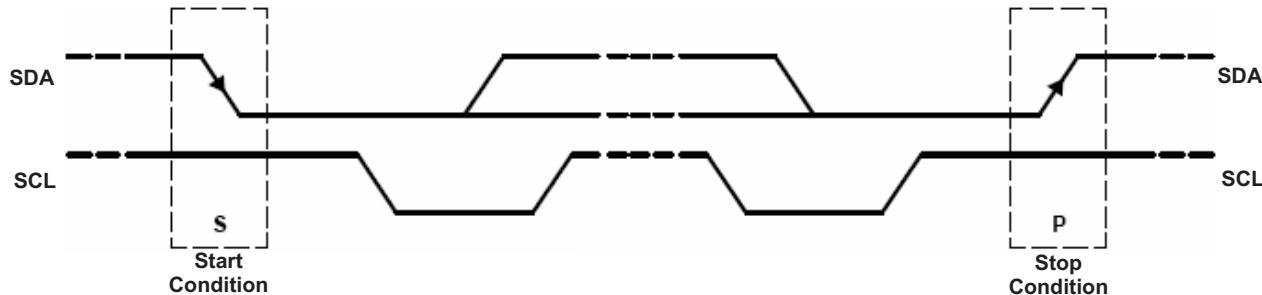
### I<sup>2</sup>C INTERFACE NOTES

The I<sup>2</sup>C interface can be used to access the internal memory of the SN75DP139. I<sup>2</sup>C is a two-wire serial interface developed by Philips Semiconductor (see I<sup>2</sup>C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C compatible devices connect to the I<sup>2</sup>C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The SN75DP139 works as a slave and supports the standard mode transfer (100 kbps) as defined in the I<sup>2</sup>C-Bus Specification.

The basic I<sup>2</sup>C start and stop access cycles are shown in [Figure 25](#).

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

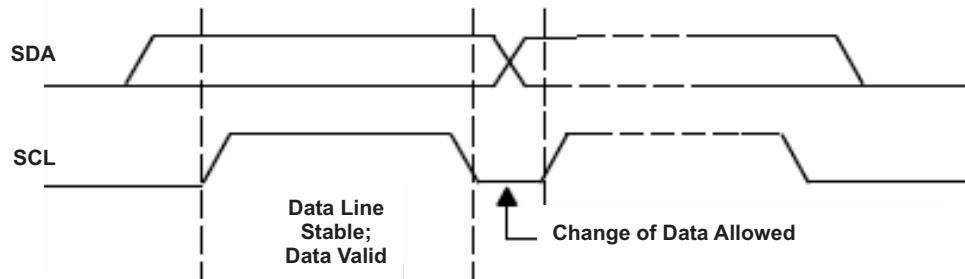
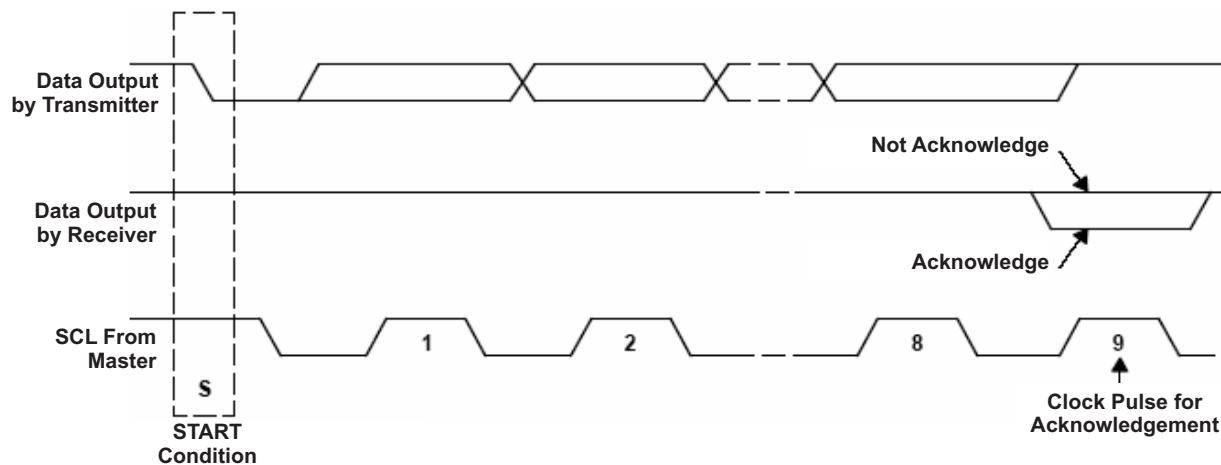
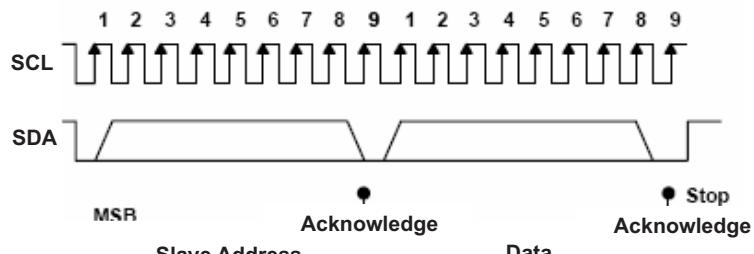


**Figure 25. I<sup>2</sup>C Start and Stop Conditions**

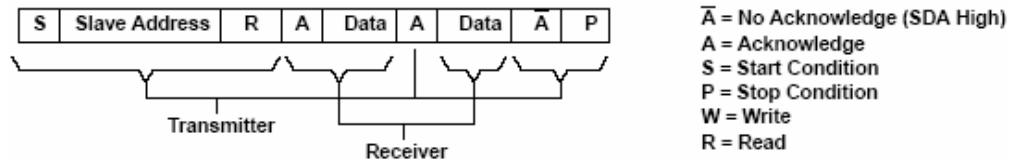
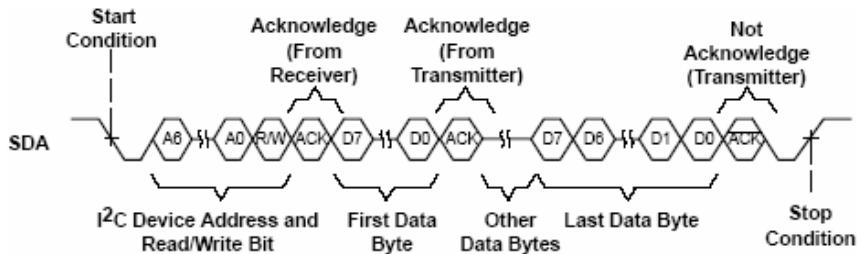
### GENERAL I<sup>2</sup>C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in [Figure 27](#). All I<sup>2</sup>C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data condition* requires the SDA line to be stable during the entire high period of the clock pulse (see [Figure 26](#)). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see [Figure 27](#)) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See [Figure 28](#) ).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see [Figure 28](#)). This releases the bus and stops the communication link

with the addressed slave. All I<sup>2</sup>C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

Figure 26. I<sup>2</sup>C Bit TransferFigure 27. I<sup>2</sup>C AcknowledgeFigure 28. I<sup>2</sup>C Address and Data Cycles

During a read cycle, the slave receiver will acknowledge the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in [Figure 29](#) and [Figure 30](#). See Example – Reading from the SN75DP139 section for more information.


**Figure 29. I<sup>2</sup>C Read Cycle**

**Figure 30. Multiple Byte Read Transfer**

## SLAVE ADDRESS

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I<sup>2</sup>C specification that ranges from 2k $\Omega$  to 19k $\Omega$ . When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7 bit address is factory preset to 1000000. [Table 2](#) lists the calls that the SN75DP139 will respond to.

**Table 2. SN75DP139 Slave Address**

Fixed Address							Read/Write Bit
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (R/W)
1	0	0	0	0	0	0	1

## Sink Port Selection Register and Source Plug-In Status Register Description (Sub-Address)

The SN75DP139 operates using a multiple byte transfer protocol similar to [Figure 30](#). The internal memory of the SN75DP139 contains the phrase “DP-HDMI ADAPTOR<EOT>” converted to ASCII characters. The internal memory address registers and the value of each can be found in [Table 3](#).

During a read cycle, the SN75DP139 will send the data in its selected sub-address in a single transfer to the master device requesting the information. See the [Example – Reading from the SN75DP139](#) section of this document for the proper procedure on reading from the SN75DP139.

**Table 3. SN75DP139 Sink Port and Source Plug-In Status Registers Selection**

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04	FF

## EXAMPLE – READING FROM THE SN75DP139:

The read operation consists of several steps. The I<sup>2</sup>C master begins the communication with the transmission of the start sequence followed by the slave address of the SN75DP139 and logic address of 00h. The SN75DP139 will acknowledge its presence to the master and begin to transmit the contents of the memory registers. After each byte is transferred the SN75DP139 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master. If an ACK is received the next byte of data will be transmitted. If a NACK is received the data transmission sequence is expected to end and the master should send the stop command.

The SN75DP139 will continue to send data as long as the master continues to acknowledge each byte transmission. If an ACK is received after the transmission of byte 0x0F the SN75DP139 will transmit byte 0x10 and continue to transmit byte 0x10 for all further ACK's until a NACK is received.

The SN75DP139 also supports an accelerated read mode where steps 1–6 can be skipped.

### SN75DP139 Read Phase

<b>Step 1</b>	<b>0</b>							
I <sup>2</sup> C Start (Master)	S							

<b>Step 2</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C General Address Write (Master)	1	0	0	0	0	0	0	0

<b>Step 3</b>	<b>9</b>							
I <sup>2</sup> C Acknowledge (Slave)	A							

<b>Step 4</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Logic Address (Master)	0	0	0	0	0	0	0	0

<b>Step 5</b>	<b>9</b>							
I <sup>2</sup> C Acknowledge (Slave)	A							

<b>Step 6</b>	<b>0</b>							
I <sup>2</sup> C Stop (Master)	P							

<b>Step 7</b>	<b>0</b>							
I <sup>2</sup> C Start (Master)	S							

<b>Step 8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C General Address Read (Master)	1	0	0	0	0	0	0	1

<b>Step 9</b>	<b>9</b>							
I <sup>2</sup> C Acknowledge (Slave)	A							

<b>Step 10</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Read Data (Slave)	Data							

Where Data is determined by the Logic values Contained in the Sink Port Register

<b>Step 11</b>	<b>9</b>							
I <sup>2</sup> C Not-Acknowledge (Master)	X							

Where X is an A (Acknowledge) or  $\bar{A}$  (Not-Acknowledge)  
An A causes the pointer to increment and step 10 is repeated.  
An  $\bar{A}$  causes the slave to stop transmitting and proceeds to step 12.

<b>Step 12</b>	<b>0</b>
I <sup>2</sup> C Stop (Master)	P

## REVISION HISTORY

Changes from Revision A (July 2010) to Revision B	Page
• Added to FEATURES "40 Pin 5 x 5 QFN (RSB) Package" .....	1
• Changed OUT_Dx terminal connections .....	3
• Added RSB package drawing .....	5
• Changed PIN FUNCTIONS to include RSB package pins .....	6
• Added RSB package to ORDERING INFORMATION table .....	10
• Changed voltage range section of Absolute Maximum Ratings .....	10
• Changed thermal resistance info and enable voltages to 3.6V .....	11
• Changed input voltages within the Recommended Operating Conditions .....	11
• Changed enable voltages from 5V to 3.6V .....	13
• Changed $V_{IH(AUX)}$ max from 5.5V to 3.6V .....	15

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75DP139RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP139	<b>Samples</b>
SN75DP139RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP139	<b>Samples</b>
SN75DP139RSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	DP139	<b>Samples</b>
SN75DP139RSBT	ACTIVE	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	DP139	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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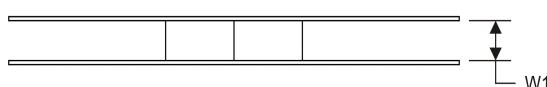
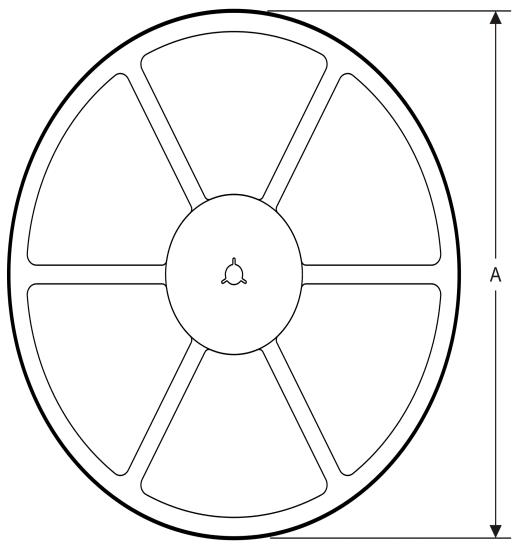
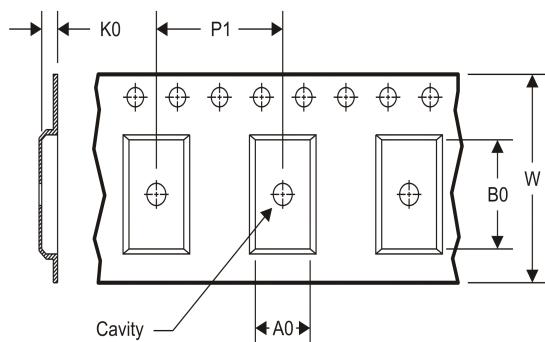


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## PACKAGE OPTION ADDENDUM

11-Apr-2013

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP139RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP139RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP139RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP139RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
SN75DP139RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

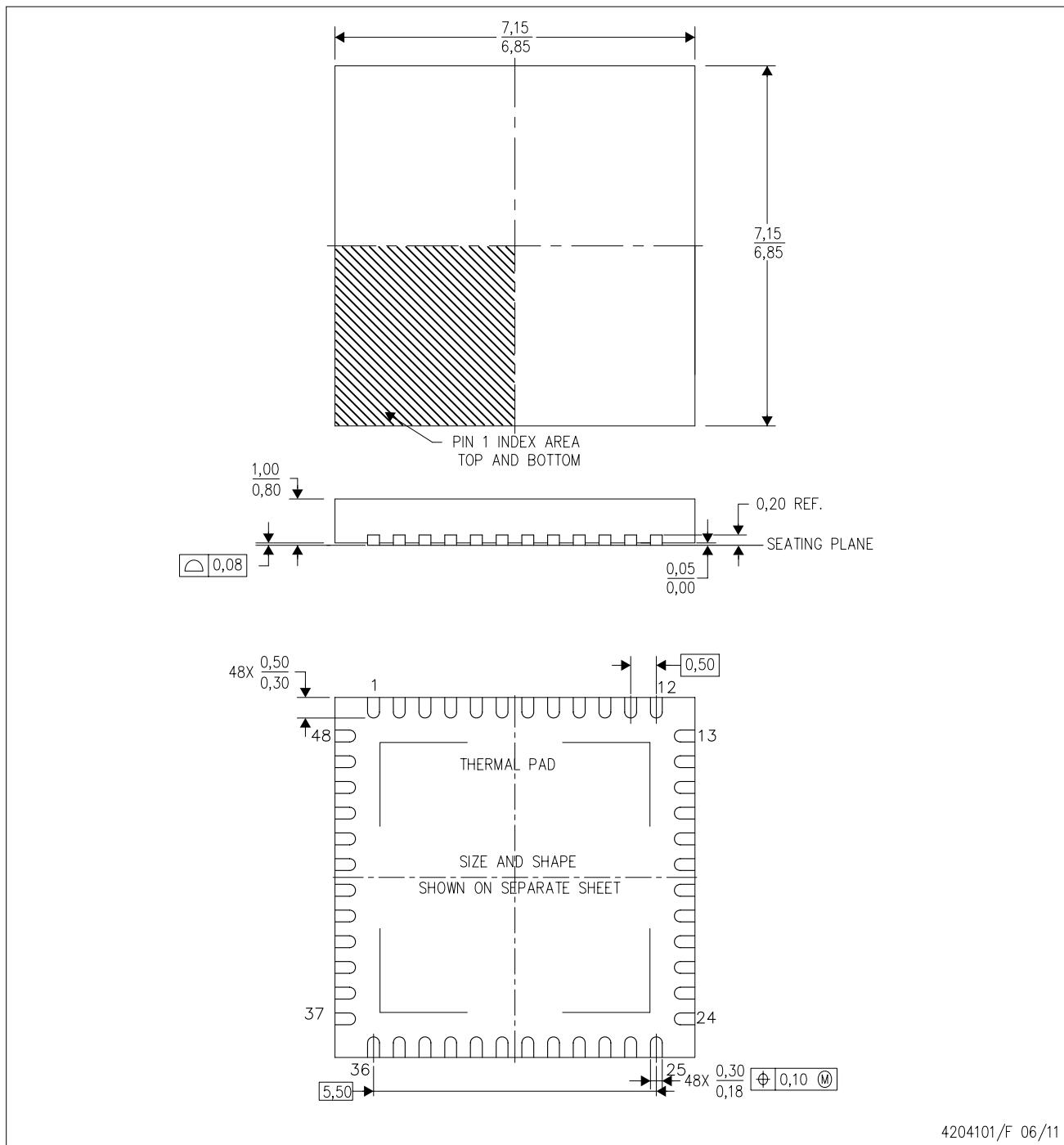
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP139RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP139RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP139RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
SN75DP139RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
SN75DP139RSBT	WQFN	RSB	40	250	210.0	185.0	35.0

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Quad Flatpack, No-leads (QFN) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RGZ (S-PVQFN-N48)

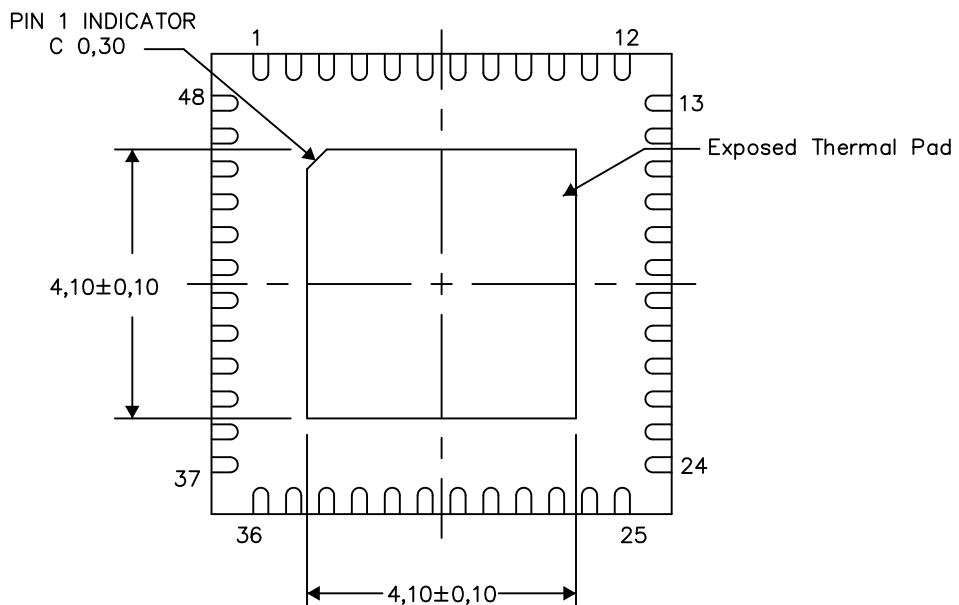
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

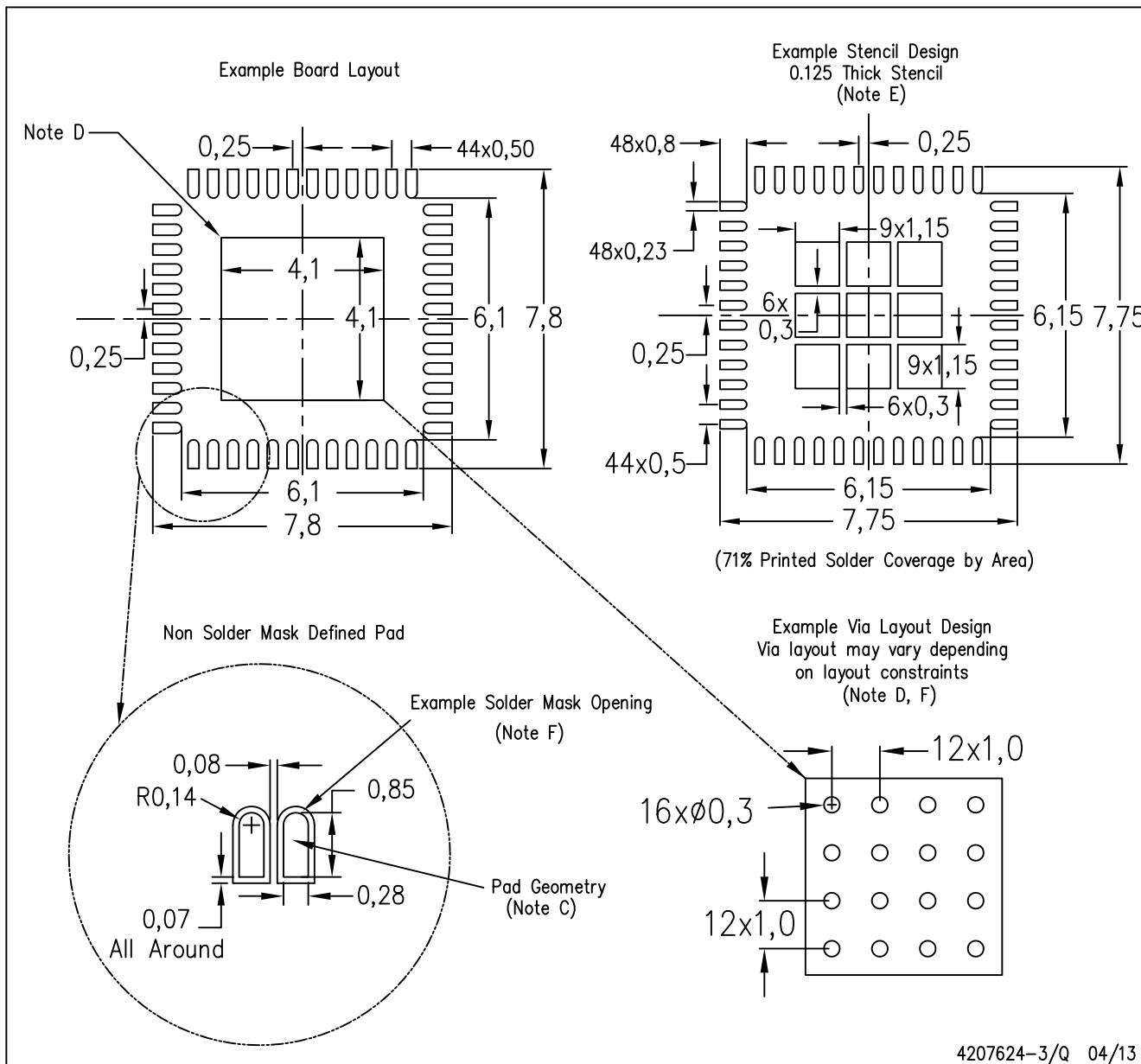
Exposed Thermal Pad Dimensions

4206354-3/U 04/13

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4207624-3/Q 04/13

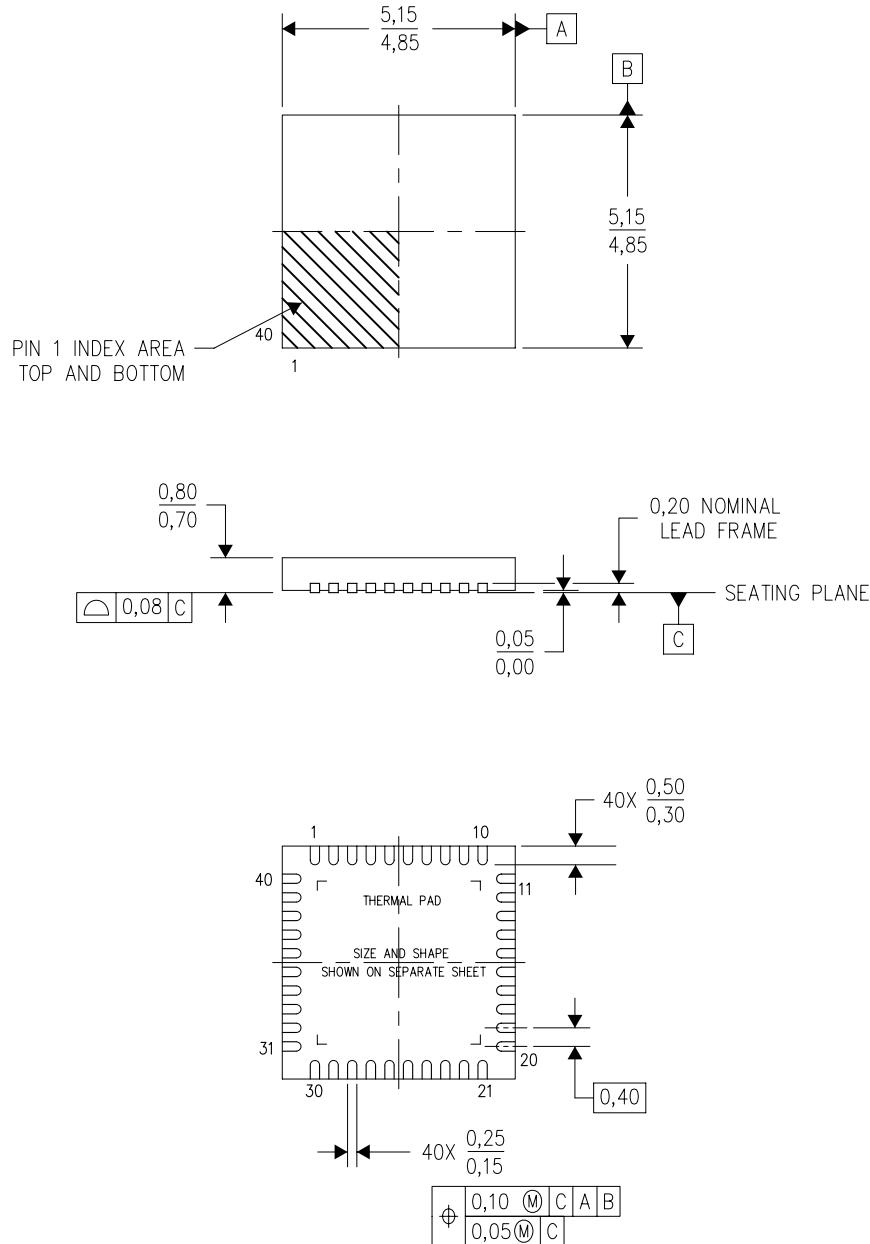
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## MECHANICAL DATA

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207182/C 05/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

# THERMAL PAD MECHANICAL DATA

RSB (S-PWQFN-N40)

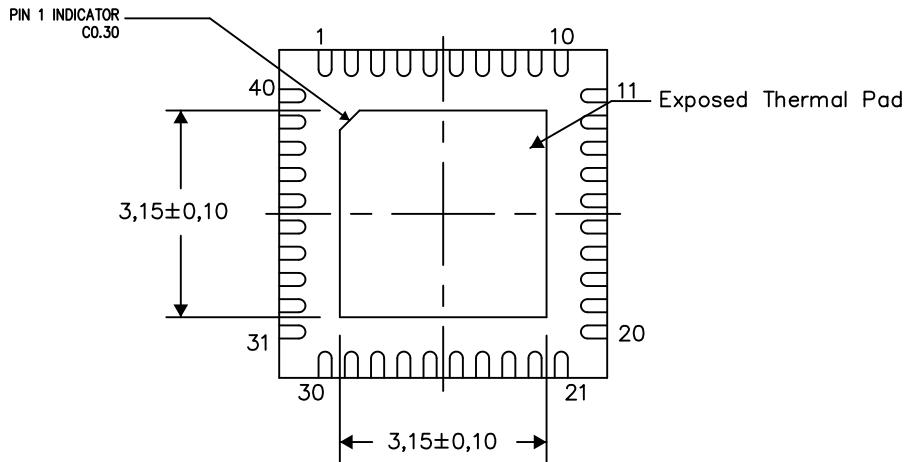
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

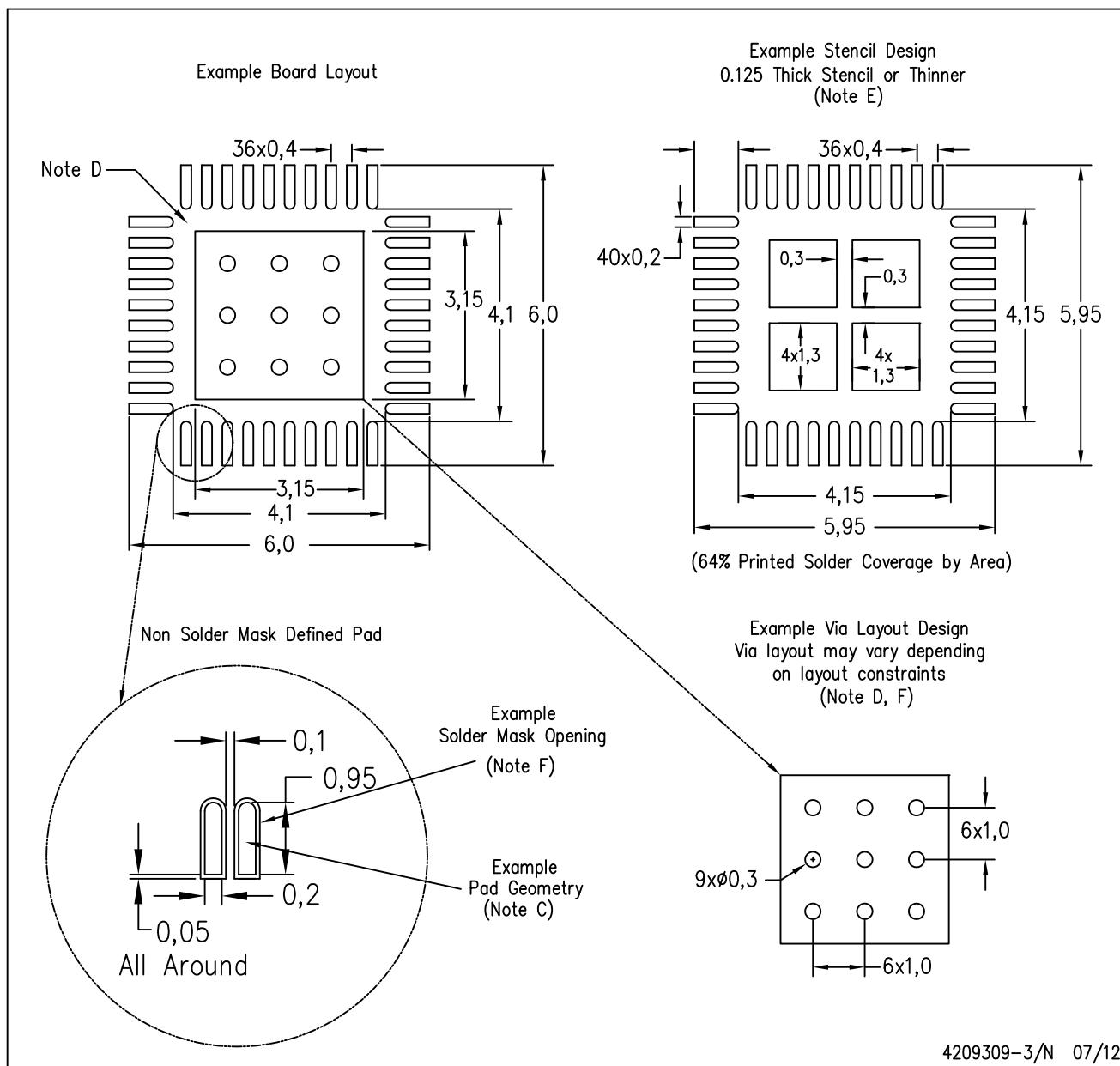
Exposed Thermal Pad Dimensions

4207183-3/P 06/12

NOTE: All linear dimensions are in millimeters

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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