

## Low-Power Dual Digital Isolators

 Check for Samples: [ISO7420](#), [ISO7420M](#), [ISO7421](#)

### FEATURES

- Highest Signaling Rate: 1 Mbps
- Low Power Consumption, Typical  $I_{CC}$  per Channel (3.3V operation):
  - ISO7420: 1.1 mA, ISO7421: 1.5 mA
- Low Propagation Delay – 9 ns Typ. and Low Skew – 300 ps Typ.
- Wide  $T_A$  Range Specified:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- UL 1577 Approved with 2.5 kVrms Rating
- 4242 Vpeak Isolation
- CSA, IEC 60950-1 and IEC 61010-1 Approved
- 50 kV/ $\mu\text{s}$  Transient Immunity, Typical
- Over 25-Year Isolation Integrity at Rated Voltage
- Operates From 3.3V and 5V Supply and Logic Levels

### APPLICATIONS

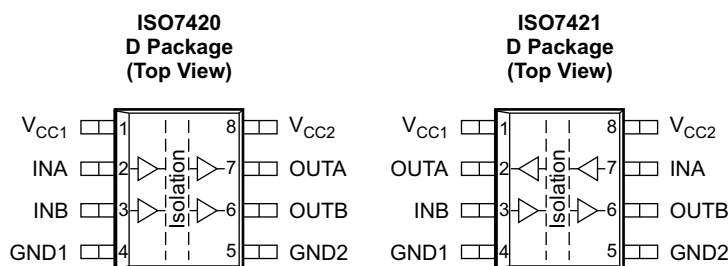
- Optocoupler Replacement in:
  - Industrial Fieldbus
  - Profibus
  - Modbus
  - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

### DESCRIPTION

The ISO7420, ISO7420M and ISO7421 provide galvanic isolation up to 2.5 kVrms for 1 minute per UL. These digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide ( $\text{SiO}_2$ ) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix M indicates wide temperature range ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ).

The devices have TTL input thresholds and require two supply voltages, 3.3V or 5V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3V supply.

Note: The ISO7420 and ISO7421 are specified for signaling rates up to 1 Mbps. Due to their fast response time, under most cases, these devices will also transmit data with much shorter pulse widths. Designers should add external filtering to remove spurious signals with input pulse duration  $< 20\text{ns}$  if desired.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
INA	7	I	Input, channel A
INB	3	I	Input, channel B
GND1	4	–	Ground connection for $V_{CC1}$
GND2	5	–	Ground connection for $V_{CC2}$
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
$V_{CC1}$	1	–	Power supply, $V_{CC1}$
$V_{CC2}$	8	–	Power supply, $V_{CC2}$

Table 1. FUNCTION TABLE<sup>(1)</sup>

INPUT SIDE VCC	OUTPUT SIDE VCC	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H <sup>(2)</sup>
PD	PU	X	H <sup>(2)</sup>

- (1) PU = Powered up ( $V_{CC} \geq 3$  V); PD = Powered down ( $V_{CC} \leq 2.4$  V);  
X = Irrelevant; H = High level; L = Low level  
(2) In fail-safe condition, output is at high level for ISO7420, ISO7420M  
and ISO7421.

### AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	RATED $T_A$	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7420	2.5 kVrms	D-8	~1.5 V (TTL) (CMOS compatible)	–40°C to 105°C	Same direction	IS7420	ISO7420D (rail) ISO7420DR (reel)
ISO7420M				–40°C to 125°C		I7420M	ISO7420MD (rail) ISO7420MDR (reel)
ISO7421				–40°C to 105°C	Opposite directions	IS7421	ISO7421D (rail) ISO7421DR (reel)

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

				VALUE	
$V_{CC}$	Supply voltage <sup>(2)</sup> , $V_{CC1}$ , $V_{CC2}$			-0.5 V to 6 V	
$V_I$	Voltage at IN, OUT			-0.5 V to 6 V	
$I_O$	Output current			±15 mA	
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4 kV
		Field-induced charged-device model	JEDEC Standard 22, Test Method C101		±1.5 kV
		Machine model	ANSI/ESDS5.2-1996		±200 V
$T_{J(Max)}$	Maximum junction temperature			150°C	
$T_{stg}$	Storage temperature			-65°C to 150°C	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
$V_{CC1}$ , $V_{CC2}$	Supply voltage - 3.3V operation	3.15	3.3	3.45	V
	Supply voltage - 5V operation	4.75	5	5.25	
$I_{OH}$	High-level output current	-4			mA
$I_{OL}$	Low-level output current			4	mA
$V_{IH}$	High-level input voltage	2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	0		0.8	V
$T_J^{(1)}$	Junction temperature	-40		136	°C
$1/t_{ui}$	Signaling rate	0		1	Mbps
$t_{ui}$	Input pulse duration	1			us

- (1) To maintain the recommended operating conditions for  $T_J$ , see the [Package Thermal Characteristics](#) table.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$  and  $V_{CC2}$  at  $5V \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for ISO7420M,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  for ISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}$ ; see <a href="#">Figure 1</a> .	$V_{CC} - 0.8$	4.6		V
		$I_{OH} = -20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .	$V_{CC} - 0.1$	5		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ ; see <a href="#">Figure 1</a> .		0.2	0.4	V
		$I_{OL} = 20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at 0 V or $V_{CC}$			10	$\mu\text{A}$
$I_{IL}$	Low-level input current		-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see <a href="#">Figure 3</a> .	25	50		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)</b>						
<b>ISO7420</b>						
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps $V_I = V_{CC}$ or 0 V, 15 pF load		0.4	1	mA
$I_{CC2}$	Supply current for $V_{CC2}$			3	6	
<b>ISO7421</b>						
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps $V_I = V_{CC}$ or 0 V, 15 pF load		2	4	mA
$I_{CC2}$	Supply current for $V_{CC2}$			2	4	

## SWITCHING CHARACTERISTICS

$V_{CC1}$  and  $V_{CC2}$  at  $5V \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for ISO7420M,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  for ISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 1</a> .		9	14	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
$t_r$	Output signal rise time	See <a href="#">Figure 1</a> .		1		ns
$t_f$	Output signal fall time			1		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 2</a> .		6		$\mu\text{s}$

(1) Also known as pulse skew.

## ELECTRICAL CHARACTERISTICS

 $V_{CC1}$  at  $5V \pm 5\%$ ,  $V_{CC2}$  at  $3.3V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $125^\circ C$  for ISO7420M,  $T_A = -40^\circ C$  to  $105^\circ C$  for ISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}$ ; see <a href="#">Figure 1</a> .	ISO7421 (5-V side)	$V_{CC} - 0.8$	4.6		V
			ISO7420 / 7421 (3.3-V side)	$V_{CC} - 0.4$	3		
				$V_{CC} - 0.1$	$V_{CC}$		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ ; see <a href="#">Figure 1</a> .			0.2	0.4	V
		$I_{OL} = 20 \text{ }\mu\text{A}$ ; see <a href="#">Figure 1</a> .			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	INx at 0 V or $V_{CC}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current				-10		$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see <a href="#">Figure 3</a> .		25	40		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)</b>							
<b>ISO7420</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		0.4	1	mA
$I_{CC2}$	Supply current for $V_{CC2}$				2	4.5	mA
<b>ISO7421</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		2	4	mA
$I_{CC2}$	Supply current for $V_{CC2}$				1.5	3.5	mA

## SWITCHING CHARACTERISTICS

 $V_{CC1}$  at  $5V \pm 5\%$ ,  $V_{CC2}$  at  $3.3V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $125^\circ C$  for ISO7420M,  $T_A = -40^\circ C$  to  $105^\circ C$  for ISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 1</a> .		10	17	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
$t_r$	Output signal rise time	See <a href="#">Figure 1</a> .		2		ns
$t_f$	Output signal fall time			2		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 2</a> .		6		$\mu\text{s}$

(1) Also known as pulse skew.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$  at  $3.3V \pm 5\%$ ,  $V_{CC2}$  at  $5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $125^\circ C$  for ISO7420M,  $T_A = -40^\circ C$  to  $105^\circ C$  for ISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}$ ; see <a href="#">Figure 1</a> .	ISO7420 / 7421 (5-V side).	$V_{CC} - 0.8$	4.6		V
			ISO7421 (3.3-V side)	$V_{CC} - 0.4$	3		
			$I_{OH} = -20 \text{ } \mu\text{A}$ ; see <a href="#">Figure 1</a>	$V_{CC} - 0.1$	$V_{CC}$		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ ; see <a href="#">Figure 1</a> .			0.2	0.4	V
		$I_{OL} = 20 \text{ } \mu\text{A}$ ; see <a href="#">Figure 1</a> .			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	INx at 0 V or $V_{CC}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current				-10		$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see <a href="#">Figure 3</a> .		25	40		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)</b>							
<b>ISO7420</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		0.2	0.7	mA
$I_{CC2}$	Supply current for $V_{CC2}$				3	6	
<b>ISO7421</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		1.5	3.5	mA
$I_{CC2}$	Supply current for $V_{CC2}$				2	4	

## SWITCHING CHARACTERISTICS

$V_{CC1}$  at  $3.3V \pm 5\%$ ,  $V_{CC2}$  at  $5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $125^\circ C$  for ISO7420M,  $T_A = -40^\circ C$  to  $105^\circ C$  for ISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 1</a> .			10	17	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $				0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time					8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time					4	ns
$t_r$	Output signal rise time	See <a href="#">Figure 1</a> .			2		ns
$t_f$	Output signal fall time				2		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 2</a> .			6		$\mu\text{s}$

(1) Also known as pulse skew.

## ELECTRICAL CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2}$  at  $3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for ISO7420M,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  for ISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4 \text{ mA}$ ; see <a href="#">Figure 1</a> .		$V_{CC} - 0.4$	3		V
		$I_{OH} = -20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .		$V_{CC} - 0.1$	3.3		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4 \text{ mA}$ ; see <a href="#">Figure 1</a> .			0.2	0.4	V
		$I_{OL} = 20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at 0 V or $V_{CC}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current					-10	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see <a href="#">Figure 3</a> .		25	40		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)</b>							
<b>ISO7420</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		0.2	0.7	mA
$I_{CC2}$	Supply current for $V_{CC2}$				2	4.5	
<b>ISO7421</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC}$ or 0 V, 15 pF load		1.5	3.5	mA
$I_{CC2}$	Supply current for $V_{CC2}$				1.5	3.5	

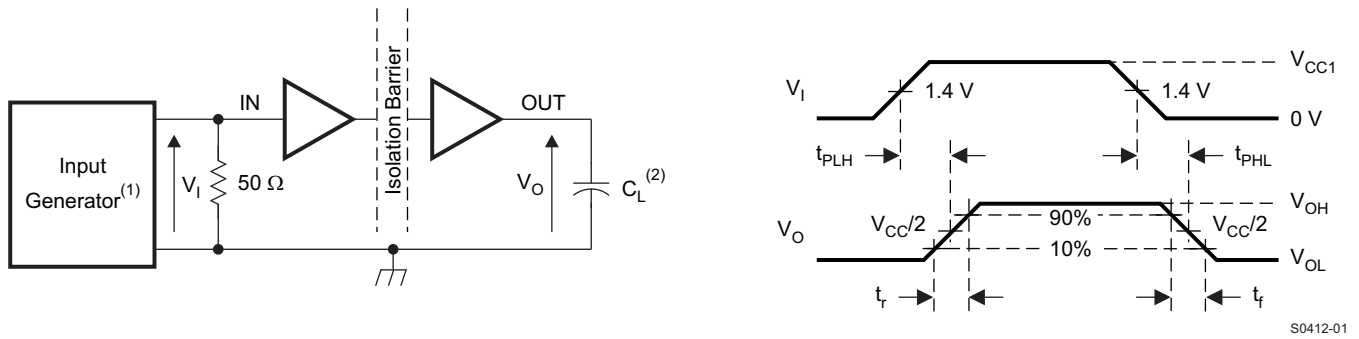
## SWITCHING CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2}$  at  $3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for ISO7420M,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  for ISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 1</a> .		12	20	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time			5.5	ns	
$t_r$	Output signal rise time	See <a href="#">Figure 1</a> .		2		ns
$t_f$	Output signal fall time			2		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 2</a> .		6		$\mu\text{s}$

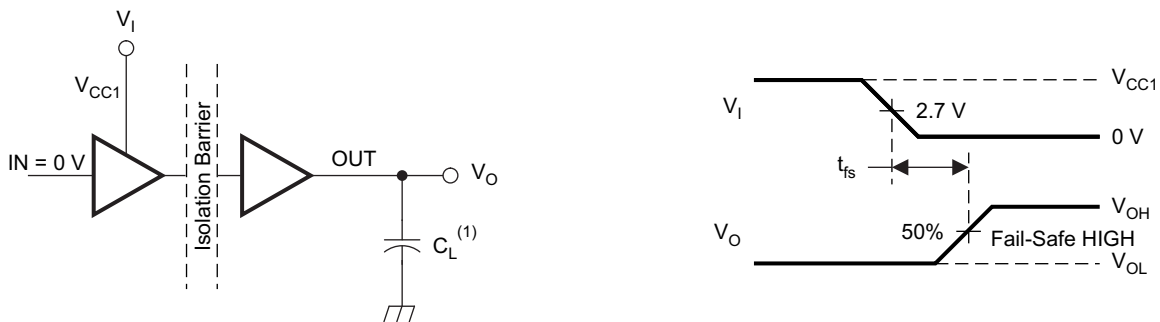
(1) Also known as pulse skew.

PARAMETER MEASUREMENT INFORMATION



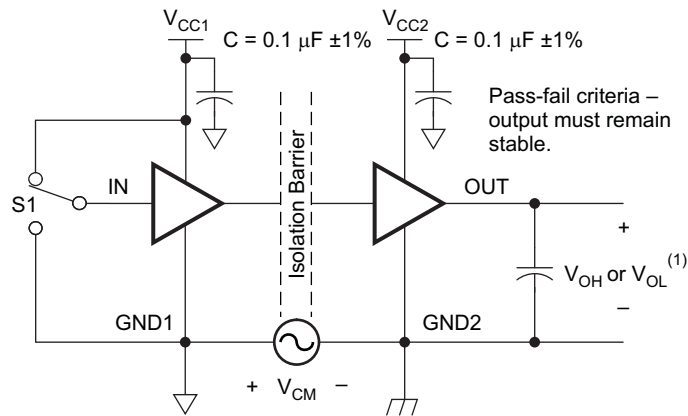
- (1) The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50 \Omega$ . At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in an actual application.
- (2)  $C_L = 15 \text{ pF} \pm 20\%$  includes instrumentation and fixture capacitance.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- (1)  $C_L = 15 \text{ pF} \pm 20\%$  includes instrumentation and fixture capacitance.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



- (1)  $C_L = 15 \text{ pF} \pm 20\%$  includes instrumentation and fixture capacitance.

Figure 3. Common-Mode Transient Immunity Test Circuit



## DEVICE INFORMATION

### PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R <sub>IO</sub>	Isolation resistance, input to output <sup>(1)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> < 100°C	>10 <sup>12</sup>			Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ max	>10 <sup>11</sup>			Ω
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(1)</sup>	V <sub>IO</sub> = 0.4 sin(2πft), f = 1 MHz		1		pF
C <sub>I</sub>	Input capacitance <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> /2 + 0.4 sin(2πft), f = 1 MHz, V <sub>CC</sub> = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.

(2) Measured from input pin to ground.

#### NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

### INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	SPECIFICATION	UNIT
V <sub>IORM</sub>	Maximum working insulation voltage <sup>(2)</sup>		566	V <sub>peak</sub>
V <sub>PR</sub>	Input-to-output test voltage	t = 1 s (100% production), partial discharge 5 pC	1062	V <sub>peak</sub>
V <sub>IOTM</sub>	Transient overvoltage	t = 60 s (qualification)	4242	V <sub>peak</sub>
		t = 1 s (100% production)		
V <sub>ISO</sub>	Isolation voltage per UL	t = 60 s (qualification)	2500	V <sub>rms</sub>
		t = 1 s (100% production)	3000	
R <sub>S</sub>	Insulation resistance	V <sub>IO</sub> = 500 V at T <sub>S</sub>	>10 <sup>9</sup>	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

(2) For applications that require DC working voltages between GND1 and GND2, contact Texas Instruments for further details.

**Table 2. IEC 60664-1 RATINGS TABLE**

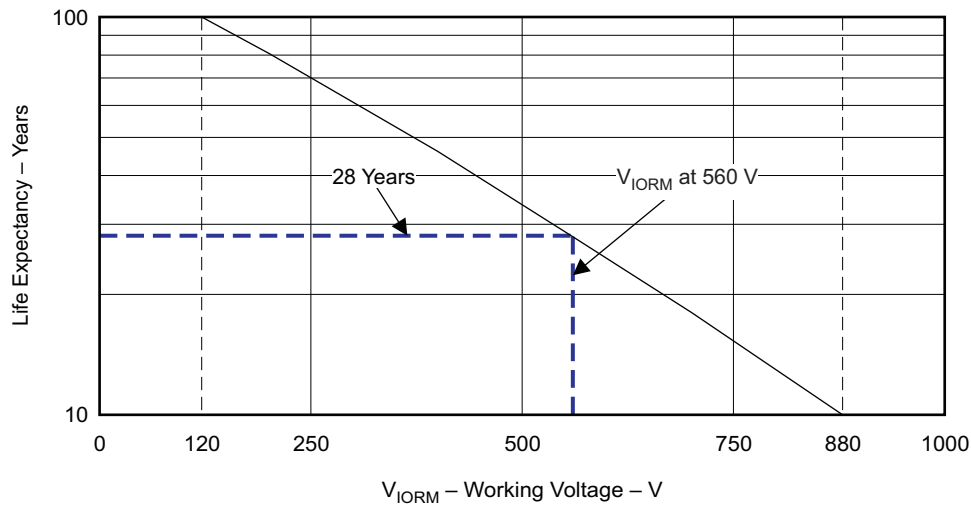
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage $\leq 150$ Vrms	I–IV
	Rated mains voltage $\leq 300$ Vrms	I–III
	Rated mains voltage $\leq 400$ Vrms	I–II

**REGULATORY INFORMATION**

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice #5A	Recognized under UL1577 Component Recognition Program <sup>(1)</sup>
Basic Insulation Maximum Transient Overvoltage, 4242 V <sub>PK</sub> Maximum Surge Voltage, 4000 V <sub>PK</sub> Maximum Working Voltage, 566 V <sub>I-PK</sub>	Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 390 VRMS maximum working voltage	Single Protection, 2500 V <sub>RMS</sub>
File number: 40016131	File number: 220991	File number: E181974

(1) Production tested  $\geq 3000$  Vrms for 1 second in accordance with UL 1577.

**LIFE EXPECTANCY vs WORKING VOLTAGE**



G001

**Figure 4. Life Expectancy vs Working Voltage**

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	$\theta_{JA} = 212^{\circ}\text{C}/\text{W}$ , $V_I = 5.25\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			112	mA
		$\theta_{JA} = 212^{\circ}\text{C}/\text{W}$ , $V_I = 3.45\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			171	
T <sub>S</sub>	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leadless Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction-to-air thermal resistance	Low-K thermal resistance <sup>(1)</sup>		212		°C/W
		High-K thermal resistance <sup>(1)</sup>		122		
$\theta_{JB}$	Junction-to-board thermal resistance			37		°C/W
$\theta_{JC}$	Junction-to-case thermal resistance			69.1		°C/W
$P_D$	Device power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , $C_L = 15\text{ pF}$ , Input a 150-Mbps 50% duty-cycle square wave			390	mW

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages

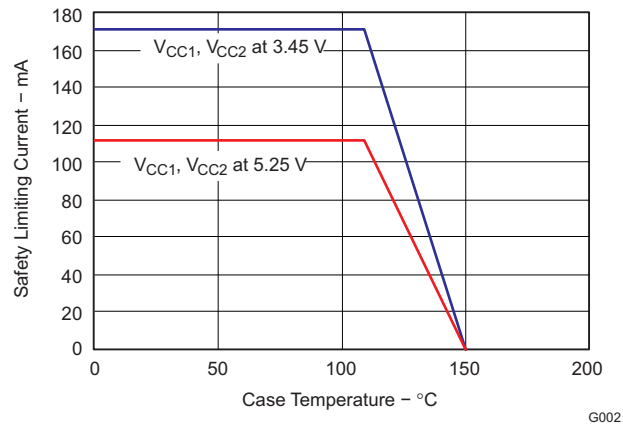


Figure 5.  $\theta_{JC}$  Thermal Derating Curve per IEC 60747-5-2

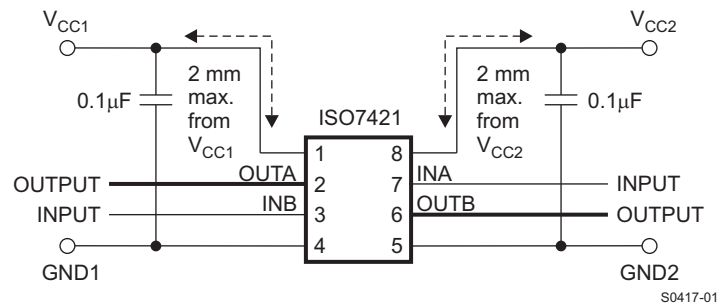


Figure 6. Typical ISO7421 Application Circuit

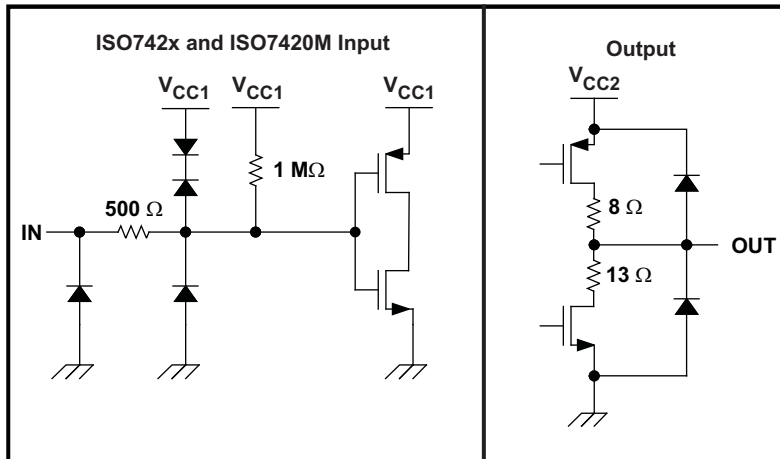


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

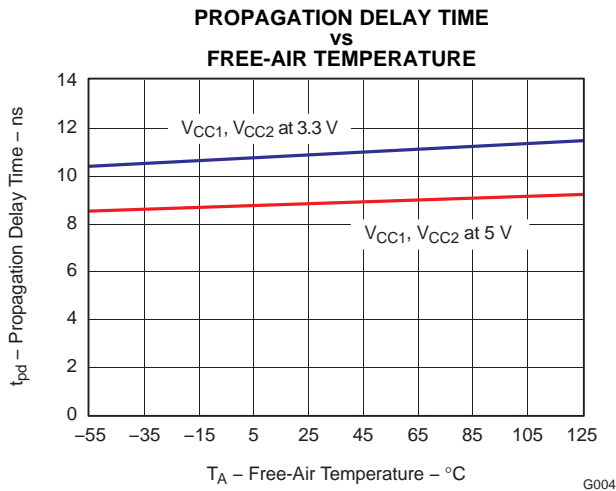


Figure 8.

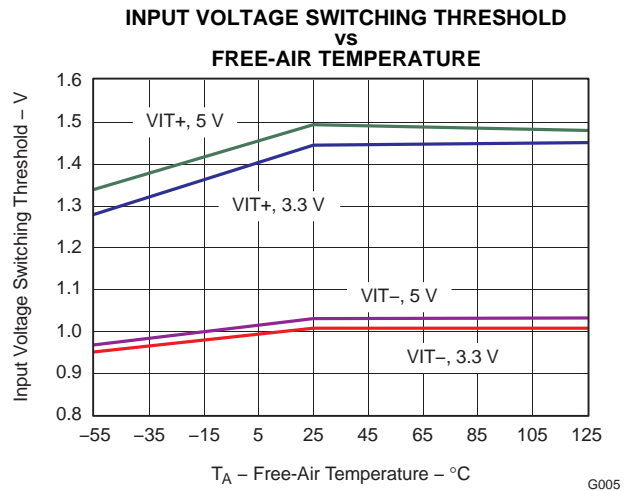


Figure 9.

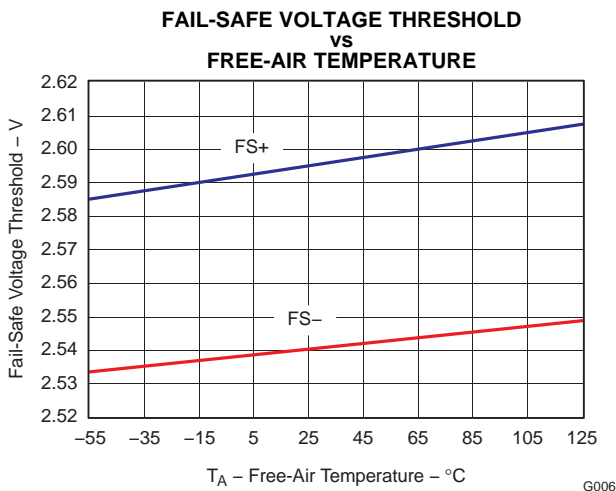


Figure 10.

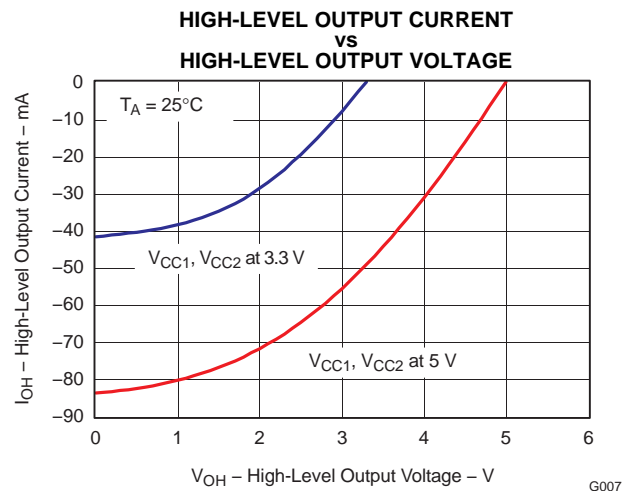


Figure 11.

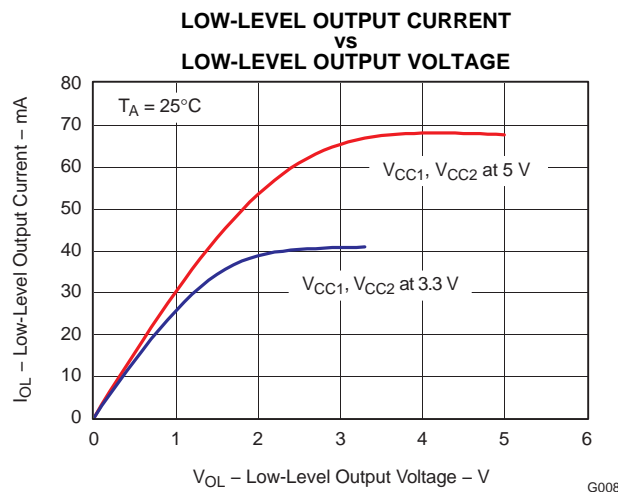


Figure 12.

## REVISION HISTORY

<b>Changes from Original (June 2009) to Revision A</b>	<b>Page</b>																																																																						
• Added devices ISO7420 and ISO7420M to the data sheet .....	1																																																																						
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• Changed <a href="#">Figure 2</a> .....	8
• Added input to output and note 1 to Isolation resistance, input to output .....	9
• Changed the Isolation resistance test conditions .....	9
• Changed the Isolation resistance test conditions .....	9
• Added note 1 to Barrier capacitance, input to output .....	9
• Added Input capacitance .....	9
• Changed $T_J = 170^\circ\text{C}$ to $T_J = 150^\circ\text{C}$ .....	11
• Changed From: 124mA To: 107mA .....	11
• Changed $T_J = 170^\circ\text{C}$ to $T_J = 150^\circ\text{C}$ .....	11
• Changed From: 190mA To: 164mA .....	11
• Changed <a href="#">Figure 5</a> .....	12
• Changed <a href="#">Figure 7</a> .....	13

**Changes from Revision C (March 2010) to Revision D**

**Page**

• Deleted devices ISO7420F and ISO7420FM from the data sheet .....	1
• Updated the Features List .....	1
• Updated the device Description. Add paragraph - Note: The ISO7420 and ISO7421 .....	1
• Changed the Function Table Output values for PU (Open) From: H/L To: H .....	2
• Changed ISO7420M $T_A$ temp From: -55 to 125 To: 40 to 125 in the Available Options Table .....	2
• Added Tstg to the Absolute Maximum Ratings Table .....	3
• Updated the Recommended Operating Conditions Table .....	3
• Updates throughout the Electrical Characteristics and Switching Characteristics tables .....	4
• Updated the Supply Current test conditions .....	4
• Changed <a href="#">Figure 2</a> .....	8
• Changed Note 1 in <a href="#">Figure 3</a> .....	8
• Changed Minimum internal gap MIN value From: 0.008 To: 0.014mm .....	9
• Changed the Barrier capacitance, input to output test conditions .....	9
• Changed the Input capacitance test conditions .....	9
• Changed the $V_{IORM}$ , $V_{PR}$ , and $V_{IOTM}$ unit values From: V To: Vpeak .....	9
• Changed $V_I$ From: 5.5V To: 5.25V .....	11
• Changed From: 107mA To: 112mA .....	11
• Changed $V_I$ From: 3.6V To: 3.45V .....	11
• Changed From: 164mA To: 171mA .....	11
• Changed <a href="#">Figure 5</a> .....	12
• Deleted the $I_{CC}$ EQUATIONS section .....	12
• Changed <a href="#">Figure 7</a> .....	13
• Deleted the SUPPLY CURRENT vs SIGNAL RATE (ALL CHANNELS) graphs and the EYE DIAGRAM plots .....	14



<b>Changes from Revision D (July 2010) to Revision E</b>	<b>Page</b>
• Added new fifth bullet to Features and deleted text from 4-kVpeak bullet item .....	1
• Changed first paragraph in Description from: ISO7420M, ISO7421, and ISO7421M to: ISO7420M and ISO7421 .....	1
• Changed Note 2 in Function Table from: ISO7420M, ISO7421, and ISO7421M to: ISO7420M and ISO7421 .....	2
• Deleted the last row in the Available Options table .....	2
• Changed ISO742xM in the ELEC CHAR and SWITCHING CHAR table to ISO7420M .....	4
• Changed the MAX value in the SWITCHING CHAR table 2nd row from 3.5 to 3.7 and 3rd row from 4 to 4.9 .....	4
• Changed ISO742xM in the ELEC CHAR and SWITCHING CHAR table to ISO7420M .....	5
• Changed the MAX value in the 2nd SWITCHING CHAR table 2nd row from 4 to 5.6 and 3rd row from 5 to 6.3 .....	5
• Changed ISO742xM in the ELEC CHAR and SWITCHING CHAR table to ISO7420M .....	6
• Changed the MAX value in the 3rd SWITCHING CHAR table 3rd row from 5 to 8.5 .....	6
• Changed ISO742xM in the ELEC CHAR and SWITCHING CHAR table to ISO7420M .....	7
• Changed the MAX value in the 4rd SWITCHING CHAR table 3rd row from 6 to 6.8 .....	7
• Changed Regulatory Information table last row, last column from: pending (E181974) to: E181974 .....	10

<b>Changes from Revision E (June 2011) to Revision F</b>	<b>Page</b>
• Changed Feature From: 242 Vpeak Maximum Isolation-per DIN EN 60747-5-2 (VDE 0884 Part 2) - To: 4~242 Vpeak Isolation .....	1
• Changed Feature From: IEC/VDE and CSA Approvals, IEC 60950-1–IEC 61010-1 End Equipment Standards Approvals, All Approvals Pending To: CSA 60950-1 and IEC 61010-1 Approved .....	1
• Changed CTI in the PACKAGE CHARACTERISTICS table, Min value From: >175 To 400 .....	9
• Changed the text of NOTE: .....	9
• Added table Note to $V_{IORM}$ .....	9
• Changed $V_{IORM}$ in the INSULATION CHARACTERISTICS table, Specification value From: 56~0 To: 56~6 .....	9
• Changed $V_{PR}$ in the Specification value From: 10~50 To: 10~62 .....	9
• Changed $V_{IOTM}$ t = 60 s (qualification) Specification value From: 4~000 To: 4~242 .....	9
• Changed the IEC 60664-1 RATINGS TABLE. Row - Basic isolation group SPECIFICATION From: III-a To: II .....	10
• Changed the REGULATORY INFORMATION table .....	10

<b>Changes from Revision F (January 2013) to Revision G</b>	<b>Page</b>
• Changed $V_{IORM}$ in the INSULATION CHARACTERISTICS table, Specification value From: 56~6 To: 566 .....	9
• Changed $V_{PR}$ in the Specification value From: 10~62 To: 1062 .....	9
• Changed $V_{IOTM}$ t = 60 s (qualification) Specification value From: 4~242 To: 4242 .....	9

<b>Changes from Revision G (May 2013) to Revision H</b>	<b>Page</b>
• Changed Feature From: 4~242 Vpeak Isolation To: 4242 Vpeak Isolation .....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ISO7420D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	IS7420	<a href="#">Samples</a>
ISO7420DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	IS7420	<a href="#">Samples</a>
ISO7420MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7420M	<a href="#">Samples</a>
ISO7420MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7420M	<a href="#">Samples</a>
ISO7421D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	IS7421	<a href="#">Samples</a>
ISO7421DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	IS7421	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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