8-Channel, Programmable T/R Switch for Ultrasound

Check for Samples: TX810

FEATURES

- **Compact T/R Switch for Ultrasound**
- **Flexible Programmability**
  - **8 Bias Current Settings**
  - **8 Power/Performance Combinations**
  - **Easy Power-Up/Down control**
- **Fast Wake Up Time**
- **Dual Supply Operation**
- **Optimized Insertion Loss**

APPLICATIONS

- **Medical Ultrasound**
- **Industrial Ultrasound**

DESCRIPTION

The TX810 provides an integrated solution for a wide range of ultrasound applications. It is an 8 channel, current programmable, transmit/receive switch in a small 6mm × 6mm package.

The internal diodes limit the output voltage when high voltage transmitter signals are applied to the input. While the insertion loss of TX810 is minimized during receive mode.

Unlike conventional T/R switches, the TX810 contains a 3-bit interface used to program bias current from 7mA to 0mA for different performance and power requirements. When the TX810 bias current is set as 0mA (i.e., high-impedance mode), the device is configured as power-down mode. In the high-impedance mode, TX810 does not add additional load to high-voltage transmitters. In addition, the device can wake up from power-down mode in less than 1µs. With these advanced programmability features, significant power saving can be achieved in systems.

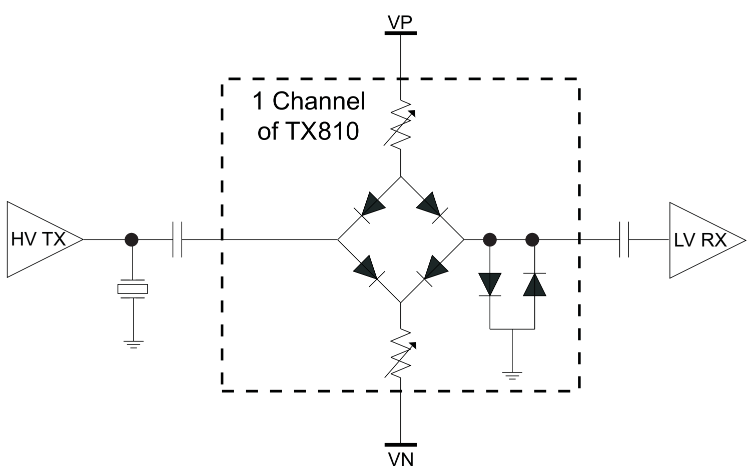


Figure 1. Block Diagram of TX810

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY	OPERATING TEMPERATURE RANGE
TX810IRHHT	S-PVQFN-N36	Tape and Reel, 250	0~70°C
TX810IRHHR		Tape and Reel, 2500	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply Voltage, VD		-0.3 ~ +6	V
Supply Voltage, VP		-0.3 ~ +6	V
Supply Voltage, VN		-6 ~ +0.3	V
Supply Voltage, VB		-0.3 ~ +6	V
Input AC voltage, INn		±100	V
Input at Vsub		-6 ~ +0.3	V
Output current, I_O		15	mA
Maximum junction temperature, continuous operation, long term reliability(2) T_J		125°C	
Storage temperature range, T_{stg}		-55°C to 150°C	
ESD ratings	HBM	500	V
	CDM	750	V
	MM	200	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

THERMAL INFORMATION

THERMAL METRIC(1) (OLFM Airflow Assumed)		TX810 RHH 36 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	29.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	27	
θ_{JB}	Junction-to-board thermal resistance (4)	7.2	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.1	
ψ_{JB}	Junction-to-board characterization parameter (6)	7.2	

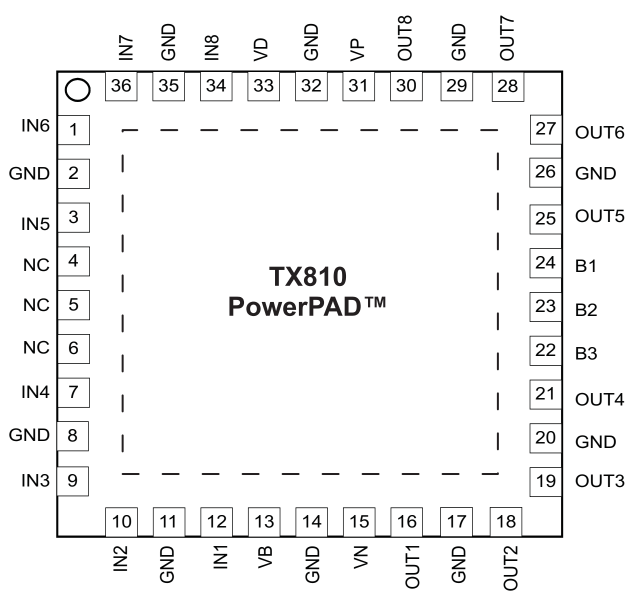
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case(top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

DEVICE INFORMATION

PIN FUNCTIONS

PIN		DESCRIPTION
NUMBER	NAME	
1, 3, 7, 9, 10, 12, 34, 36	INn	Inputs for Channel n
16, 18, 19, 21, 25, 27, 28, 30	OUTn	Outputs for Channel n
33	VD	Logic Supply Voltage; +2.5 V to +5 V; bypass to ground with 0.1 µF and 10 µF capacitors
31	VP	Positive Supply Voltage; +5 V; bypass to ground with 0.1 µF and 10 µF capacitors
15	VN	Negative Supply Voltage; –5 V; bypass to ground with 0.1 µF and 10 µF capacitors
13	VB	Bias voltage; connect to 0 V (GND) for ±5 V operation
2, 8, 11, 14, 17, 20, 26, 29, 32, 35	GND	Ground
24	B1	Bit 1; Current program bit
23	B2	Bit 2; Current program bit
22	B3	Bit 3; Current program bit
4, 5, 6	NC	No internal connection.
0	Vsub	PowerPAD™ of the package. –5 V to 0 V for ±5 V operation. The thermal pad is needed for thermal dissipation.

PQFN (RHH) Package
6 × 6mm, 0.5mm Pitch
(Top View)



ELECTRICAL CHARACTERISTICS

All Specifications at T_A = 25°C, VP = 5V, VN = -5V, VB = 0V, V_{sub}= -5V, R_{LOAD} = 400Ω; f = 5MHz, B3B2B1 = 111, V_{IN} = 0.25V_{PP}, unless otherwise noted. Test Level: A: Final tester limits; B: bench evaluation/simulation; C: Simulation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level
DC POWER SPECIFICATIONS						
Positive Supply VP			5		V	B
Negative Supply VN			-5			
Quiescent current, VP, VN	No Signal			50	µA	A
Substrate Voltage, V_{SUB}	PowerPAD™		VN	0	V	B
Digital Supply, VD		2.5	5		V	B
Quiescent current, VD	No Signal			50	µA	A
Bias current, VP, VN path	B3B2B1 = 001	1.25	1	0.75	mA/CH	A
Bias current, VP, VN path	B3B2B1 = 111	5.95	7	8.05	mA/CH	A
Leakage Current	Any output; B3B2B1 = 000; No Input			0.5	µA	A
LOGIC INPUTS						
Logic High Input Voltage; V_{IH}		2		VD	V	A
Logic High Input Current; I_{IH}				20	µA	A
Logic Low Input Voltage; V_{IL}		0		0.4	V	A
Logic Low Input Current; I_{IL} Input				20	µA	A
Capacitance, C_{IN}			5		pF	C
POWER DISSIPATION	All channels					
Power-Down Dissipation	B3B2B1 = 000; no signal			200	µW	A
Total Power Dissipation	B3B2B1 = 001; no signal		80	92	mW	A
	B3B2B1 = 111; no signal		560	644	mW	A
AC SPECIFICATIONS						
Input Amplitude, V_{IN}	1 µs positive and negative pulse applied seperately at PRF = 10 kHz	-90		90	V	A
	CW mode (continuous wave)	-10		10	V	B
Insertion loss, I_L	B3B2B1 = 111		-0.9	-1.8	dB	A
	B3B2B1 = 100		-1.1	-1.8	dB	A
	B3B2B1 = 001		-1.3	-2	dB	A
	B3B2B1 = 111, R_{LOAD} = 50Ω		-4.1		dB	B
	B3B2B1 = 001, R_{LOAD} = 50Ω		-7		dB	B
Channel to channel I_L matching	B3B2B1 = 111		0.06		dB	B
Insertion Loss, I_L	B3B2B1 = 111, at 20MHz		-0.9		dB	B
Equivalent Resistance, R_{ON}	B3B2B1 = 111, R_{LOAD} = 50 Ω		30		Ω	B
	B3B2B1 = 001, R_{LOAD} = 50 Ω		62		Ω	B
	B3B2B1 = 111		44		Ω	B
	B3B2B1 = 001		67		Ω	B
-3dB Bandwidth, BW	B3B2B1 = 111		140		MHz	B
	B3B2B1 = 100		115		MHz	B
	B3B2B1 = 001		65		MHz	B
2nd Harmonic Distortion, HD2, 5MHz	B3B2B1 = 111, V_{IN} = 0.5V_{PP} 5MHz		-74		dBc	B
	B3B2B1 = 100, V_{IN} = 0.5V_{PP} 5MHz		-74		dBc	B
	B3B2B1 = 001, V_{IN} = 0.5V_{PP} 5MHz		-73		dBc	B

ELECTRICAL CHARACTERISTICS (continued)

All Specifications at T_A = 25°C, VP = 5V, VN = -5V, VB = 0V, V_{sub}= -5V, R_{LOAD} = 400Ω; f = 5MHz, B3B2B1 = 111, V_{IN} = 0.25V_{PP}, unless otherwise noted. Test Level: A: Final tester limits; B: bench evaluation/simulation; C: Simulation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level
2nd Harmonic Distortion, HD2, 10MHz	B3B2B1 = 111, V_{IN} = 0.5 V_{PP} 10MHz		-78		dBc	B
	B3B2B1 = 100, V_{IN} = 0.5 V_{PP} 10MHz		-77		dBc	B
	B3B2B1 = 001, V_{IN} = 0.5 V_{PP} 10MHz		-74		dBc	B
Cross-talk, Xtalk	B3B2B1 = 111 at 10MHz		-70		dBc	B
	B3B2B1 = 100 at 10MHz		-69		dBc	B
	B3B2B1 = 001 at 10MHz		-61		dBc	B
3rd order Intermodulation, IMD3 (1)	B3B2B1 = 111		-68		dBc	B
	B3B2B1 = 100		-65		dBc	B
	B3B2B1 = 001		-50		dBc	B
Power Supply Modulation Ratio, PSMR (2)	B3B2B1 = 111		-76		dBc	B
	B3B2B1 = 100		-76		dBc	B
	B3B2B1 = 001		-76		dBc	B
Power Supply Rejection Ratio, PSRR	B3B2B1 = 111, 1KHz and 1MHz		-64		dBc	B
Input Referred Noise, IRN	B3B2B1 = 111		0.91		nV/rtHz	B
	B3B2B1 = 100		1.05		nV/rtHz	B
	B3B2B1 = 001		1.12		nV/rtHz	B
Recovery Time 140 V_{PP} IN, V_{OUT} < 20mV_{PP}	B3B2B1 = 111		1		µs	B
	B3B2B1 = 100		0.5		µs	B
	B3B2B1 = 001		0.3		µs	B
Turn-on Delay Time (3), t_{EN_ON}	B3B2B1 = 000→111		0.6		µs	B
	B3B2B1 = 000→100		0.5		µs	B
	B3B2B1 = 000→001		0.5		µs	B
Turn-off Delay Time (3), t_{EN_OFF}	B3B2B1 = 111→000		2.4		µs	B
	B3B2B1 = 100→000		2.7		µs	B
	B3B2B1 = 001→000		2.2		µs	B
Bias Current Switching Time	B3B2B1 = 001→111		0.7		µs	B
Propagation Delay Time (3), t_{DELAY}	B3B2B1 = 111		1.3		ns	B
	B3B2B1 = 100		1.6		ns	B
	B3B2B1 = 001		1.7		ns	B
Clamp Voltage, excludes overshoot	B3B2B1 = 111		1.9		V_{PP}	B
	B3B2B1 = 001		1.7		V_{PP}	B
	B3B2B1 = 000		1.4		V_{PP}	B

(1) 5MHz 1V_{PP}, and 5.01MHz 0.5V_{PP} input.
(2) PSMR is defined as the ratio between carrier 5MHz and side band signals with 1KHz and 1MHz 50mV_{PP} Noise applied on supply pins.
(3) See the timing diagram show in Figure 2.

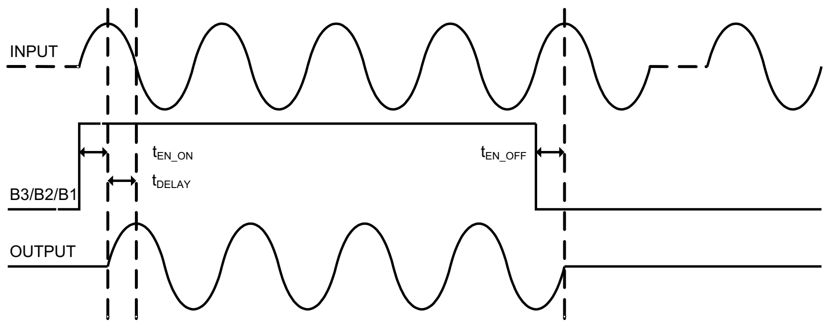


Figure 2. Timing Diagram

TYPICAL CHARACTERISTICS

All Specifications at T_A = 25°C, VP = 5V, VN = -5V, VB = 0V, V_{SUB} = -5V, R_{IN} = 75Ω, R_{LOAD} = 400Ω; f = 5MHz, B3B2B1=111, V_{IN} = 0.25V_{PP}, unless otherwise noted.

A typical bench setup is shown in Figure 3.

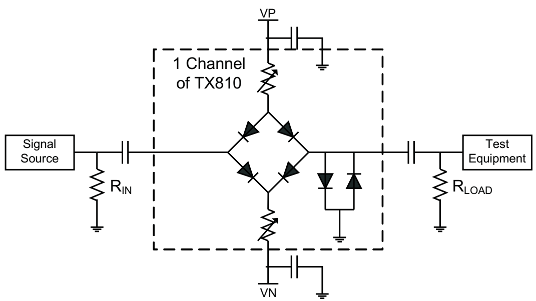


Figure 3. Typical Test Setup

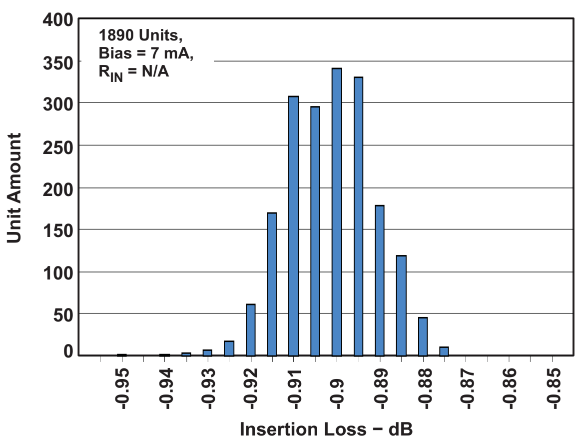
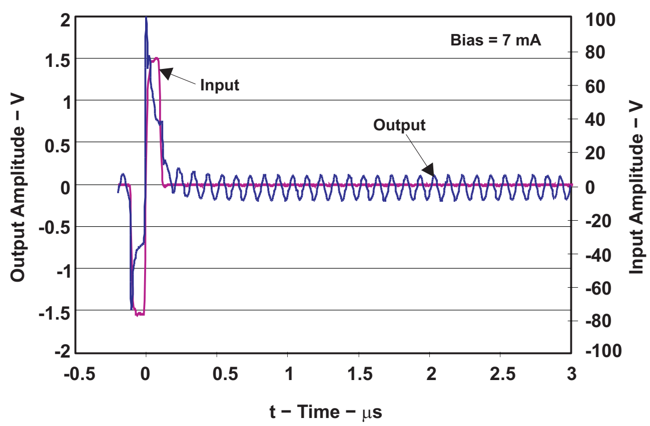


Figure 4. Insertion Loss Distribution

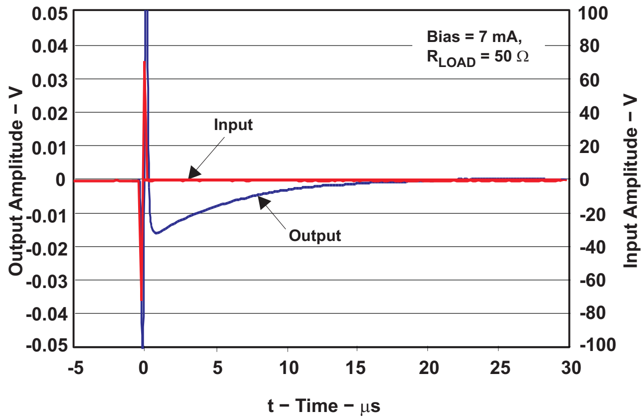


AC coupling is used between High voltage pulser and TX810. The input signal is a combination of 0.25Vpp signal followed by a 1-cycle 140Vpp pulse

Figure 5. Recovery Time With Small Input Signal

TYPICAL CHARACTERISTICS (continued)

All Specifications at T_A = 25°C, VP = 5V, VN = -5V, VB = 0V, V_{SUB} = -5V, R_{IN} = 75Ω, R_{LOAD} = 400Ω; f = 5MHz, B3B2B1=111, V_{IN} = 0.25V_{PP}, unless otherwise noted.



AC coupling is used between High voltage pulser and TX810. The input signal is a 1-cycle 140Vpp pulse

Figure 6. Recovery Time Without Signal

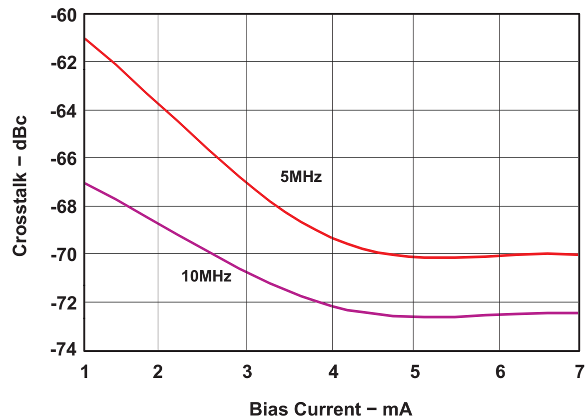


Figure 7. Cross-talk vs. Bias Currents vs. Frequency

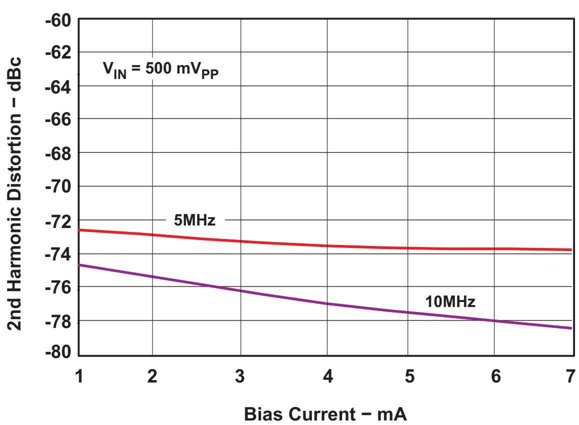


Figure 8. HD2 vs. Bias Current vs. Frequency

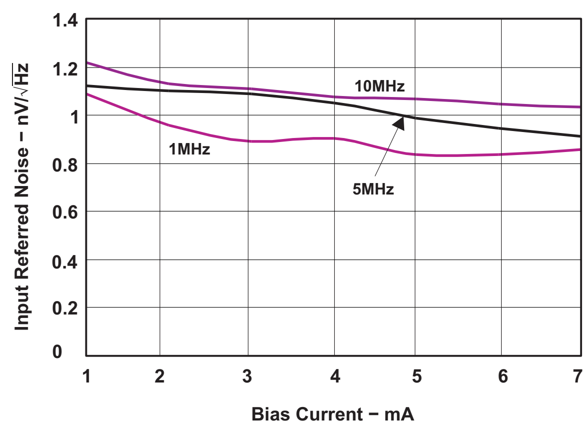


Figure 9. Input Referred Noise vs. Bias Current vs. Frequency

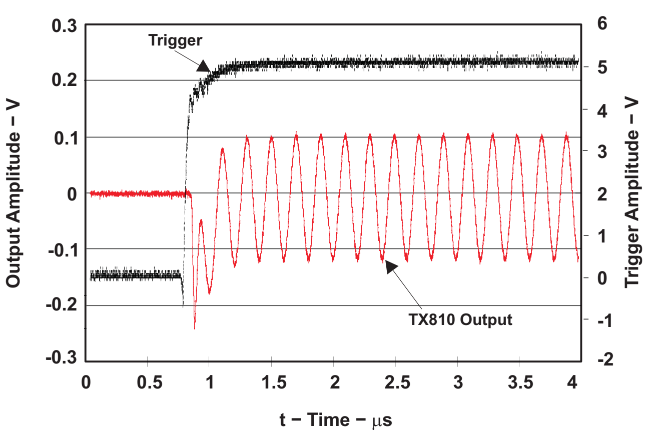


Figure 10. Power On Response Time (0mA to 7mA)

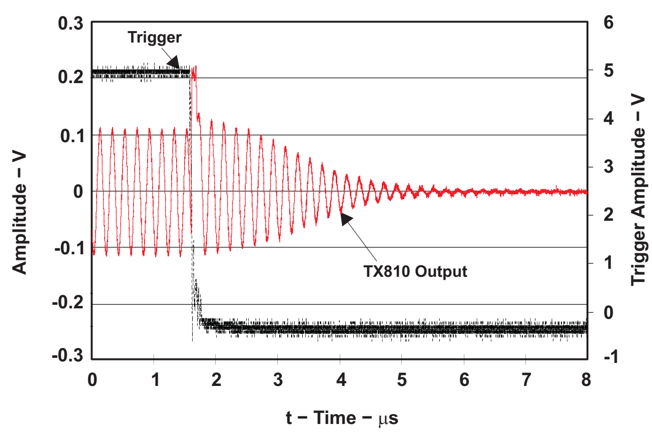


Figure 11. Power Down Response Time (7mA to 0mA)

TYPICAL CHARACTERISTICS (continued)

All Specifications at T_A = 25°C, VP = 5V, VN = -5V, VB = 0V, V_{SUB} = -5V, R_{IN} = 75Ω, R_{LOAD} = 400Ω; f = 5MHz, B3B2B1=111, V_{IN} = 0.25V_{PP}, unless otherwise noted.

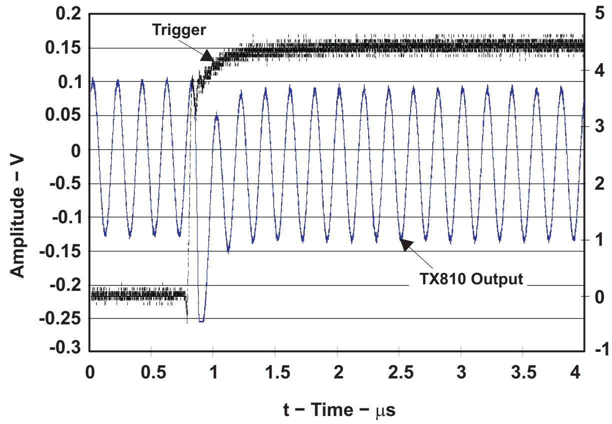


Figure 12. Bias Current Adjustment Response Time (1mA to 7mA)

THEORY OF OPERATION

A typical ultrasound block diagram is shown in Figure 13.

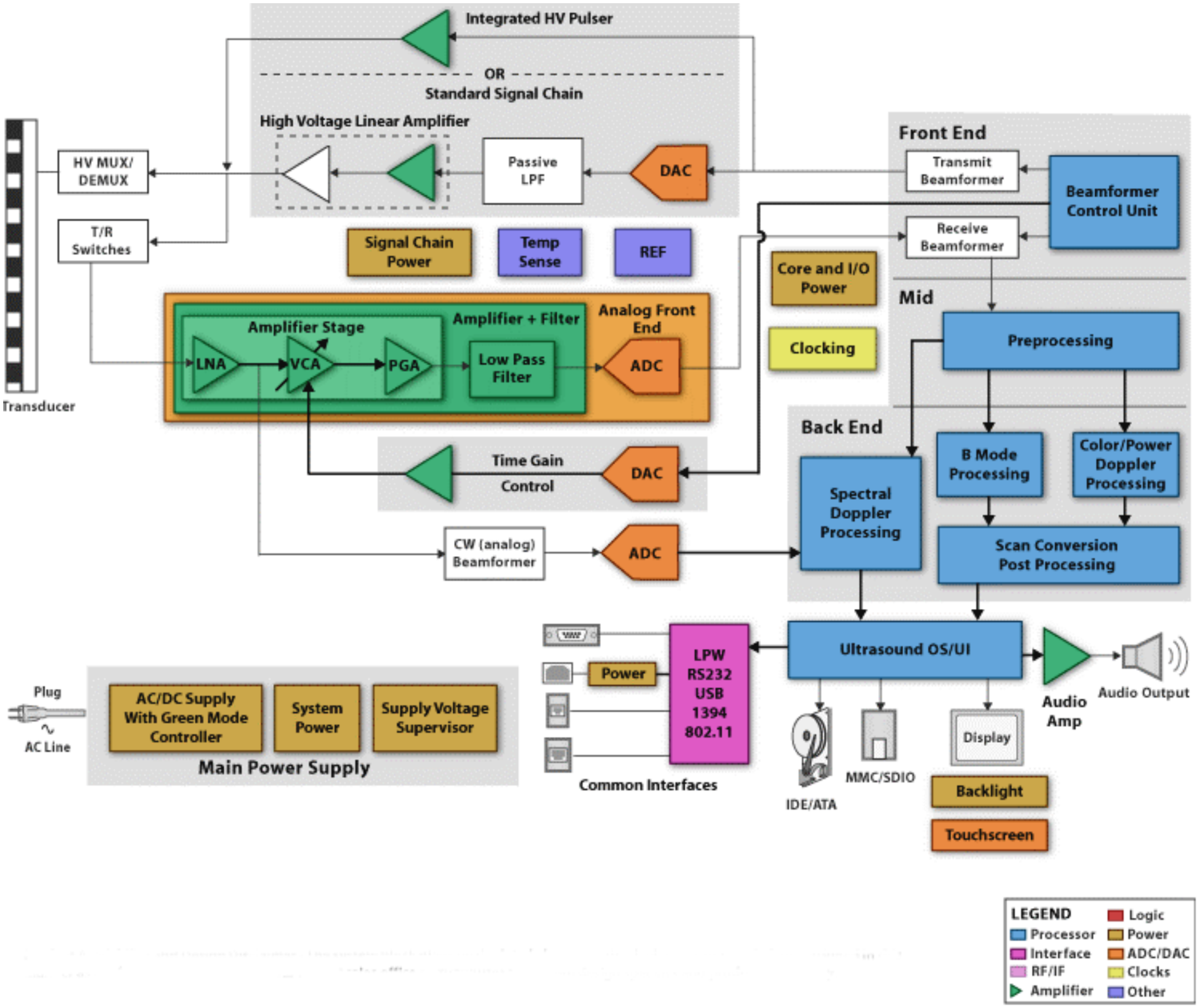


Figure 13. Ultrasound System Block Diagram

A transducer is excited by high voltage pulsers. It converts the electrical energy to mechanical energy. After each excitation, the transducer sends out ultrasonic wave to medium. Partial ultrasonic wave gets reflected by inhomogeneous medium and received by the transducer again, i.e. echo signal. Thus, the transducer is a duplex device on which both high voltage and low voltage signals exist. The transducer can not be connected to amplifier stages directly; otherwise, the high voltage signal can permanently destroy amplifiers. The TX810, i.e. T/R switches, is sitting between integrated HV pulser and low noise amplifier (LNA). The main function of TX810 is to isolate the LNA from high-voltage transmitter. TX810 limits the high voltage pulse and let echo signals reaching amplifier. Therefore, an ideal T/R switch should completely block high voltage signals and maintain all information from echoes.

The detail architecture of the TX810 is listed in Figure 14.

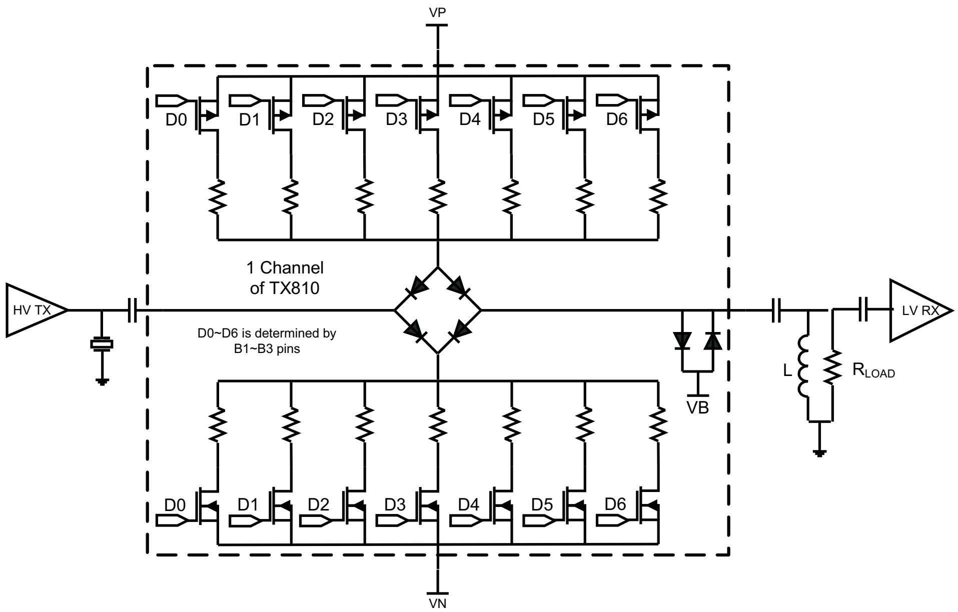


Figure 14. TX810 Block Diagram

TX810 includes four parts: Diode Bridge, bias network, clamp diodes, and logic controller. A decoder is used to convert 3-bit logic (B1 to B3) input to 7 control signals (D0 to D6) for 7 MOSFET switches. +2.5V to +5V logic input is level shifted internally to drive the switches. The bias current of the bridge diode is adjusted proportionally by these switches. When all switches are on, the bias current is 7mA. Each bit difference will adjust the bias current approximately 1mA. When all switches are off, the TX810 enters the power down mode. Comparing to discrete T/R switches, TX810 can be shut down and turned on quickly as shown in the typical characteristics plots. Considering the low duty cycle of ultrasound imaging, significant power saving can be achieved.

All 6 diodes are high-voltage Schottky diodes to achieve fast recovery time. Following the bridge, a pair of back-to-back diode limits the output voltage of TX810 to about 2Vpp. Different power/performance combination can be selected by users. The TX810 is specified to operate at ±5V and VB is biased at 0V. The characteristics of the T/R switch are mainly determined by bias currents. Lower power can be achieved with lower supply voltages. Also, Table 1 shows the relationship among bias current, insertion loss, input noise, power consumption and equivalent resistance.

Table 1. Bias current vs Performance

Test Conditions: VP = 5V, VN = -5V; VB = 0V; R_{LOAD} = 50Ω							
B3	**B2**	**B1**	**I (mA)**	**I_L (dB)**	**IRN (nV/rtHz)**	**R_{ON} (Ω)**	**Power (mW/CH)**
0	0	0	0	N/A	N/A	High Impedance	0
0	0	1	1	-7	1.12	62	10
0	1	0	2	-5.6	1.10	45	20
0	1	1	3	-5	1.09	39	30
1	0	0	4	-4.6	1.05	35	40
1	0	1	5	-4.4	0.99	33	50
1	1	0	6	-4.2	0.95	31	60
1	1	1	7	-4.1	0.91	30	70

APPLICATION INFORMATION

Similar to discrete T/R switch solutions, external components can be used to optimize system performance. Inductor L and resistor R_{LOAD} before the low voltage receiver amplifier (LVRx) can improve overload recovery time and reduce reflection. The L acts as a high pass filter thus overshoot or recovery response spikes can be suppressed to minimal. The L and R_{LOAD} terminate the entire signal path and can reduce reflection; therefore axial resolution in ultrasound image might be improved. However, the combined impedance of L and R_{LOAD} may affect the system sensitivity. The insertion loss of T/R switch is determined by the input impedance of receiver amplifier and R_{ON} of the TX810. L also creates a DC path for any offset caused by mismatching.The inductor can be as low as 10s µH to suppress low frequency signals from transmitter, transducer, multiplexer, and TX810. The optimization of L and R_{LOAD} is always an important topic for system designers. AC coupling are typically used between transmitter and T/R switch or T/R switch and amplifier. Thus amplifiers with DC biased inputs will not interference with T/R switch.

One challenge for integrating multiple channel circuits on a small package is how to reduce cross talk. In ultrasound systems, acoustic cross talk from adjacent transducer elements is a dominant source. The cross talk from transducer elements is in a range of -30 to -35dBc for array transducers. Circuit cross talk is usually at least 20dB better than the transducer cross talk. The special considerations were implemented in both TX810 design and layout. The cross talk among TX810 channels is reduced to below -60 dBc as show in the specification table.

In ultrasound Doppler applications, modulation effect in system can influence image quality and sensitivity. Ultrasound system is a complex mixed-signal system with all kinds of digital and analog circuits. Digital signals and clock signals can contaminate analog signals on system level or on chip level. Nonlinear components, such as transistors and diodes, can modulate noise and contaminate signals. In Doppler applications, the Doppler signal frequency could range from 20Hz to >50KHz. Meanwhile, multiple system clocks are also in this range, such as frame clock, image line clock, and etc. These noise signals could enter chip through ground and power supply pins. It is important to study the power supply modulation ratio (PSMR) at chip level. Noise signal with certain frequency and amplitude can be applied on supply pins. Side band signals could be found if modulation effect exists. The PSMR is expressed as an amplitude ratio between carrier and side band signals. Beside PSMR, 3rd order intermodulation ratio (IMD3) is a standard specification for mixed-signal ICs. Users can use IMD3 to estimate the potential artifact Doppler mirror signals. Both specs can be found in the specification table.

The schematic of the basic connection for TX810 is shown in Figure 15. Optional inductors and resistors can be used at TX810 outputs depending on transducer characteristics as discussed above. Standard decoupling capacitors 0.1µF should be placed close to power supply pins. The pin out of TX810 is optimized for PCB layout. All signals are going from left to right straightly.

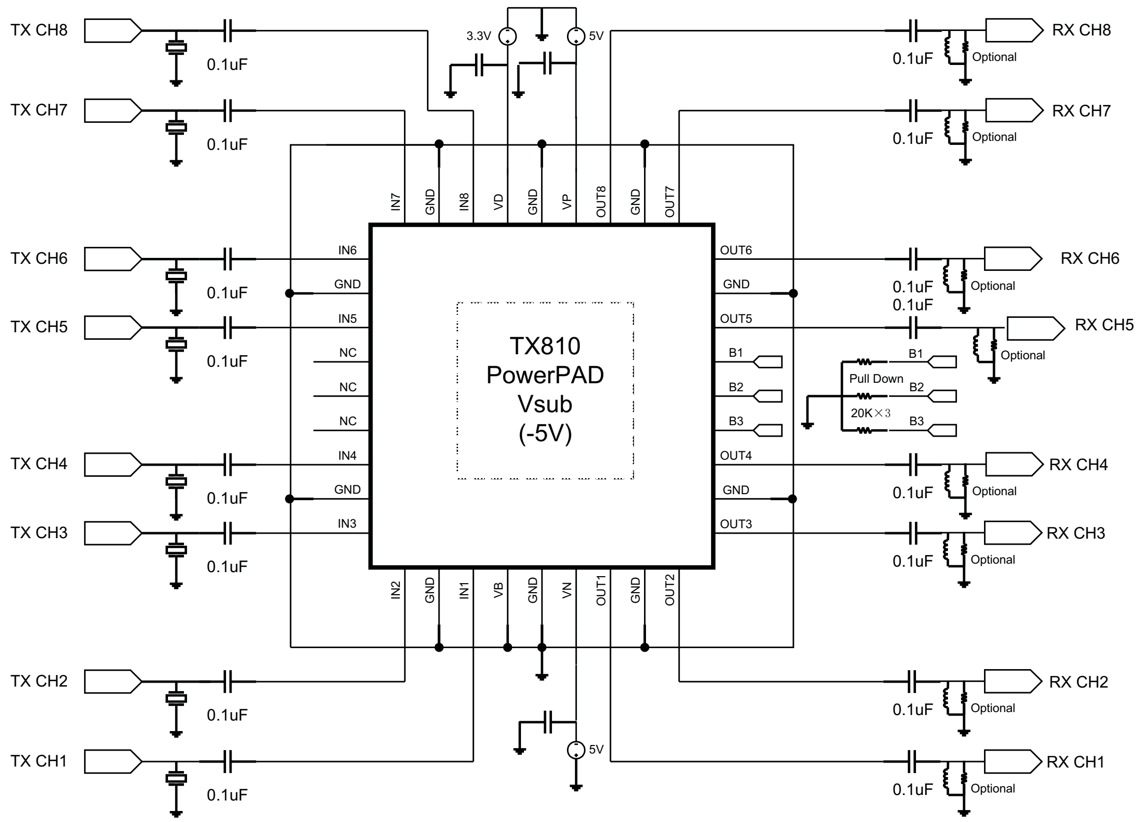


Figure 15. Schematic of TX810

REVISION HISTORY

Changes from Original (September 2009) to Revision A	**Page**
• Changed From: Product Preview To: Production. The Product Preview was a two page data sheet containing the front page and the pin out section	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TX810IRHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TX810IRHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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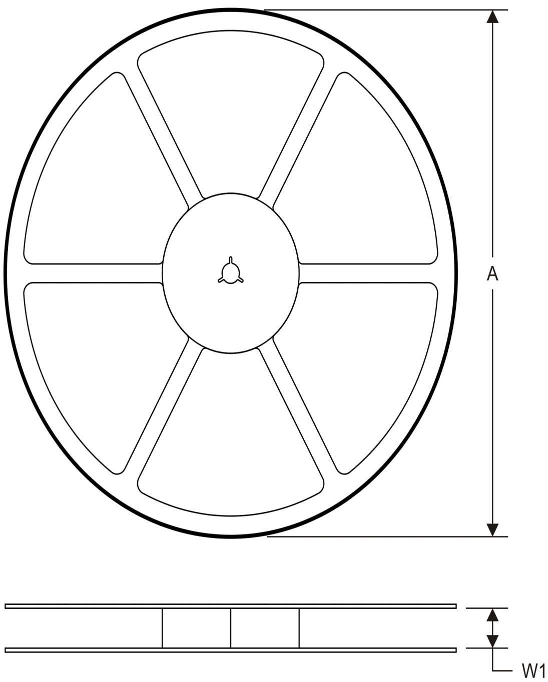
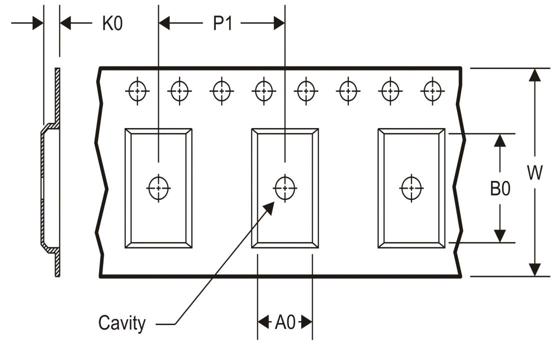
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



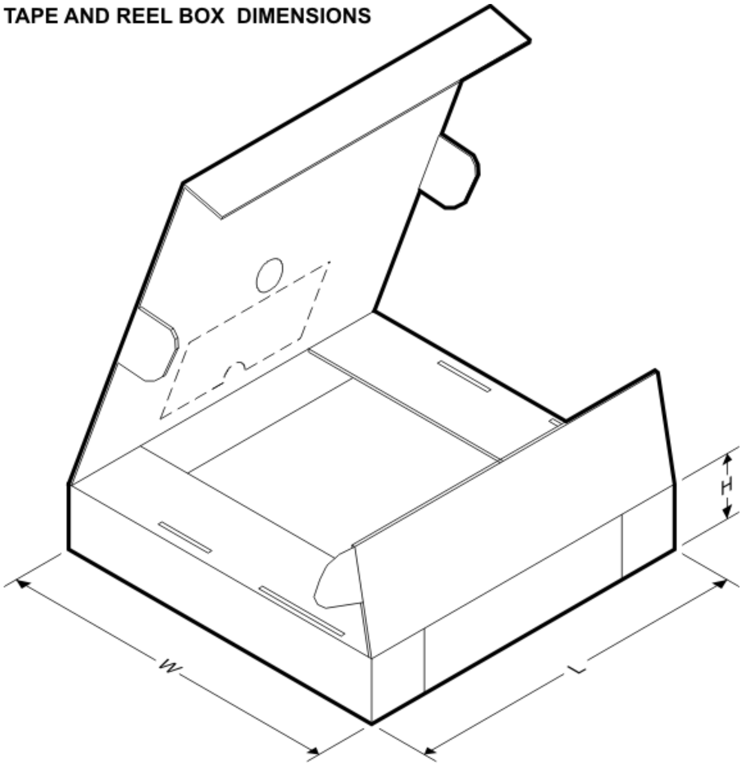
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TX810IRHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TX810IRHHT	VQFN	RHH	36	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

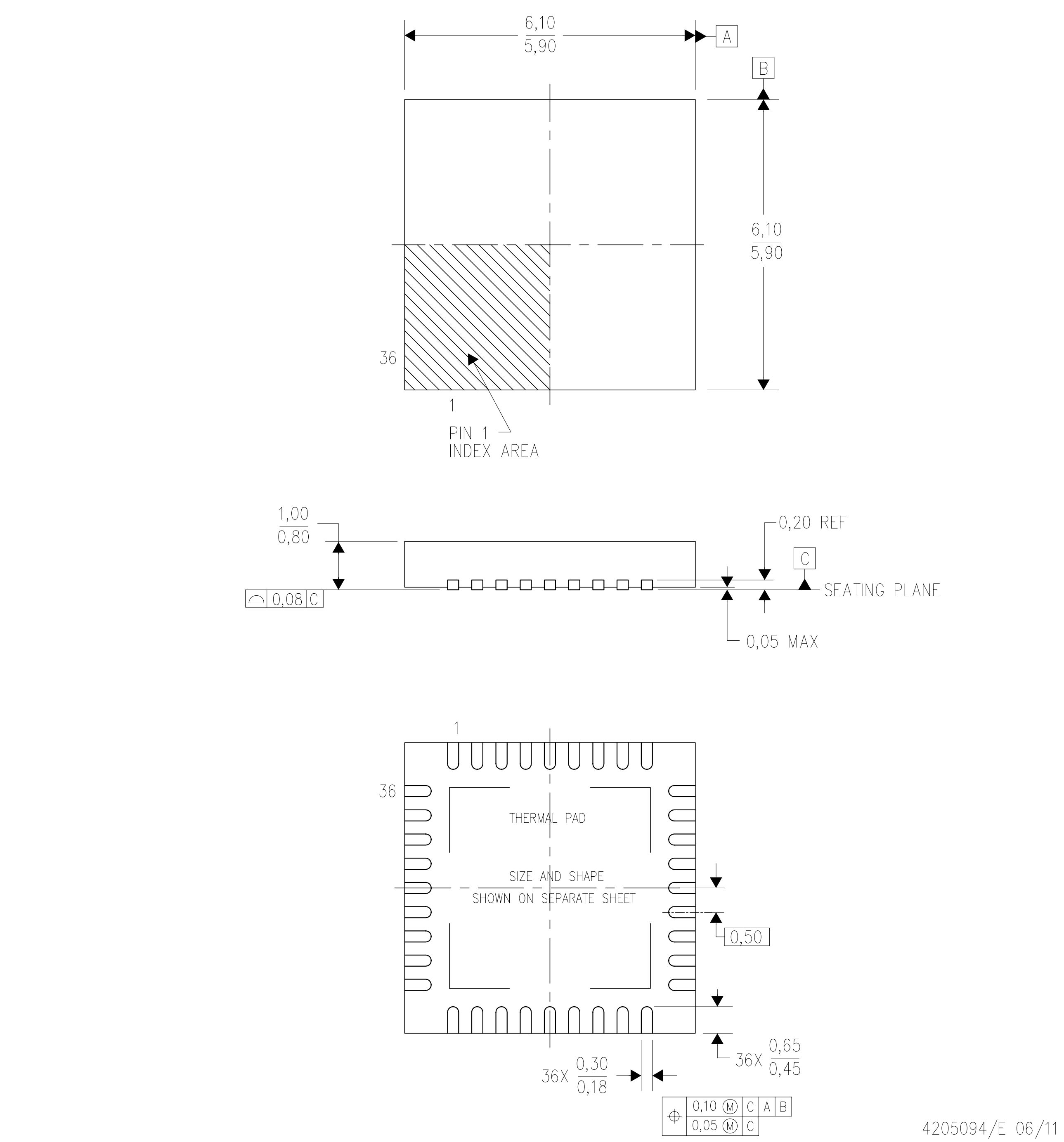
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TX810IRHHR	VQFN	RHH	36	2500	336.6	336.6	28.6
TX810IRHHT	VQFN	RHH	36	250	336.6	336.6	28.6

RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

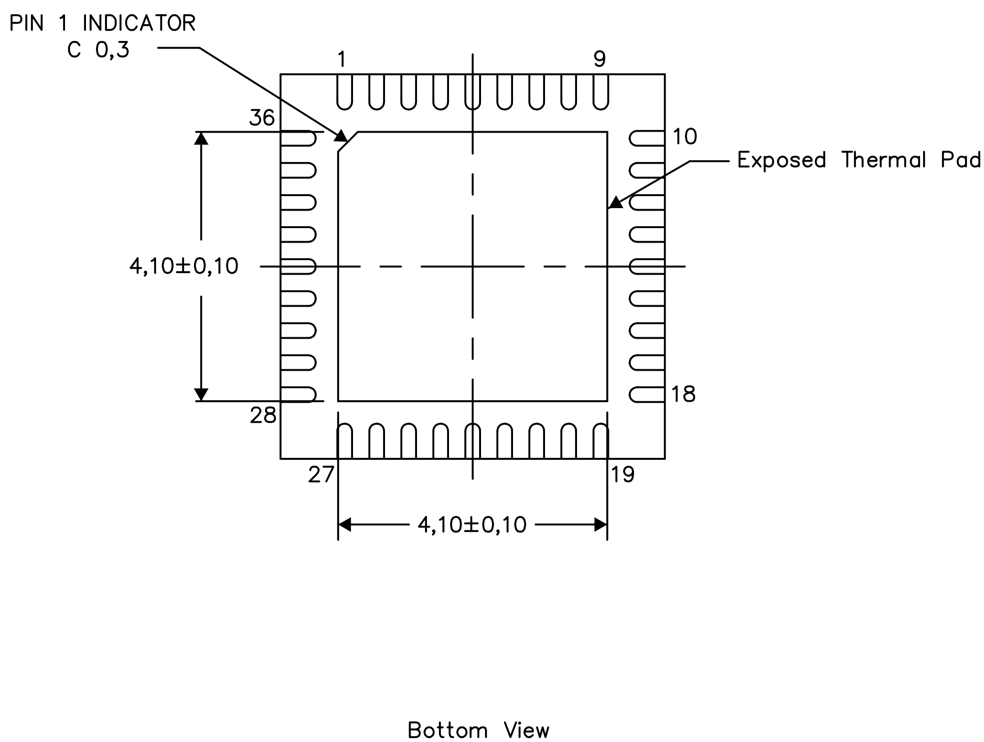
RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

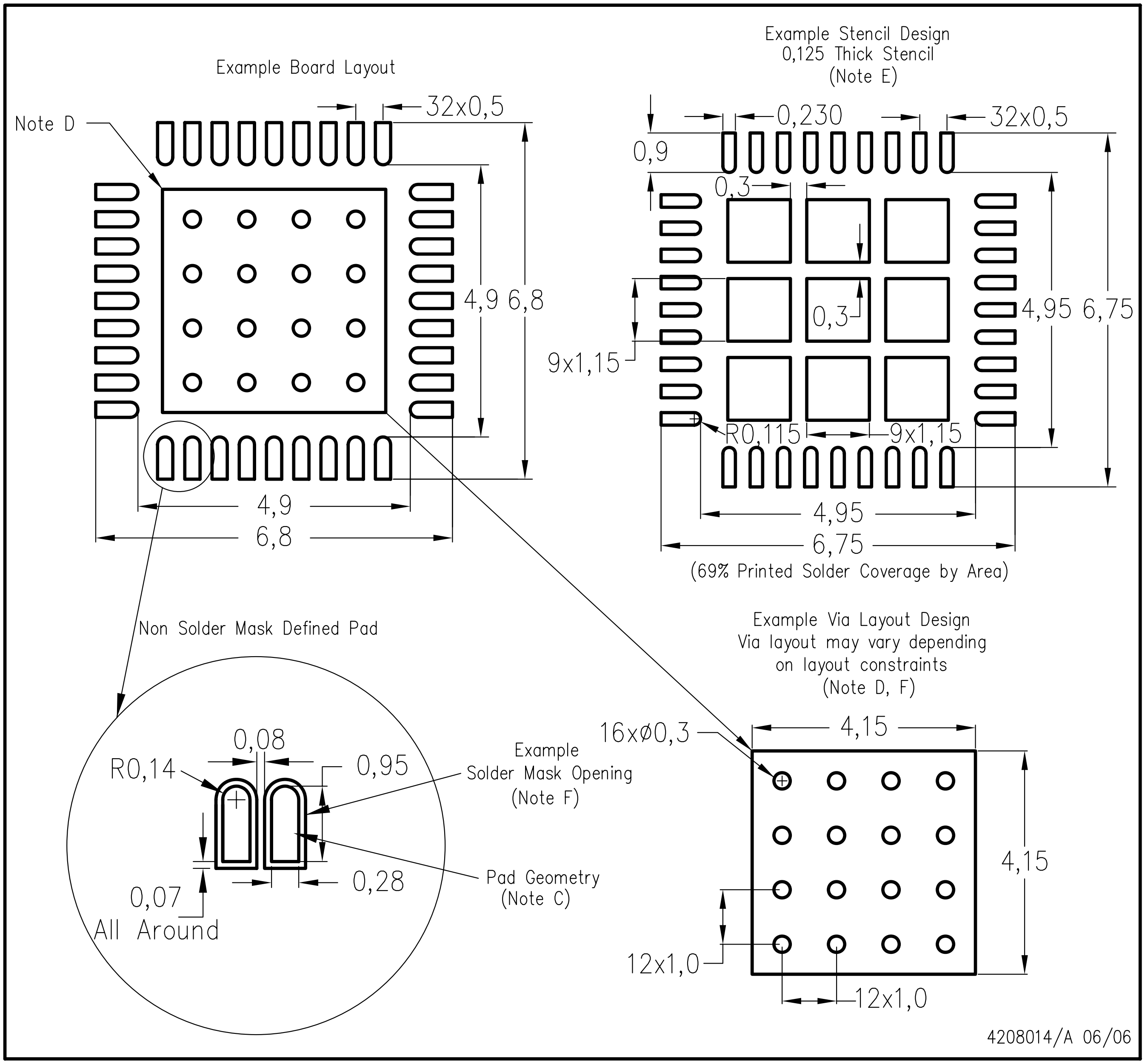


Exposed Thermal Pad Dimensions

4206362-3/K 09/12

NOTE: All linear dimensions are in millimeters

RHH (S-PQFP-N36)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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