

3.3V-Supply RS-485 with IEC ESD Protection

Check for Samples: [SN65HVD72](#), [SN65HVD75](#), [SN65HVD78](#)

FEATURES

- **Small-size MSOP Packages Save Board Space, or SOIC for Drop-in Compatibility**
- **Bus I/O Protection**
 - > ±15kV HBM protection
 - > ±12kV IEC61000-4-2 Contact Discharge
 - > ±12kV IEC61000-4-2 Air-Gap Discharge
- **Extended Industrial Temperature Range –40°C to 125°C**
- **Large Receiver Hysteresis (80 mV) for Noise Rejection**
- **Low Unit-loading allows over 200 connected nodes**
- **Low Power Consumption**
 - **Low Standby Supply Current: < 2 µA**
 - **I_{CC} <1 mA Quiescent During Operation**
- **5V-Tolerant Logic Inputs Compatible With 3.3 V or 5 V Controllers**
- **Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps**

APPLICATIONS

- **Factory Automation**
- **Telecomm Infrastructure**
- **Motion Control**

DESCRIPTION

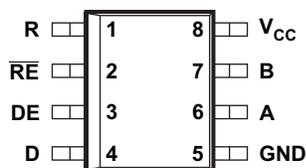
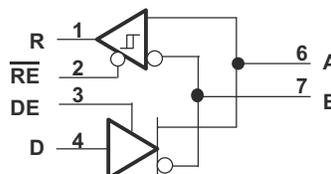
These devices have robust 3.3V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model and IEC Contact Discharge specifications.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These devices all feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from -40°C to 125°C.

Table 1. Product Selection Guide

| Part Number | Signaling Rate | Cable Length | Duplex | Enables | Package | Nodes |
|-------------|----------------|--------------|--------|---------|---------------------------|-------|
| SN65HVD72 | up to 250 kbps | up to 2000 m | Half | DE, RE | MSOP-8 SOIC-8 SON-8 | 256 |
| SN65HVD75 | up to 20 Mbps | up to 100 m | Half | DE, RE | MSOP-8 SOIC-8 SON-8 | 256 |
| SN65HVD78 | up to 50 Mbps | up to 50 m | Half | DE, RE | MSOP-8 SOIC-8 SON-8 | 96 |

SN65HVD72, 75, 78


Logic Diagram (Positive Logic)


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 2. DRIVER FUNCTION TABLE

| INPUT | ENABLE | OUTPUTS | | |
|-------|--------|---------|---|------------------------------------|
| | | A | B | |
| D | DE | | | |
| H | H | H | L | Actively drive bus High |
| L | H | L | H | Actively drive bus Low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drive bus High by default |

Table 3. RECEIVER FUNCTION TABLE

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | |
|------------------------------|--------|--------|------------------------------|
| $V_{ID} = V_A - V_B$ | RE | R | |
| $V_{IT+} < V_{ID}$ | L | H | Receive valid bus High |
| $V_{IT-} < V_{ID} < V_{IT+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{IT-}$ | L | L | Receive valid bus Low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | fail-safe high output |
| Idle (terminated) bus | L | H | fail-safe high output |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | VALUE | | UNIT |
|--|---|-----------|--------------|
| | MIN | MAX | |
| Supply Voltage, V_{CC} | -0.5 | 5.5 | V |
| Voltage range at A or B Inputs | -13 | 16.5 | V |
| Input voltage range at any logic pin | -0.3 | 5.7 | V |
| Voltage input range, transient pulse, A and B, through 100 Ω | -100 | 100 | V |
| Receiver Output Current | -24 | 24 | mA |
| Junction Temperature, T_J | | 170 | $^{\circ}$ C |
| Storage Temperature, | -65 | 150 | $^{\circ}$ C |
| Continuous total power dissipation | See the Thermal Characteristics table | | |
| IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND | | ± 12 | kV |
| IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND | | ± 12 | kV |
| IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND | | ± 4 | kV |
| IEC 60749-26 ESD (Human Body Model), bus terminals and GND | | ± 15 | kV |
| JEDEC Standard 22, Test Method A114 (Human Body Model), all pins | | ± 8 | kV |
| JEDEC Standard 22, Test Method C101 (Charged Device Model), all pins | | ± 1.5 | kV |
| JEDEC Standard 22, Test Method A115 (Machine Model), all pins | | ± 300 | V |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|----------------------|--|-------|-----|----------|--------------|
| V_{CC} | Supply voltage | 3 | 3.3 | 3.6 | V |
| V_I | Input voltage at any bus terminal (separately or common mode) ⁽¹⁾ | -7 | | 12 | V |
| V_{IH} | High-level input voltage (Driver, driver enable, and receiver enable inputs) | 2 | | V_{CC} | V |
| V_{IL} | Low-level input voltage (Driver, driver enable, and receiver enable inputs) | 0 | | 0.8 | V |
| V_{ID} | Differential input voltage | -12 | | 12 | V |
| I_O | Output current, Driver | -60 | | 60 | mA |
| I_O | Output current, Receiver | -8 | | 8 | mA |
| R_L | Differential load resistance | 54 | 60 | | Ω |
| C_L | Differential load capacitance | | 50 | | pF |
| $1/t_{UI}$ | Signaling rate | HVD72 | | 250 | kbps |
| | | HVD75 | | 20 | Mbps |
| | | HVD78 | | 50 | Mbps |
| T_A ⁽²⁾ | Operating free-air temperature (See the application section for thermal information) | -40 | | 125 | $^{\circ}$ C |
| T_J | Junction Temperature | -40 | | 150 | $^{\circ}$ C |

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
 (2) Operation is specified for internal (junction) temperatures up to 150 $^{\circ}$ C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170 $^{\circ}$ C.

ELECTRICAL CHARACTERISTICS

over recommended operating range (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | | |
|--------------------------|---|--|--------------------------------------|---|----------------------|--------------------|------|----|----|
| V _{OD} | Driver differential output voltage magnitude | R _L = 60 Ω, 375 Ω on each output to -7 V to 12 V | See Figure 1 | 1.5 | 2 | | V | | |
| | | R _L = 54 Ω (RS-485) | | 1.5 | 2 | | V | | |
| | | R _L = 100 Ω (RS-422) T _J ≥ 0°C, V _{CC} ≥ 3.2V | | 2 | 2.5 | | V | | |
| Δ V _{OD} | Change in magnitude of driver differential output voltage | R _L = 54 Ω, C _L = 50 pF | See Figure 2 | -50 | 0 | 50 | mV | | |
| V _{OC(SS)} | Steady-state common-mode output voltage | Center of two 27-Ω load resistors | | 1 | V _{CC} /2 | 3 | V | | |
| ΔV _{OC} | Change in differential driver output common-mode voltage | | | -50 | 0 | 50 | mV | | |
| V _{OC(PP)} | Peak-to-peak driver common-mode output voltage | | | | 200 | | mV | | |
| C _{OD} | Differential output capacitance | | | 15 | | pF | | | |
| V _{IT+} | Positive-going receiver differential input voltage threshold | | | See ⁽¹⁾ | -70 | -20 | mV | | |
| V _{IT-} | Negative-going receiver differential input voltage threshold | | | -200 | -150 | See ⁽¹⁾ | mV | | |
| V _{HYS} | Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-}) | | | 50 | 80 | | mV | | |
| V _{OH} | Receiver high-level output voltage | I _{OH} = -8 mA | | 2.4 | V _{CC} -0.3 | | V | | |
| V _{OL} | Receiver low-level output voltage | I _{OL} = 8 mA | | | 0.2 | 0.4 | V | | |
| I _I | Driver input, driver enable, and receiver enable input current | | | -2 | | 2 | μA | | |
| I _{OZ} | Receiver output high-impedance current | V _O = 0 V or V _{CC} , \overline{RE} at V _{CC} | | -1 | | 1 | μA | | |
| I _{OS} | Driver short-circuit output current | | | -160 | | 160 | mA | | |
| I _I | Bus input current (disabled driver) | V _{CC} = 3 to 3.6 V or V _{CC} = 0 V, DE at 0 V | HVD72, 75 | V _I = 12 V | | 75 | 150 | μA | |
| | | | | V _I = -7 V | -100 | -40 | | μA | |
| | | | HVD78 | V _I = 12 V | | 240 | 333 | | μA |
| | | | | V _I = -7 V | -267 | -180 | | | μA |
| I _{CC} | Supply current (quiescent) | Driver and Receiver enabled | DE=V _{CC} , RE=GND, No load | | 750 | 950 | μA | | |
| | | | Driver enabled, receiver disabled | DE=V _{CC} , RE=V _{CC} , No load | | 300 | 500 | μA | |
| | | | Driver disabled, receiver enabled | DE=GND, RE=GND, No load | | 600 | 800 | μA | |
| | | | Driver and receiver disabled | DE=GND, D=open RE=V _{CC} , No load | | 0.1 | 2 | μA | |
| Supply current (dynamic) | | See the TYPICAL CHARACTERISTICS section | | | | | | | |

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

SWITCHING CHARACTERISTICS

250 kbps devices (HVD70, 71, 72) bit time > 4 μ s (over recommended operating conditions)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|--|--|---|-------------------|-----|-----|---------|
| DRIVER | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 3 | 0.3 | 0.7 | 1.2 | μ s |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | | 0.7 | 1 | μ s |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | | 0.2 | μ s |
| t_{PHZ}, t_{PLZ} | Driver disable time | Receiver enabled | See Figure 4 and Figure 5 | | 0.1 | 0.4 | μ s |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver disabled | | 0.5 | 1 |
| | | | | | 3 | 9 | μ s |
| RECEIVER | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 6 | | 12 | 30 | ns |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | | 75 | 100 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 3 | 15 | ns |
| t_{PLZ}, t_{PHZ} | Receiver disable time | | | | 40 | 100 | ns |
| $t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$ | Receiver enable time | Driver enabled | See Figure 7 | | 20 | 50 | ns |
| | | Driver disabled | See Figure 8 | | 3 | 8 | μ s |

SWITCHING CHARACTERISTICS

20 Mbps devices (HVD73, 74, 75) bit time > 50 ns (over recommended operating conditions)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|--|--|--|---|-------------------|-----|-----|---------|----|
| DRIVER | | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 3 | 2 | 7 | 14 | ns | |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | | 7 | 11 | 17 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | | 0 | 2 | ns |
| t_{PHZ}, t_{PLZ} | Driver disable time | Receiver enabled | See Figure 4 and Figure 5 | | 12 | 50 | ns | |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver disabled | | 10 | 20 | ns |
| | | | | | 3 | 7 | μ s | |
| RECEIVER | | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 6 | | 5 | 10 | ns | |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | | 60 | 70 | ns | |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 0 | 6 | ns | |
| t_{PLZ}, t_{PHZ} | Receiver disable time | | | | 15 | 30 | ns | |
| $t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$ | Receiver enable time | Driver enabled | See Figure 7 | | 10 | 50 | ns | |
| | | Driver disabled | See Figure 8 | | 3 | 8 | μ s | |

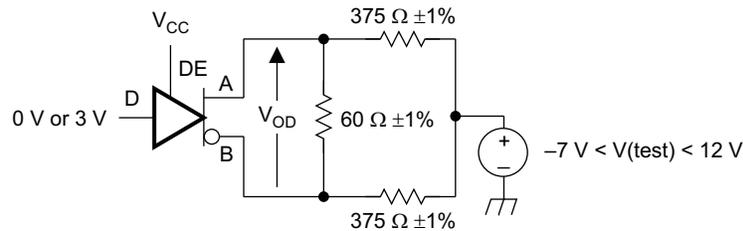
SWITCHING CHARACTERISTICS

50 Mbps devices (HVD76, 77, 78) bit time > 20 ns (over recommended operating conditions)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------|--|--|---------------------------|-------------------|-----|-----|---------------|
| DRIVER | | | | | | | |
| t_r, t_f | Driver differential output rise/fall time | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ | See Figure 3 | 1 | 3 | 6 | ns |
| t_{PHL}, t_{PLH} | Driver propagation delay | | | | 9 | 15 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | 0 | 1 | ns |
| t_{PHZ}, t_{PLZ} | Driver disable time | Receiver enabled | See Figure 4 and Figure 5 | | 10 | 30 | ns |
| t_{PZH}, t_{PZL} | Driver enable time | | | Receiver disabled | | 10 | 30 |
| | | | | | | 8 | μs |
| RECEIVER | | | | | | | |
| t_r, t_f | Receiver output rise/fall time | $C_L = 15 \text{ pF}$ | See Figure 6 | 1 | 3 | 6 | ns |
| t_{PHL}, t_{PLH} | Receiver propagation delay time | | | | | 35 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $ t_{PHL} - t_{PLH} $ | | | | | 2.5 | ns |
| t_{PLZ}, t_{PHZ} | Receiver disable time | | | 8 | 30 | ns | |
| $t_{pZL(1)}, t_{pZH(1)}$ | Receiver enable time | Driver enabled | See Figure 7 | | 10 | 30 | ns |
| $t_{pZL(2)}, t_{pZH(2)}$ | | Driver disabled | See Figure 8 | | 3 | 8 | μs |

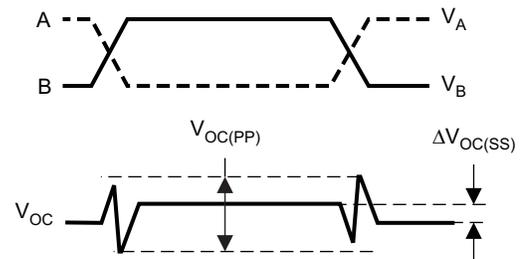
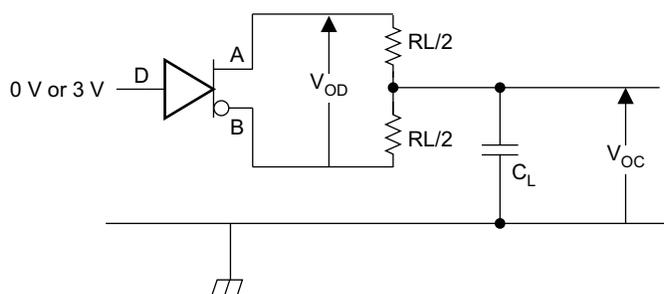
PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω .



S0301-01

Figure 1. Measurement of Driver Differential Output Voltage with Common-Mode Load



S0302-01

Figure 2. Measurement of Driver Differential and Common-Mode output with RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

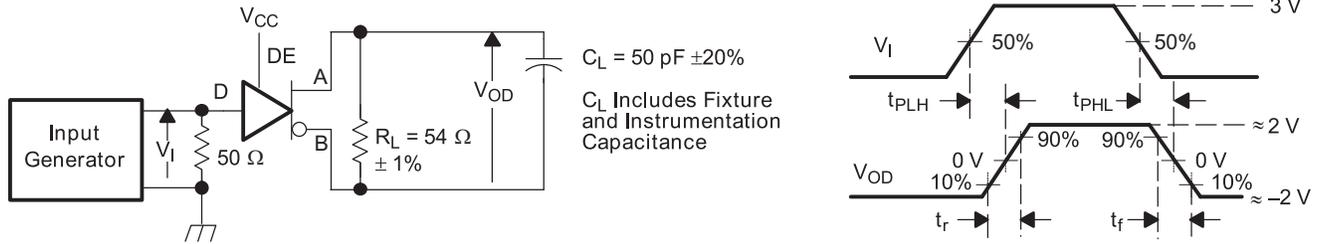
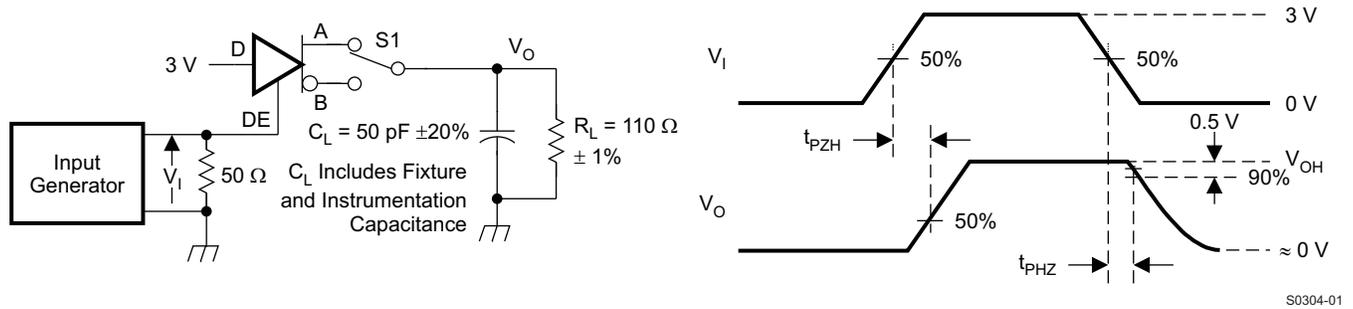
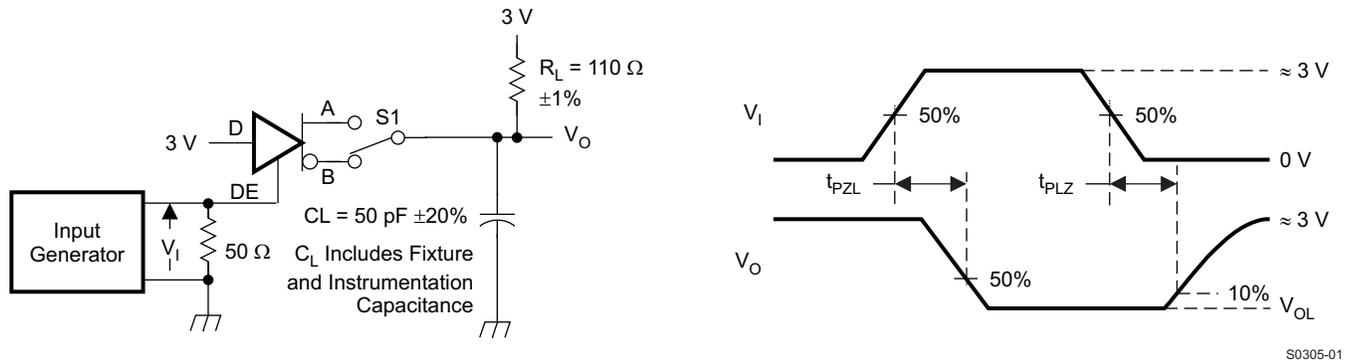


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times with Active High Output and Pull-Down Load



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-Up Load

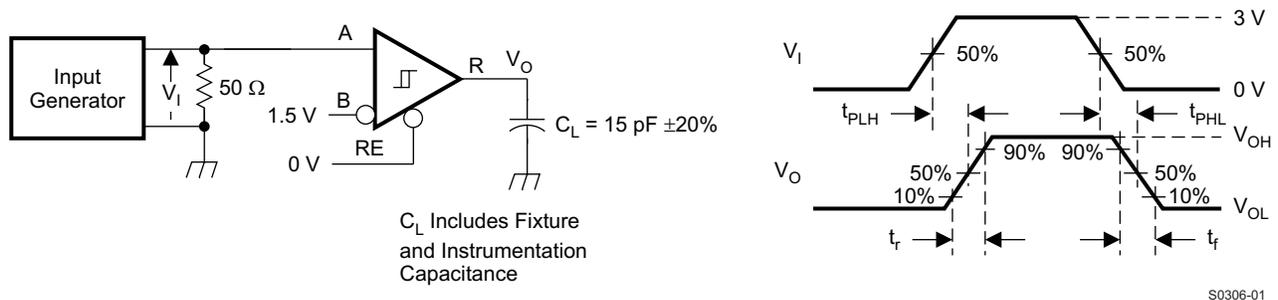
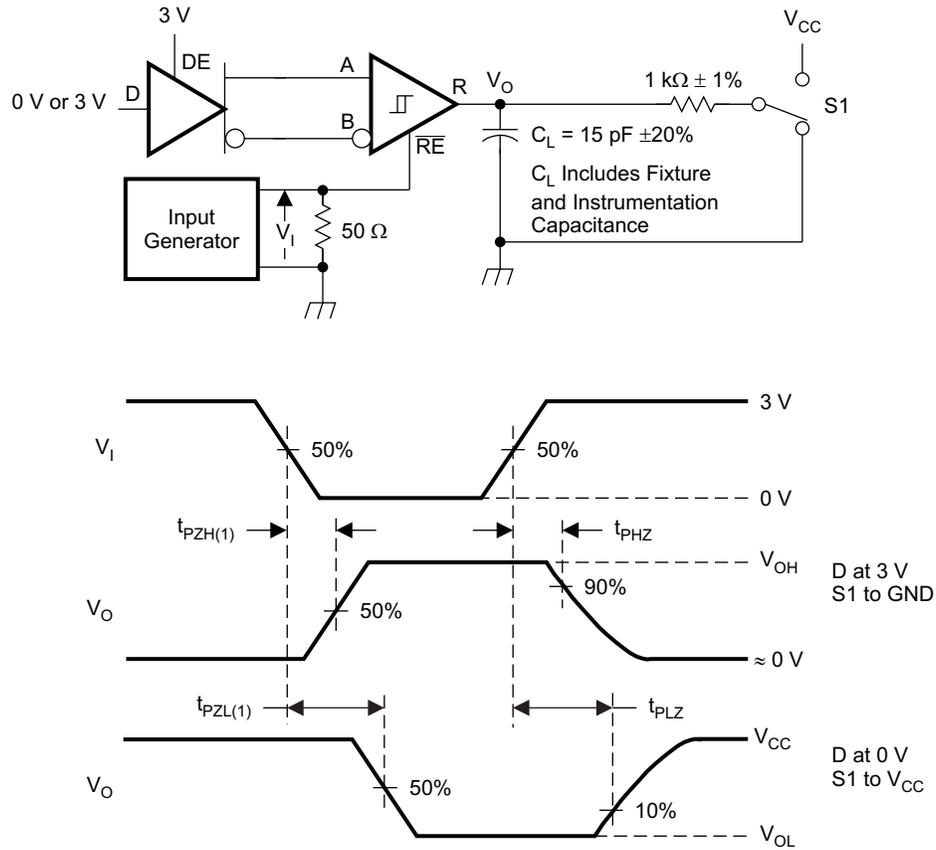


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)



S0307-01

Figure 7. Measurement of Receiver Enable/Disable Times with Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

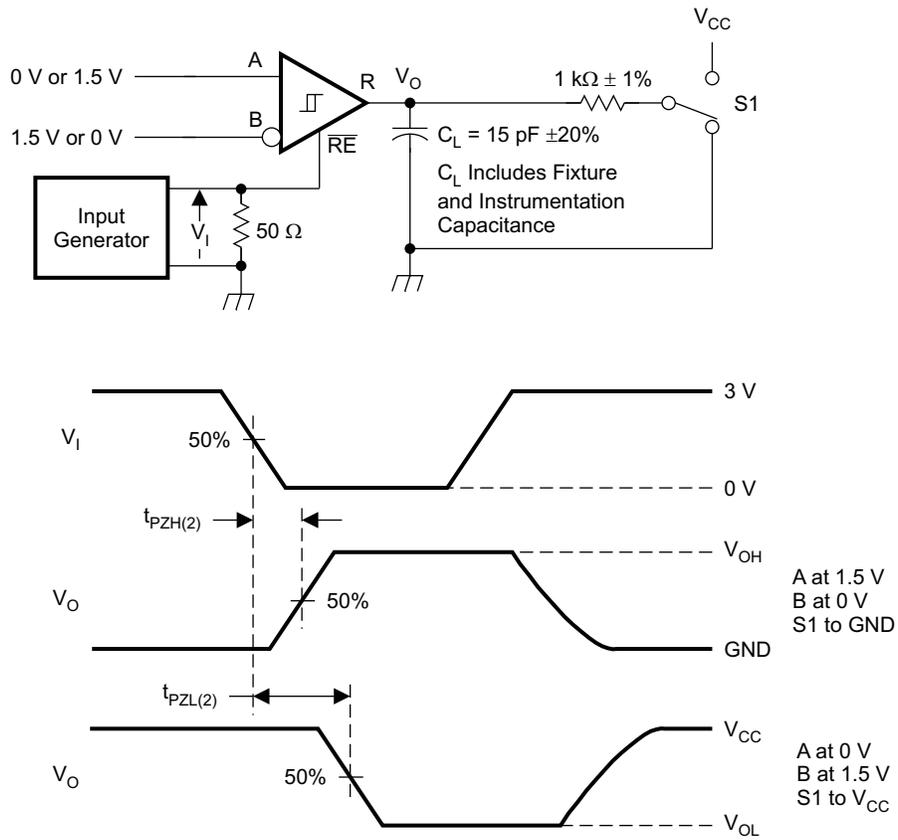


Figure 8. Measurement of Receiver Enable Times with Driver Disabled

TYPICAL CHARACTERISTICS

**DRIVER OUTPUT VOLTAGE
 vs
 DRIVER OUTPUT CURRENT**

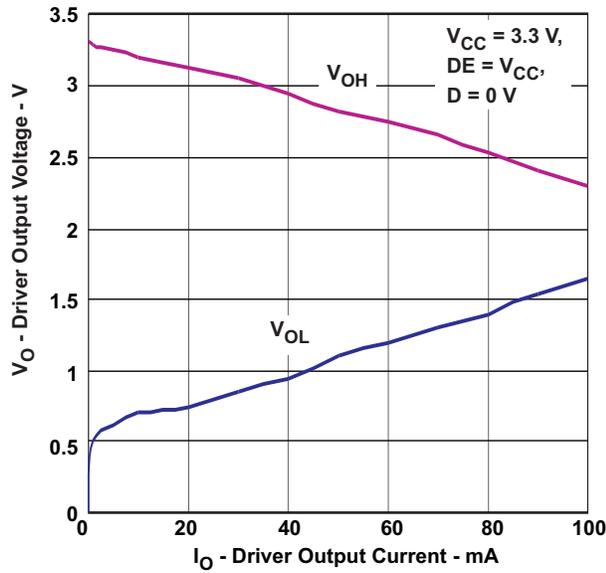


Figure 9.

**DRIVER DIFFERENTIAL OUTPUT VOLTAGE
 vs
 DRIVER OUTPUT CURRENT**

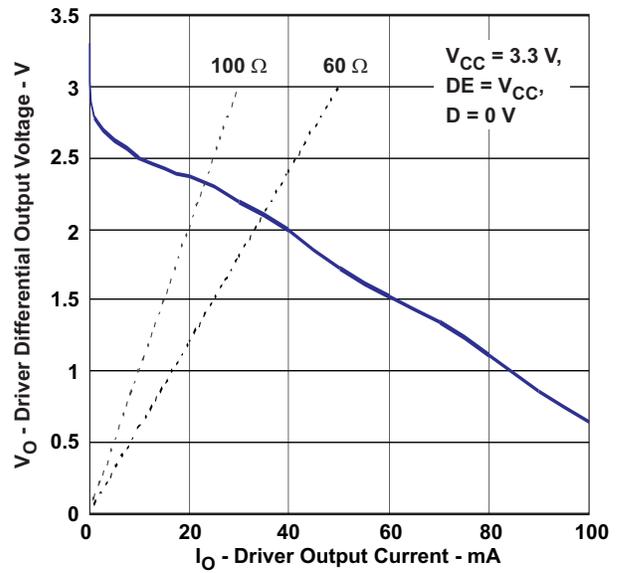


Figure 10.

**DRIVER OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE**

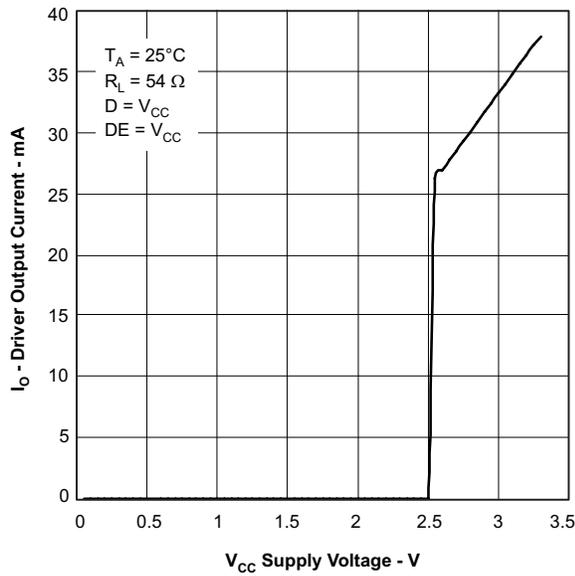


Figure 11.

**'HVD78
 DRIVER RISE and FALL TIME
 vs
 TEMPERATURE**

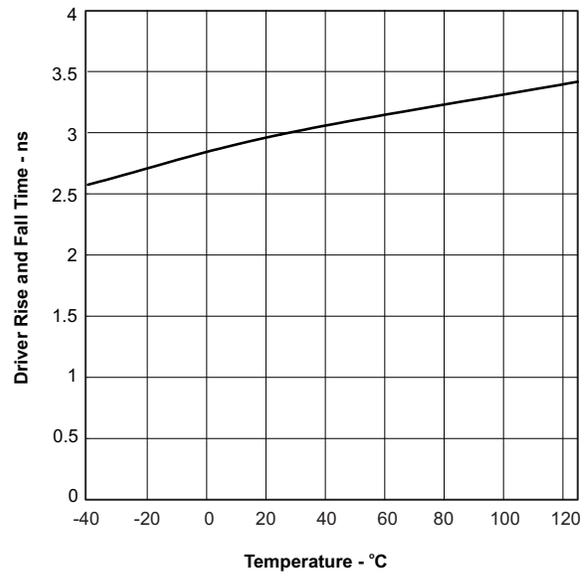


Figure 12.

TYPICAL CHARACTERISTICS (continued)

'HVD78
DRIVER PROPAGATION DELAY
vs
TEMPERATURE

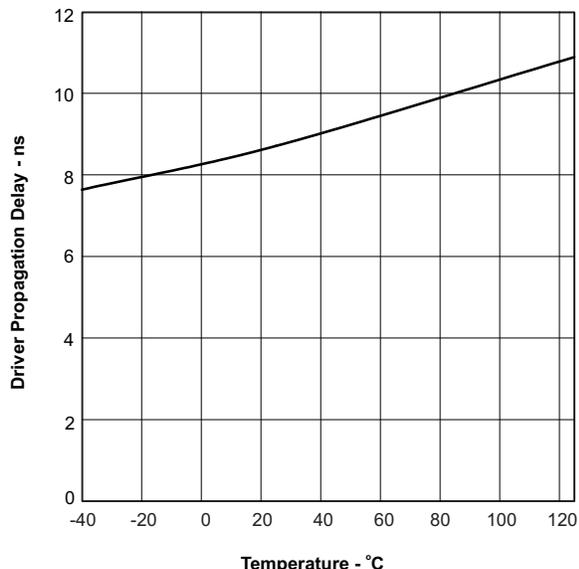


Figure 13.

'HVD72
SUPPLY CURRENT
vs
SIGNAL RATE

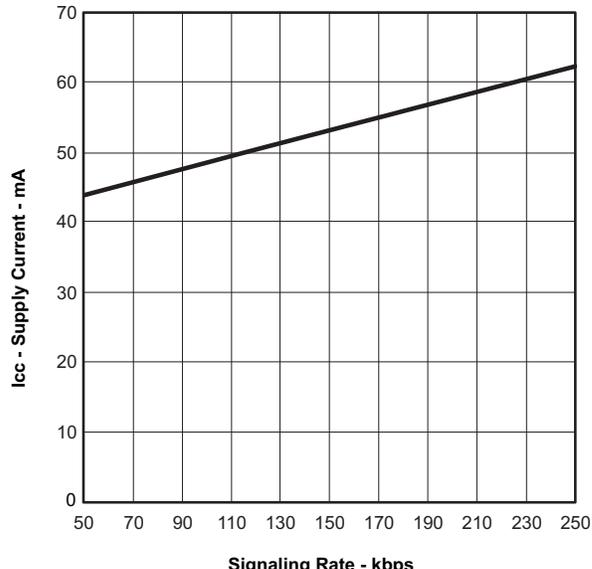


Figure 14.

'HVD75
SUPPLY CURRENT
vs
SIGNAL RATE

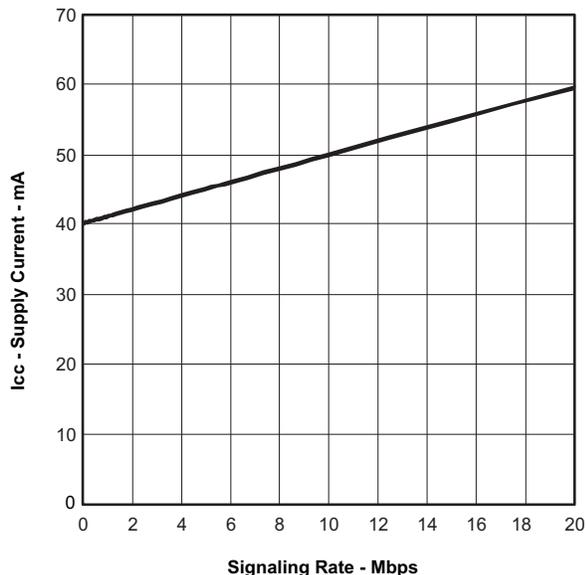


Figure 15.

'HVD78
SUPPLY CURRENT
vs
SIGNAL RATE

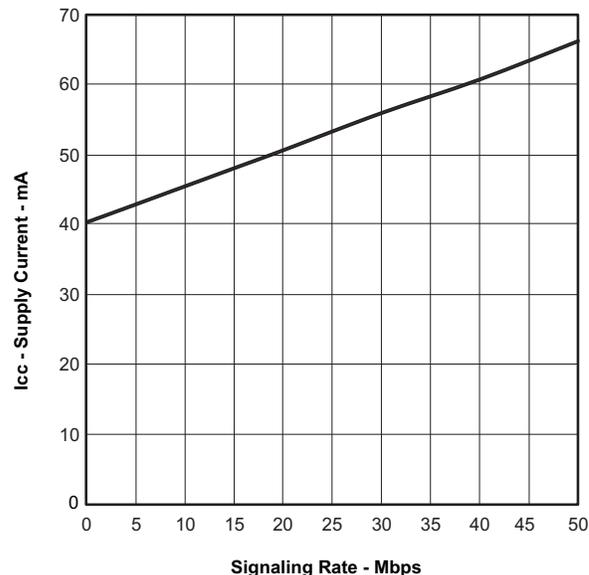
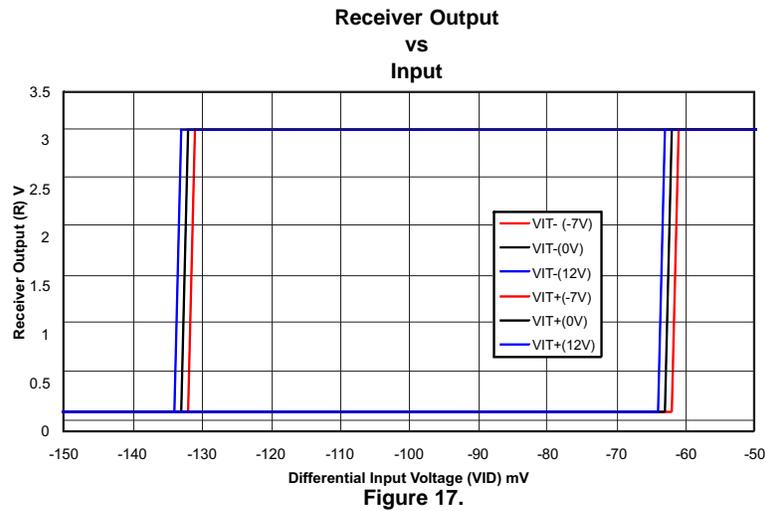


Figure 16.

TYPICAL CHARACTERISTICS (continued)



DEVICE INFORMATION

Table 4. Thermal Information

| PARAMETER | | D SOIC-8 | DGK MSOP-8 | DRB SON-8 | Units |
|--------------------|--|-------------|---------------|--------------|-------|
| Θ_{JA} | Junction-to-Ambient Thermal Resistance | 110.7 | 168.7 | 40.0 | °C/ W |
| Θ_{JB} | Junction-to-Board Thermal Resistance | 51.3 | 89.5 | 15.5 | |
| $\Theta_{JC(top)}$ | Junction-to-Case(top) Thermal Resistance | 54.7 | 62.2 | 49.6 | |
| $\Theta_{JC(top)}$ | Junction-to-Case(top) Thermal Resistance | n/a | n/a | 3.9 | |
| Ψ_{JT} | Junction-to-Top thermal parameter | 9.2 | 7.4 | 0.6 | |
| Ψ_{JB} | Junction-to-Board thermal parameter | 50.7 | 87.9 | 15.7 | |
| T_{TSD} | Thermal Shut-down junction temperature | 170 | | | °C |

Table 5. Power Dissipation

| PARAMETER | | TEST CONDITIONS | | VALUE | UNITS | |
|-----------|--|-----------------|--|-------|-------|----|
| PD | Power Dissipation driver and receiver enabled, $V_{CC} = 3.6$ V, $T_J = 150^\circ$ C 50% duty cycle square-wave signal at signaling rate: <ul style="list-style-type: none"> • HVD72 at 250 kbps • HVD75 at 20 Mbps • HVD78 at 50 Mbps | Unterminated | $R_L = 300 \Omega$, $C_L = 50$ pF (driver) | HVD72 | 120 | mW |
| | | | | HVD75 | 160 | |
| | | | | HVD78 | 200 | |
| | | RS-422 load | $R_L = 100 \Omega$, $C_L = 50$ pF (driver) | HVD72 | 155 | mW |
| | | | | HVD75 | 195 | |
| | | | | HVD78 | 230 | |
| | | RS-485 load | $R_L = 54 \Omega$, $C_L = 50$ pF (driver), | HVD72 | 190 | mW |
| | | | | HVD75 | 230 | |
| | | | | HVD78 | 260 | |

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS} . As seen in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+} .

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

Low-Power Standby Mode

When both the driver and receiver are disabled (DE low and RE high) the device is in standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 100 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

APPLICATION INFORMATION

Device Configuration

The SN65HVD72, 'HVD75 and 'HVD78 are half-duplex RS-485 transceivers operating from a single 3.3V $\pm 10\%$ supply. The driver and receiver enable pins allow for the configuration of different operating modes.

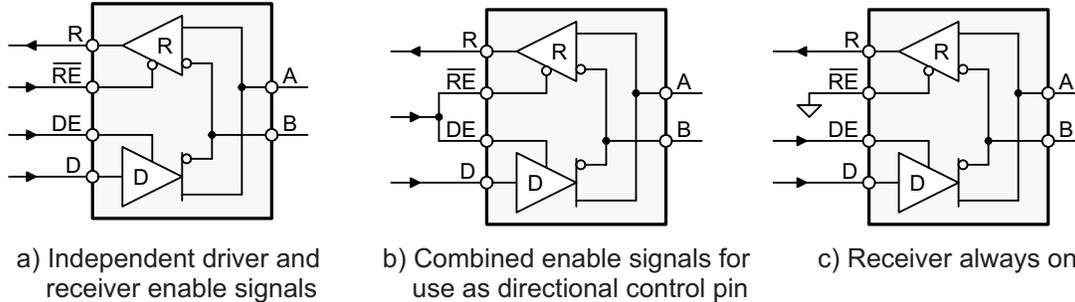


Figure 18. Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

Bus – Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

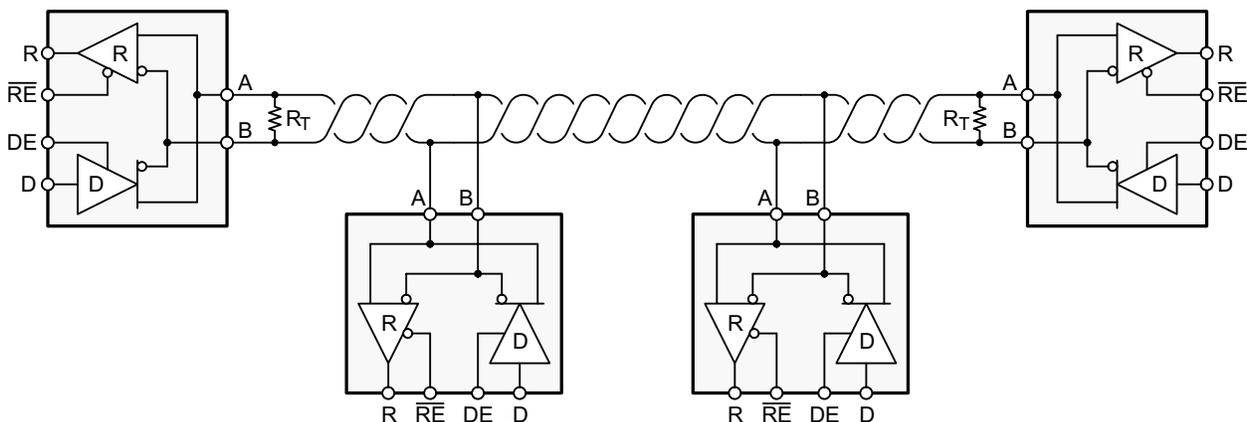


Figure 19. Typical RS-485 network with SN65HVD7x Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with $Z_0 = 100 \Omega$, and RS-485 cable with $Z_0 = 120 \Omega$. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ± 200 mV. When the differential input voltage, V_{ID} , is greater than + 200 mV, the receiver output turns high, for $V_{ID} < -200$ mV the receiver outputs low.

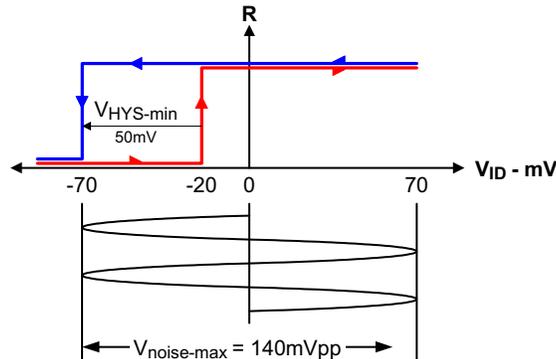


Figure 20. SN65HVD7x Noise Immunity

The SN65HVD7x transceiver family implements high receiver noise-immunity by providing a maximum positive-going input threshold of - 20 mV and a minimum hysteresis of 50 mV. In the case of a noisy input condition therefore, a differential noise voltage of up to 140 mVPP can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environments.

Transient Protection

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ± 15 kV human body model (HBM) and ± 12 kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50 % higher charge capacitance, C_S , and 78 % lower discharge resistance, R_D of the IEC-model produce significantly higher discharge currents than the HBM-model.

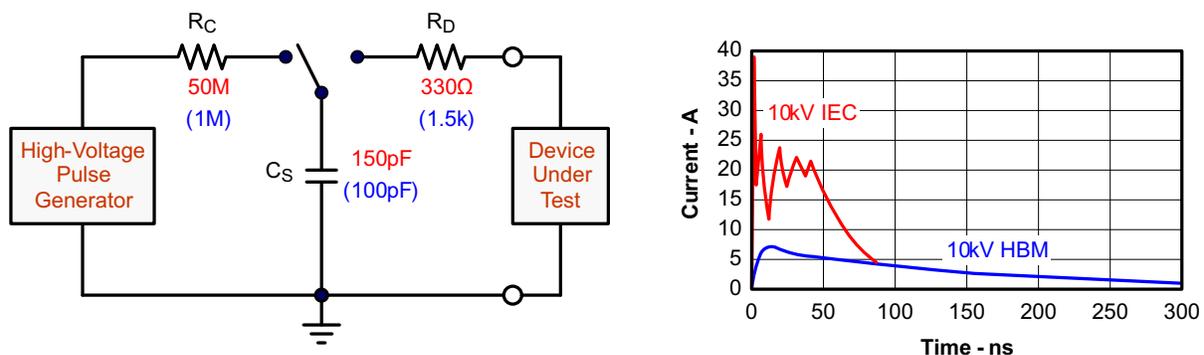


Figure 21. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The implementation of IEC-ESD protection on-chip increases the robustness of equipment significantly, which most likely experience discharge events due to human contact with connectors and cables. Designers may also want to implement protection against much longer duration transients, typically referred to as surge transients. Figure 9 therefore suggests two circuit designs providing protection against light and heavy surge transients, in addition to ESD and EFT transients. Table A1 presents the associated bill of material.

Table 6. Bill of Materials

| Device | Function | Order Number | Manufacturer |
|------------|--|--------------------|--------------|
| XCVR | 3.3V, 250kbps RS-485 Transceiver | SN65HVD72D | TI |
| R1, R2 | 10Ω, Pulse-Proof Thick-Film Resistor | CRCW0603010RJNEAHP | Vishay |
| TVS | Bidirectional 400W Transient Suppressor | CDSOT23-SM712 | Bourns |
| TBU1, TBU2 | Bidirectional. | TBU-CA-065-200-WH | Bourns |
| MOV1, MOV2 | 200mA Transient Blocking Unit 200V, Metal-Oxide Varistor | MOV-10D201K | Bourns |

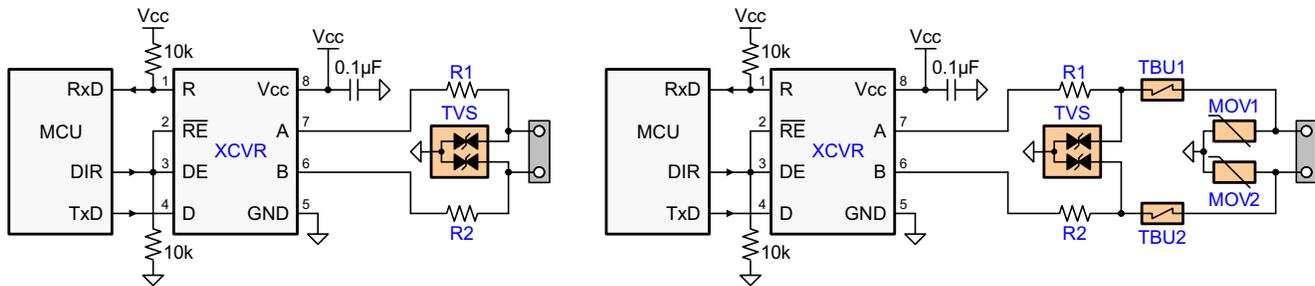


Figure 22. Transient Protections Against ESD, EFT, and Surge Transients

The left circuit provides surge protection of ≥ 500 V transients, while the right protection circuits can withstand surge transients of 5 kV.

Design and Layout Considerations For Transient Protection

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100 nF to 220 nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 23).

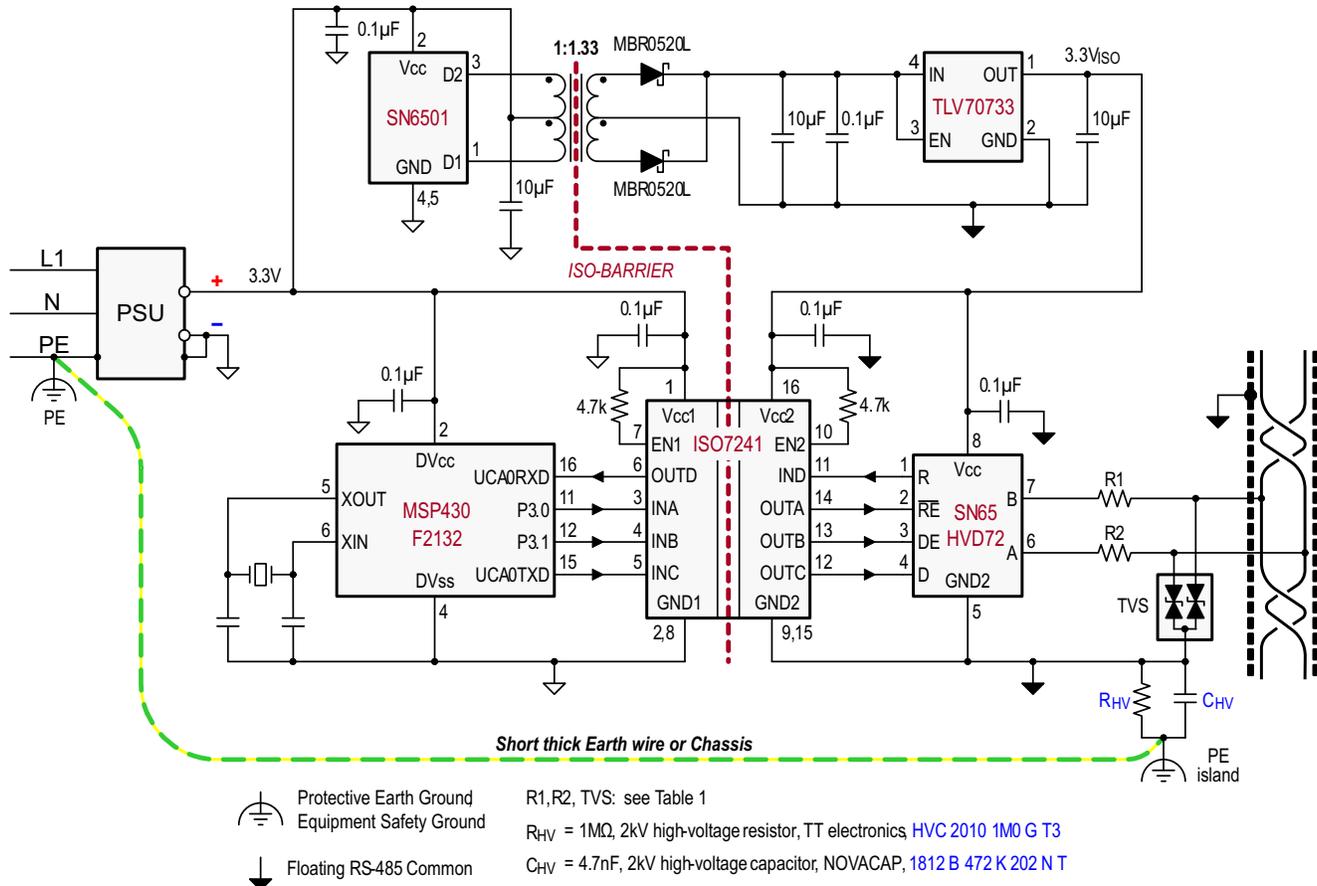


Figure 23. Isolated Bus Node With Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7k resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 22(left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

REVISION HISTORY

| Changes from Original (March 2012) to Revision A | Page |
|--|------|
| • Changed the Switching Characteristics condition statement From: 15 kbps devices (HVD73, 74, 75) bit time > 65 ns To: 20 Mbps devices (HVD73, 74, 75) bit time > 50 ns | 5 |
| • Changed the Switching Characteristics condition statement From: 50 kbps devices (HVD76, 77, 78) bit time > 20 ns To: 50 Mbps devices (HVD76, 77, 78) bit time > 20 ns | 6 |
| • Added Figure 12 to TYPICAL CHARACTERISTICS. | 10 |
| • Added Figure 13 to TYPICAL CHARACTERISTICS. | 11 |
| • Added Figure 14 to TYPICAL CHARACTERISTICS. | 11 |
| • Added Figure 15 to TYPICAL CHARACTERISTICS. | 11 |
| • Added Figure 16 to TYPICAL CHARACTERISTICS. | 11 |
| • Added Figure 17 to TYPICAL CHARACTERISTICS. | 12 |
| • Added VALUEs to the Thermal Characteristics table in the DEVICE INFORMATION section. | 12 |
| • Added APPLICATION INFORMATION section to data sheet. | 14 |

| Changes from Original (May 2012) to Revision B | Page |
|---|------|
| • Added the SON-8 package and Nodes column to Table 1 , | 1 |
| • Changed the SN65HVD72, 75, 78 Logic Diagram | 1 |
| • Changed the Voltage range at A or B Inputs MIN value From: –8 V To: –13 V | 3 |
| • Added foot note for free-air temperature to the RECOMMENDED OPERATING CONDITIONS table | 3 |
| • Changed the Bus input current (disabled driver) TYP values for HVD78 $V_I = 12\text{ V}$ From: 150 To: 240 and $V_I = -7\text{ V}$ From: –120 To: –180 | 4 |
| • Added TYP values to the SWITCHING CHARACTERISTICS table | 5 |
| • Added TYP values to the SWITCHING CHARACTERISTICS table | 6 |
| • Changed Table 4 , Thermal Information | 12 |
| • Changed Table 5 , Thermal Characteristics | 12 |
| • Added section: LOW-POWER STANDBY MODE | 13 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN65HVD72D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD72 | Samples |
| SN65HVD72DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD72 | Samples |
| SN65HVD72DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD72 | Samples |
| SN65HVD72DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD72 | Samples |
| SN65HVD72DRBR | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD72 | Samples |
| SN65HVD72DRBT | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD72 | Samples |
| SN65HVD75D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD75 | Samples |
| SN65HVD75DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD75 | Samples |
| SN65HVD75DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD75 | Samples |
| SN65HVD75DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD75 | Samples |
| SN65HVD75DRBR | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD75 | Samples |
| SN65HVD75DRBT | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD75 | Samples |
| SN65HVD78D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD78 | Samples |
| SN65HVD78DGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD78 | Samples |
| SN65HVD78DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HVD78 | Samples |
| SN65HVD78DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD78 | Samples |
| SN65HVD78DRBR | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD78 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---|
| SN65HVD78DRBT | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HVD78 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

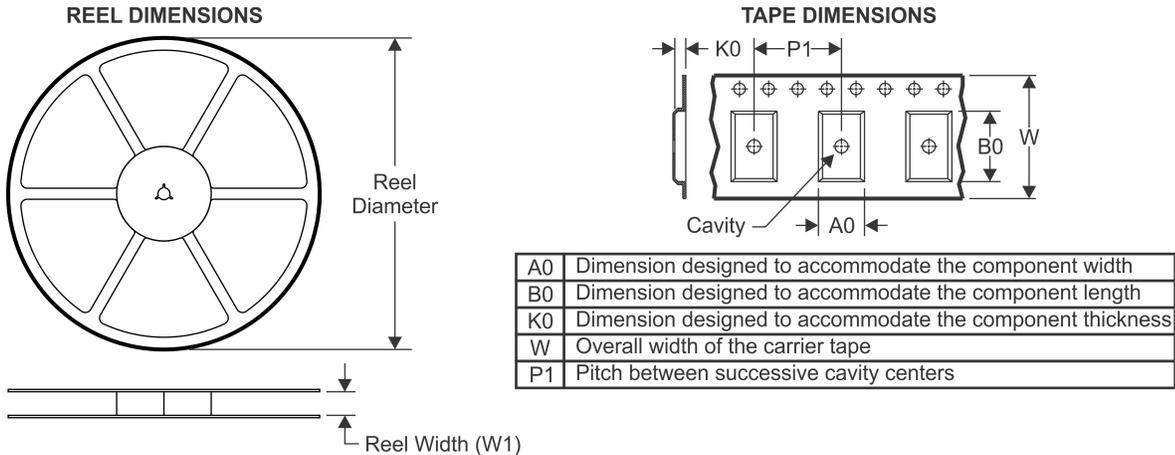
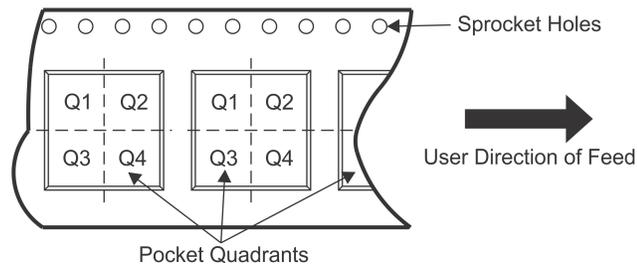
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

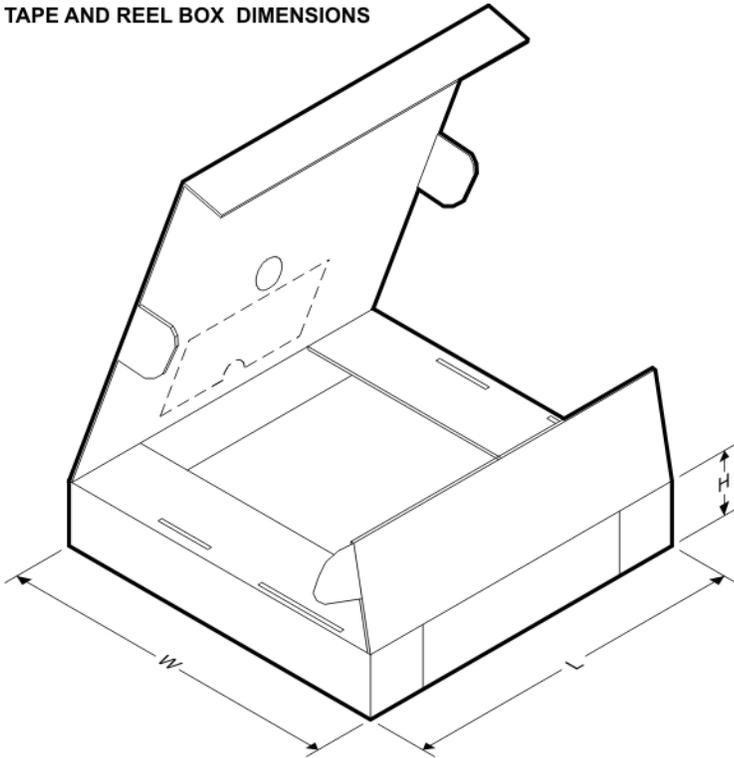
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD72DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD72DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD72DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD72DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD75DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD75DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD75DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD75DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD78DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD78DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD78DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD78DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

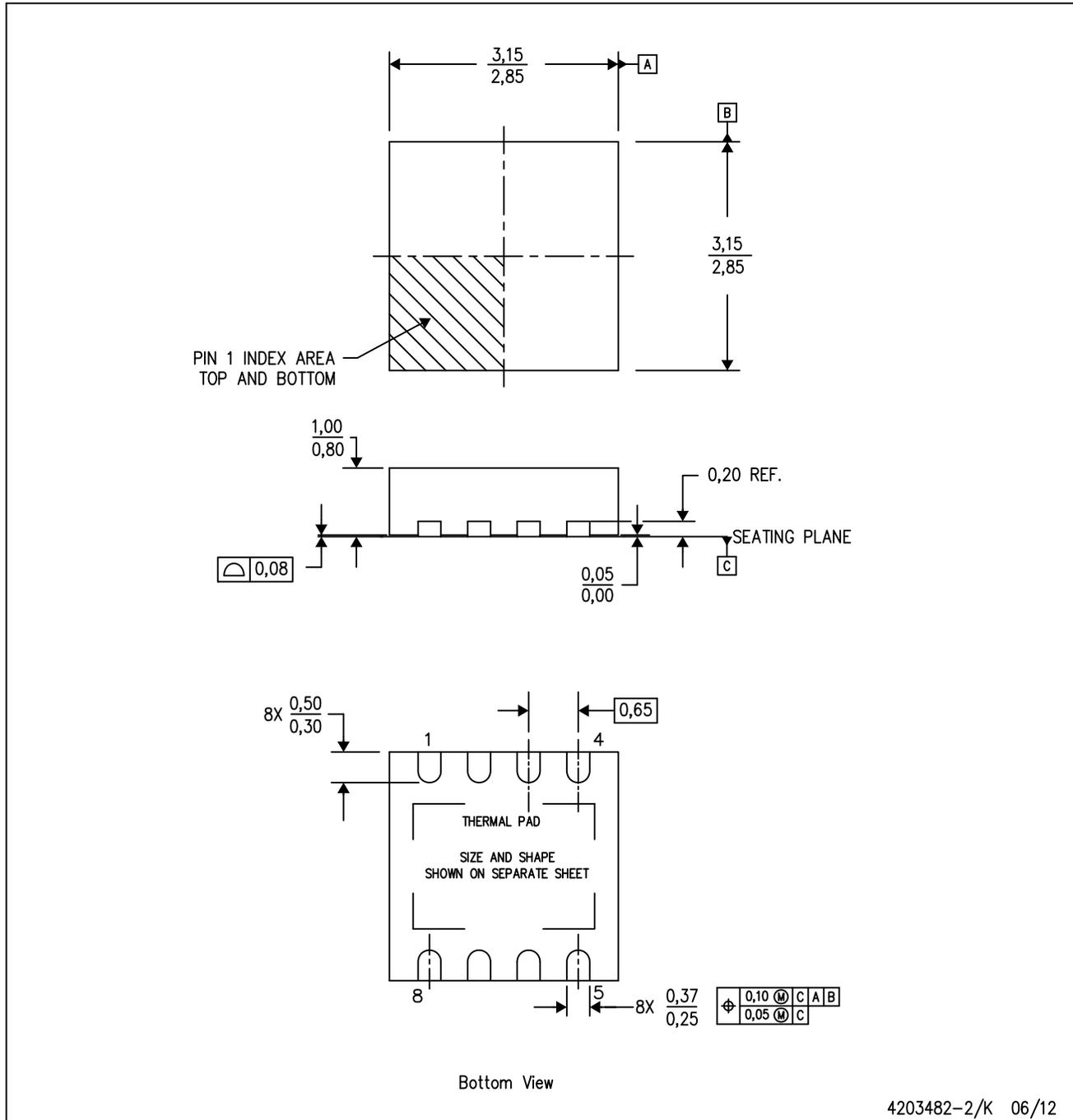
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD72DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD72DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| SN65HVD72DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| SN65HVD72DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| SN65HVD75DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD75DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| SN65HVD75DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| SN65HVD75DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| SN65HVD78DGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| SN65HVD78DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| SN65HVD78DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| SN65HVD78DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

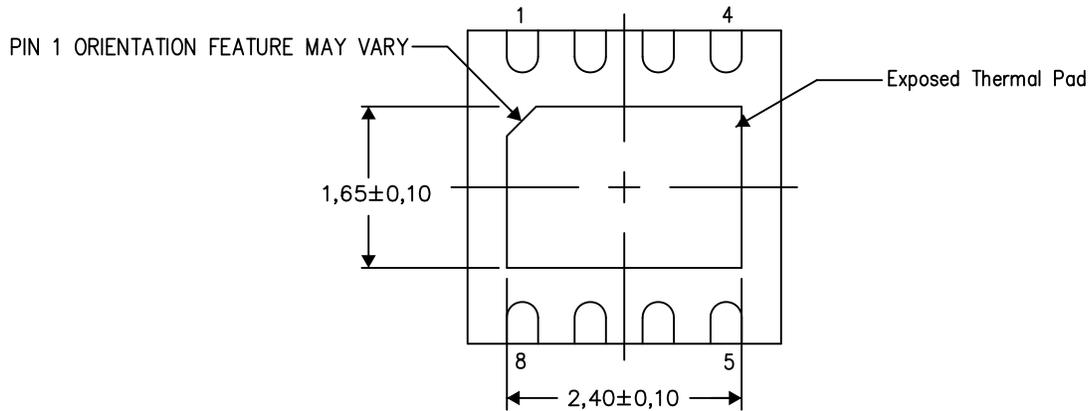
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

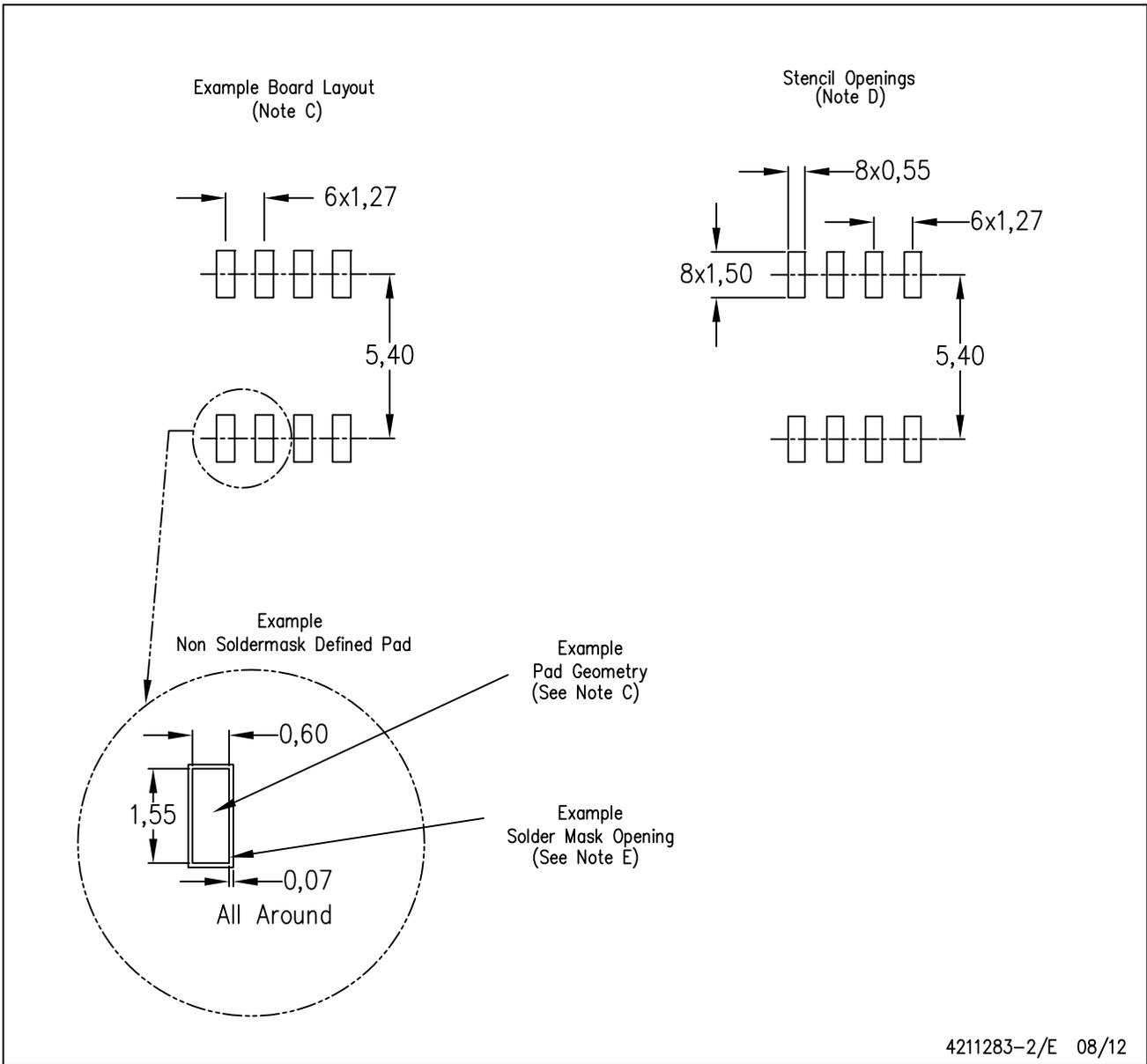
Exposed Thermal Pad Dimensions

4206340-3/N 09/12

NOTE: All linear dimensions are in millimeters

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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