TUSB8040
USB 3.0 Four Port Hub

Data Manual

Literature Number: SLLSE42G
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USB 3.0 Four Port Hub

Check for Samples: TUSB8040

1 PRODUCT OVERVIEW

1.1 Features

- **USB 3.0 Compliant Four Port Hub, TID# 330000003**
  - **Upstream Port Supports SuperSpeed, High-Speed and Full-Speed Connections**
  - **Each of the Four Downstream Ports Support SuperSpeed, High-Speed, Full-Speed/Low-Speed Connections**
- **USB 2.0 Hub Features**
  - **Multi Transaction Translator (MTT) Hub: Four Transaction Translators, One Per Port**
  - **Four (Over USB Required Minimum of Two) Asynchronous Endpoint Buffers Per Transaction Translator for Better Throughput**
- **Supports Charging Downstream Port (CDP) Applications**
  - **Battery Charging 1.2 Compliant**
- **Supports Operation as a USB 3.0 or USB 2.0 Compound Device**
- **Supports Per Port or Ganged Power Switching and Over-Current Protection**
- **Provides the following status outputs:**
  - **High-Speed Upstream Connection**
  - **High-Speed Upstream Port Suspended**
  - **SuperSpeed Upstream Connection**
  - **SuperSpeed Upstream Port Suspended**
- **Optional Serial EEPROM or SMBus Slave Interface for Custom Configurations:**
  - **VID/PID**
  - **Manufacturer and Product Strings**
  - **Serial Number**
- **Using Pin Selection or the EEPROM/SMBus Slave Interface, Each Downstream Port Can Be Independently:**
  - **Enabled or Disabled**
  - **Marked as Removable or Permanently Attached (for Compound Applications)**
  - **Have Battery Charging Enabled or Disabled**
- **Provides 128-Bit Universally Unique Identifier (UUID)**
- **Optionally Supports USB 2.0 Compliant Port Indicator LEDs**
- **Configurable SMBus Address to Support Multiple Devices on the Same SMBus Segment**
- **Supports On-Board and In-System EEPROM Programming Via the USB 2.0 Upstream Port**
- **Single Clock Input, 24-MHz Crystal or Oscillator**
- **Industrial Temperature Range, –40°C to 85°C**

1.2 Introduction

The TUSB8040 is USB 3.0 compliant hub available in an 80-pin QFP or 100-pin QFN package. The QFP device is designed for operation over the industrial temperature range of –40°C to 85°C. The QFN device is designed for operation over the commercial temperature range of 0°C to 70°C.

The TUSB8040 provides simultaneous SuperSpeed and high-speed/full-speed connections on the upstream port and provides SuperSpeed, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed and high-speed connectivity are disabled on the downstream ports.

The TUSB8040 supports up to four downstream ports. It may be configured to report one to four downstream ports by pin selection or an attached EEPROM or SMBus controller. The configuration options provide the ability to scale the device by application.

A typical system view of the TUSB8040 is shown in Figure 1-1.

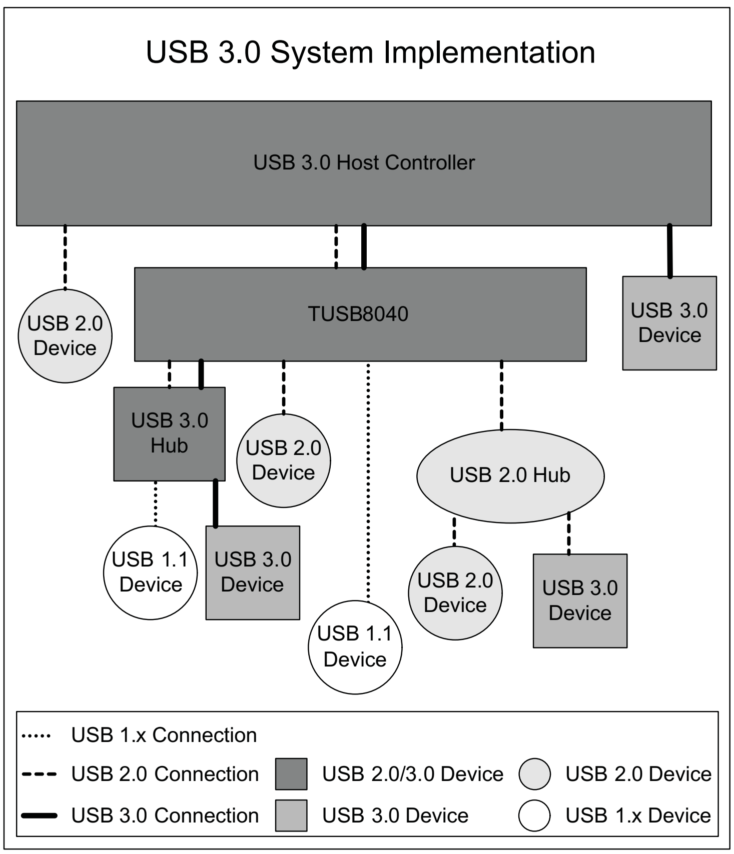


Figure 1-1. Typical Application

1.3 Functional Block Diagram

The TUSB8040RKM (QFN) supports both per port or ganged power switching and over-current protection. An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when a individually port power controlled hub senses an over-current event, power to only the affected downstream port will be switched off.

A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off. The TUSB8040RKM also provides customization using an I^{2}C EEPROM or configuration via an SMBus host for vendor specific PID, VID, and strings. Ports can also be marked as disabled or permanently attached using pin selection, I^{2}C EEPROM or an SMBus host. The Device Status and Command Register at F8h cannot be modified by the contents of the I^{2}C EEPROM.

The TUSB8040PFP (QFP) is a reduced footprint hub that supports ganged power switching and over-current protection only. A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off. The TUSB8040PFP also provides customization using an I^{2}C EEPROM or configuration via an SMBus host for vendor specific PID, VID, and strings. Ports can also be marked as disabled or permanently attached using an I^{2}C EEPROM or an SMBus host.

The Device Status and Command Register at F8h cannot be modified by the contents of the I^{2}C EEPROM.

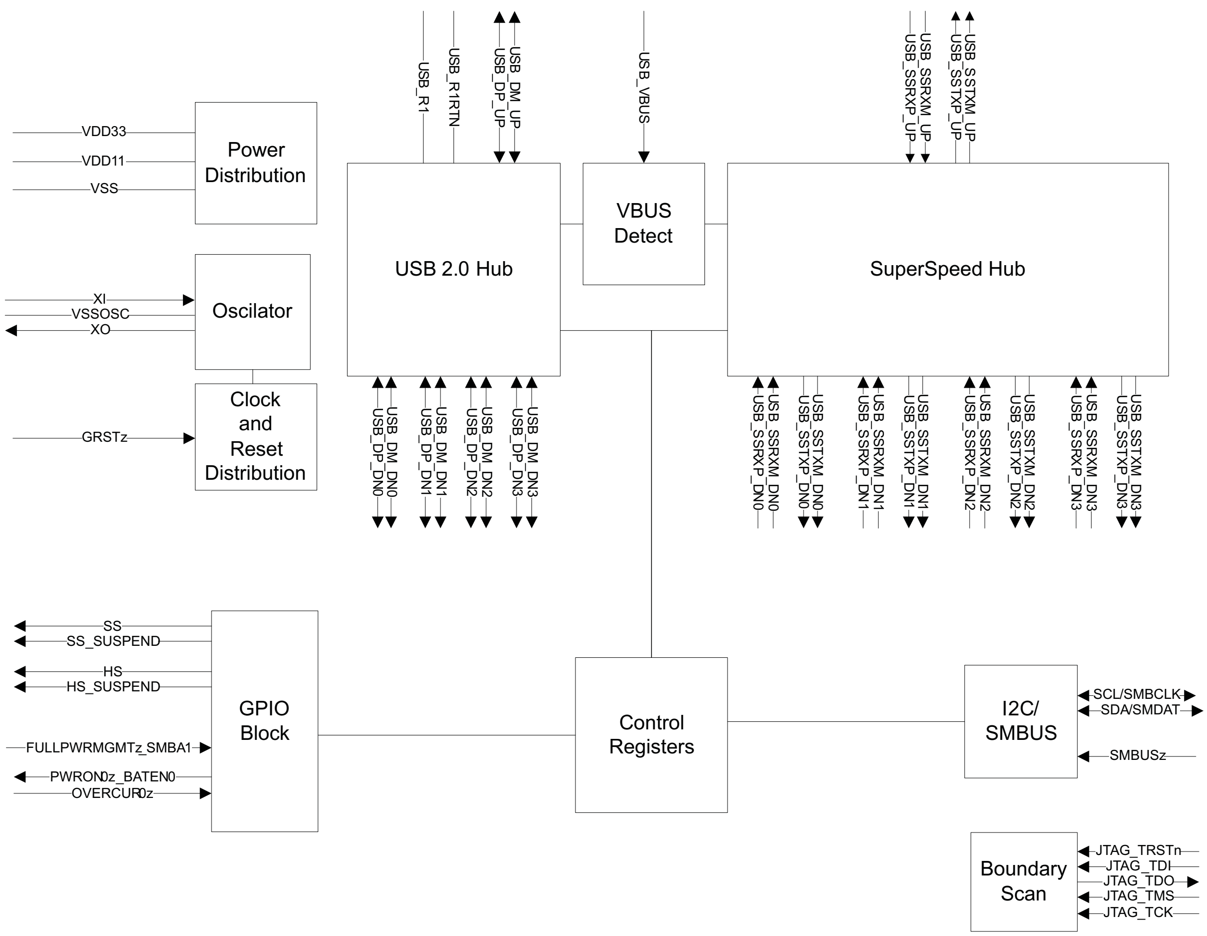
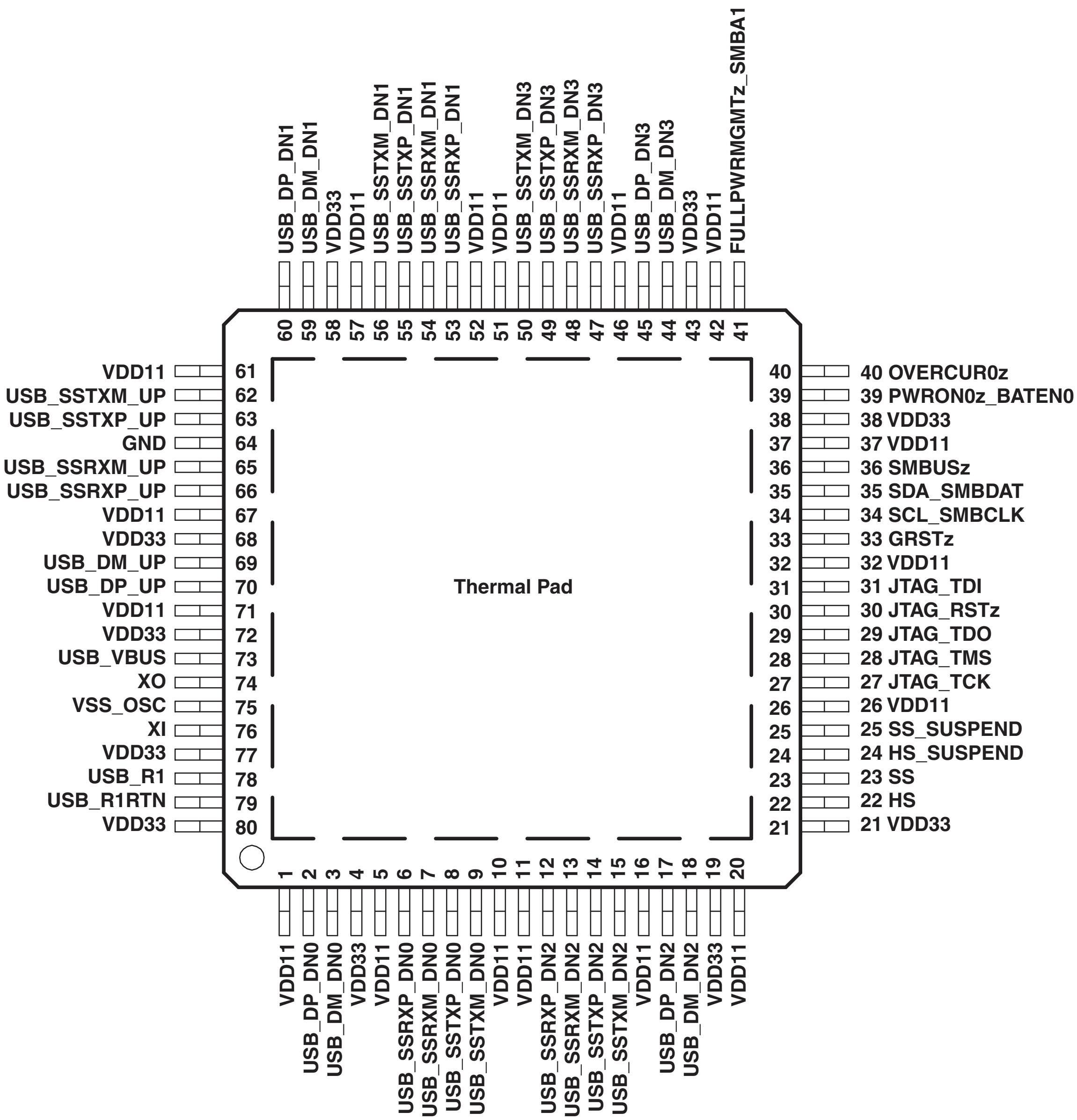


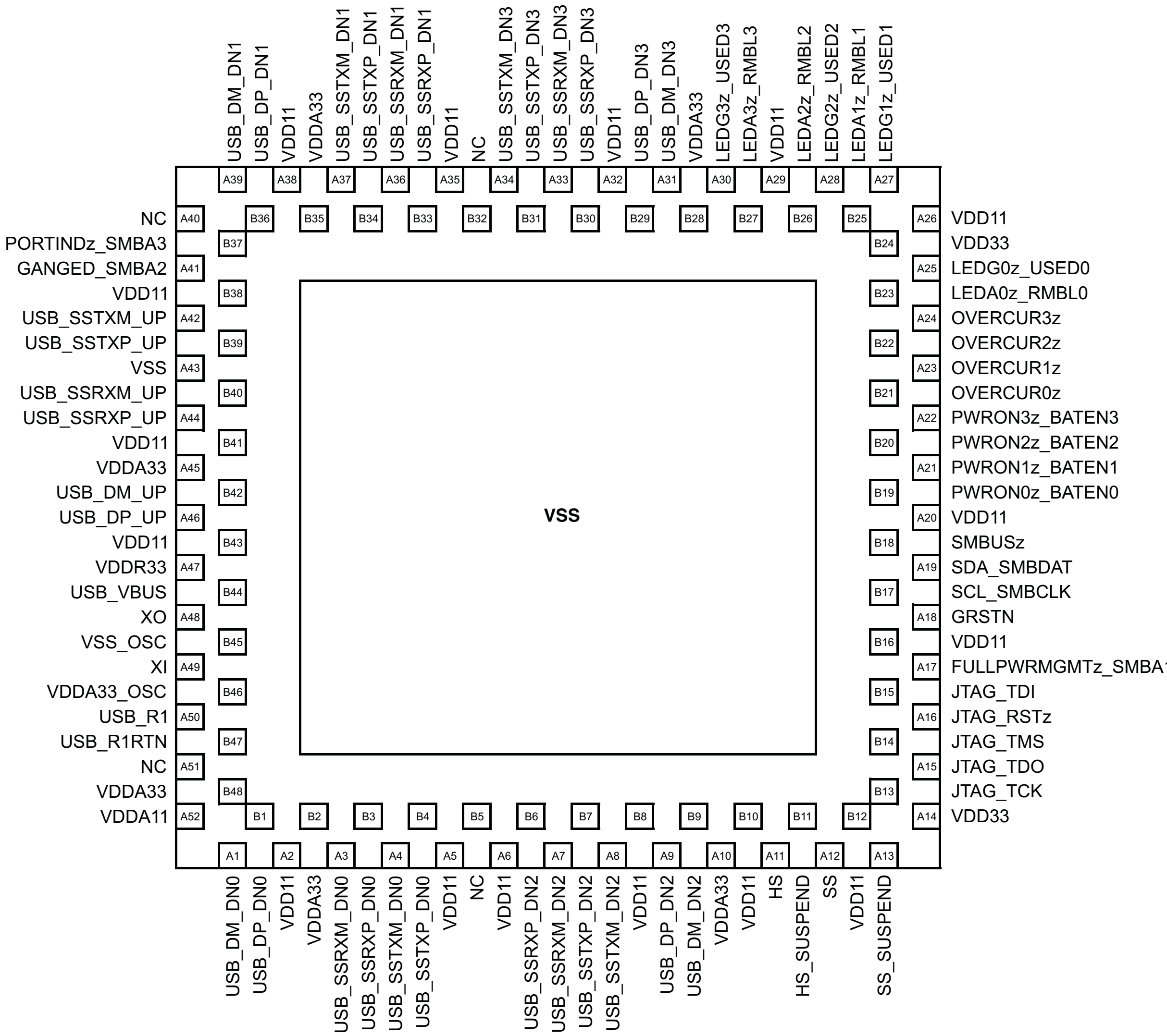
Figure 1-2. TUSB8040PFP Functional Block Diagram

2 PIN DESCRIPTIONS

PFP PACKAGE
(TOP VIEW)



RKM PACKAGE
(TOP VIEW)



TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PD, PU	Internal pull-down/pull-up
PT	Passive pass through
P	Power Supply
G	Ground

2.1 Clock and Reset Signals

Table 2-1. Clock and Reset Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
GRSTz	I, PU	33	A18	Global power reset. This reset brings all of the TUSB8040 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional. GRSTz should be asserted a minimum of 3 ms after all power rails are valid at the device.
XI	I	76	A49	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	O	74	A48	Crystal output. This terminal is crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
VSSOSC	I	75	B45	Oscillator return. If using a crystal, the load capacitors should use this signal as the return path and it should not be connected to the PCB ground. If using an oscillator, this terminal should be connected to PCB Ground.

2.2 USB Upstream Signals

Table 2-2. USB Upstream Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
USB_SSTXP_UP	O	63	B39	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	O	62	A42	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	I	66	A44	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	I	65	B40	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	I/O	70	A46	USB high-speed differential transceiver (positive)
USB_DM_UP	I/O	69	B42	USB high-speed differential transceiver (negative)
USB_R1	PT	78	A50	Precision resistor reference. A 9.09-KΩ ±1% resistor should be connected between USB_R1 and USB_R1RTN.
USB_R1RTN	PT	79	B47	Precision resistor reference return
USB_VBUS	I	73	B44	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-KΩ ±1% resistor, and to ground through a 10-KΩ ±1% resistor from the signal to ground.

2.3 USB Downstream Signals

Table 2-3. USB Downstream Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
USB_SSTXP_DN0	O	8	B4	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN0	O	9	A4	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN0	I	6	B3	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN0	I	7	A3	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN0	I/O	2	B1	USB high-speed differential transceiver (positive)
USB_DM_DN0	I/O	3	A1	USB high-speed differential transceiver (negative)
PWRON0z_BATEN0	I/O, PD	39	B19	USB port power on control for downstream power/battery charging enable. The terminal is used for control of the downstream power switch; in addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for the port as indicated in the Battery Charger Support register: 0 = Battery charging not supported 1 = Battery charging supported The TUSB8040PFP only supports ganged mode. This terminal provides the port power control for all downstream ports. This terminal also determines the battery charging support of all downstream ports.
OVERCUR0z	I, PU	40	B21	USB downstream port over-current detection. The TUSB8040PFP only supports ganged mode. This terminal receives the over-current indication for all downstream ports. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
USB_SSTXP_DN1	O	55	B34	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN1	O	56	A37	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN1	I	53	B33	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN1	I	54	A36	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN1	I/O	60	B36	USB High-speed differential transceiver (positive)
USB_DM_DN1	I/O	59	A39	USB High-speed differential transceiver (negative)
PWRON1z_BATEN1	I/O, PD		A21	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 1 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR1z	I, PU		A23	USB Port 1 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10K resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN2	O	14	B7	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN2	O	15	A8	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN2	I	12	B6	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN2	I	13	A7	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN2	I/O	17	A9	USB High-speed differential transceiver (positive)
USB_DM_DN2	I/O	18	B9	USB High-speed differential transceiver (negative)

Table 2-3. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
PWRON2z_BATEN2	I/O, PD		B20	USB Port 2 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 2. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 2 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR2z	I, PU		B22	USB Port 2 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10K resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN3	O	49	B31	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN3	O	50	A34	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN3	I	47	B30	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN3	I	48	A33	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN3	I/O	45	B29	USB High-speed differential transceiver (positive)
USB_DM_DN3	I/O	44	A31	USB High-speed differential transceiver (negative)
PWRON3z_BATEN3	I/O, PD		A22	USB Port 3 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 3. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 3as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR3z	I, PU		A24	USB Port 3 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred
LEDA0z_RMBL0	I, PU		B23	USB Port 0 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable Device removable option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDA1z_RMBL1	I/O, PU		B25	USB Port 1 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable Device removable option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDA2z_RMBL2	I/O, PU		B26	USB Port 2 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable Device removable option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDA3z_RMBL3	I/O, PU		B27	USB Port 3 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable Device removable option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP

Table 2-3. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
LEDG0z_USED0	I/O, PU		A25	USB Port 0 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used Port used option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDG1z_USED1	I/O, PU		A27	USB Port 1 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used Port used option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDG2z_USED2	I/O, PU		A28	USB Port 2 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used Port used option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP
LEDG3z_USED3	I/O, PU		A30	USB Port 3 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used Port used option can be set via I2C EEPROM or SMBUS host on the TUSB8040PFP

2.4 I²C/SMBUS Signals

Table 2-4. I²C/SMBUS Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
SCL/SMBCLK	I/O, PD	34	B17	I²C clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	I/O, PD	35	A19	I²C data/SMBus data. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial data interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host. The SDA_SMBDAT terminal is sampled at the deassertion of reset to determine if SuperSpeed USB low power states U1 and U2 are disabled. If SDA_SMBDAT is high, U1 and U2 low power states are disabled. If SDA_SMBDAT is low, U1 and U2 low power states are enabled. If the optional EEPROM or SMBUS is implemented, the value of the u1u2Disable bit of the Device Configuration Register determines if the low power states U1 and U2 are enabled. Can be left unconnected if external interface not implemented and U1 and U2 are to be enabled.
SMBUSz	I, PU	36	B18	I²C/SMBus mode select. 1 = I²C Mode Selected 0 = SMBus Mode Selected Can be left unconnected if external interface not implemented.

2.5 Test and Miscellaneous Signals

Table 2-5. Test and Miscellaneous Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
JTAG_TCK	I/O, PD	27	B13	JTAG test clock. Can be left unconnected.
JTAG_TDI	I/O, PU	31	B15	JTAG test data in. Can be left unconnected.
JTAG_TDO	I/O, PD	29	A15	JTAG test data out. Can be left unconnected.
JTAG_TMS	I/O, PU	28	B14	JTAG test mode select. Can be left unconnected.
JTAG_RSTz	I/O, PD	30	A16	JTAG reset. Pull down using an external 1-KΩ resistor for normal operation.
HS_SUSPEND	O	24	B11	High-speed suspend status output. 0 = High-speed upstream port not suspended 1= High-speed upstream port suspended Can be left unconnected.
SS_SUSPEND	O	25	A13	SuperSpeed suspend status output. 0 = SuperSpeed upstream port not suspended 1= SuperSpeed upstream port suspended Can be left unconnected.

Table 2-5. Test and Miscellaneous Signals (continued)

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
HS	O	22	A11	High-speed status. The terminal is to indicate the connection status of the upstream port as documented below: 0 = Hub in low/full speed mode 1 = Hub in high-speed mode Can be left unconnected.
SS	O	23	A12	SuperSpeed status. The terminal is to indicate the connection status of the upstream port as documented below: 0 = Hub not in SuperSpeed mode 1 = Hub in SuperSpeed mode Can be left unconnected.
FULLPWRMGMTz_ SMBA1	I, PU	41	A17	Full power management enable/SMBus address bit 1. The value of the terminal is sampled at the de-assertion of reset to set the power switch control follows: 0 = Full power management supported 1 = Full Power management not supported Full power management is the ability to control power to the downstream ports of the TUSB8040 using the PWRON0z_BATEN0 terminal. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bits 2 and 3 are always 1 for the TUSB8040. Can be left unconnected if full power management and SMBus are not implemented.
GANGED_SMBA2	I, PU		A41	Ganged operation enable/SMBus Address bit 2. The value of the terminal is sampled at the deassertion of reset to set the power switch and over current detection mode as follows: 0 = Individual Power Gangs Supported 1 = Power Gangs Supported When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 2. SMBus slave address bits 2 and 3 are always 1 for the TUSB8040PFP.
PORTINDz_SMBA3	I, PU		B37	Port Indicator LED Status/SMBus Address bit 3. The value of the terminal is sampled at the deassertion of reset to determine the port indicator support for the hub as follows: 0 = Port Indicator LEDs are enabled 1 = Port Indicator LEDs are not enabled When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 3. SMBus slave address bits 2 and 3 are always 1 for the TUSB8040PFP.

2.6 Power Signals

Table 2-6. Power Signals

SIGNAL NAME	TYPE	PIN NO.		DESCRIPTION
		PFP	RKM	
VDD33	P	4, 19, 21, 38, 43, 58 68, 72, 77, 80	B2, A10, A14, B24, B28, B35, A45, A47, B46, B48	3.3-V power rail
VDD11	P	1, 5, 10, 11, 16, 20, 26, 32, 37, 42, 46, 51, 52, 57, 61, 67, 71	A2, A5, A6, B8, B10, B12, B16, A20, A26, A29, A32, A35, A38, B38, B41, B43, A52	1.1-V power rail
GND	G	64, 81	A43, A53	Ground, Power Pad
GND_NC	G		C1, C2, C3, C4	The corner pins, which are for mechanical stability of the package, are connected to ground internally. These pins may be connected to GND or left unconnected.
NC	NC		B5, B32, A40, A51	No connect

3 FUNCTIONAL DESCRIPTION

Table 3-1. TUSB8040 Register Map

BYTE ADDRESS	CONTENTS
00h	ROM Signature (55h)
01h	Vendor ID LSB
02h	Vendor ID MSB
03h	Product ID LSB
04h	Product ID MSB
05h	Device Configuration Register
06h	Battery Charging Support Register
07h	Device Removable Configuration Register
08h	Port Used Configuration Register
09h-0Fh	Reserved
10h-1Fh	Reserved
20h-21h	LangID Byte [1:0]
22h	Serial Number String Length
23h	Manufacturer String Length
24h	Product String Length
25h-2Fh	Reserved
30h-4Fh	Serial Number String Byte [31:0]
50h-8Fh	Manufacturer String Byte [63:0]
90h-CFh	Product String Byte [63:0]
D0-F7h	Reserved
F8h	Device Status and Command Register
F9-FFh	Reserved

3.1 I^{2}C EEPROM Operation

The TUSB8040 supports a single-master, standard mode (100 Kbit/s) connection to a dedicated I^{2}C EEPROM when the I^{2}C interface mode is enabled. In I^{2}C mode, the TUSB8040 reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0. If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8040 loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8040 exits the I^{2}C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed.

Note, the bytes located below offset 9h are optional. The requirement for data in those addresses is dependent on the options configured in the Device Configuration and Phy Custom Configuration registers.

For details on I^{2}C operation refer to the UM10204 I^{2}C-bus Specification and User Manual.

3.2 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8040 supports read block and write block protocols as a slave-only SMBus device.

The supported slave address of 1000 11xy for the TUSB8040PFP is:

- x is the state of FULLPWRMGMTz_SMBA1 at reset, and
- y indicates read (logic 1) or write (logic 0) access.

The supported slave address of 1000 pgxy for the TUSB8040RKM is:

- p is the state of PORTINDz_SMBA3 at reset,
- g is the state of GANGED_SMBA2 at reset,

- x is the state of FULLPWRMGMTz_SMBA1 at reset, and
- y indicates read (logic 1) or write (logic 0) access.

If the TUSB8040 is addressed by a host using an unsupported protocol it will not respond. The TUSB8040 will wait indefinitely for configuration by the SMBus host and will not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements refer to the System Management Bus Specification.

3.3 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8040 is in I^2C or SMBus mode.

3.3.1 *ROM Signature Register*

Table 3-2. Register Offset 0h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-3. Bit Descriptions – ROM Signature Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8040 in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8040 aborts the EEPROM load and executes with the register defaults.

3.3.2 *Vendor ID LSB Register*

Table 3-4. Register Offset 1h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	1

Table 3-5. Bit Descriptions – Vendor ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	vendorIdLsb	RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

3.3.3 *Vendor ID MSB Register*

Table 3-6. Register Offset 2h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0

Table 3-7. Bit Descriptions – Vendor ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	vendorIdMsb	RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

3.3.4 Product ID LSB Register

Table 3-8. Register Offset 3h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0

Table 3-9. Bit Descriptions – Product ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	productIdLsb	RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments; the default value of this register is 40h representing the LSB of the product ID assigned by Texas Instruments. The value of this register will be reported as configured for the SuperSpeed Device descriptor. The USB 2.0 Device descriptor will report the value in this register with bit [1] toggled. This ensures that the USB drivers load properly for both hubs. The value may be over-written to indicate a customer product ID.

3.3.5 Product ID MSB Register

Table 3-10. Register Offset 4h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

Table 3-11. Bit Descriptions – Product ID MSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	productIdMsb	RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 80h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID.

3.3.6 Device Configuration Register

Table 3-12. Register Offset 5h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	X	X	X	X	X

Table 3-13. Bit Descriptions – Device Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	customStrings	RW	Custom Strings enable. When this bit is set to 1 and the TUSB8040 is in I^2C mode, the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are loaded from the contents of the EEPROM. When the value of this bit is 1 and the TUSB8040 is in SMBUS mode, the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may written by an SMBus host.
6	customSernum	RW	Custom Serial Number Enable. When the TUSB8040 is in I^2C mode, the TUSB8040 loads the serial number register from the contents of the EEPROM. When the TUSB8040 is in SMBUS mode, the Serial Number registers may written by an SMBus host. This bit is always 1.

Table 3-13. Bit Descriptions – Device Configuration Register (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5	u1u2Disable	RW	U1 U2 Disable When this bit is set, the TUSB8040 will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP command. After receiving or sending a FLPMA LMP command, the TUSB8040 will continue to enable U1 or U2 until it gets a power on reset or is disconnected on its upstream port. This bit is loaded at the deassertion of reset with the value of the SDA_SMDAT terminal. When the TUSB8040 is in I^2C mode, the TUSB8040 loads this bit from the contents of the EEPROM. When the TUSB8040 is in SMBUS mode, the value may be over-written by a SMBUS host.
4	portIndz	RW	Port Indicator Status. For the TUSB8040PFP: This bit shall be 1. It shall not be over-written by EEPROM or an SMBus host. For the TUSB8040RKM: This bit shall be loaded at the de-assertion of reset with the value of PORTINDz_SMBA3 terminal. When the TUSB8040 is in I^2C mode, the TUSB8040 loads this bit from the contents of the EEPROM. When the TUSB8040 is in SMBUS mode, the value may be overwritten by an SMBus host.
3	ganged	RW	Ganged. This bit is always 1. For the TUSB8040PFP: This bit shall be 1. It shall not be over-written by EEPROM or an SMBus host. For the TUSB8040RKM: This bit shall be loaded at the de-assertion of reset with the value of GANGEd_SMBA2 terminal. When the TUSB8040 is in I^2C mode, the TUSB8040 loads this bit from the contents of the EEPROM. When the TUSB8040 is in SMBUS mode, the value may be overwritten by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz_SMBA1 terminal. When the TUSB8040 is in I^2C mode, the TUSB8040 loads this bit from the contents of the EEPROM. When the TUSB8040 is in SMBUS mode, the value may be over-written by an SMBus host.
1:0	RSVD	RO	Reserved. This field is reserved and returns 0 when read.

3.3.7 Battery Charging Support Register

Table 3-14. Register Offset 6h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	X	X	X	X

Table 3-15. Bit Descriptions – Battery Charging Support Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	batEn[3:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. A value of 0 indicates the port does not implement the charging port features. A value of 1 indicates the port does support the charging port features. Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 0. When in I^2C/SMBus mode the bits in this field corresponding to the enabled ports per used[3:0] may be over-written by EEPROM contents or by an SMBus host. For the TUSB8040PFP: The default value for these bits are loaded at the de-assertion of reset with the value of the PWRON0z_BATEN0: Four-port hub - bateEn[3:0] defaults to wxyzb, where w, x, y and z are all the value of PWRON0z_BATEN0. For the TUSB8040RKM: The default value for these bits are loaded at the de-assertion of reset with the value of PWRON[3:0]z_BATEN[3:0]: Four-port hub - bateEn[3:0] defaults to wxyzb, where w is PWRON3z_BATEN3, x is PWRON2z_BATEN2, y is PWRON1z_BATEN1 and z is PWRON0z_BATEN0.

3.3.8 Device Removable Configuration Register

Table 3-16. Register Offset 7h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-17. Bit Descriptions – Device Removable Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	rmbl[3:0]	RW	Removable. The bits in this field indicate whether a device attached to downstream ports 3 through 0 are removable or permanently attached. A value of 0 indicates the device attached to the port is not removable. A value of 1 indicates the device attached to the port is removable. Each bit corresponds directly to a downstream port, i.e. rmbl0 corresponds to downstream port 0. For the TUSB8040PFP: The default value for these bits are loaded at the de-assertion of reset with the value of Four-port hub - rmbl[3:0] defaults to 1111b. For the TUSB8040RKM: The default value for these bits are loaded at the de-assertion of reset with the value of LEDA[3:0]z_RMBL[3:0]: Four-port hub - rmbl[3:0] defaults to wxyzb, where w is LEDA3z_RMBL3, x is LEDA2z_RMBL2, y is LEDA1z_RMBL1 and z is LEDA0z_RMBL0. When in I^2C/SMBus mode the bits in this field corresponding to the enabled ports per rmbl[3:0] may be over-written by EEPROM contents or by an SMBus host.

3.3.9 Port Used Configuration Register

Table 3-18. Register Offset 8h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-19. Bit Descriptions – Port Used Configuration Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	used3:0]	RW	Used. The bits in this field indicate whether downstream ports 3 through 0 are enabled or disabled for use. A value of 0 indicates the port is not used. A value of 1 indicates the port is used. Each bit corresponds directly to a downstream port, i.e. used0 corresponds to downstream port 0. For the TUSB8040PFP: The default value for these bits are loaded at the de-assertion of reset with the value of Four-port hub - used[3:0] defaults to 1111b. For the TUSB8040RKM: The default value for these bits are loaded at the de-assertion of reset with the value of LEDG[3:0]z_USED[3:0]: Four-port hub - used[3:0] defaults to wxyzb, where w is LEDG3z_USED3, x is LEDG2z_USED2, y is LEDG1z_USED1 and z is LEDG0z_USED0. When in I^2C/SMBus mode the bits in this field corresponding to the enabled ports per used[3:0] may be over-written by EEPROM contents or by an SMBus host.

3.3.10 Language ID LSB Register

Table 3-20. Register Offset 20h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	0	0	1

Table 3-21. Bit Descriptions – Language ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	langIdLsb	RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8040 only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

3.3.11 Language ID MSB Register

Table 3-22. Register Offset 21h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0

Table 3-23. Bit Descriptions – Language ID LSB Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	langIdMsb	RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8040 only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

3.3.12 Serial Number String Length Register

Table 3-24. Register Offset 22h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	1	0	0	0

Table 3-25. Bit Descriptions – Serial Number String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RW	Serial number string length. The string length in bytes for the serial number string. The default value is 0, indicating that a serial number string is not supported. The maximum string length is 32 bytes. This field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers. If the string length in the Serial Number String Length Register is set to zero, the Manufacturing String Length and Product String Length must also be set to a length of zero.

3.3.13 Manufacturer String Length Register

Table 3-26. Register Offset 23h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-27. Bit Descriptions – Manufacturer String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. If the string length in the Serial Number String Length Register is set to zero, the Manufacturing String must also be set to a length of zero. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

3.3.14 Product String Length Register

Table 3-28. Register Offset 24h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-29. Bit Descriptions – Product String Length Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. If the string length in the Serial Number String Length Register is set to zero, the Product String must also be set to a length of zero. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

3.3.15 Serial Number Registers

Table 3-30. Register Offset 30h-4Fh

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	x	x	x	xx	x	x	x	x

Table 3-31. Bit Descriptions – Serial Number Byte N Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	serialNumber[n]	RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host. The same serial number will be returned in both the USB 2.0 and USB 3.0 descriptors of the TUSB8040.

3.3.16 Manufacturer String Registers

Table 3-32. Register Offset 50h-8Fh

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-33. Bit Descriptions – Manufacturer String Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	mfgStringByte[n]	RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

3.3.17 Product String Registers

Table 3-34. Register Offset 90h-CFh

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-35. Bit Descriptions – Product String Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:0	prodStringByte[n]	RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

3.3.18 Device Status and Command Register

Table 3-36. Register Offset F8h

BIT NO.	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 3-37. Bit Descriptions – Device Status and Command Register

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit resets the SMBus slave interface to its default state and loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect. (Not used with I^2C)
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8040 is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8040 does not connect on the upstream port while this bit is 1. When in I^2C mode, the bit is cleared by hardware when the TUSB8040 exits the I^2C mode. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

4 CLOCK GENERATION

The TUSB8040 accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below. Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

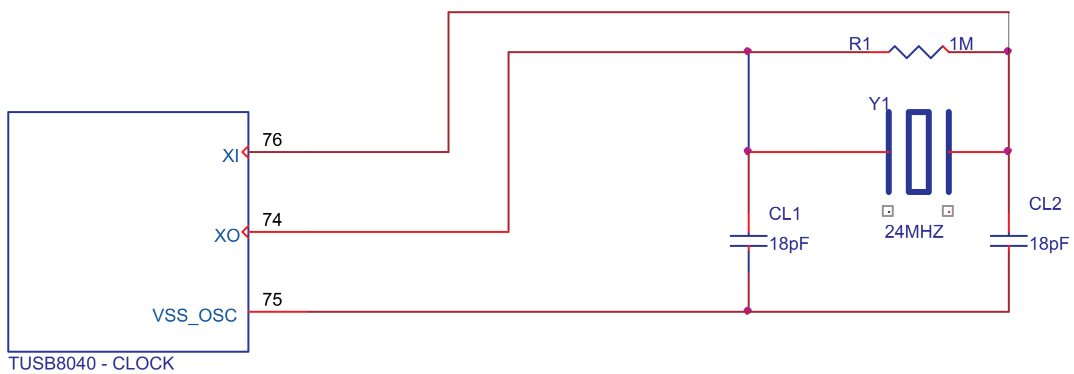


Figure 4-1. TUSB8040 Clock

4.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF - 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent se-ries resistance (ESR) of 50 Ω is recommended. A parallel, 18-pF load capacitor should be used if a crystal source is used. VSSOSC should not be connected to the PCB ground plane.

4.2 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating. VSSOSC should be connected to the PCB ground plane.

5 POWER UP AND RESET

The TUSB8040 does not have specific power sequencing requirements with respect to the core power (VDD11) or I/O and analog power (VDD33). The core power (VDD11) or I/O power (VDD33) may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

6 ELECTRICAL SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD33}	Supply voltage	-0.3 to 3.8	V
V_{DD11}		-0.3 to 1.4	
T_{stg}	Storage temperature range	-65 to 150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability

6.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD33}	Supply voltage	3	3.3	3.6	V
V_{DD11}		1.045	1.100	1.26	
T_A	Operating free-air temperature range	-40	25	85	°C
T_J	Operating junction temperature range	-40	25	105	°C

6.3 THERMAL INFORMATION

THERMAL METRIC		TUSB8040 PFP 80 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	24.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	21.5	
θ_{JB}	Junction-to-board thermal resistance(3)	8.37	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(5)	8.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	1.6	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.4 3.3-V I/O ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0	0.8	V
			JTAG pins only	0	0.55	
V_I	Input voltage			0	VDD33	V
V_O	Output voltage(2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.13 x VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33		±225	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers.

6.5 HUB INPUT SUPPLY CURRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER				CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	VDD11	1.1 V	US: SuperSpeed and high-speed, DS: 4 ports actively transmitting data at SuperSpeed	655	730	805	mA
				US: SuperSpeed and High-speed, DS: no DS connections	390	430	470	
				US: High-Speed, DS: 4 ports actively transmit-ting data at high-speed	395	435	475	
				US: High-Speed, DS: 4 ports connected at high-speed and idle	385	425	465	
				US: High-Speed (SUSPEND MODE), DS: no DS connections	370	410	450	
			1.2 V	US: SuperSpeed and high-speed, DS: 4 ports actively transmitting data at SuperSpeed	765	840	905	
				US: SuperSpeed and High-speed, DS: no DS connections	420	470	520	
				US: High-Speed, DS: 4 ports actively transmit-ting data at high-speed	430	480	530	
				US: High-Speed, DS: 4 ports connected at high-speed and idle	420	470	520	
				US: High-Speed (SUSPEND MODE), DS: no DS connections	405	450	495	
		VDD33		US: SuperSpeed and high-speed, DS: 4 ports actively transmitting data at SuperSpeed	105	120	135	mA
				US: SuperSpeed and High-speed, DS: no DS connections	105	120	135	
				US: High-Speed, DS: 4 ports actively transmit-ting data at high-speed	105	120	135	
				US: High-Speed, DS: 4 ports connected at high-speed and idle	105	120	135	
				US: High-Speed, DS: no DS connections	105	120	135	
				US: High-Speed (SUSPEND MODE), DS: no DS connections	55	60	65	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TUSB8040BRKMR	NRND	WQFN	RKM	100		TBD	Call TI	Call TI			
TUSB8040BRKMT	NRND	WQFN	RKM	100		TBD	Call TI	Call TI			
TUSB8040PFP	NRND	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	0 to 70	TUSB8040	
TUSB8040PFPR	NRND	HTQFP	PFP	80		TBD	Call TI	Call TI			
TUSB8040PFPT	NRND	HTQFP	PFP	80		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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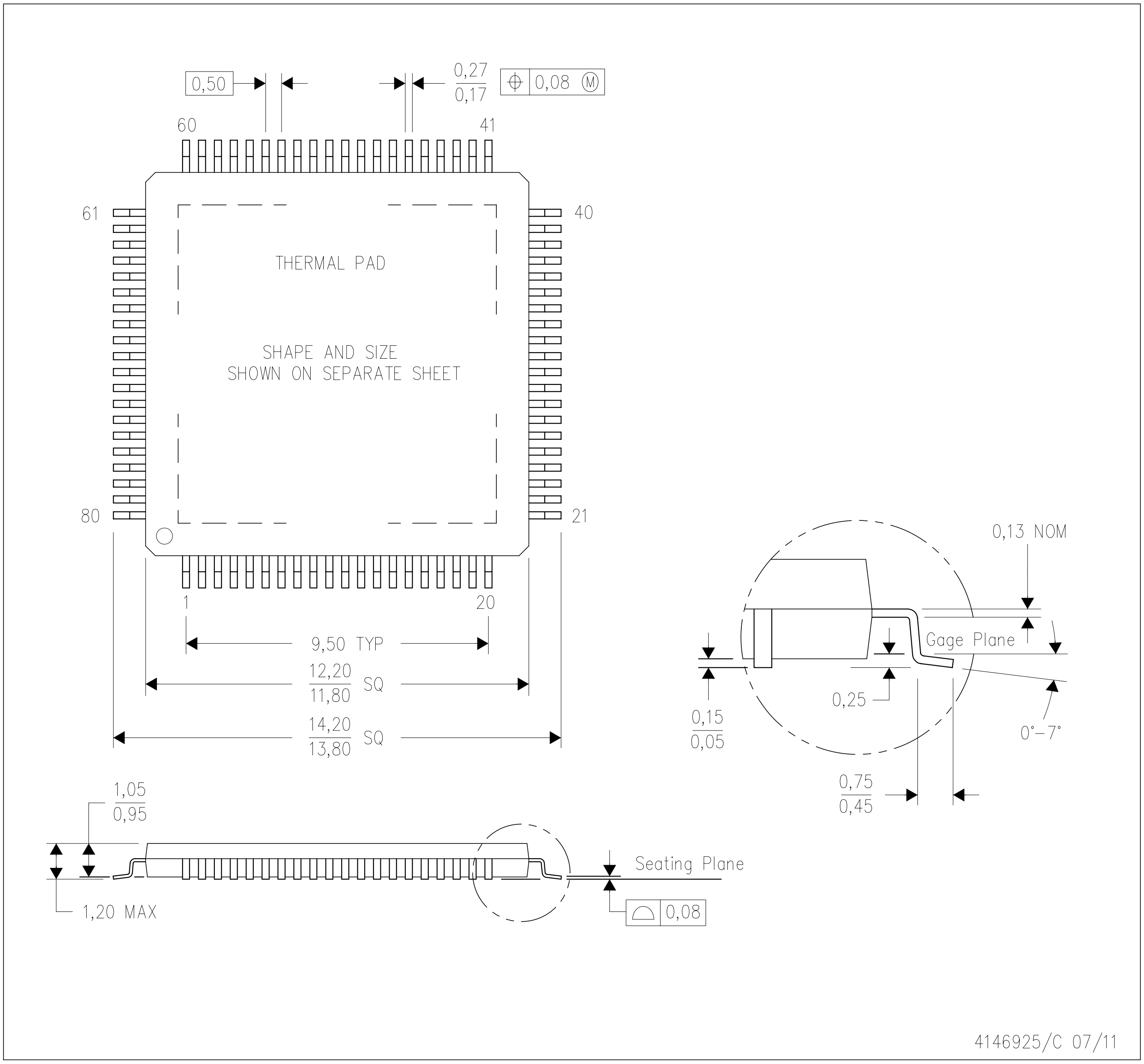
PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MS-026

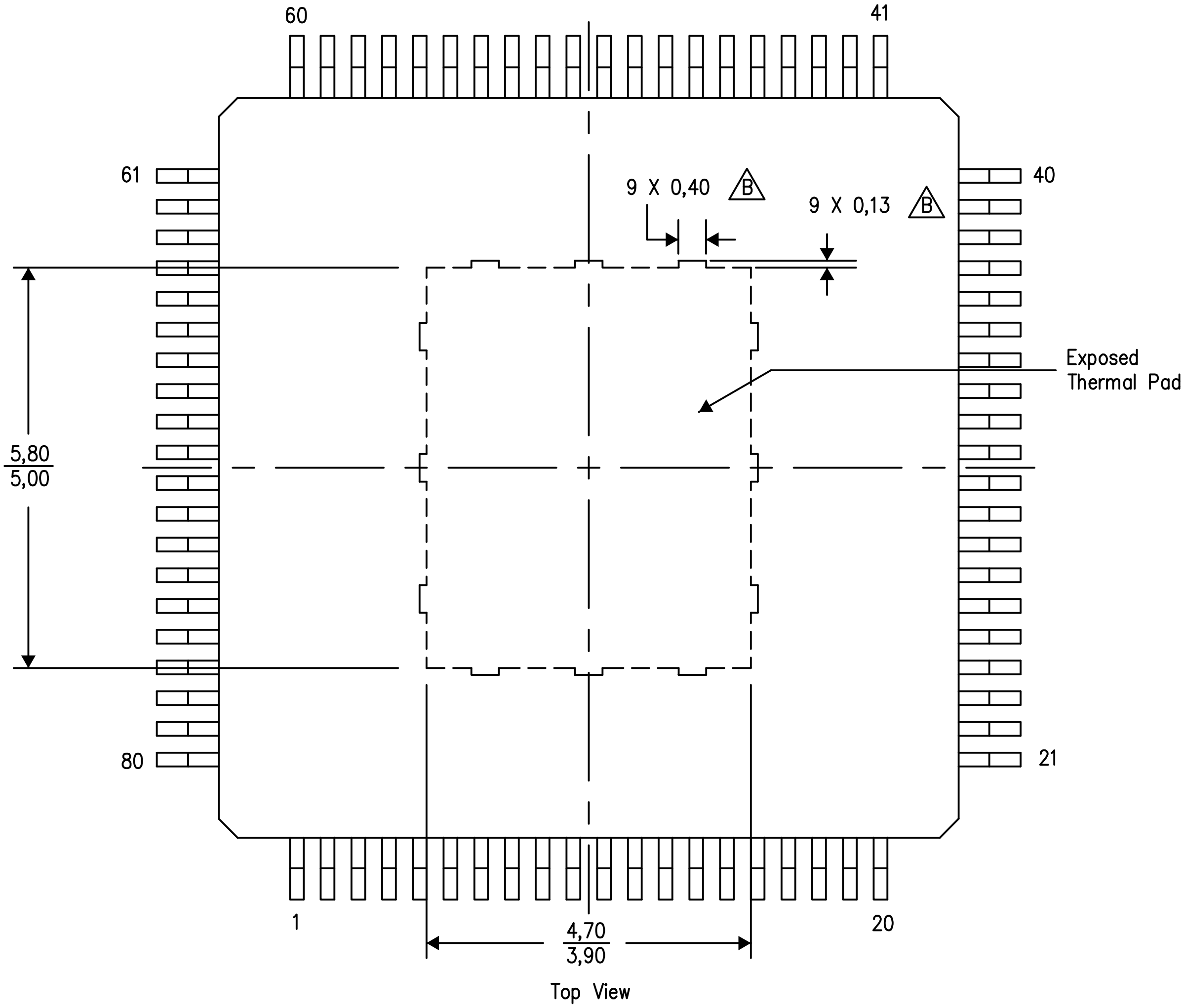
PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

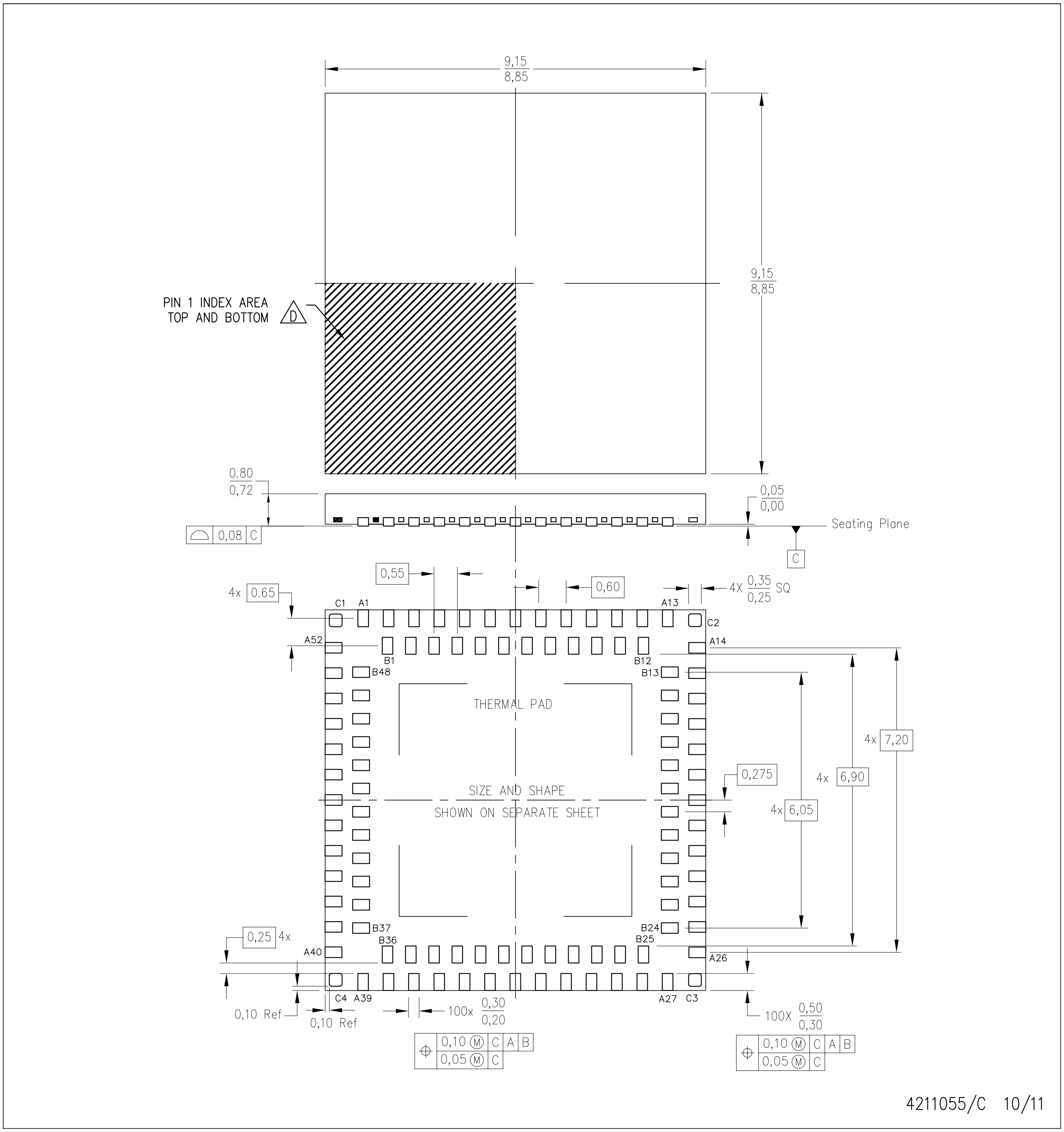
4206327-20/O 07/12

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) staggered multi–row package configuration.
D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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