

CLASS V 2x2 LVDS CROSSPOINT SWITCH

 Check for Samples: [SN55LVCP22-SP](#)

FEATURES

- High Speed (>1000 Mbps) Upgrade for DS90CP22 2x2 LVDS Crosspoint Switch
- Low-Jitter Fully Differential Data Path
- 50 ps (Typ), of Peak-to-Peak Jitter With PRBS = $2^{23}-1$ Pattern
- Less Than 200 mW (Typ), 300 mW (Max) Total Power Dissipation
- Output (Channel-to-Channel) Skew Is 80 ps (Typ)
- Configurable as 2:1 Mux, 1:2 Demux, Repeater or 1:2 Signal Splitter
- Inputs Accept LVDS, LVPECL, and CML Signals
- Fast Switch Time of 1.7 ns (Typ)
- Fast Propagation Delay of 0.65 ns (Typ)
- Available in 16 pin CFP Package
- Inter-Operates With TIA/EIA-644-A LVDS Standard
- Military Temperature Range: -55°C to 125°C

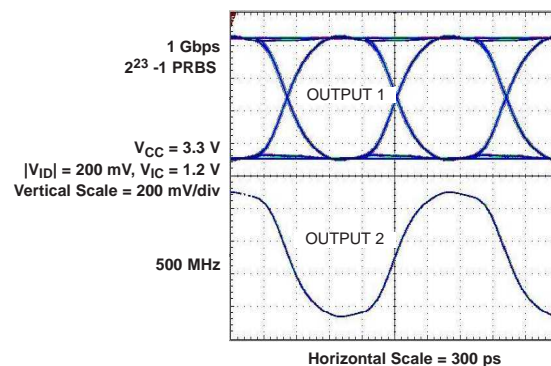
APPLICATIONS

- Base Stations
- Add/Drop Muxes
- Protection Switching for Serial Backplanes
- Network Switches/Routers
- Optical Networking Line Cards/Switches
- Clock Distribution

DESCRIPTION

The SN55LVCP22 is a 2x2 crosspoint switch providing greater than 1000 Mbps operation for each path. The dual channels incorporate wide common-mode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals. The dual outputs are LVDS drivers to provide low-power, low-EMI, high-speed operation. The SN55LVCP22 provides a single device supporting 2:2 buffering (repeating), 1:2 splitting, 2:1 multiplexing, 2x2 switching, and LVPECL/CML to LVDS level translation on each channel. The flexible operation of the SN55LVCP22 provides a single device to support the redundant serial bus transmission needs (working and protection switching cards) of fault-tolerant switch systems found in optical networking, wireless infrastructure, and data communications systems. TI offers additional gigabit repeater/ translator and crosspoint products in the SN65LVDS100 and SN65LVDS122.

The SN55LVCP22 uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter. Output channel-to-channel skew is 80 ps (typ) to ensure accurate alignment of outputs in all applications. Both SOIC and TSSOP package options are available to allow easy upgrade for existing solutions, and board area savings where space is critical.

OUTPUTS OPERATING SIMULTANEOUSLY


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

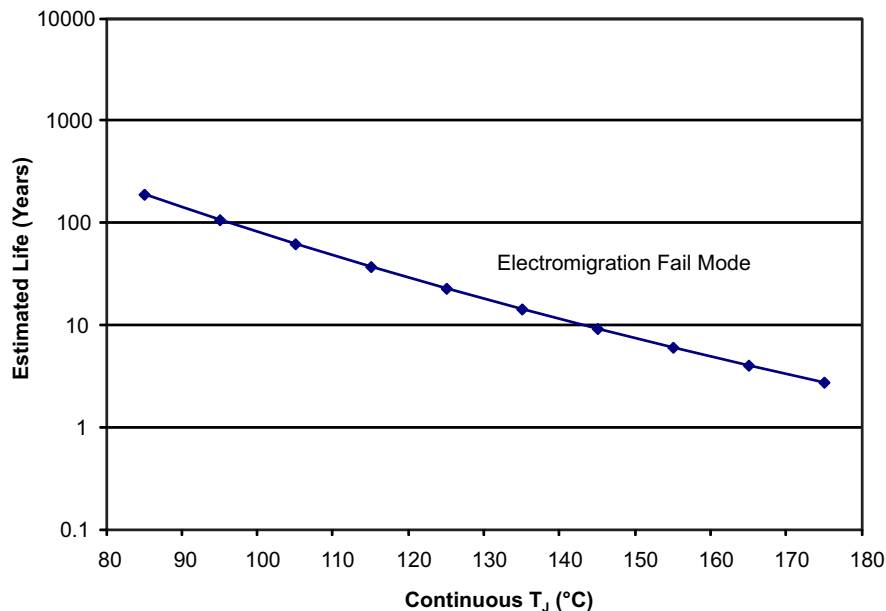
Table 1. PACKAGE/ORDERING INFORMATION⁽¹⁾

TEMPERATURE	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C T _{case}	16 / W	5962-1124201VFA	5962-1124201VFA LVCP22W-SP
25°C		SN55LVCP22WMPR	SN55LVCP22W/EM ⁽²⁾ EVAL ONLY

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. No Burn-In, etc.) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of -55°C to 125°C or operating life.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		VALUE	UNITS
θ_{JA}	Junction-to-ambient thermal resistance			82.5	°C/W
θ_{JC}	Junction-to-case thermal resistance			7.5	°C/W
P_D	Device power dissipation	Typical	$V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}, 1\text{ Gbps}$	198	mW
		Maximum	$V_{CC} = 3.6\text{ V}, T_A = 125^\circ\text{C}, 1\text{ Gbps}$	313	



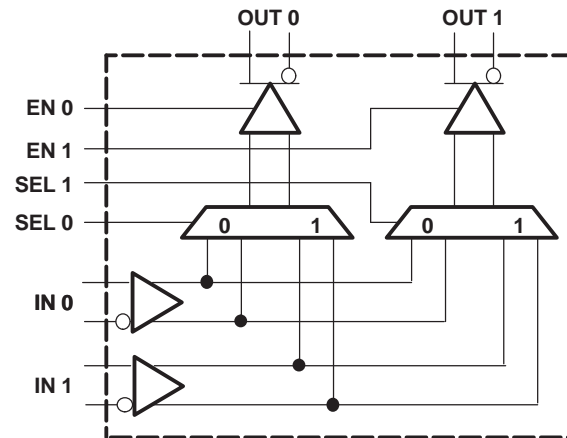
- A. See datasheet for absolute maximum and minimum recommended operating conditions.
- B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

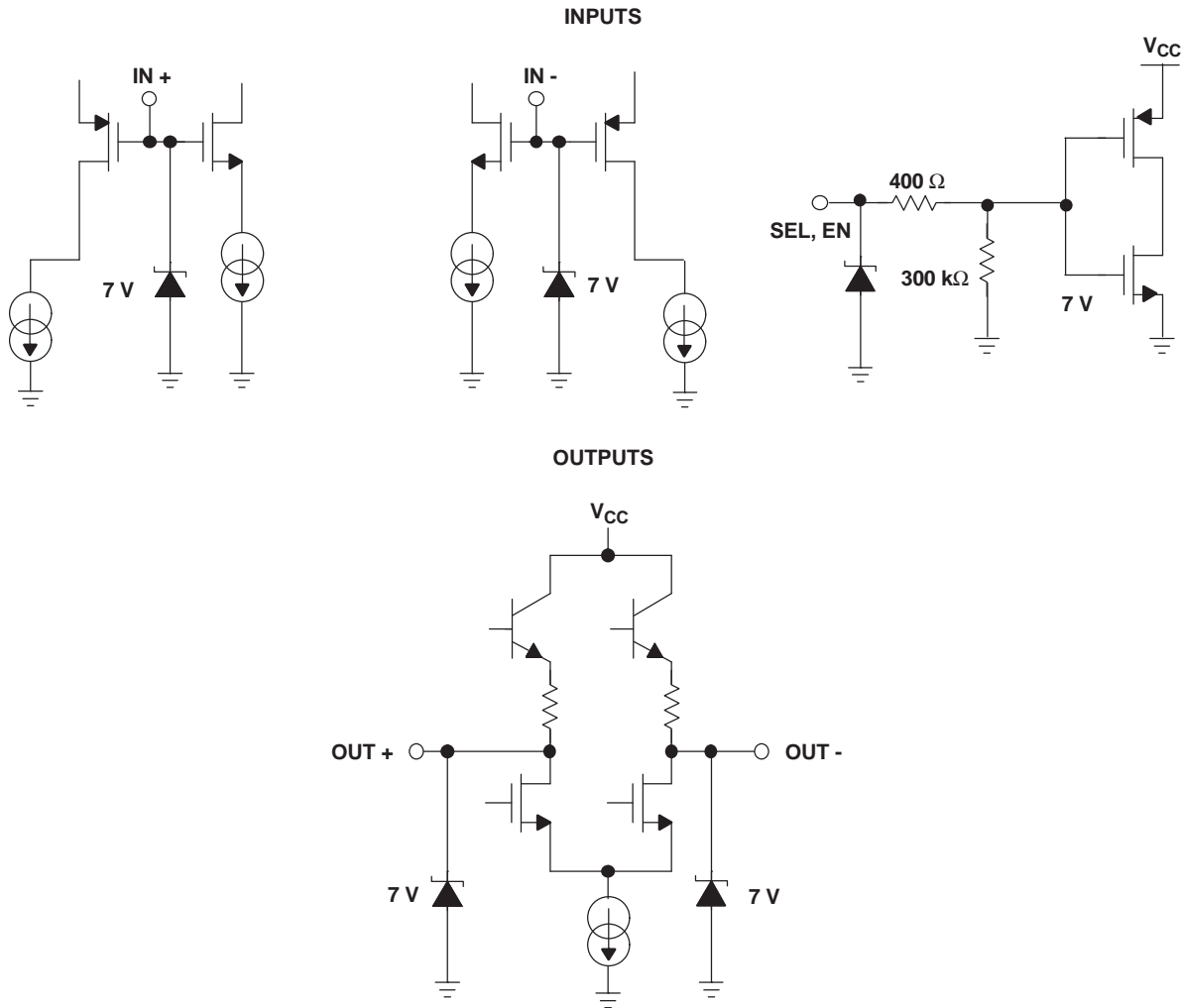
Figure 1. SN55LVCP22-SP Operating Life Derating Chart

Table 2. FUNCTION TABLE

SEL0	SEL1	OUT0	OUT1	FUNCTION
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

FUNCTIONAL BLOCK DIAGRAM



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range unless otherwise noted⁽¹⁾

		UNITS
Supply voltage ⁽²⁾ range, V_{CC}		–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)		–0.5 V to 4 V
LVDS receiver input voltage (IN+, IN–)		–0.7 V to 4.3 V
LVDS driver output voltage (OUT+, OUT–)		–0.5 V to 4 V
LVDS output short circuit current		Continuous
Storage temperature range		–65°C to 125°C
Maximum Junction temperature		150°C
Electrostatic discharge	Human body model ⁽³⁾	All pins ±5 kV
	Charged-device mode ⁽⁴⁾	All pins ±500 V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	0		4	V
Operating Case Temperature range, T_C ⁽¹⁾	-55		125	°C
Magnitude of differential input voltage $ V_{ID} $	0.1		3	V

(1) Maximum case temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)					
V_{IH} High-level input voltage		2		V_{CC}	V
V_{IL} Low-level input voltage		GND		0.8	V
I_{IH} High-level input current	$V_{IN} = 3.6\text{ V or }2.0\text{ V}, V_{CC} = 3.6\text{ V}$	-25	±3	25	µA
I_{IL} Low-level input current	$V_{IN} = 0.0\text{ V or }0.8\text{ V}, V_{CC} = 3.6\text{ V}$	-15	±1	15	µA
V_{CL} Input clamp voltage	$I_{CL} = -18\text{ mA}$		-0.8	-1.5	V
LVDS OUTPUT SPECIFICATIONS (OUT0, OUT1)					
$ V_{OD} $ Differential output voltage	$R_L = 75\ \Omega$, See Figure 3	255	365	475	mV
	$R_L = 75\ \Omega, V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$, See Figure 3	285	365	440	
$\Delta V_{OD} $ Change in differential output voltage magnitude between logic states	$V_{ID} = \pm 100\text{ mV}$, See Figure 3	-25		25	mV
V_{OS} Steady-state offset voltage	See Figure 4	1	1.2	1.45	V
ΔV_{OS} Change in steady-state offset voltage between logic states	See Figure 4	-25		25	mV
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage	See Figure 4		50		mV
I_{OZ} High-impedance output current	$V_{OUT} = \text{GND or } V_{CC}$	-15		15	µA
I_{OFF} Power-off leakage current	$V_{CC} = 0\text{ V}, 1.5\text{ V}; V_{OUT} = 3.6\text{ V or GND}$	-15		15	µA
I_{OS} Output short-circuit current	V_{OUT+} or $V_{OUT-} = 0\text{ V}$			-8	mA
I_{OSB} Both outputs short-circuit current	V_{OUT+} and $V_{OUT-} = 0\text{ V}$	-8		8	mA
C_O Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		3		pF
LVDS RECEIVER DC SPECIFICATIONS (IN0, IN1)					
V_{TH} Positive-going differential input voltage threshold	See Figure 2 and Table 3			100	mV
V_{TL} Negative-going differential input voltage threshold	See Figure 2 and Table 3	-100			mV
$V_{ID(HYS)}$ Differential input voltage hysteresis			25	150	mV
V_{CMR} Common-mode voltage range	$V_{ID} = 100\text{ mV}, V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.05		3.95	V
I_{IN} Input current	$V_{IN} = 4\text{ V}, V_{CC} = 3.6\text{ V or }0.0$	-18	±1	18	µA
	$V_{IN} = 0\text{ V}, V_{CC} = 3.6\text{ V or }0.0$	-18	±1	18	
C_{IN} Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		3		pF
SUPPLY CURRENT					
I_{CCQ} Quiescent supply current	$R_L = 75\ \Omega, \text{EN0}=\text{EN1}=\text{High}$		60	87	mA
I_{CCD} Total supply current	$R_L = 75\ \Omega, C_L = 5\text{ pF}, 500\text{ MHz (1000 Mbps)}, \text{EN0}=\text{EN1}=\text{High}$		63	87	mA
I_{CCZ} 3-state supply current	$\text{EN0} = \text{EN1} = \text{Low}$		25	35	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Input to SEL setup time	See Figure 7	2.2	0.8		ns
t_{HOLD}	Input to SEL hold time	See Figure 7	2.2	1.0		ns
t_{SWITCH}	SEL to switched output	See Figure 7		1.7	2.6	ns
t_{PHZ}	Disable time, high-level-to-high-impedance	See Figure 6		2	8	ns
t_{PLZ}	Disable time, low-level-to-high-impedance	See Figure 6		2	8	ns
t_{PZH}	Enable time, high-impedance -to-high-level output	See Figure 6		2	8	ns
t_{PZL}	Enable time, high-impedance-to-low-level output	See Figure 6		2	8	ns
t_{LHT}	Differential output signal rise time (20%-80%) ⁽¹⁾	$C_L = 5$ pF, See Figure 5		280	620	ps
t_{HLT}	Differential output signal fall time (20%-80%) ⁽¹⁾	$C_L = 5$ pF, See Figure 5		280	620	ps
t_{JIT}	Added peak-to-peak jitter	$V_{ID} = 200$ mV, 50% duty cycle, $V_{CM} = 1.2$ V, 500 MHz, $C_L = 5$ pF		20		ps
		$V_{ID} = 200$ mV, PRBS = 2 ²³⁻¹ data pattern, $V_{CM} = 1.2$ V at 1000 Mbps, $C_L = 5$ pF		50		ps
t_{Jrms}	Added random jitter (rms)	$V_{ID} = 200$ mV, 50% duty cycle, $V_{CM} = 1.2$ V at 500 MHz, $C_L = 5$ pF		1.1		ps _{RMS}
t_{PLHD}	Propagation delay time, low-to-high-level output ⁽¹⁾		200	650	2350	ps
t_{PHLD}	Propagation delay time, high-to-low-level output ⁽¹⁾		200	650	2350	ps
t_{skew} ⁽²⁾	Pulse skew ($ t_{PLHD} - t_{PHLD} $) ⁽³⁾	$C_L = 5$ pF, See Figure 5		45	160	ps
t_{CCS}	Output channel-to-channel skew, splitter mode	$C_L = 5$ pF, See Figure 5		80		ps
f_{MAX} ⁽²⁾	Maximum operating frequency ⁽⁴⁾		1			GHz

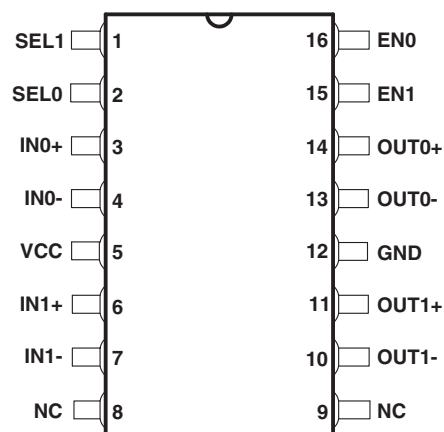
 (1) Input: $V_{IC} = 1.2$ V, $V_{ID} = 200$ mV, 50% duty cycle, 1 MHz, $t_r/t_f = 500$ ps

 (2) Pulse Skew and f_{MAX} parameters are guaranteed by characterization, but not production tested.

 (3) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.

 (4) Signal generator conditions: 50% duty cycle, t_r or $t_f \leq 100$ ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% $V_{OD} \geq 300$ mV.

PIN ASSIGNMENTS

 W PACKAGE
(TOP VIEW)


NC - No internal connection

PARAMETER MEASUREMENT INFORMATION

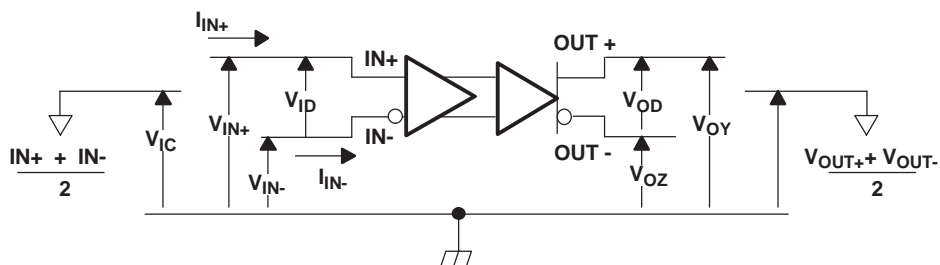


Figure 2. Voltage and Current Definitions

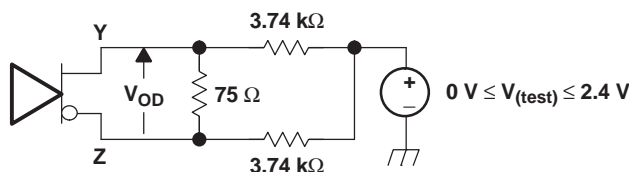
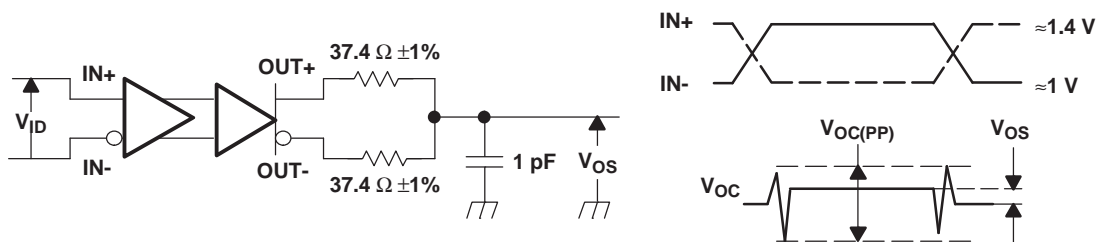


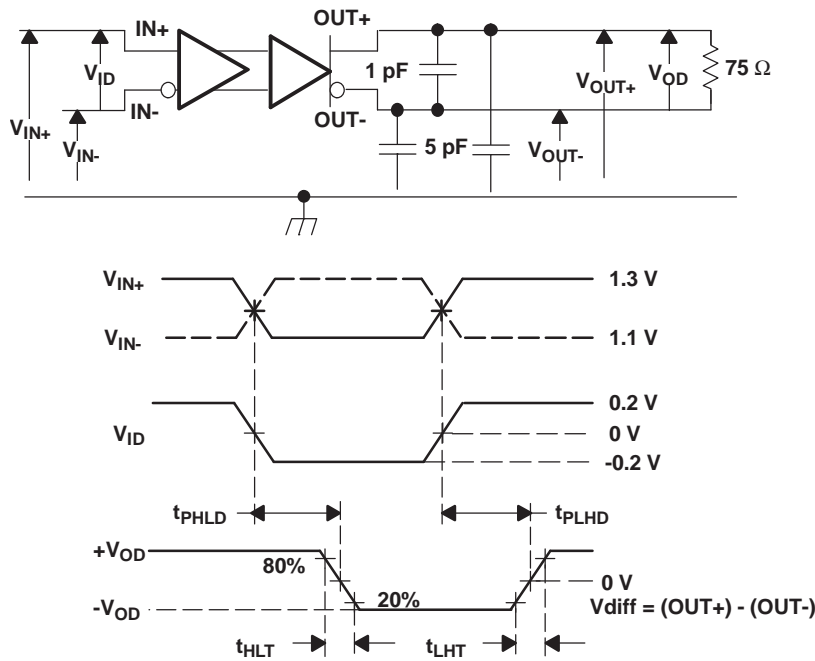
Figure 3. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns; $R_L = 100 \Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

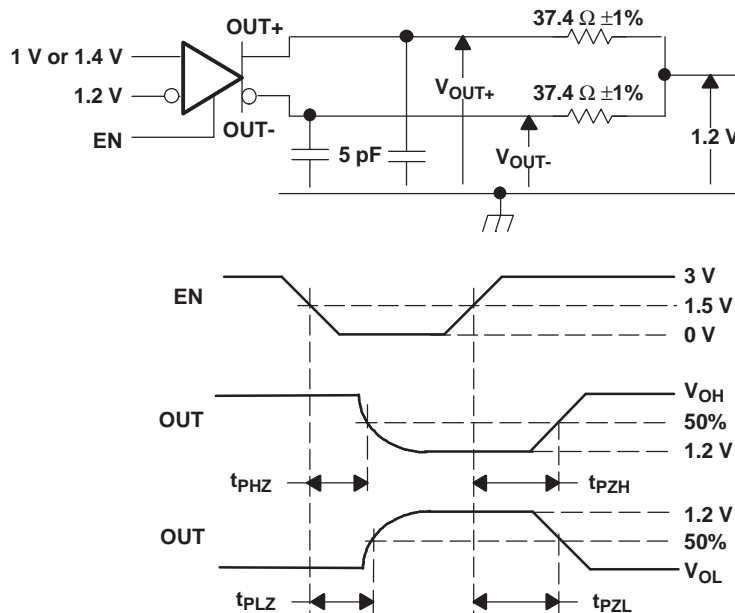
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Timing Test Circuit and Waveforms



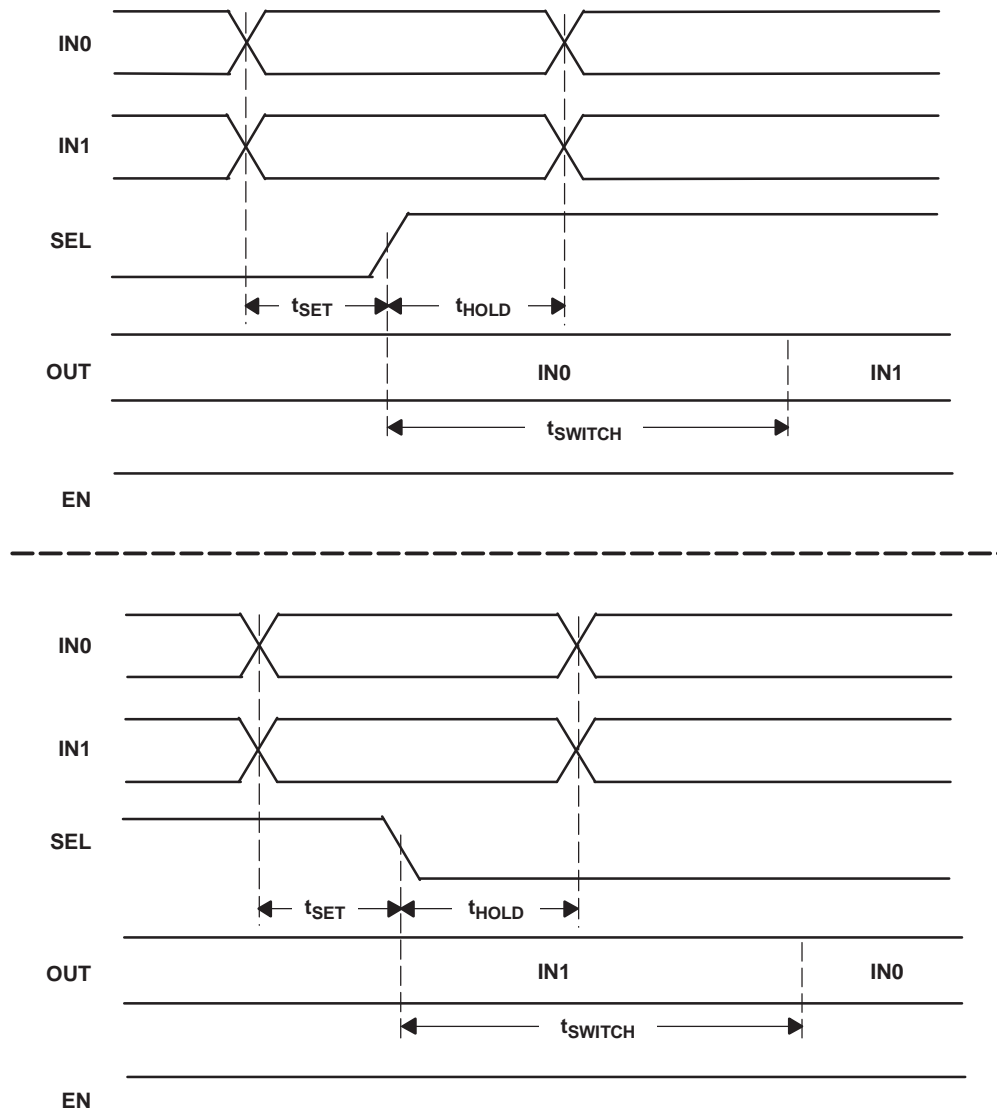
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 6. Enable and Disable Time Circuit and Definitions

Table 3. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	OUTPUT ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	-100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

(1) H = high level, L = low level



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

**DIFFERENTIAL OUTPUT VOLTAGE
vs
RESISTIVE LOAD**

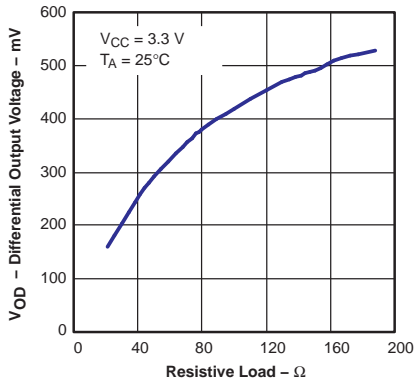


Figure 8.

**SUPPLY CURRENT
vs
FREQUENCY**

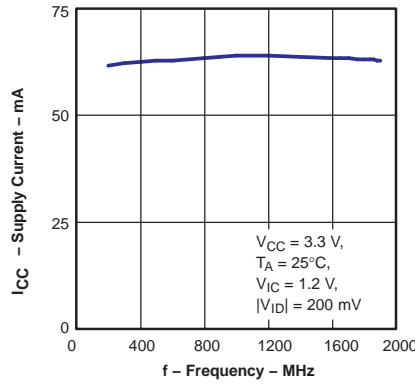


Figure 9.

**PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**

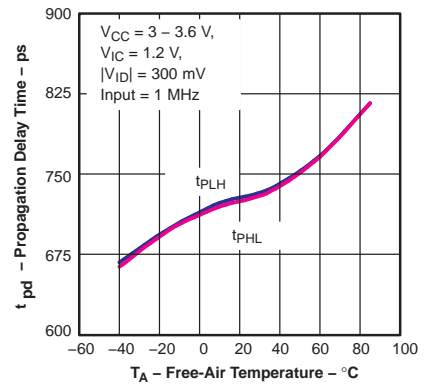


Figure 10.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

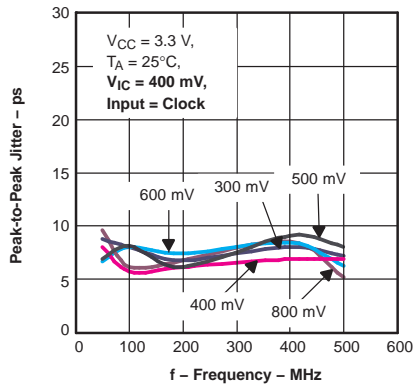


Figure 11.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

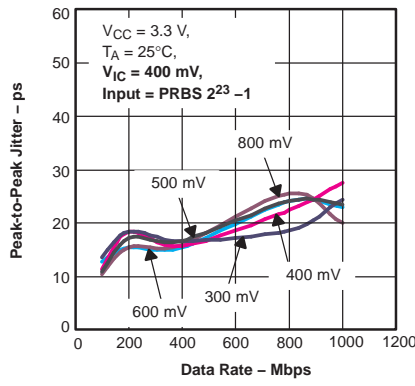


Figure 12.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

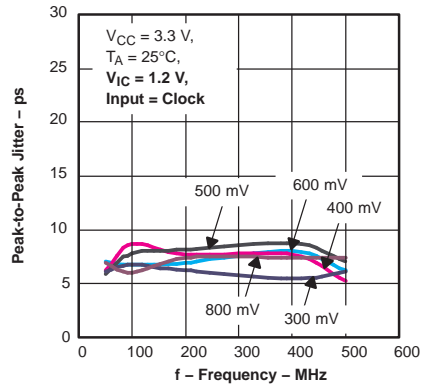


Figure 13.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

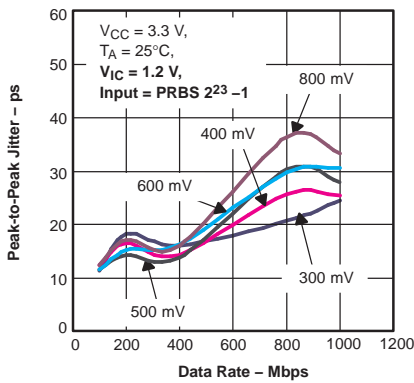


Figure 14.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

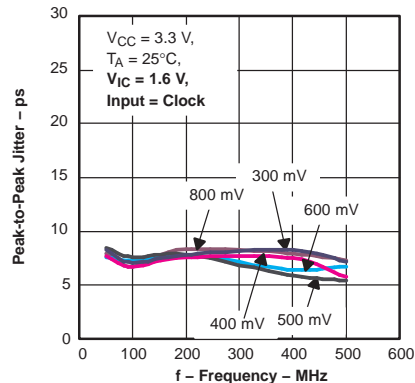


Figure 15.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

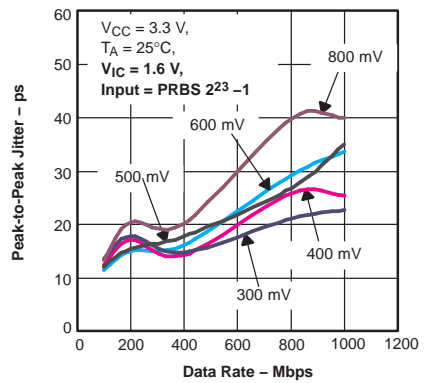


Figure 16.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK JITTER
vs
FREQUENCY

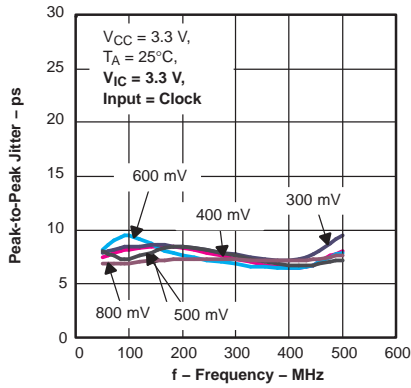


Figure 17.

PEAK-TO-PEAK JITTER
vs
DATA RATE

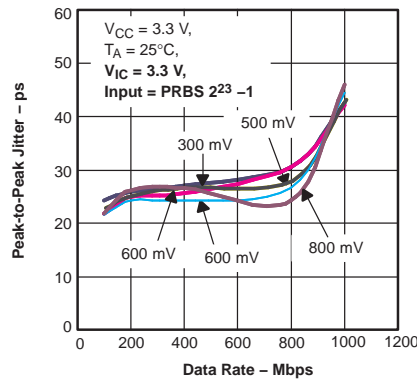


Figure 18.

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREQUENCY

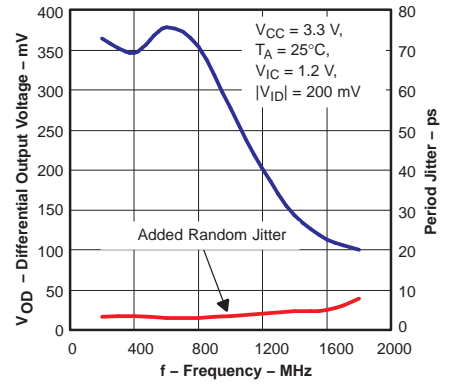


Figure 19.

PEAK-TO-PEAK JITTER
vs
DATA RATE

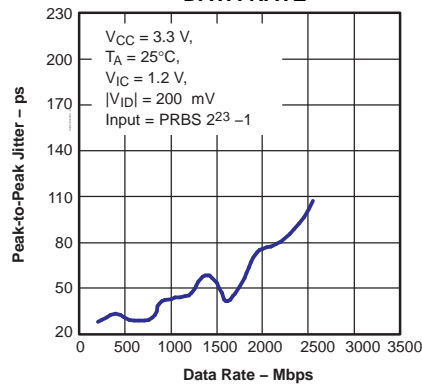


Figure 20.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

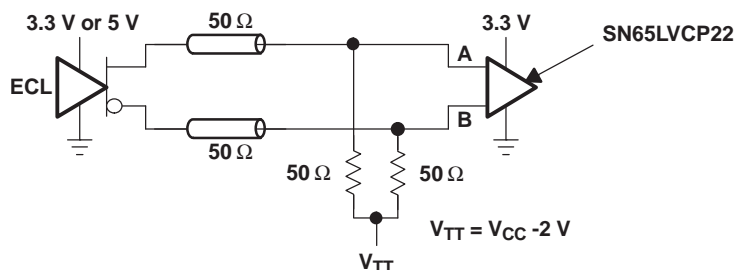


Figure 21. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

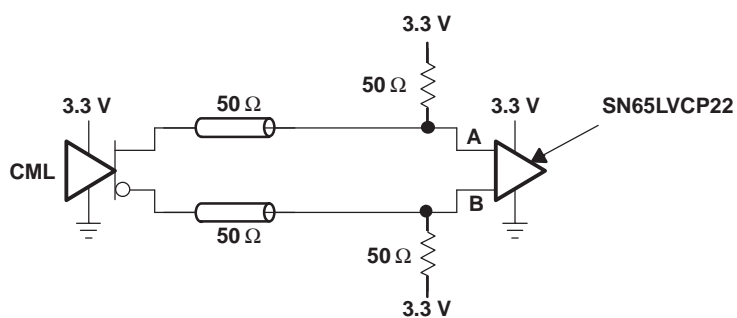


Figure 22. Current-Mode Logic (CML)

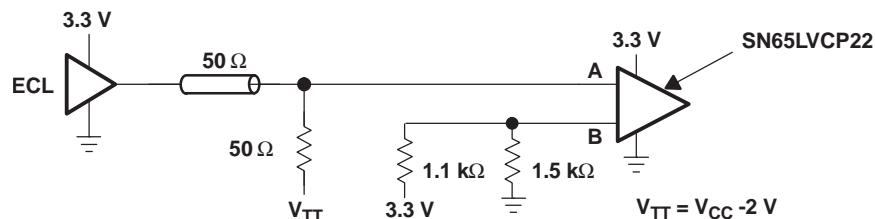


Figure 23. Single-Ended (LVPECL)

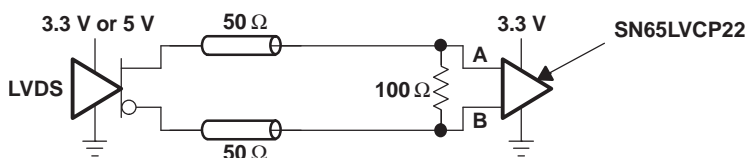


Figure 24. Low-Voltage Differential Signaling (LVDS)

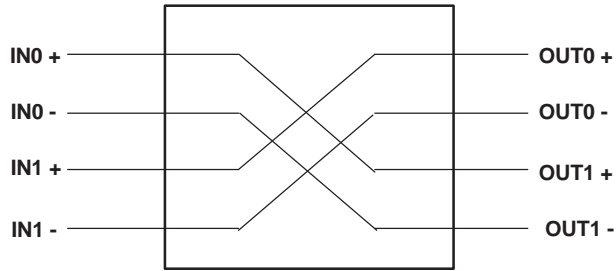


Figure 25. 2 x 2 Crosspoint

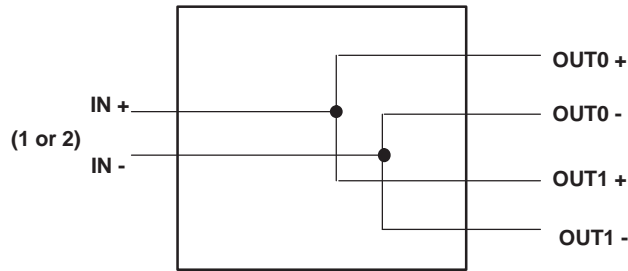


Figure 26. 1:2 Splitter



Figure 27. Dual Repeater

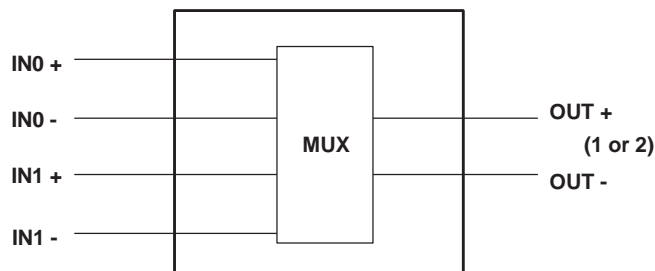


Figure 28. 2:1 MUX

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1124201VFA	ACTIVE	CFP	W	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-1124201VF A LVCP22W-SP	Samples
SN55LVCP22W/EM	PREVIEW	CFP	W	16		TBD	A42	N / A for Pkg Type	-55 to 125	SN55LVCP22W/EM EVAL ONLY	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com