



HIGH SPEED, TRIPLE DIGITAL ISOLATORS

Check for Samples: [ISO7230C-Q1](#), [ISO7231C-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 25 and 150-Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew
 - Low Pulse-Width Distortion (PWD)
 - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (See Application Note [SLLA197](#) and [Figure 14](#))
- 4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}
 - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IE 61010-1, IEC 60950-1 and CSA Approved
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (See Application Note [SLLA181](#))
- –40°C to 125°C Operating Range

DESCRIPTION

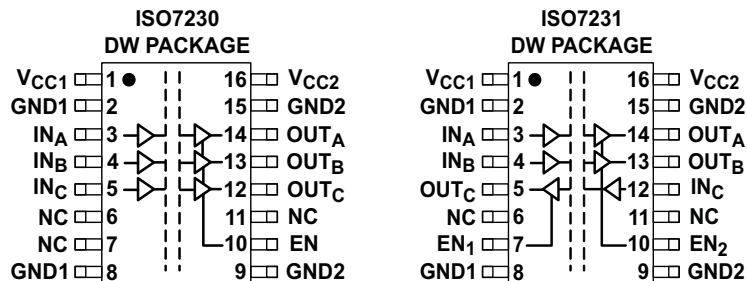
The ISO7230C-Q1 and ISO7231C-Q1 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO₂) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7230C-Q1 triple-channel device has all three channels in the same direction while the ISO7231C-Q1 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state.

The ISO7230C-Q1 and ISO7231C-Q1 have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

In each device, a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS. These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

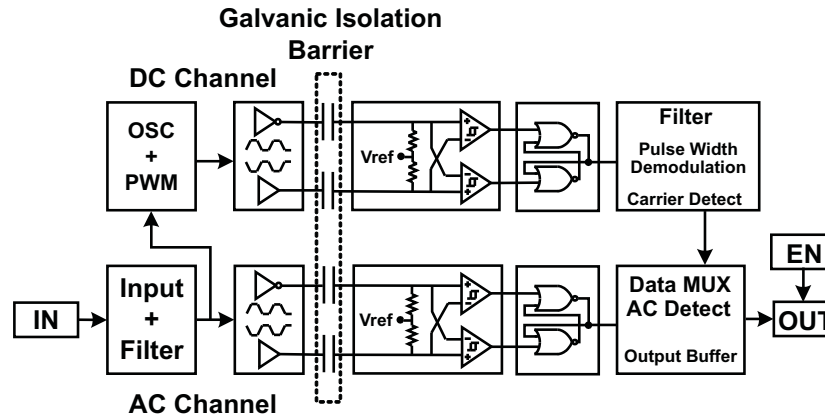


Table 1. Device Function Table ISO723xC-Q1 ⁽¹⁾

| INPUT V_{CC} | OUTPUT V_{CC} | INPUT (IN) | OUTPUT ENABLE (EN) | OUTPUT (OUT) |
|----------------|-----------------|------------|--------------------|--------------|
| PU | PU | H | H or Open | H |
| | | L | H or Open | L |
| | | X | L | Z |
| | | Open | H or Open | H |
| PD | PU | X | H or Open | H |
| PD | PU | X | L | Z |

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| -40°C to 125°C | SOIC - DW | Reel of 2000 | ISO7230CQDWRQ1 | PREVIEW |
| | | | ISO7231CQDWRQ1 | ISO7231CQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | VALUE | UNIT | | |
|-----------------|---|------------------------------------|----------|----|----|
| V _{CC} | Supply voltage ⁽²⁾ , V _{CC1} , V _{CC2} | -0.5 to 6 | V | | |
| V _I | Voltage at IN, OUT, EN | -0.5 to 6 | V | | |
| I _O | Output current | ±15 | mA | | |
| ESD | Electrostatic discharge | Human Body Model | All pins | ±4 | kV |
| | | Field-Induced-Charged Device Model | | ±1 | |
| | | Machine Model | ±200 | V | |
| T _J | Maximum junction temperature | 150 | °C | | |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|-------------------|---|------|-------------------|-----------------|------|
| V _{CC} | Supply voltage ⁽¹⁾ , V _{CC1} , V _{CC2} | 3.15 | | 5.5 | V |
| I _{OH} | High-level output current | -4 | | | mA |
| I _{OL} | Low-level output current | | | 4 | mA |
| t _{ui} | Input pulse width | 40 | | | ns |
| 1/t _{ui} | Signaling rate | 0 | 30 ⁽²⁾ | 25 | Mbps |
| V _{IH} | High-level input voltage (IN) (EN on all devices) | 2 | | V _{CC} | V |
| V _{IL} | Low-level input voltage (IN) (EN on all devices) | 0 | | 0.8 | |
| T _A | Operating free-air temperature | -40 | | 125 | °C |
| H | External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification | | | 1000 | A/m |

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
- (2) Typical signalling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------------------|--|---|----------------|-----|-----|-------------|
| SUPPLY CURRENT | | | | | | | |
| I_{CC1} | ISO7230C-Q1 | Quiescent | $V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V | 1 | | 3 | mA |
| | | 25 Mbps | | 7 | | 9.5 | |
| | ISO7231C-Q1 | Quiescent | $V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V | 6.5 | | 11 | mA |
| | | 25 Mbps | | 11 | | 17 | |
| I_{CC2} | ISO7230C-Q1 | Quiescent | $V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V | 15 | | 22 | mA |
| | | 25 Mbps | | 17 | | 24 | |
| | ISO7231C-Q1 | Quiescent | $V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V | 13 | | 20 | mA |
| | | 25 Mbps | | 17.5 | | 27 | |
| ELECTRICAL CHARACTERISTICS | | | | | | | |
| I_{OFF} | Sleep mode output current | EN at 0 V, Single channel | | 0 | | | μ A |
| V_{OH} | High-level output voltage | $I_{OH} = -4$ mA, See Figure 1 | | $V_{CC} - 0.8$ | | | V |
| | | $I_{OH} = -20$ μ A, See Figure 1 | | $V_{CC} - 0.1$ | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 4$ mA, See Figure 1 | | | | 0.4 | V |
| | | $I_{OL} = 20$ μ A, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | 150 | | | mV |
| I_{IH} | High-level input current | IN from 0 V to V_{CC} | | | | 10 | μ A |
| I_{IL} | Low-level input current | | | -10 | | | |
| C_1 | Input capacitance to ground | IN at V_{CC} , $V_1 = 0.4 \sin(4E6\pi t)$ | | 2 | | | pF |
| CMTI | Common-mode transient immunity | $V_1 = V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/ μ s |

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|------------------------------|-----|-----|-----|---------|
| t_{PLH} , t_{PHL} | Propagation delay | See Figure 1 | 18 | | 45 | ns |
| PWD | Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | | 5 | |
| $t_{sk(pp)}$ | Part-to-part skew ⁽²⁾ | | | | 8 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew ⁽³⁾ | | 0 | | 4 | ns |
| t_r | Output signal rise time | See Figure 1 | | | 2 | ns |
| t_f | Output signal fall time | | | | 2 | |
| t_{PHZ} | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | | 15 | ns |
| t_{PZH} | Propagation delay, high-impedance-to-high-level output | | | | 25 | |
| t_{PLZ} | Propagation delay, low-level-to-high-impedance output | | | | 15 | |
| t_{PZL} | Propagation delay, high-impedance-to-low-level output | | | | 25 | |
| t_{fs} | Failsafe output delay time from input power loss | See Figure 3 | | | 12 | μ s |

- (1) Also referred to as pulse skew.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------------------|--|--|----------------|------|-----|-------------|
| SUPPLY CURRENT | | | | | | | |
| I_{CC1} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V | | 1 | 3 | mA |
| | | 25 Mbps | | | 7 | 9.5 | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V | | 6.5 | 11 | mA |
| | | 25 Mbps | | | 11 | 17 | |
| I_{CC2} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V | | 9 | 15 | mA |
| | | 25 Mbps | | | 10 | 17 | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V | | 8 | 12 | mA |
| | | 25 Mbps | | | 10.5 | 16 | |
| ELECTRICAL CHARACTERISTICS | | | | | | | |
| I_{OFF} | Sleep mode output current | EN at 0 V, Single channel | | | 0 | | μ A |
| V_{OH} | High-level output voltage | $I_{OH} = -4$ mA, See Figure 1 | ISO7230C-Q1 | $V_{CC} - 0.4$ | | | V |
| | | | ISO7231C-Q1 (5-V side) | $V_{CC} - 0.8$ | | | |
| | | $I_{OH} = -20$ μ A, See Figure 1 | $V_{CC} - 0.1$ | | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 4$ mA, See Figure 1 | | | 0.4 | | V |
| | | $I_{OL} = 20$ μ A, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | 150 | | mV |
| I_{IH} | High-level input current | IN from 0 V to V_{CC} | | | | 10 | μ A |
| I_{IL} | Low-level input current | | | | | -10 | |
| C_I | Input capacitance to ground | IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$ | | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See Figure 4 | | | 25 | 50 | kV/ μ s |

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|------------------------------|-----|-----|-----|---------|
| t_{PLH} , t_{PHL} | Propagation delay, low-to-high-level output | See Figure 1 | 20 | | 50 | ns |
| PWD | Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | | 4 | |
| $t_{sk(pp)}$ | Part-to-part skew ⁽²⁾ | | | | 10 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew ⁽³⁾ | | | 0 | 4 | ns |
| t_r | Output signal rise time | See Figure 1 | | 2 | | ns |
| t_f | Output signal fall time | | | 2 | | |
| t_{PHZ} | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 25 | ns |
| t_{PZH} | Propagation delay, high-impedance-to-high-level output | | | 15 | 25 | |
| t_{PLZ} | Propagation delay, low-level-to-high-impedance output | | | 15 | 25 | |
| t_{PZL} | Propagation delay, high-impedance-to-low-level output | | | 15 | 25 | |
| t_{fs} | Failsafe output delay time from input power loss | See Figure 3 | | 18 | | μ s |

(1) Also known as pulse skew

 (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

 (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------------------|--|--|----------------|-----|-----|-------------|
| SUPPLY CURRENT | | | | | | | |
| I_{CC1} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V | 0.5 | | 1 | mA |
| | | 25 Mbps | | 3 | | 5 | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V | 4.5 | | 7 | mA |
| | | 25 Mbps | | 6.5 | | 11 | |
| I_{CC2} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V | 15 | | 22 | mA |
| | | 25 Mbps | | 17 | | 24 | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V | 13 | | 20 | mA |
| | | 25 Mbps | | 17.5 | | 27 | |
| ELECTRICAL CHARACTERISTICS | | | | | | | |
| I_{OFF} | Sleep mode output current | EN at 0 V, Single channel | | 0 | | | μ A |
| V_{OH} | High-level output voltage | $I_{OH} = -4$ mA, See Figure 1 | ISO7230C-Q1 | $V_{CC} - 0.4$ | | | V |
| | | | ISO7231C-Q1 (5-V side) | $V_{CC} - 0.8$ | | | |
| | | $I_{OH} = -20$ μ A, See Figure 1 | $V_{CC} - 0.1$ | | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 4$ mA, See Figure 1 | | 0.4 | | | V |
| | | $I_{OL} = 20$ μ A, See Figure 1 | | 0.1 | | | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | 150 | | | mV |
| I_{IH} | High-level input current | IN from 0 V to V_{CC} | | 10 | | | μ A |
| I_{IL} | Low-level input current | | | -10 | | | |
| C_I | Input capacitance to ground | IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$ | | 2 | | | pF |
| CMTI | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/ μ s |

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----|-----|-----|---------|
| t_{PLH} , t_{PHL} | Propagation delay | See Figure 1 | 20 | | 51 | ns |
| PWD | Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | | 4 | |
| $t_{sk(pp)}$ | Part-to-part skew ⁽²⁾ | | | | 10 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew ⁽³⁾ | | | 0 | 4 | ns |
| t_r | Output signal rise time | See Figure 1 | | 2 | | ns |
| t_f | Output signal fall time | | | 2 | | |
| t_{PHZ} | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 25 | ns |
| t_{PZH} | Propagation delay, high-impedance-to-high-level output | | | 15 | 25 | |
| t_{PLZ} | Propagation delay, low-level-to-high-impedance output | | | 15 | 25 | |
| t_{PZL} | Propagation delay, high-impedance-to-low-level output | | | 15 | 25 | |
| t_{fs} | Failsafe output delay time from input power loss | See Figure 3 | | 12 | | μ s |

(1) Also known as pulse skew

 (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

 (3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V⁽¹⁾ OPERATION

, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------------------|--------------------------------|--|---|----------------|-----|-----|-------------|
| SUPPLY CURRENT | | | | | | | |
| I_{CC1} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V | 0.5 | 1 | | mA |
| | | 25 Mbps | | 3 | 5 | | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V | 4.5 | 7 | | mA |
| | | 25 Mbps | | 6.5 | 11 | | |
| I_{CC2} | ISO7230C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V | 9 | 15 | | mA |
| | | 25 Mbps | | 10 | 17 | | |
| | ISO7231C-Q1 | Quiescent | $V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V | 8 | 12 | | mA |
| | | 25 Mbps | | 10.5 | 16 | | |
| ELECTRICAL CHARACTERISTICS | | | | | | | |
| I_{OFF} | Sleep mode output current | EN at 0 V, single channel | | 0 | | | μ A |
| V_{OH} | High-level output voltage | $I_{OH} = -4$ mA, See Figure 1 | | $V_{CC} - 0.4$ | | | V |
| | | $I_{OH} = -20$ μ A, See Figure 1 | | $V_{CC} - 0.1$ | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 4$ mA, See Figure 1 | | 0.4 | | | V |
| | | $I_{OL} = 20$ μ A, See Figure 1 | | 0.1 | | | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | 150 | | | mV |
| I_{IH} | High-level input current | IN from 0 V or V_{CC} | | 10 | | | μ A |
| I_{IL} | Low-level input current | | | -10 | | | |
| C_I | Input capacitance to ground | IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$ | | 2 | | | pF |
| CMTI | Common-mode transient immunity | $V_I = V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/ μ s |

- (1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

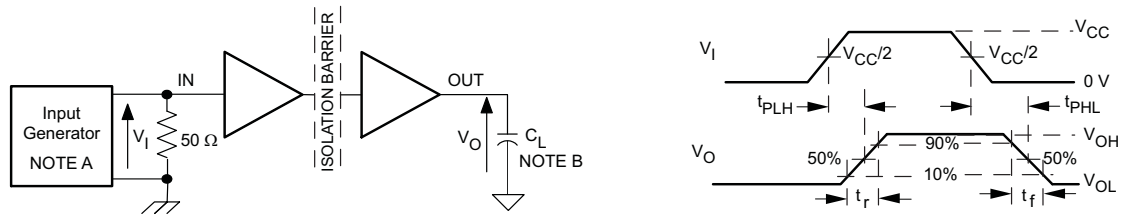
over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|------------------------------|-----|-----|-----|---------|
| t_{PLH} , t_{PHL} | Propagation delay | See Figure 1 | 25 | | 56 | ns |
| PWD | Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $ | | | | 4 | |
| $t_{sk(pp)}$ | Part-to-part skew ⁽²⁾ | | | | 10 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew | | | 0 | 4 | ns |
| t_r | Output signal rise time | See Figure 1 | | 2 | | ns |
| t_f | Output signal fall time | | | 2 | | |
| t_{PHZ} | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 25 | ns |
| t_{PZH} | Propagation delay, high-impedance-to-high-level output | | | 15 | 25 | |
| t_{PLZ} | Propagation delay, low-level-to-high-impedance output | | | 15 | 25 | |
| t_{PZL} | Propagation delay, high-impedance-to-low-level output | | | 15 | 25 | |
| t_{fs} | Failsafe output delay time from input power loss | See Figure 3 | | 18 | | μ s |

(1) Also referred to as pulse skew.

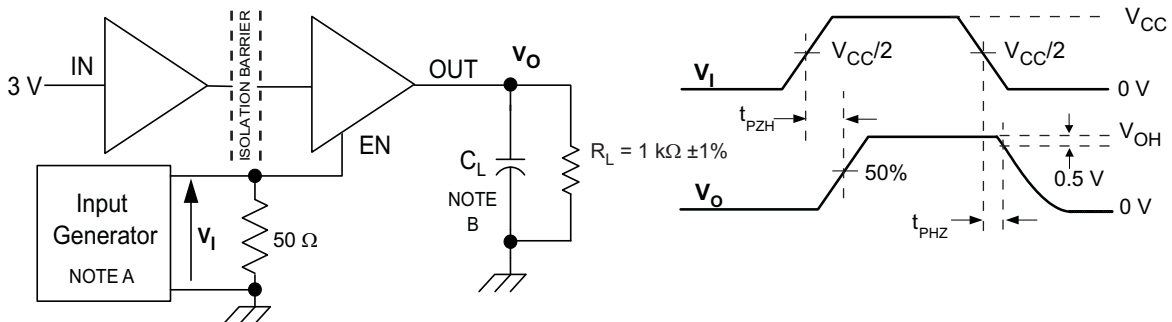
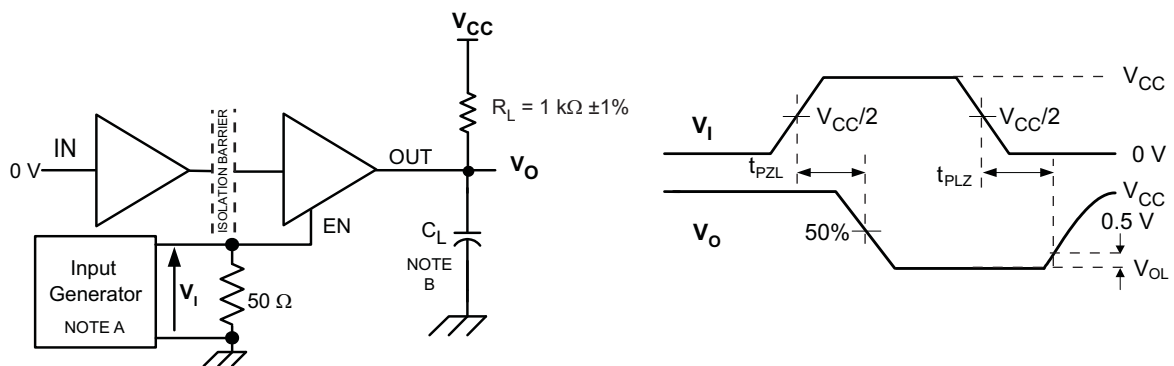
 (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

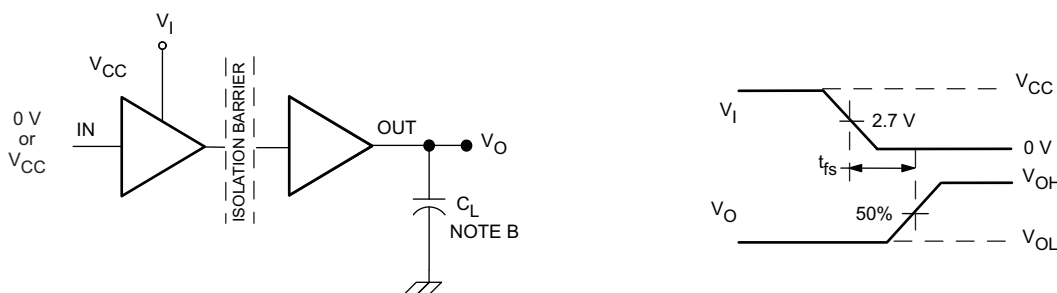
Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

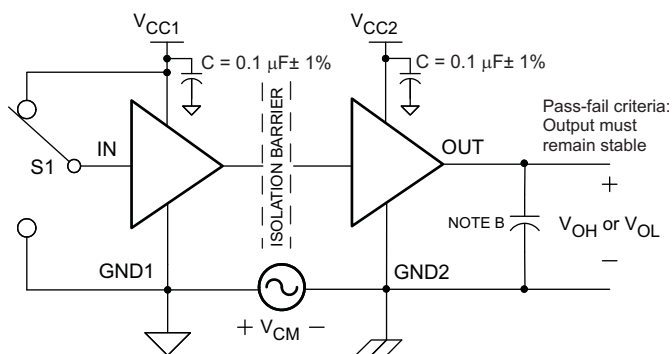
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



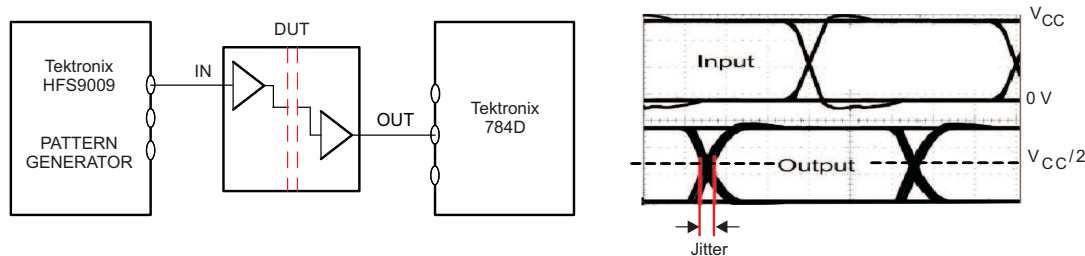
- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Pek Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

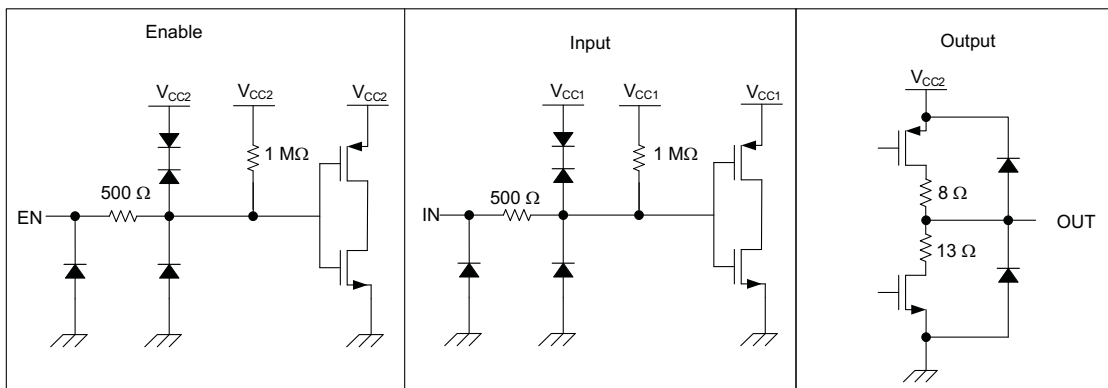
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-------|-------------------|-----|------|
| L(I01) Minimum air gap (Clearance) | Shortest terminal-to-terminal distance through air | 8.34 | | | mm |
| L(I02) Minimum external tracking (Creepage) | Shortest terminal-to-terminal distance across the package surface | 8.1 | | | mm |
| Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| R _{IO} Isolation resistance | Input to output, V _{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T _A < 100°C | | >10 ¹² | | Ω |
| | Input to output, V _{IO} = 500 V, 100°C ≤ T _A ≤ T _A max | | >10 ¹¹ | | Ω |
| C _{IO} Barrier capacitance Input to output | V _I = 0.4 sin (4E6πt) | | 2 | | pF |
| C _I Input capacitance to ground | V _I = 0.4 sin (4E6πt) | | 2 | | pF |

REGULATORY INFORMATION

| VDE | CSA | UL |
|--------------------------------------|--|--|
| Certified according to IEC 60747-5-2 | Approved under CSA Component Acceptance Notice | Recognized under 1577 Component Recognition Program ⁽¹⁾ |
| File Number: 40016131 | File Number: 220991 | File Number: E181974 |

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



NOTE: Input is assumed to be on V_{CC1} side and Output on V_{CC2} side.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|------|-----|------|
| θ _{JA} Junction-to-air | Low-K Thermal Resistance ⁽¹⁾ | | 168 | | °C/W |
| | High-K Thermal Resistance | | 96.1 | | |
| θ _{JB} Junction-to-Board Thermal Resistance | | | 61 | | °C/W |
| θ _{JC} Junction-to-Case Thermal Resistance | | | 48 | | °C/W |
| P _D Device Power Dissipation | V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 50% duty cycle square wave | | | 220 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

ISO7230 C/M RMS SUPPLY CURRENT
vs
SIGNALING RATE

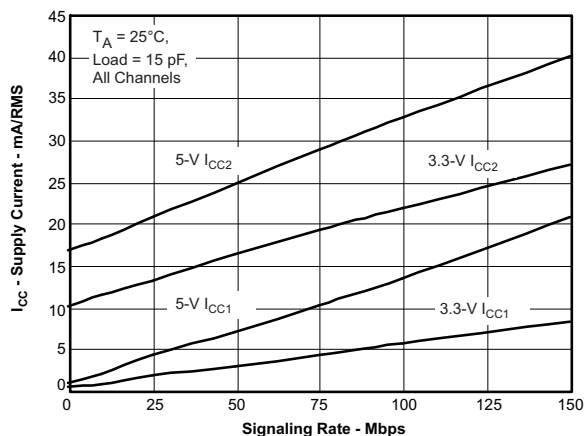


Figure 6.

ISO7231 C/M RMS SUPPLY CURRENT
vs
SIGNALING RATE

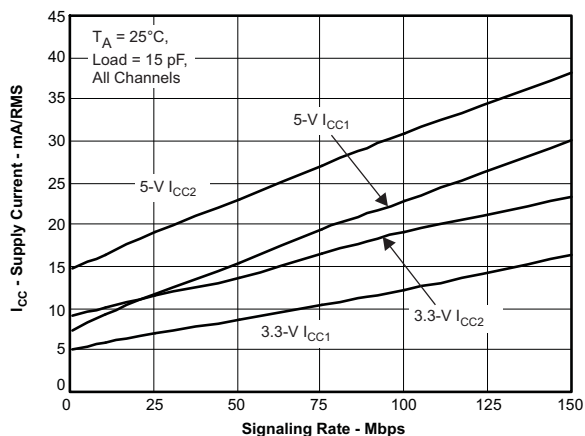


Figure 7.

PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

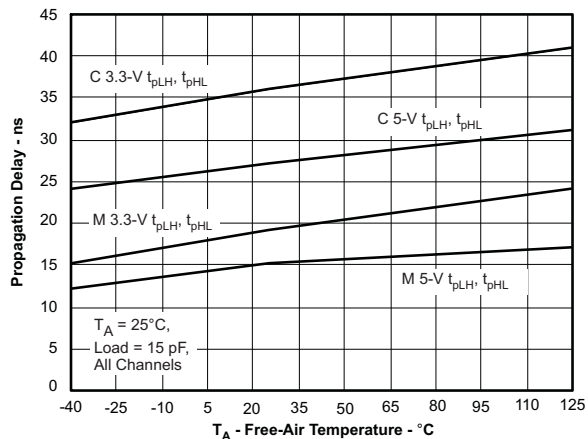


Figure 8.

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

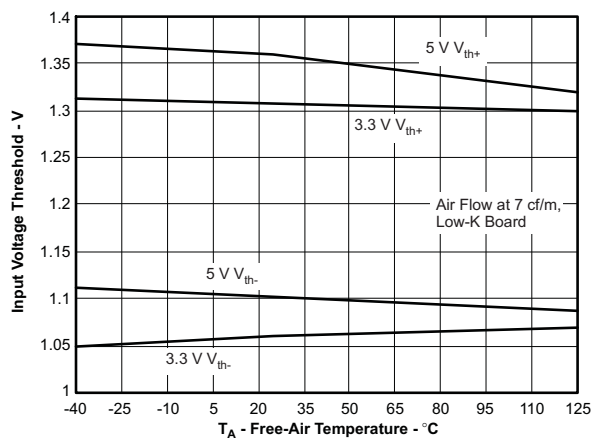


Figure 9.

TYPICAL CHARACTERISTIC CURVES (continued)

**V_{CC1} FAILSAFE THRESHOLD
vs
FREE-AIR TEMPERATURE**

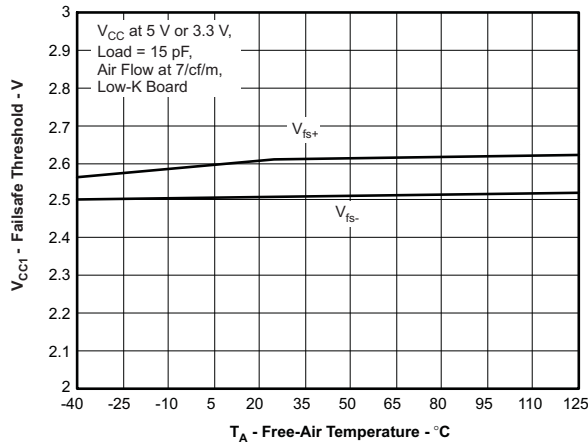


Figure 10.

**HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE**

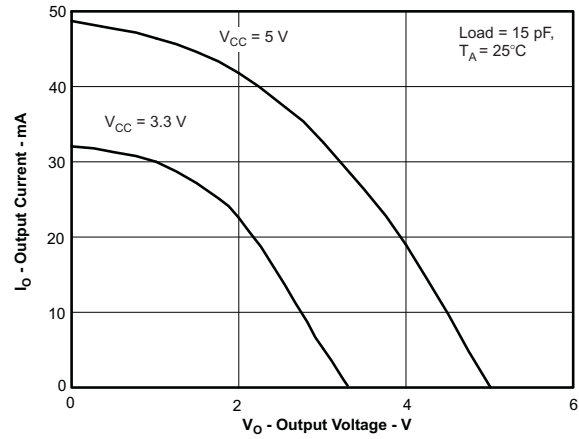


Figure 11.

**LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE**

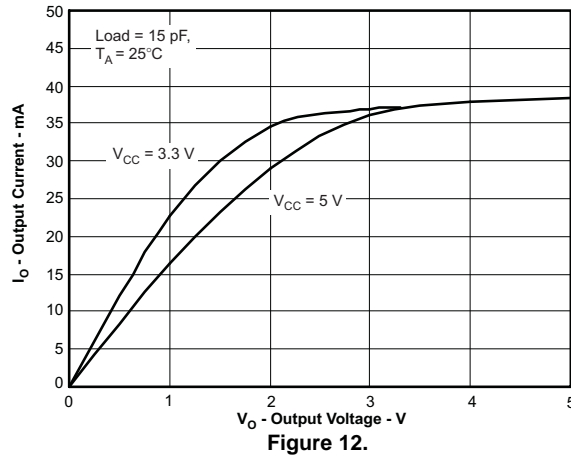


Figure 12.

APPLICATION INFORMATION

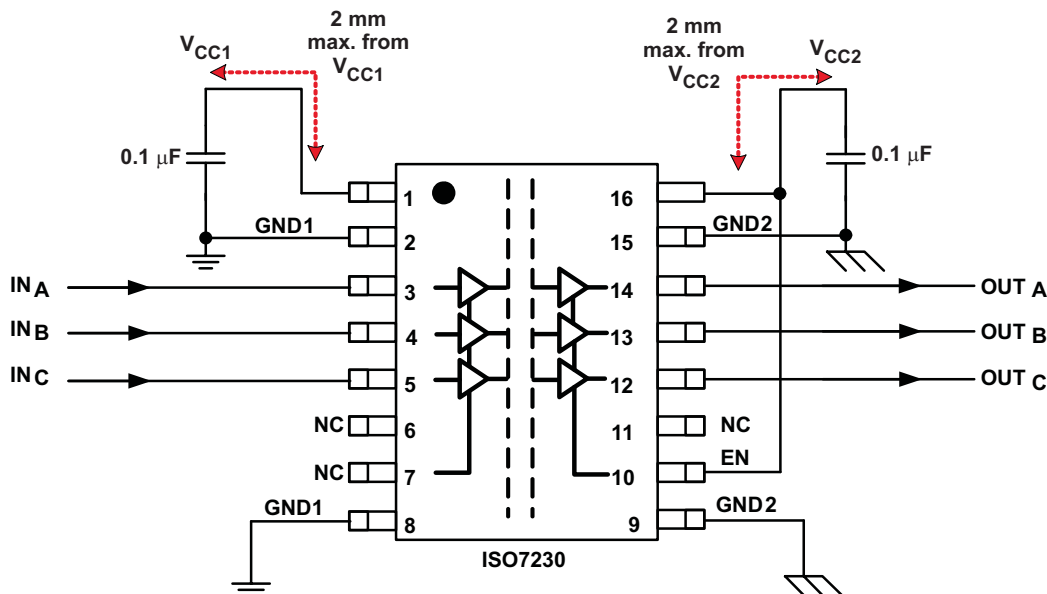


Figure 13. Typical ISO7230 Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

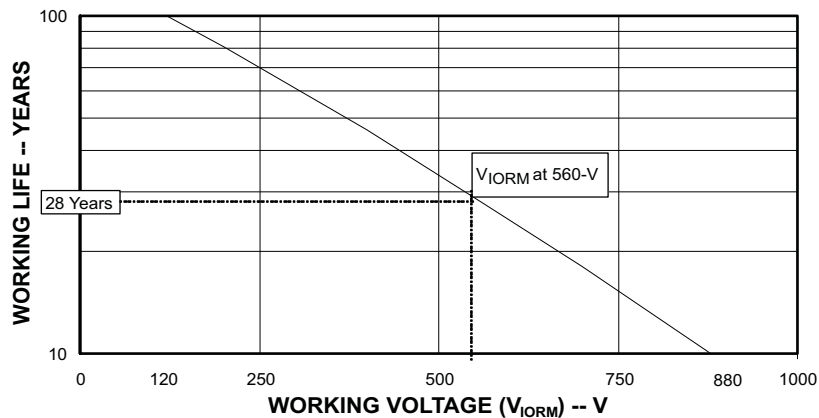


Figure 14. Time Dependant Dielectric Breakdown Testing Results

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| ISO7231CQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7231CQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO7231C-Q1 :

- Catalog: [ISO7231C](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO7231CQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

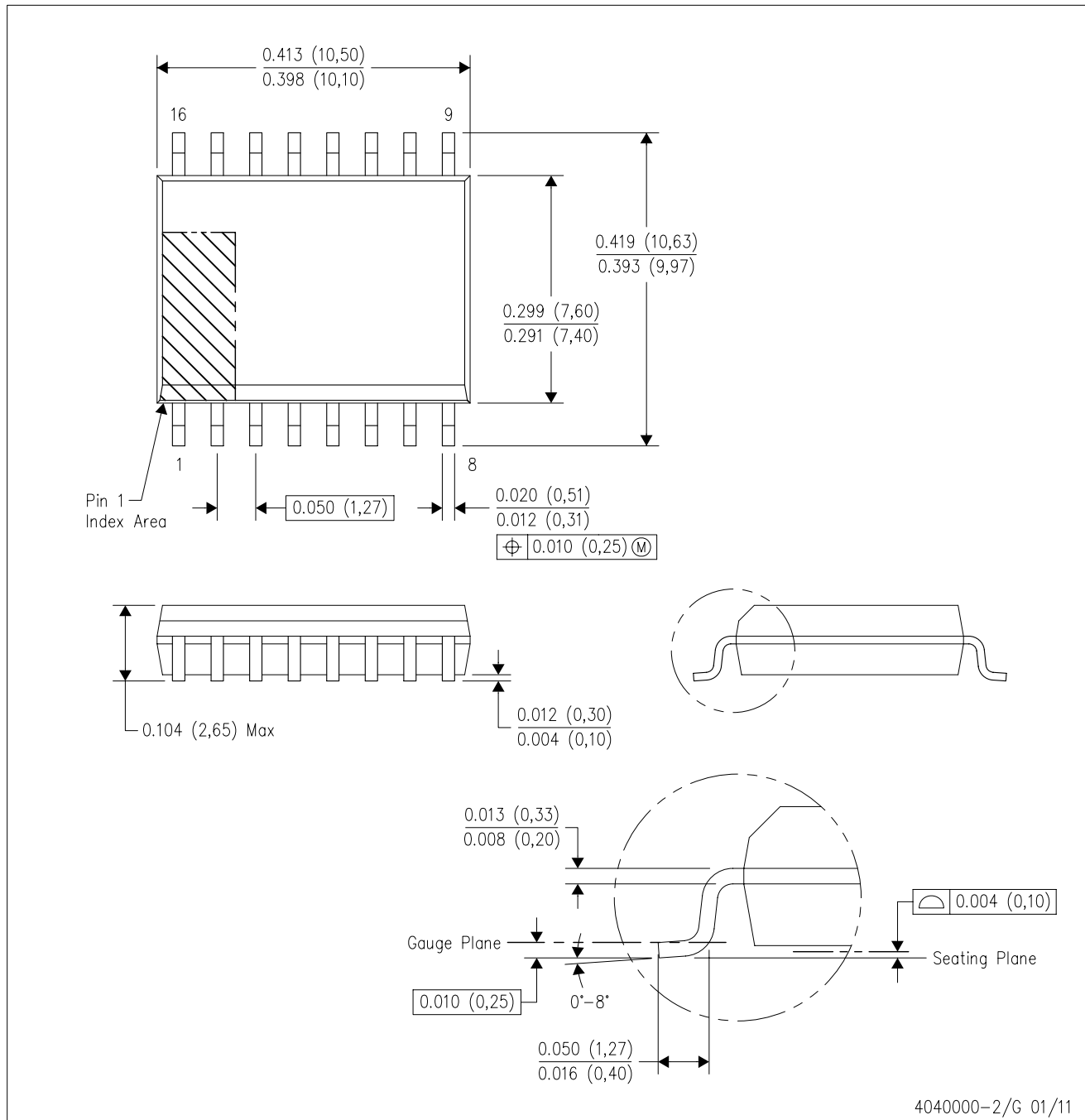


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO7231CQDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R-PDSO-G16)

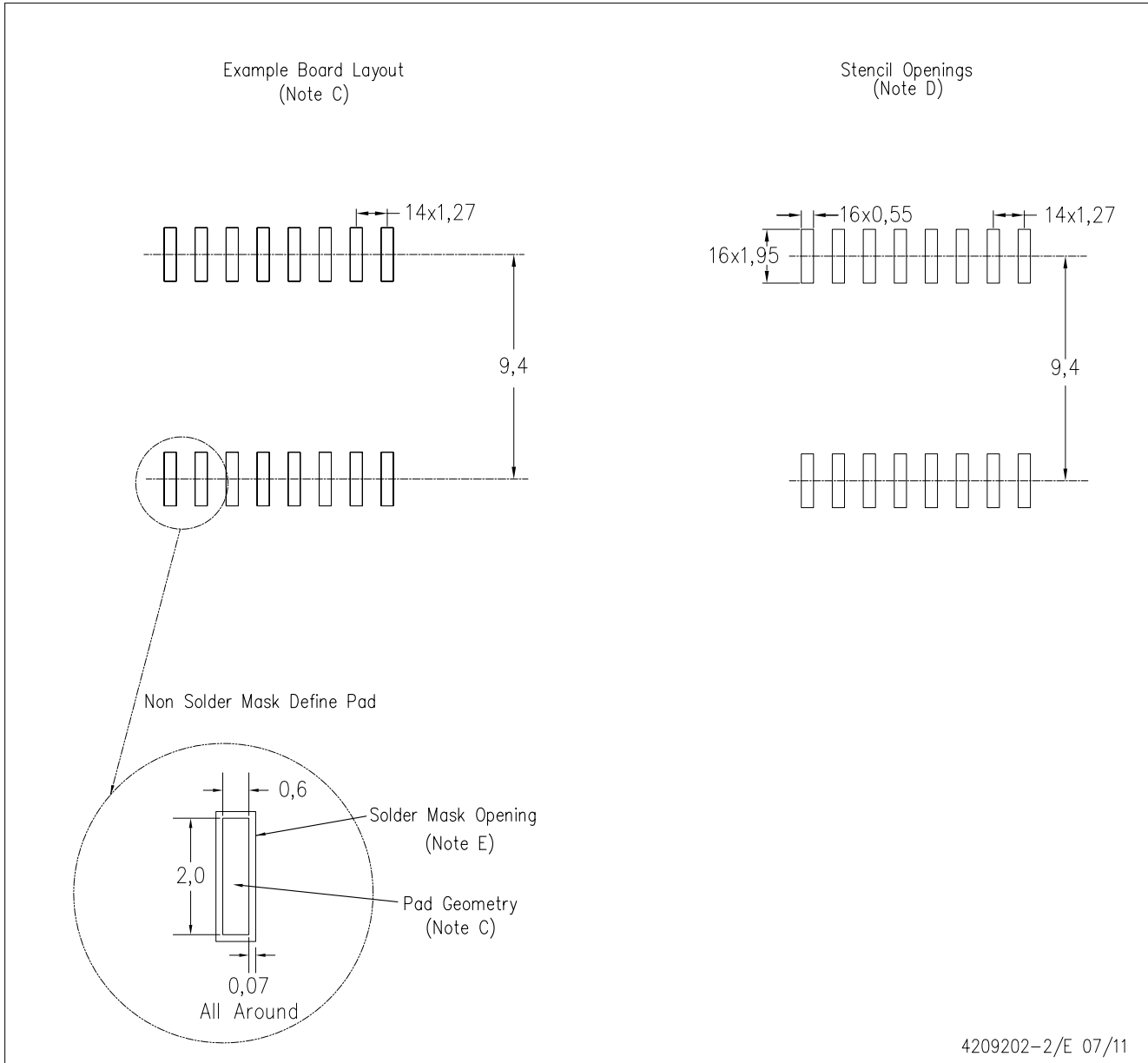
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4209202-2/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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