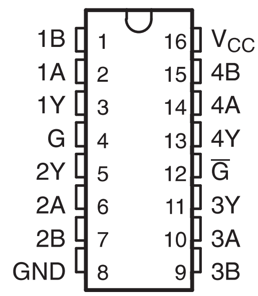
# HIGH-SPEED DIFFERENTIAL LINE RECEIVER

**Check for Samples: SN55LVDS32-SP**

## FEATURES

- **QML-V Qualified, SMD 5962-97621**
- **Operate From a Single 3.3-V Supply**
- **Designed for Signaling Rates of up to 100 Mbps**
- **Differential Input Thresholds ±100 mV Max**
- **Typical Propagation Delay Times of 2.1 ns**
- **Power Dissipation 60 mW Typical Per Receiver at Maximum Data Rate**
- **Bus-Terminal ESD Protection Exceeds 8 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels**
- **Open-Circuit Fail-Safe**
- **Cold Sparing for Space and High Reliability Applications Requiring Redundancy**

**J OR W PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The SN55LVDS32 is a differential line receiver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ±100-mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media and the noise coupling to the environment.

The SN55LVDS32 is characterized for operation from –55°C to 125°C.

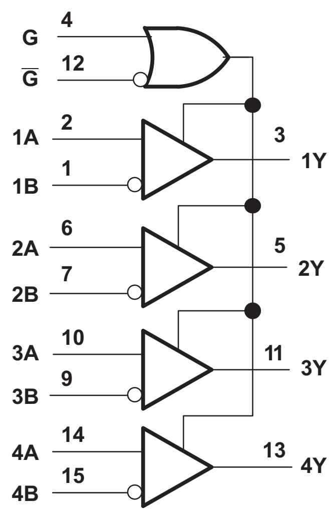
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| –55°C to 125°C | CDIP - J | 5962-9762201VEA | 5962-9762201VEA |
| | CFP - W | 5962-9762201VFA | 5962-9762201VFA |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### SN55LVDS32 logic diagram (positive logic)



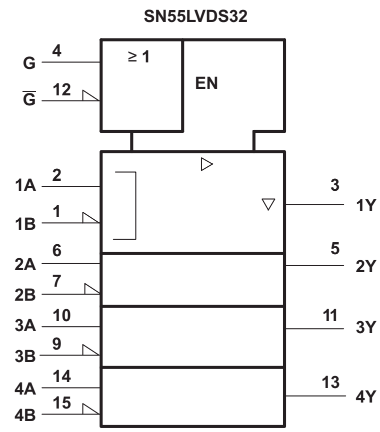

 

### Table 1. FUNCTION TABLE(1)

| SN55LVDS32 | | | |
|---|---|---|---|
| DIFFERENTIAL INPUT A, B | ENABLES | | OUTPUT |
| | G | $\overline{G}$ | Y |
| $V_{ID} \geq 100$ mV | H | X | H |
| | X | L | H |
| $-100$ mV < $V_{ID} \leq 100$ mV | H | X | ? |
| | X | L | ? |
| $V_{ID} \leq -100$ mV | H | X | L |
| | X | L | L |
| X | L | H | Z |
| Open | H | X | H |
| | X | L | H |

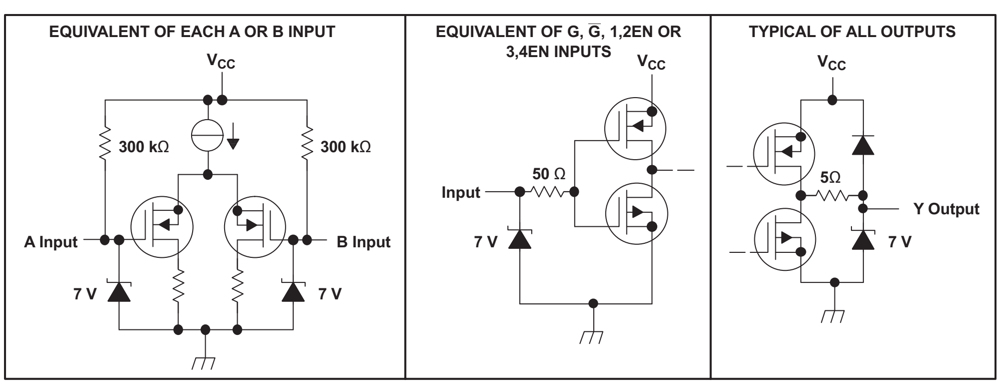
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

**logic symbol†**




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

| | | | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range[(2)] | | –0.5 V to 4 V |
| $V_I$ | Input voltage range | Enables and output | –0.5 V to $V_{CC}$ + 0.5 V |
| | | A or B | –0.5 V to 4 V |
| | Continuous total power dissipation | | See Dissipation Rating Table |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR[(1)] ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING | $T_A$ = 125°C POWER RATING |
|---|---|---|---|---|---|
| J | 1375 mW | 11 mW/°C | 880 mW | 715 mW | 275 mW |
| W | 1000 mW | 8 mW/°C | 640 mW | 520 mW | 200 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | G, $\overline{G}$, 1,2EN, or 3,4EN | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | G, $\overline{G}$, 1,2EN, or 3,4EN | | | 0.8 | V |
| $\lvert V_{ID}\rvert$ | Magnitude of differential input voltage | | 0.1 | | 0.6 | V |
| $V_{IC}$ | Common-mode input voltage (see Figure 1) | | $\lvert V_{ID}\rvert/2$ | | 2.4 - $\lvert V_{ID}\rvert/2$ | V |
| | | | | | $V_{CC}$ - 0.8 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | °C |

COMMON-MODE INPUT VOLTAGE RANGE
vs
DIFFERENTIAL INPUT VOLTAGE

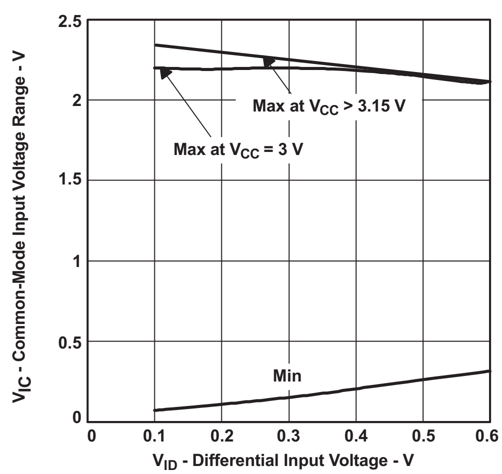



**Figure 1. $V_{IC}$ Versus $V_{ID}$ and $V_{CC}$**

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ITH+}$ | Positive-going differential input voltage threshold | See Figure 2, Table 2, and (2) | | | | 100 | mV |
| $V_{ITH-}$ | Negative-going differential input voltage threshold(3) | See Figure 2, Table 2, and (2) | | -100 | | | mV |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA | | | | 0.4 | V |
| $I_{CC}$ | Supply current | Enabled, No load | | | 10 | 18 | mA |
| | | Disabled | | | 0.25 | 0.5 | |
| $I_I$ | Input current (A or B inputs) | $V_I$ = 0 | | -2 | -10 | -20 | µA |
| | | $V_I$ = 2.4 V | | -1.2 | -3 | | |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | $V_{CC}$ = 0, | $V_I$ = 2.4 V | | 6 | 20 | µA |
| $I_{IH}$ | High-level input current (EN, G, or $\overline{G}$ inputs) | $V_{IH}$ = 2 V | | | | 10 | µA |
| $I_{IL}$ | Low-level input current (EN, G, or $\overline{G}$ inputs) | $V_{IL}$ = 0.8 V | | | | 10 | µA |
| $I_{OZ}$ | High-impedance output current | $V_O$ = 0 or $V_{CC}$ | | | | ±12 | µA |

(1) All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3 V.
(2) $|V_{ITH}|$ = 200 mV for operation at –55°C.
(3) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 10 pF, See Figure 3 | 1.3 | 2.3 | 6 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1.4 | 2.2 | 6.1 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew(1) | | | 0.1 | | ns |
| $t_r$ | Differential output signal rise time (20% to 80%) | | | 0.6 | | ns |
| $t_f$ | Differential output signal fall time (80% to 20%) | | | 0.7 | | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | See Figure 4 | | 6.5 | 12 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 5.5 | 12 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | | | 8 | 12 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 3 | 12 | ns |

(1) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

## PARAMETER MEASUREMENT INFORMATION

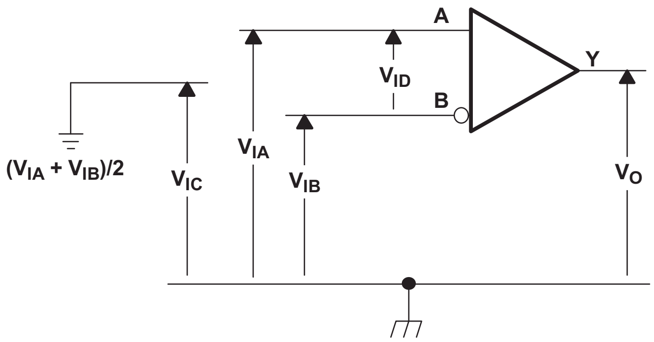


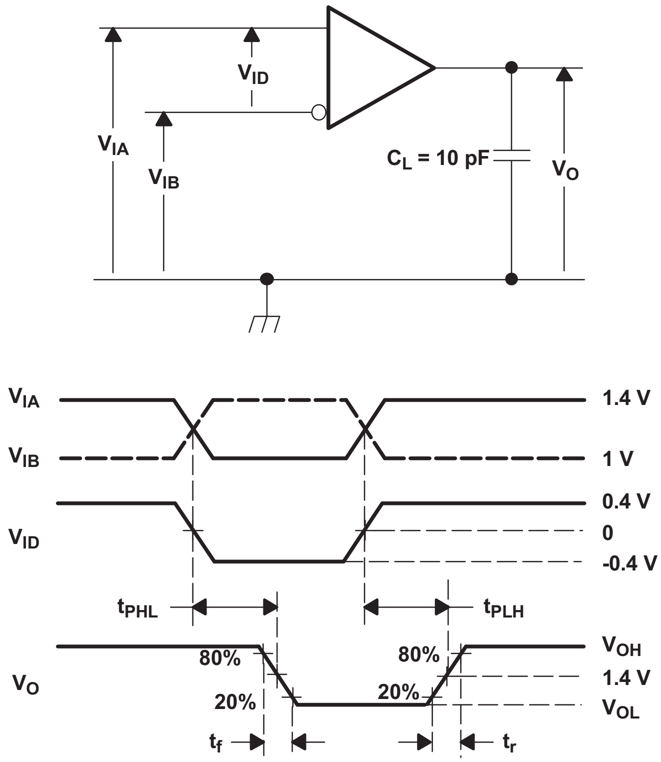

**Figure 2. Voltage Definitions**

### Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages

| APPLIED VOLTAGES[(1)] | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE |
|---|---|---|---|
| $V_{IA}$ (mV) | $V_{IB}$ (mV) | $V_{ID}$ (mV) | $V_{IC}$ (mV) |
| 1.25 | 1.15 | 100 | 1.2 |
| 1.15 | 1.25 | -100 | 1.2 |
| 2.4 | 2.3 | 100 | 2.35 |
| 2.3 | 2.4 | -100 | 2.35 |
| 0.1 | 0 | 100 | 0.05 |
| 0 | 0.1 | -100 | 0.05 |
| 1.5 | 0.9 | 600 | 1.2 |
| 0.9 | 1.5 | -600 | 1.2 |
| 2.4 | 1.8 | 600 | 2.1 |
| 1.8 | 2.4 | -600 | 2.1 |
| 0.6 | 0 | 600 | 0.3 |
| 0 | 0.6 | -600 | 0.3 |

(1) These voltages are applied for a minimum of 1.5 µs.

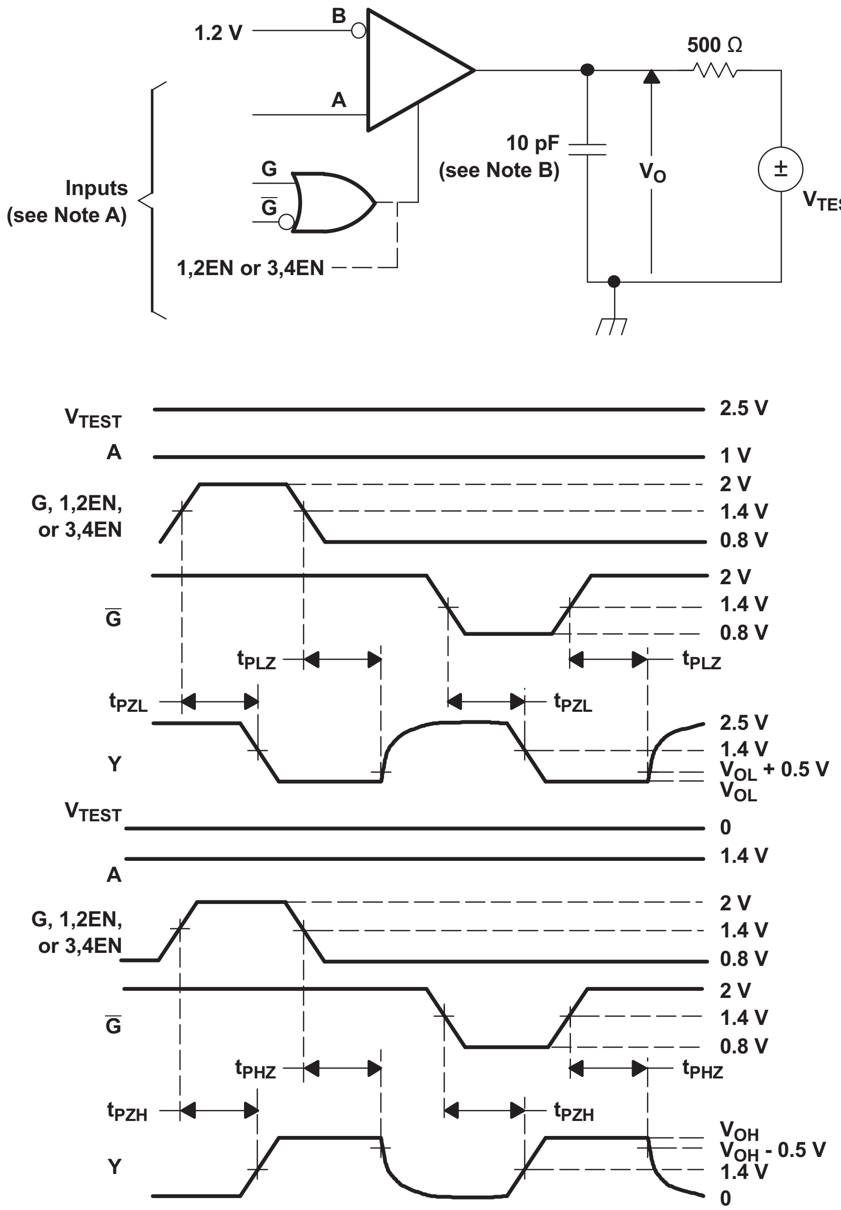
 




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate(PRR) = 50 Mpps, pulse width = 10 ±0.2 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

**Figure 3. Timing Test Circuit and Waveforms**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate(PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

**Figure 4. Enable- and Disable-Time Test Circuit and Waveforms**

## TYPICAL CHARACTERISTICS

## TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
FREQUENCY

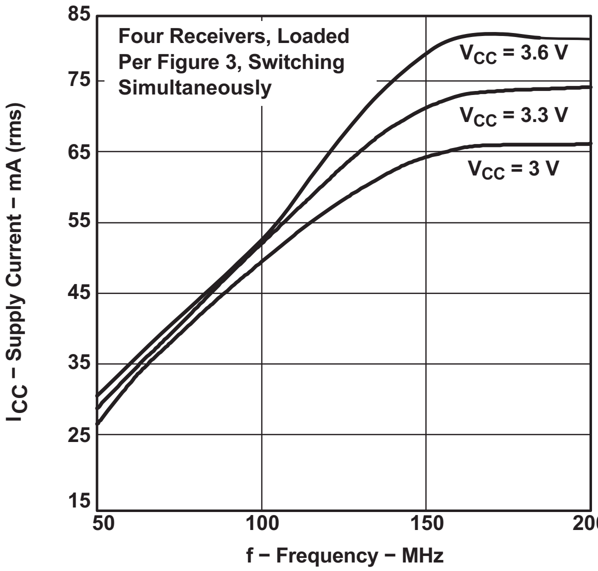



Figure 5.

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

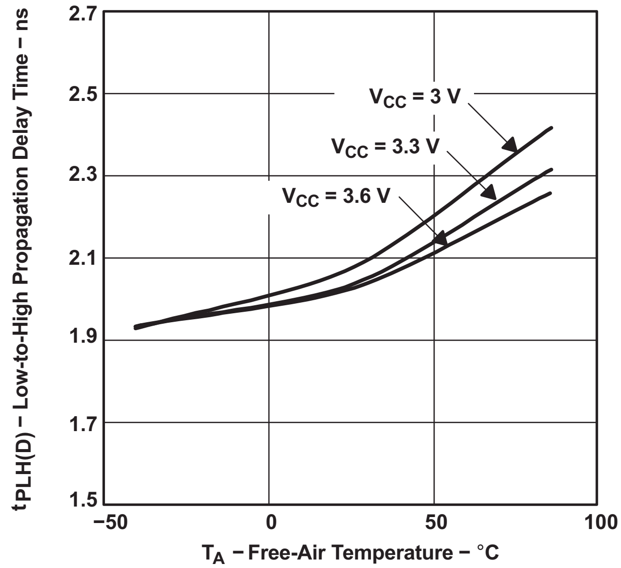



Figure 6.

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

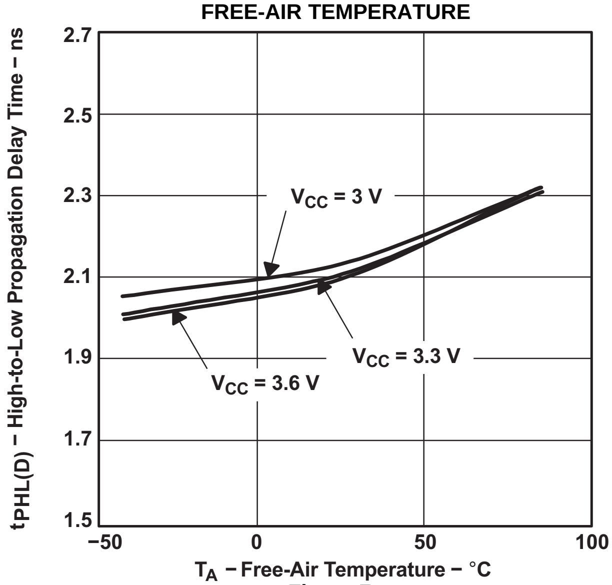



Figure 7.

## TYPICAL CHARACTERISTICS (continued)

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

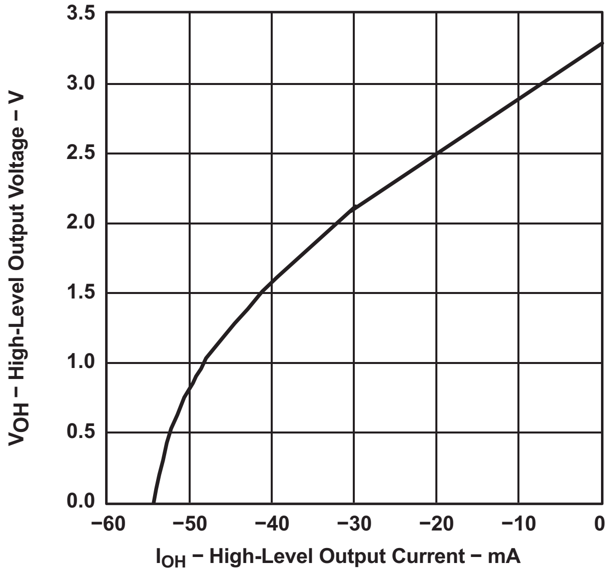



**Figure 8.**

**HIGH-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

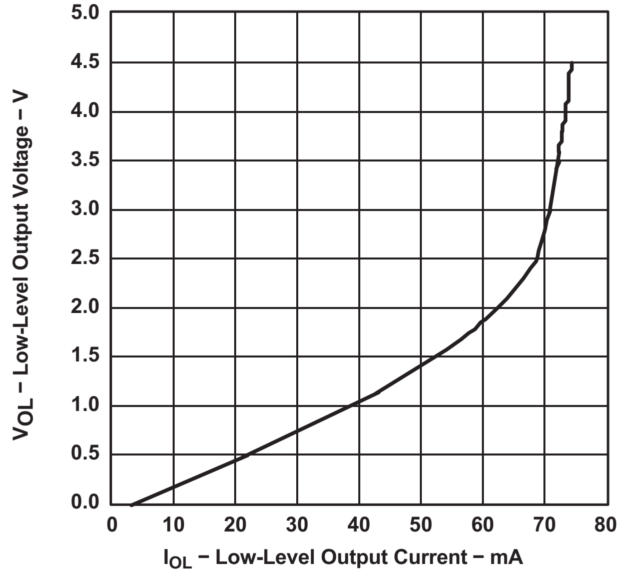



**Figure 9.**

## APPLICATION INFORMATION

## EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

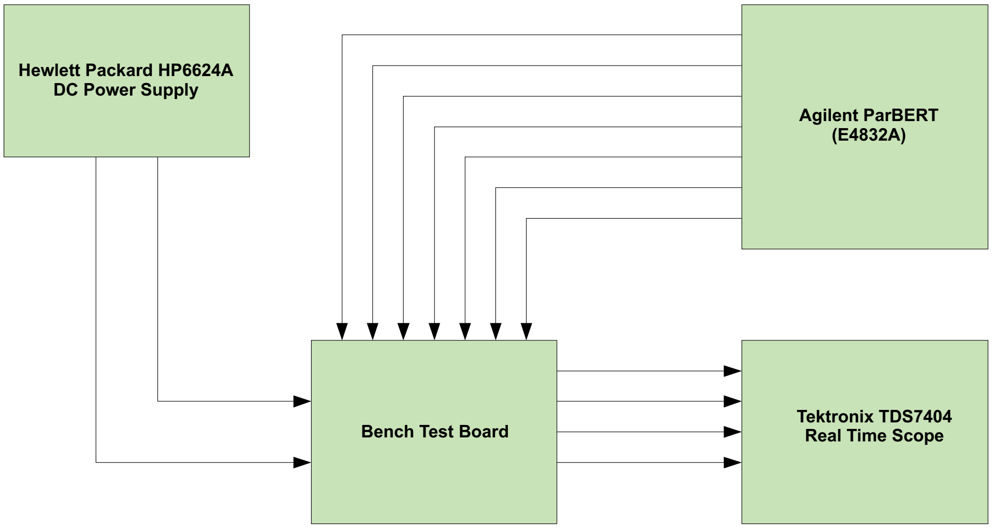
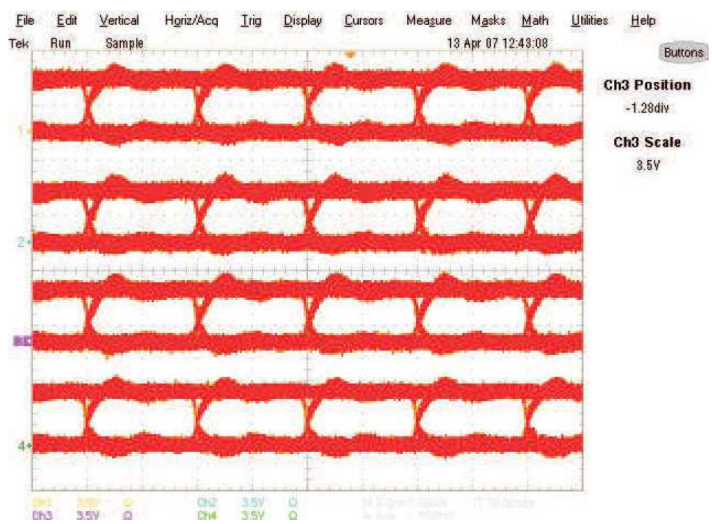



**Figure 10. Equipment Setup**




All Rx running at 100 Mbps; Channel 1: 1Y, Channel 2: 2Y; Channel 3: 3Y; Channel 4: 4Y

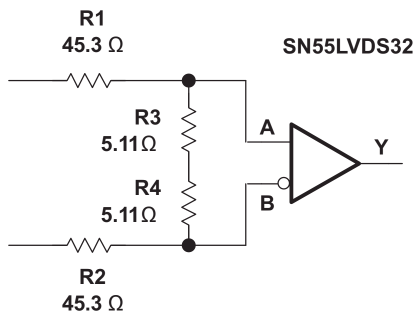
**Figure 11. Typical Eye Patterns SN55LVDS32: (T = 25°C; $V_{CC}$ = 3.6 V; PRBS = $2^{23-1}$)**

### USING AN LVDS RECEIVER WITH RS-422 DATA

Receipt of data from a TIA/EIA-422 line driver can be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than ±1 V), the answer can be as simple as shown in Figure 12. A resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of 100 Ω to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal, or 6 V, is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a greater than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.

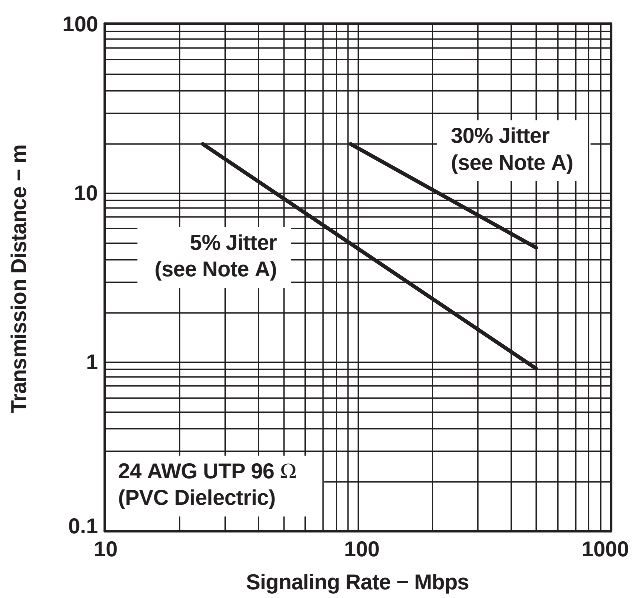



NOTE: The components used were standard values. (1) R1, R2 = NRC12F45R3TR, NIC components, 45.3 Ω, 1/8 W, 1%, 1206 package (2) R3, R4 = NRC12F5R11TR, NIC components, 5.11 Ω, 1/8 W, 1%, 1206 package (3) The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than 100 Ω in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

**Figure 12. RS-422 Data Input to an LVDS Receiver Under Low Ground-Noise Conditions**

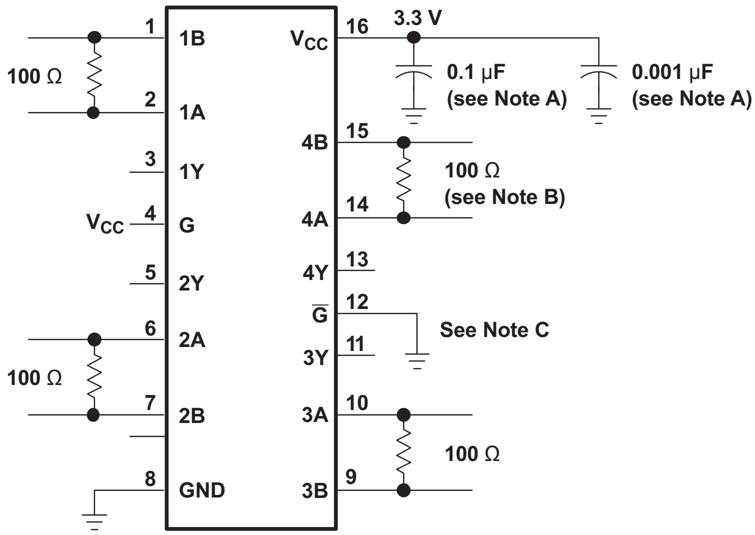
If ground noise between the RS-422 driver and LVDS receiver is a concern, the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from ±1 V to greater than ±4.5 V.

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual-supply requirements.




A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

**Figure 13. Typical Transmission Distance Versus Signaling Rate**

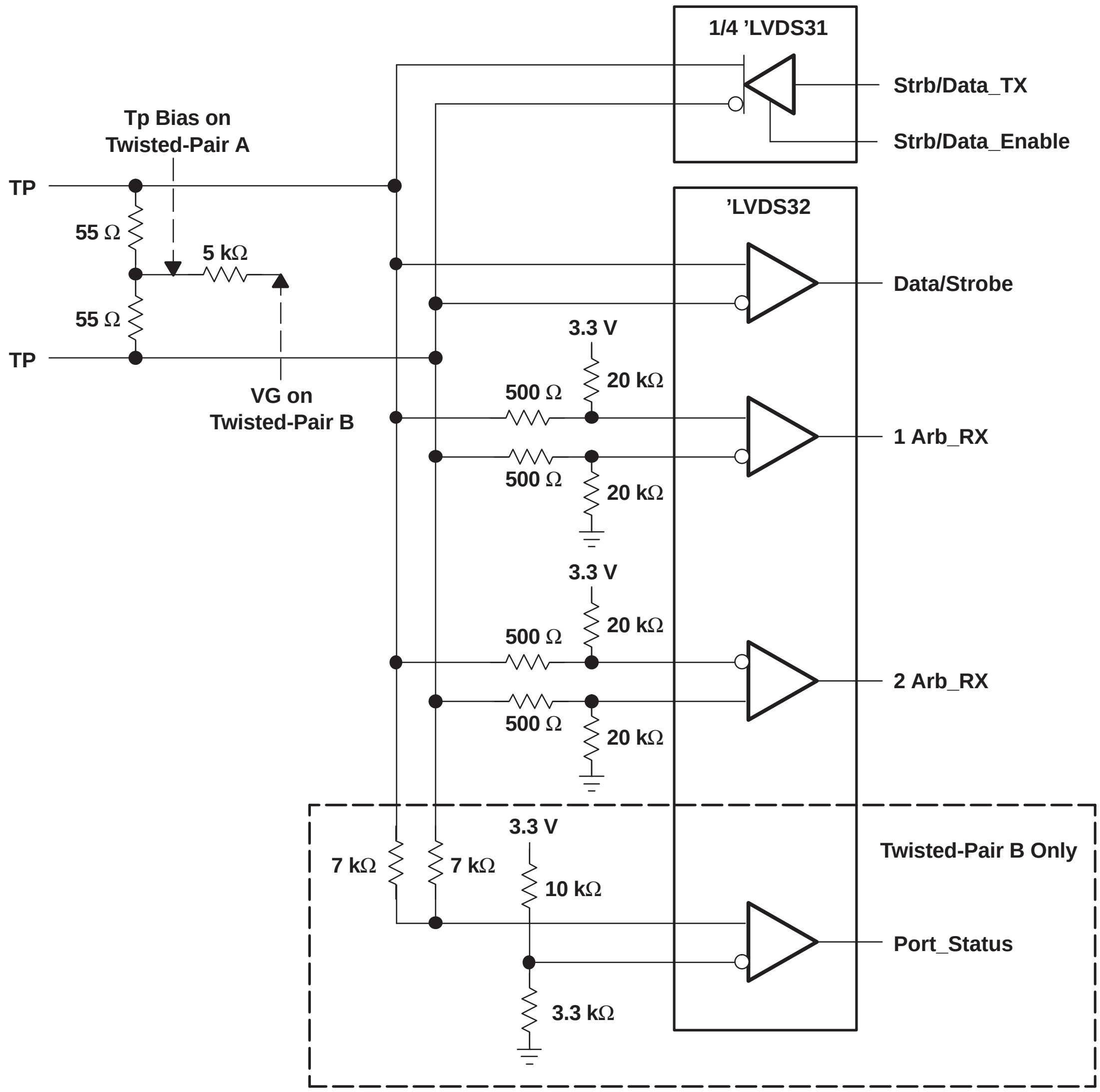



A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between VCC and the ground plane. The capacitors should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to $V_{CC}$ or GND as appropriate.

**Figure 14. Typical Application Circuit Schematic**




NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
B. Decoupling capacitance is not shown, but recommended.
C. $V_{CC}$ is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

**Figure 15. 100-Mbps IEEE 1394 Transceiver**

## FAIL-SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and100 mV if it is within its recommended input common-mode voltage range. However, TI LVDS receivers handle the open-input circuit situation differently.

Open-input circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors (see Figure 16). The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level, regardless of the differential input voltage.

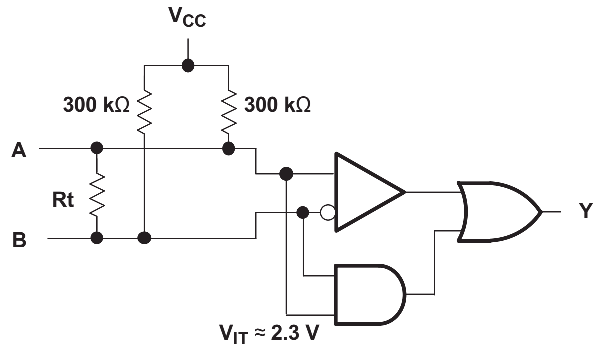
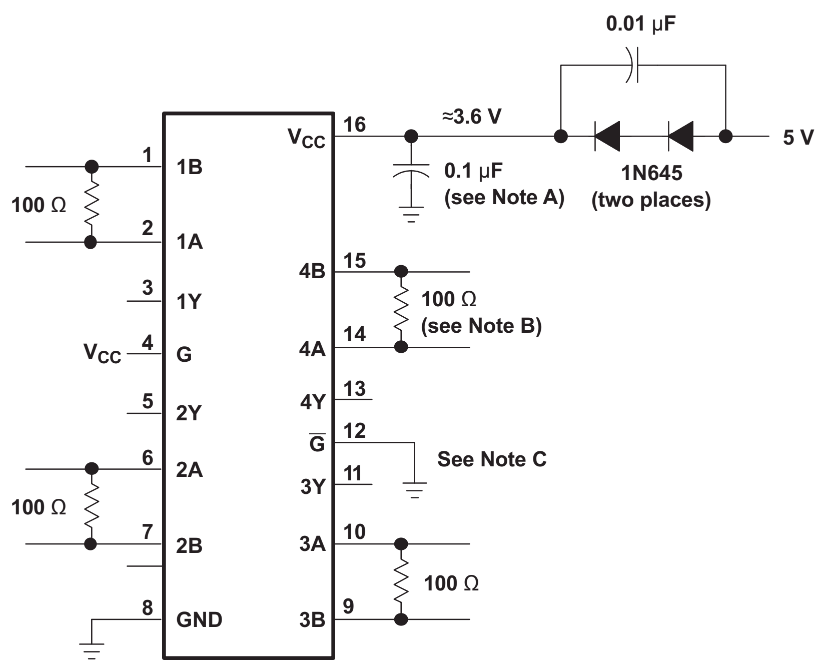



**Figure 16. Open-Circuit Fail-Safe of LVDS Receiver**

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 16. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.




A. Place a 0.1-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between $V_{CC}$ and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to $V_{CC}$ or GND, as appropriate.

**Figure 17. Operation With 5-V Supply**

## COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, $V_{CC}$ must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

## RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9762201VFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9762201VF<br>A<br>SNV55LVDS32W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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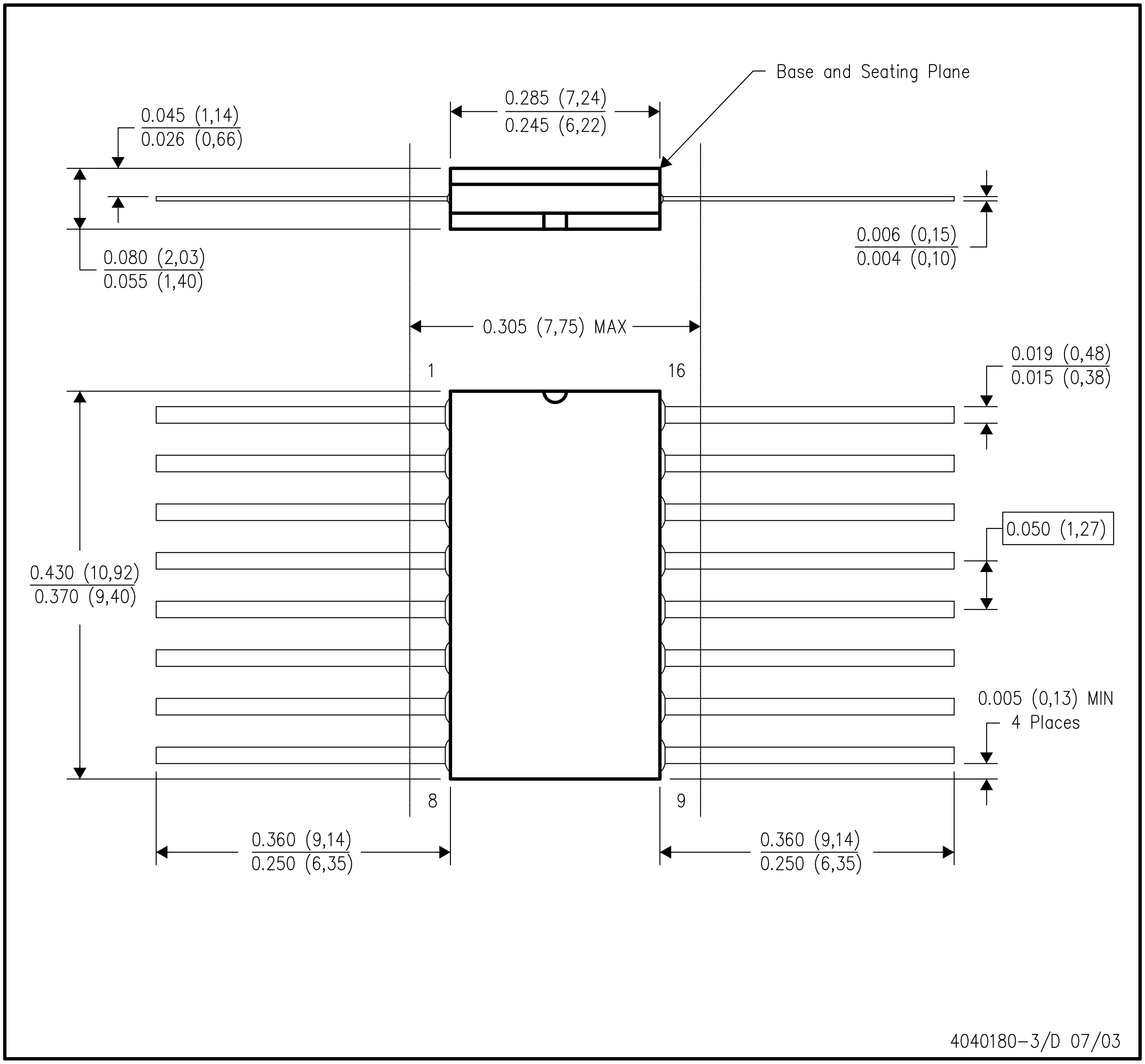
**OTHER QUALIFIED VERSIONS OF SN55LVDS32-SP :**

- Catalog: SN55LVDS32

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## W (R-GDFP-F16) CERAMIC DUAL FLATPACK




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

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