QUAD-CHANNEL XAUI/10GBASE-KR TRANSCEIVER

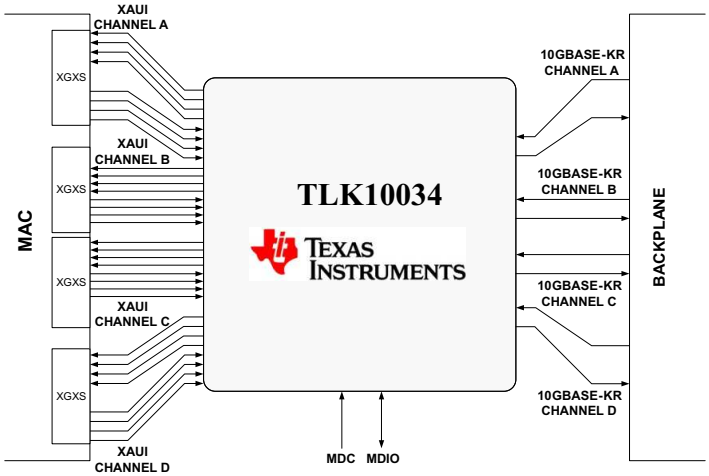
Check for Samples: TLK10034

FEATURES

- Quad Channel Multi-Rate Transceiver
- Supports 10GBASE-KR, XAUI, and 1GBASE-KX Ethernet Standards
- Supports all CPRI and OBSAI Data Rates up to 10 Gbps
- Supports Multi-Rate SERDES Operation with up to 10.3125Gbps Data Rate on the High Speed Side and up to 5Gbps on the Low Speed Side
- Differential CML I/Os on Both High Speed and Low Speed Sides
- Interface to Backplanes, Passive and Active Copper Cables, or SFP+ Optical Modules
- Selectable Reference Clock per Channel with Multiple Output Clock Options
- Loopback Capability on Both High Speed and Low Speed Sides
- Supports Data Retime Operation
- Supports PRBS, CRPAT, CJPAT, High- /Low-/Mixed-Frequency Patterns, and KR Pseudo-Random Pattern Generation and Verification, Square-Wave Generation
- Two Power Supplies: 1.0V, and 1.5 or 1.8V Nominal
- No Power Supply Sequencing Requirements
- Transmit De-emphasis and Receive Adaptive Equalization to Allow Extended Backplane/Cable Reach on Both High Speed and Low Speed Sides
- Programmable Transmit Output Swing on Both High Speed and Low Speed Sides
- Loss of Signal (LOS) Detection
- Supports 10G-KR Link Training, Forward Error Correction, Auto-Negotiation
- Jumbo Packet Support
- JTAG; IEEE 1149.1 /1149.6 Test Interface
- Industry Standard MDIO Clause 45 and 22 Control Interfaces
- 65nm Advanced CMOS Technology
- Industrial Ambient Operating Temperature (–40°C to 85°C)
- Power Consumption: 825mW per Channel (Nominal)
- Device Package: 19mm x 19mm, 324-pin PBGA, 1-mm Ball-Pitch

APPLICATIONS

- 10GBASE-KR Compliant Backplane Links
- 10 Gigabit Ethernet Switch, Router, and Network Interface Cards
- 10 Gigabit Ethernet Blade Servers
- Proprietary Cable/Backplane Links
- High-Speed Point- to-Point Transmission Systems



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DESCRIPTION

The TLK10034 is a quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems. This device supports three primary modes. It can be used as a XAUI to 10GBASE-KR transceiver, as a general-purpose 8b/10b multi-rate 4:1, 2:1, or 1:1 serializer/deserializer, or can be used in 1G-KX mode.

While operating in the 10GBASE-KR mode, the TLK10034 performs serialization of the 8B/10B encoded XAUI data stream presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs in 64B/66B encoding format. Likewise, the TLK10034 performs deserialization of 64B/66B encoded data streams presented on its high speed side data inputs. The deserialized 64B/66B data is presented in 8B/10B format on the low speed side outputs. Link Training is supported in this mode as well as Forward Error Correction (FEC) for extended length applications.

While operating in the General Purpose SERDES mode, the TLK10034 performs 2:1 and 4:1 serialization of the 8B/10B encoded data streams presented on its low speed (LS) side data inputs. The serialized 8B/10B encoded data is presented on the high speed (HS) side outputs. Likewise, the TLK10034 performs 1:2 and 1:4 deserialization of 8B/10B encoded data streams presented on its high speed side data inputs. The deserialized 8B/10B encoded data is presented on the low speed side outputs. Depending on the serialization/deserialization ratio, the low speed side data rate can range from 0.5Gbps to 5Gbps and the high speed side data rate can range from 1Gbps to 10Gbps. 1:1 retime mode is also supported but limited to 1Gbps to 5Gbps rates.

The TLK10034 also supports 1G-KX (1.25Gbps) mode with PCS (CTC) capabilities. This mode can be enabled via software provisioning or via auto negotiation. If software provisioning is used, data rates up to 3.125 Gbps are supported.

Both low speed and high speed side data inputs and outputs are of differential current mode logic (CML) type with integrated termination resistors.

The TLK10034 provides flexible clocking schemes to support various operations. They include the support for clocking with an externally-jitter-cleaned clock recovered from the high speed side. The device is also capable of performing clock tolerance compensation (CTC) in 10GBASE-KR and 1G-KX modes, allowing for asynchronous clocking.

The TLK10034 provides low speed side and high speed side loopback modes for self-test and system diagnostic purposes.

The TLK10034 has built-in pattern generators and verifiers to help in system tests. The device supports generation and verification of various PRBS, High, Low, Mixed, CRPAT long/short, CJPAT, and KR pseudo-random test patterns and square wave generation. The types of patterns supported on the low speed and high speed side are dependent on the operational mode chosen.

The TLK10034 has an integrated loss of signal (LOS) detection function on both high speed and low speed sides. LOS is asserted in conditions where the input differential voltage swing is less than the LOS assert threshold.

In the 10GBASE-KR mode, the lane alignment for each channel is achieved through the standard XAUI lane alignment scheme. In the General Purpose SERDES mode the low speed side lane alignment for each channel is achieved through a proprietary lane alignment scheme. The upstream link partner device needs to implement the lane alignment scheme for the correct link operation. Normal link operation resumes only after lane alignment is achieved.

The four TLK10034 channels are fully independent. They can be operated with different reference clocks, at different data rates, and with different serialization/deserialization ratios.

The low speed side of the TLK10034 is ideal for interfacing with an FPGA or ASIC capable of handling lower-rate serial data streams. The high speed side is ideal for interfacing with remote systems through optical fibers, electrical cables, or backplane interfaces. The TLK10034 supports operation with SFP and SFP+ optical modules, as well as 10GBASE-KR compatible backplane systems.

PHYSICAL CHARACTERISTICS

Block Diagram

Various interfaces of the TLK10034 device are shown in Figure 1 for Channel A. The implementation of all four channels is identical. The block diagrams for the transmit and receive data paths are shown in Figure 2. This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including channel synchronization, lane alignment, 8B/10B and 64B/66B encoding/decoding, as well as test pattern generation and verification.

The TLK10034 provides a management data input/output (MDIO) interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed description of the TLK10034 pin functions is provided in TLK10034 data manual.

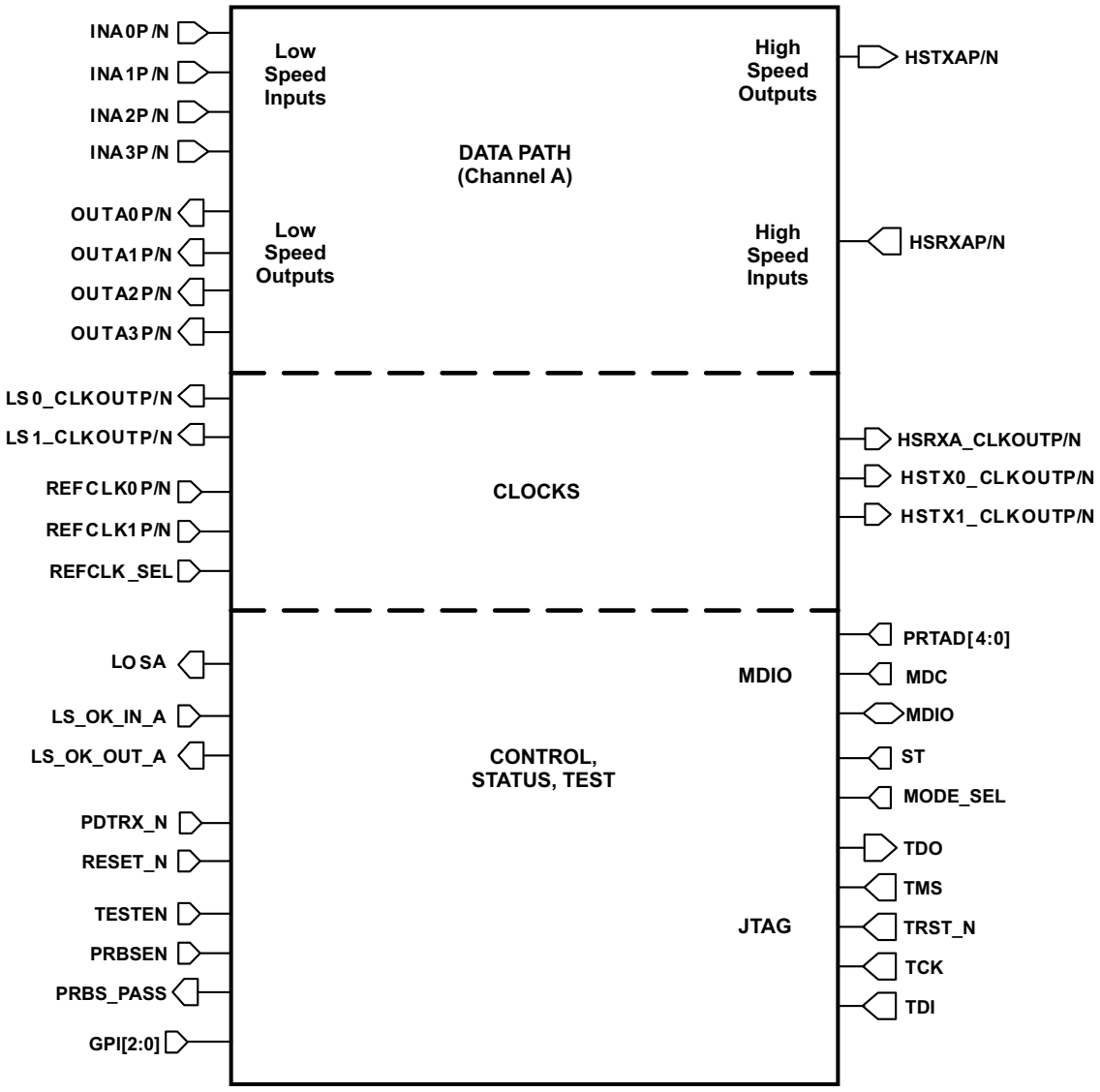

Figure 1. TLK10034 Interfaces

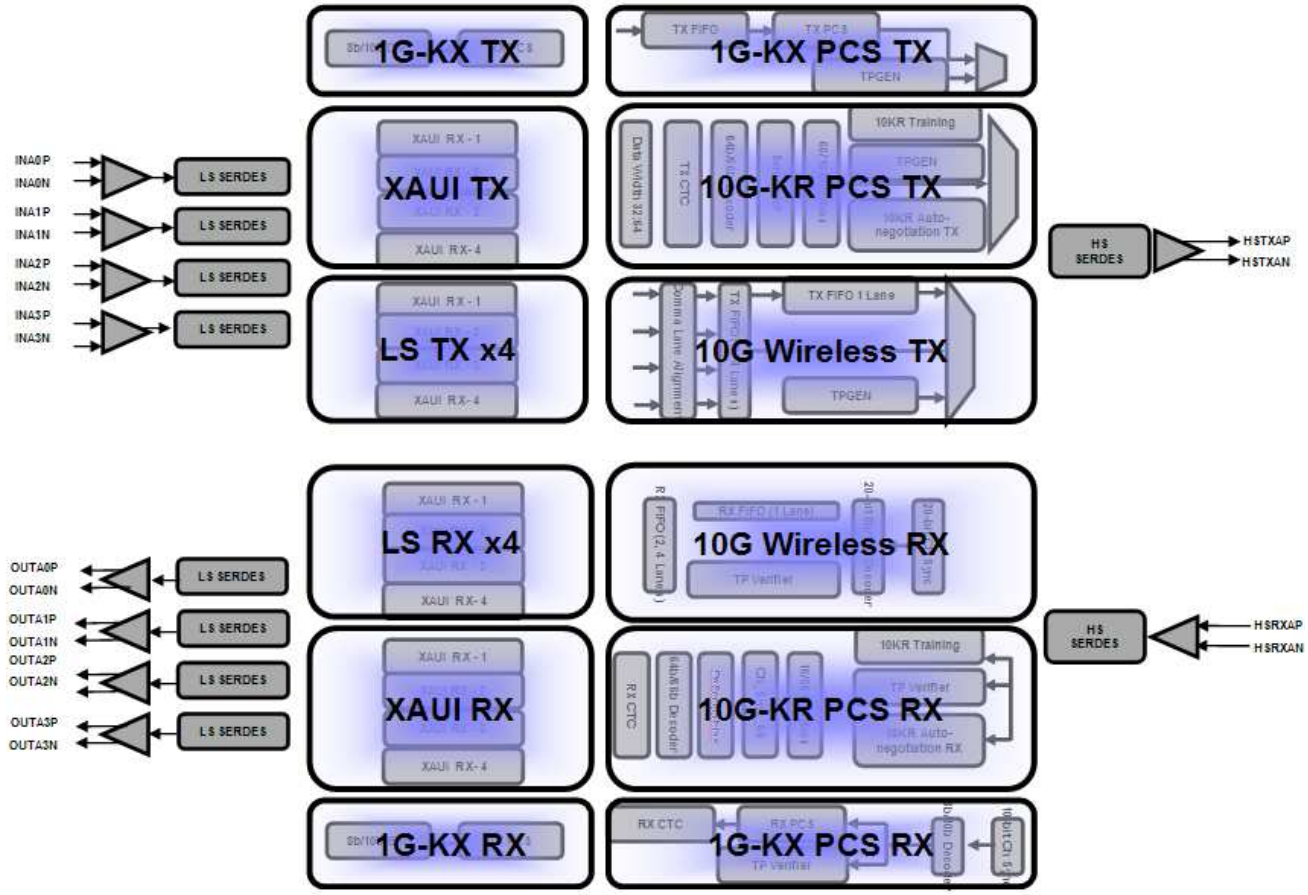

Figure 2. A Simplified One Channel Block Diagram of the TLK10034 Data Paths

Request Complete Data Manual at:

TLK10034_inquiries@list.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLK10034AAJ	ACTIVE	FCBGA	AAJ	324	84	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10034	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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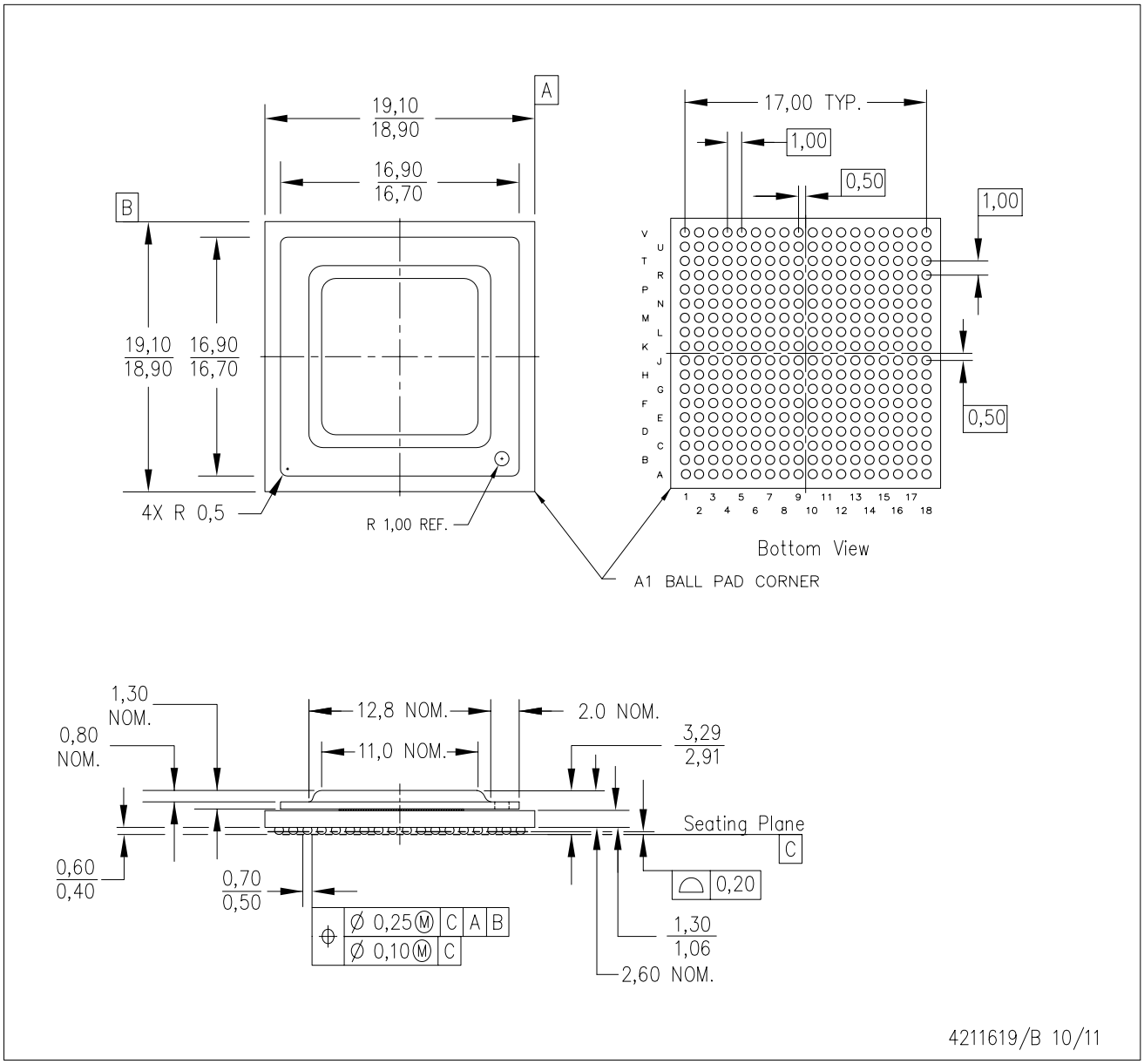
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

AAJ (S–PBGA–N324) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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