14.2-GBPS Dual Channel, Dual Mode Linear Equalizer

Check for Samples: SN65LVCP1412

FEATURES

- **Dual Channel, Uni-Directional, Multi-Rate, Dual-Mode Linear Equalizer with Operation up to 14.2Gbps Serial Data Rate for Backplane and Cable Interconnects**
- **Linear Equalization Increases Link Margin for Systems Implementing Decision Feedback Equalizers (DFE)**
- **18dB Analog Equalization at 7.1GHz with 1dB Step Control for Backplane Mode or Cable Mode**
- **Output Linear Dynamic Range: 1200mV**
- **Bandwidth: >20GHz – Typical**
- **Better than 15dB Return Loss at 7.1GHz**
- **Supports Out-of-Band (OOB) Signaling**
- **Low Power: Typically 75mW per Channel at 2.5V VCC**
- **24-Terminal QFN (Quad Flatpack, No-Lead) 4mm x 5mm x 0.75mm; 0.5mm Terminal Pitch**
- **Excellent Impedance Matching to 100Ω Differential PCB Transmission Lines**
- **GPIO or I^2C Control**
- **2.5V and 3.3V±5% Single Power Supply**
- **2kV ESD (HBM)**
- **Flow-Through Pin-Out Provides Ease of Routing**
- **Small Package Size Saves Board Space**

APPLICATIONS

- **High Speed Links in Telecommunication and Data communication**
- **Backplane and Cable Interconnects for 10GbE, 16GFC,10G SONET, SAS, SATA, CPRI, OBSAI, Infiniband, 10GBase-KR, and XFI/SFI**

DESCRIPTION

The SN65LVCP1412 is an asynchronous, protocol-agnostic, low latency, two-channel linear equalizer optimized for use up to 14.2Gbps and compensates for losses in backplane or active cable applications. The architecture of SN65LVCP1412 is designed to work with an ASIC or a FPGA with digital equalization employing Decision Feedback Equalizers (DFE). SN65LVCP1412 linear equalizer preserves the shape of the transmitted signal ensuring optimum DFE performance. SN65LVCP1412 provides a low power solution while at the same time extending the effectiveness of DFE.

SN65LVCP1412 is configurable via I^2C or GPIO interface. Using the I^2C interface of the SN65LVCP1412 enables the user to control independently the Equalization, Path Gain, and Output Dynamic Range for each individual channel. In GPIO mode, Equalization, Path Gain, and Output Dynamic Range can be set for all channels using the GPIO Input pins.

SN65LVCP1412 outputs can be disabled independently via I^2C.

The SN65LVCP1412 operates from a single 2.5V or 3.3V power supply.

The package for the SN65LVCP1412 is a 24 pin 4mm x 5mm x 0.75mm QFN (Quad Flatpack, No-lead) lead-free package with 0.5mm pitch, and characterized for operation from –40°C to 85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

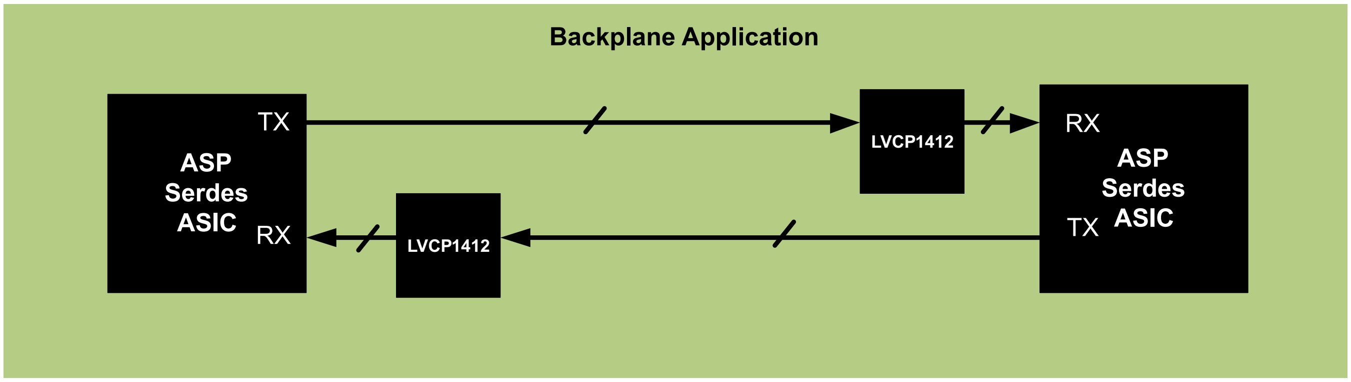


Figure 1. Typical Backplane Application – Trace Mode

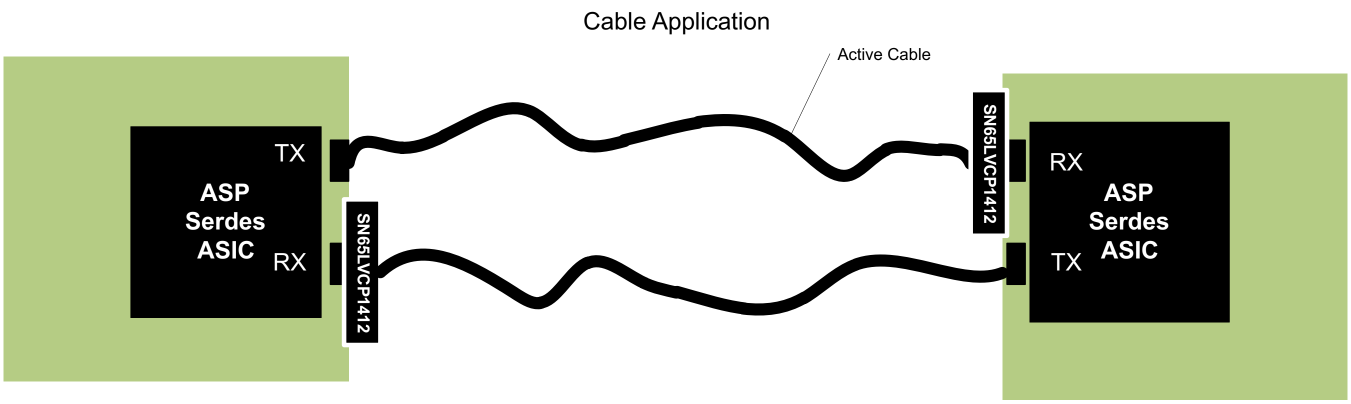


Figure 2. Typical Cable Application – Cable Mode

BLOCK DIAGRAM (GPIO or I²C Mode)

A simplified block diagram of the SN65LVCP1412 is shown in Figure 3 for GPIO or I²C input control mode. This compact, low power, 14.2Gbps daul-channel dual-mode linear analog equalizer consists of two high-speed data paths and an input GPIO pin logic-control block and a two-wire interface with a control-logic block.

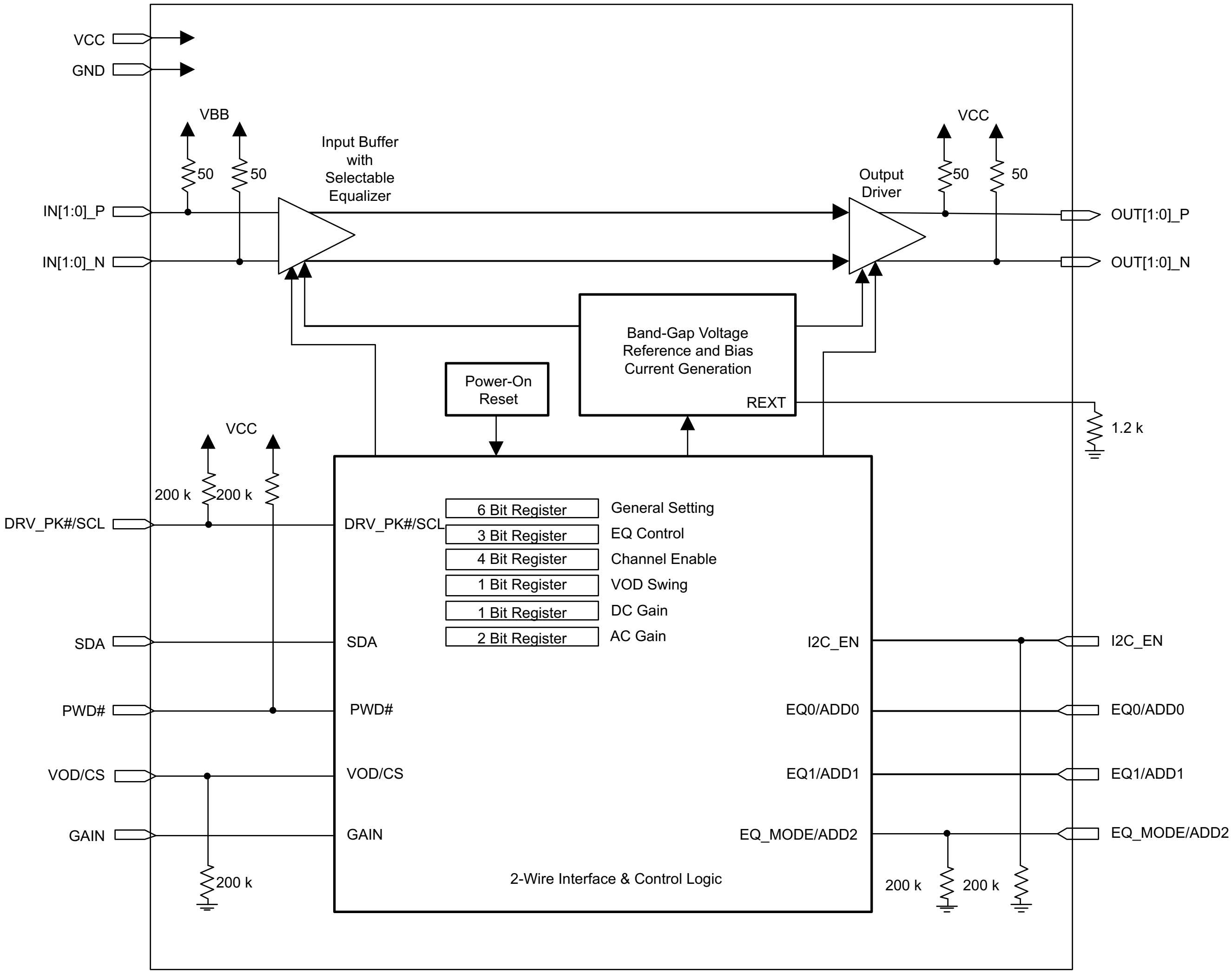


Figure 3. Simplified Block Diagram of the SN65LVCP1412

PACKAGE

The package pin locations and assignments are shown in Figure 4. The SN65LVCP1412 is packaged in a 4mm x 5mm x 0.75mm, 24 pin, 0.5mm pitch lead-free QFN.

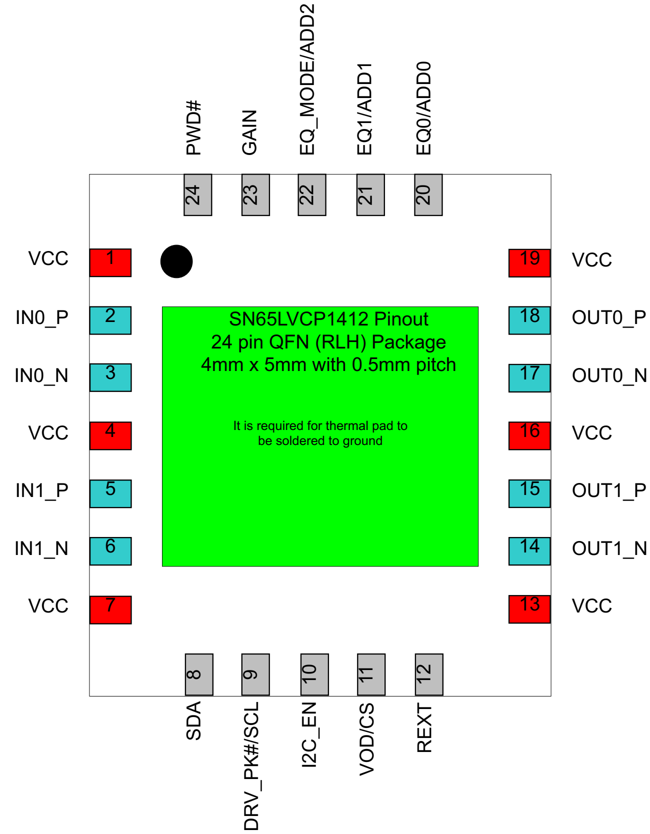


Figure 4. Package Drawing (Top View)

PIN DESCRIPTIONS

PINS		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	NO.			
DIFFERENTIAL HIGH-SPEED I/O				
IN0_P IN0_N	2 3	Input, (with 50 Ω termination to input common mode)	Differential input, lane 0	
IN1_P IN1_N	5 6	Input, (with 50 Ω termination to input common mode)	Differential input, lane 1	
OUT0_P OUT0_N	18 17	Output	Differential output, lane 0	
OUT1_P OUT1_N	15 14	Output	Differential output, lane 1	
CONTROL SIGNALS				
SDA	8	Input Output, Open drain	**GPIO mode** No action needed	**I^2C mode** I^2C data. Connect a 10kΩ pull-up resistor externally
DRV_PK#/SCL	9	Input. (with 200kΩ pull-up)	**GPIO mode** HIGH: disable Driver peaking LOW: enables Driver 6dB AC peaking	**I^2C mode** I^2C clock. Connect a 10kΩ pull-up resistor externally
I2C_EN	10	Input, (wtih 200kΩ pull-down) 2.5V/3.3V CMOS	Configures the device operation for I^2C or GPIO mode: HIGH: enables I^2C mode LOW: enables GPIO mode	

PIN DESCRIPTIONS (continued)

<table>
<tr><th colspan="2">PINS</th><th rowspan="2">DIRECTION TYPE SUPPLY</th><th colspan="2" rowspan="2">DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th></tr>
<tr><td>VOD/CS</td><td>11</td><td>Input, (with 200kΩ pull-down)
2.5V/3.3V CMOS</td><td>GPIO mode
HIGH: set high VOD range
LOW: set low VOD range</td><td>I²C mode
HIGH: acts as Chip Select
LOW: disables I²C interface</td></tr>
<tr><td>REXT</td><td>12</td><td>Input, Analog</td><td colspan="2">External Bias Resistor:
1,200 Ω to GND</td></tr>
<tr><td>EQ0/ADD0</td><td>20</td><td>Input, 2.5V/3.3V CMOS - 3-state</td><td>GPIO mode
Working with EQ1 to determine input EQ gain.</td><td>I²C mode
ADD0 along with pins ADD1 and ADD2 comprise the three bits of I²C slave address.
ADD2:ADD1:ADD0:XXX</td></tr>
<tr><td rowspan="2">EQ1/ADD1</td><td rowspan="2">21</td><td rowspan="2">Input, 2.5V/3.3V CMOS - 3-state</td><td>GPIO mode
Working with EQ0 to determine input EQ gain steps of approximately 2dB
<table>
<tr><th>EQ1</th><th>EQ0</th><th>EQ GAIN</th></tr>
<tr><td>GND</td><td>GND</td><td>000</td></tr>
<tr><td>GND</td><td>HiZ</td><td>000</td></tr>
<tr><td>GND</td><td>VCC</td><td>001</td></tr>
<tr><td>HiZ</td><td>GND</td><td>010</td></tr>
<tr><td>HiZ</td><td>HiZ</td><td>011</td></tr>
<tr><td>HiZ</td><td>VCC</td><td>100</td></tr>
<tr><td>VCC</td><td>GND</td><td>101</td></tr>
<tr><td>VCC</td><td>HiZ</td><td>110</td></tr>
<tr><td>VCC</td><td>VCC</td><td>111</td></tr>
</table></td><td>I²C mode
ADD1 along with pins ADD0 and ADD2 comprise the three bits of I²C slave address
ADD2:ADD1:ADD0:XXX</td></tr>
<tr><td colspan="2">EQ1 and EQ0 work with AC_GAIN and DC_GAIN to determine final EQ gain as this:
<table>
<tr><th>EQ1/ EQ0</th><th>GAIN</th><th>DC GAIN (dB)</th><th>EQ GAIN (dB)</th></tr>
<tr><td>000 ~ 111</td><td>LOW</td><td>-6</td><td>1 ~ 9</td></tr>
<tr><td>000 ~ 111</td><td>HiZ</td><td>-6</td><td>7 ~ 17</td></tr>
<tr><td>000 ~ 111</td><td>HIGH</td><td>0</td><td>1 ~ 9</td></tr>
</table></td></tr>
<tr><td>EQ_MODE/ ADD2</td><td>22</td><td>Input, (with 200kΩ pull-down),
2.5V/3.3V CMOS</td><td>GPIO mode
HIGH: Trace mode
LOW: Cable mode</td><td>I²C mode
ADD2 along with pins ADD1 and ADD0 comprise the three bits of I²C slave address.
ADD2:ADD1:ADD0:XXX</td></tr>
<tr><td>GAIN</td><td>23</td><td>Input, 2.5V/3.3V CMOS - 3-state</td><td>GPIO mode
Work with EQ1/EQ0 to set total EQ Gain. See table above.</td><td>I²C mode
No action needed</td></tr>
<tr><td>PWD#</td><td>24</td><td>Input, (with 200kΩ pull-up),
2.5V/3.3V CMOS</td><td colspan="2">HIGH: Normal Operation
LOW: Powers down the device, inputs off and outputs disabled, resets I²C</td></tr>
<tr><td colspan="5">POWER SUPPLY</td></tr>
<tr><td>VCC</td><td>1, 4, 7, 13, 16, 19</td><td>Power</td><td colspan="2">Power supply 2.5V±5%, 3.3V±5%</td></tr>
<tr><td>GND Center Pad</td><td></td><td>Ground</td><td colspan="2">The ground center pad is the metal contact at the bottom of the package. This pad must be connected to the GND plane. At least 9 PCB vias are recommended to minimize inductance and provide a solid ground. Refer to the package drawing (RLH-package) for the via placement.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUES	UNIT
V_{CC}	Supply voltage range[2]	–0.3 to 4	V
$V_{IN,DIFF}$	Differential Voltage between INx_P and INx_N	±2.5	V
$V_{IN+, IN–}$	Voltage at Inx_P and fINx_N	–0.5 V to VCC+0.5	V
V_{IO}	Voltage on Control IO pins	–0.5 V to VCC+0.5	V
I_{IN+} $I_{IN–}$	Continuous Current at high speed differential data inputs (differential)	–25 to 25	mA
I_{OUT+} $I_{OUT–}$	Continuous Current at high speed differential data outputs	–25 to 25	mA
ESD	Human Body Model[3] (All Pins)	2.0	kV
	Charged-Device Model[4] (All Pins)	500	V
Moisture Sensitivity level		2	
Shelf Life Conditions In Moisture Barrier Bag		24 Months at <40ºC and <90% Humidity	
Reflow Temperature package soldering, 4 sec		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

THERMAL INFORMATION

THERMAL METRIC[1]		SN65LVCP1412	UNITS
		RLH (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance[2]	34.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	33.8	
θ_{JB}	Junction-to-board thermal resistance[4]	12.5	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.50	
ψ_{JB}	Junction-to-board characterization parameter[6]	12.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	2.00	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
dR	Operating Data Rate			14.2	Gbps
V_{CC}	Supply voltage	2.375	2.5	2.625	V
V_{CC}	Supply voltage	3.135	3.3	3.465	V
TC	Junction temperature	–10		125	°C
TB	Maximum board temperature			85	°C
CMOS DC SPECIFICATIONS					
V_{IH}	High-level input voltage	0.8×V_{CC}			V
V_{MID}	Mid-level input voltage	V_{CC}×0.4		V_{CC}×0.6	V
V_{IL}	Low-level input voltage	–0.5		0.2×V_{CC}	V
PSNR BG	Bandgap Circuit PSNR	20			dB

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 2.5V VCC with all 4 channels active.		150	250	mW
PD_H	Device power dissipation	VOD = HIGH, at 2.5V VCC with all 4 channels active.		225	400	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I²C section for device configuration. 2.5V VCC		5		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 3.3V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 3.3V VCC with all 4 channels active.		225	375	mW
PD_H	Device power dissipation	VOD = HIGH, at 3.3V VCC with all 4 channels active.		330	525	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I²C section for device configuration. 3.3V VCC		5		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%, 3.3V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS DC SPECIFICATIONS						
I_{IH}	High level input current	VIN = 0.9 × V_{CC}	-40	17	40	µA
I_{IL}	Low level input current	VIN = 0.1 × V_{CC}	-40	17	40	µA
CML INPUTS (IN[3:0]_P, IN[3:0]_N)						
r_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{IN}	Input linear dynamic range	Gain = 0.5		1200		mV_{pp}
V_{ICM}	Input common mode voltage	Internally biased		V_{CC}–0.8		V
SCD11	Input differential to common mode conversion	100MHz to 7.1GHz		–20		dB
SDD11	Differential input return loss	100MHz to 7.1GHz		–15		dB

(1) All typical values are at 25°C and with 2.5V and 3.3V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%, 3.3V ±5%) (continued)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = HIGH		1200		mV_{pp}
		R_L = 100 Ω, V_{OD} = LOW		600		mV_{pp}
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs		10		mV_{pp}
V_{OCM}	Output common mode voltage	See Figure 5		V_{CC}-0.4		V
$V_{CM,RIP}$	Common mode output ripple	K28.5 pattern at 14.2Gbps on all 4 channels, no interconnect loss, VOD = HIGH		10	20	mV_{RMS}
$V_{OD,RIP}$	Differential path output ripple	K28.5 pattern at 14.2Gbps on all channels, no interconnect loss, VIN = 1200mVpp.			20	mV_{pp}
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			±10		mV
t_R	Rise time(2)	Input signal with 30ps rise time. 20% to 80%. See Figure 7		31		ps
t_F	Fall time(2)	Input signal with 30ps fall time. 20% to 80%. See Figure 7		32		ps
SDD22	Differential output return loss	100MHz to 7.1GHz		–15		dB
SCC22	Common-mode output return loss	100MHz to 7.1GHz		–8		dB
t_{PLH}	Low-to-high propagation delay	See Figure 6		65		ps
t_{PHL}	High-to-low propagation delay			65		ps
$t_{SK(O)}$	Inter-Pair (lane to lane) output skew(3)	All outputs terminated with 100 Ω, See Figure 8		3		ps
$t_{SK(PP)}$	Part-to-part skew(4)	All outputs terminated with 100 Ω			50	ps
r_{OT}	Single ended output resistance	Single ended on-chip termination to VCC. Outputs will be AC coupled.		50		Ω
r_{OM}	Output termination mismatch at 1MHz	$\Delta rom = 2 \times \frac{rp - rn}{rp + rn} \times 100$		5		%
Ch_{iso}	Channel-to-channel isolation	Frequency at 7.1GHz	35	45		dB
OUT_{NOISE}	Output referred noise(5)	10MHz to 7.1GHz. No other noise source present. VOD = LOW		400		µVRMS
		10MHz to 7.1GHz. No other noise source present. VOD = HIGH		500		µVRMS
EQUALIZATION						
EQ_{Gain}	At 7.1GHz input signal	Equalization Gain, EQ = MAX	15	18		dB
Vpre	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measure it on the output signal, Refer Figure 9. Vpre = 20log(V3/V2)		3.75		dB
Vpst	Output post-cursor pre-emphasis	Input signal with 12dB post-cursor and measure it on the output signal, Refer Figure 9. Vpst = 20log(V1/V2)		12		dB
DJ1	Residual deterministic jitter at 10.3125 Gbps	Transmit Side application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0”. See Figure 11		0.016		UIp-p
DJ2	Residual deterministic jitter at 10.3125 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 12” (9dB loss at 5GHz) See Figure 10		0.11		UIp-p
DJ3	Residual Deterministic Jitter at 14.2 Gbps	Transmit Side Application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0”. See Figure 11		0.041		UIp-p
DJ4	Residual Deterministic Jitter at 14.2 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 8” (9dB loss at 7GHz) See Figure 10		0.13		UIp-p

(2) Rise and Fall measurements include board and channel effects of the test environment, refer to Figure 10 and Figure 11
(3) $t_{SK(O)}$ is the magnitude of the time difference between the channels.
(4) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(5) All noise sources added.

PARAMETER MEASUREMENT INFORMATION

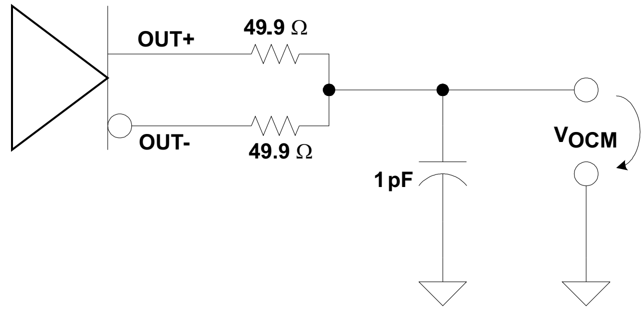


Figure 5. Common Mode Output Voltage Test Circuit

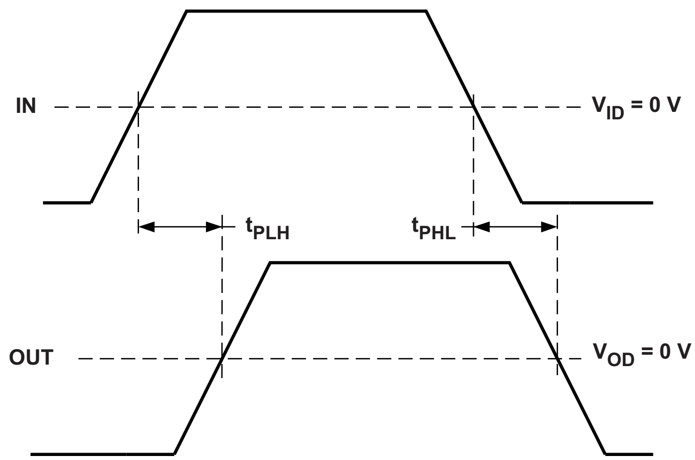


Figure 6. Propagation Delay Input to Output

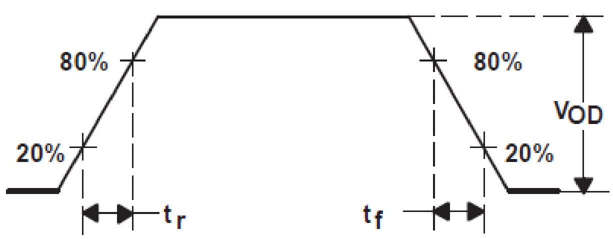


Figure 7. Output Rise and Fall Time

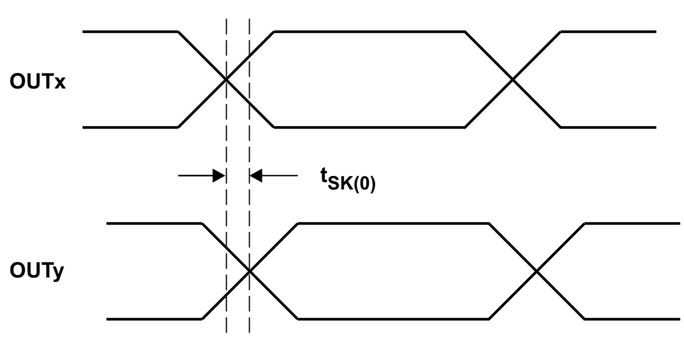


Figure 8. Output Inter-Pair Skew

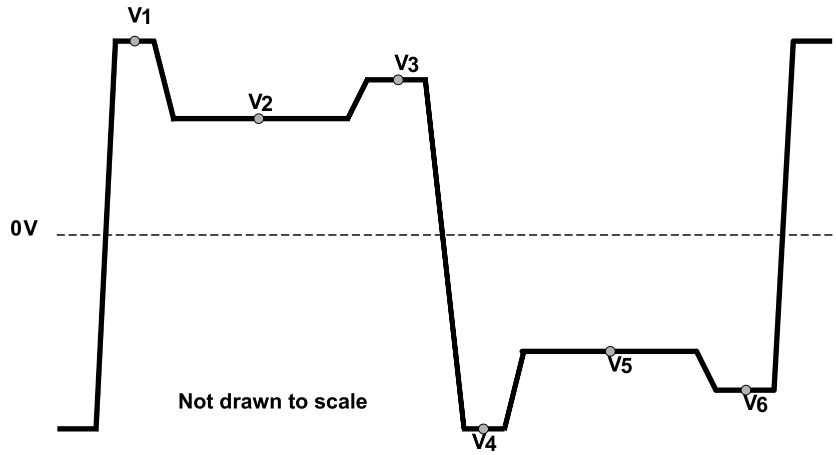


Figure 9. Vpre and Vpost (The test pattern is 1111111100000000 (8-1s, 8-0s))

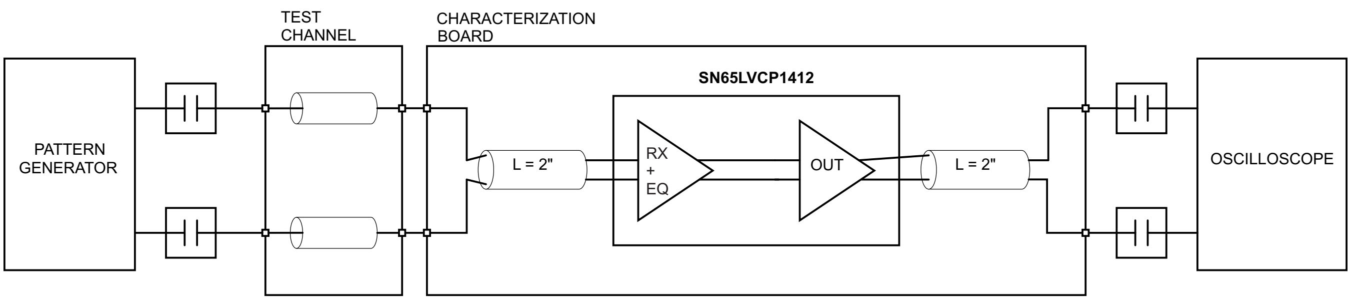


Figure 10. Receive Side Performance Test Circuit

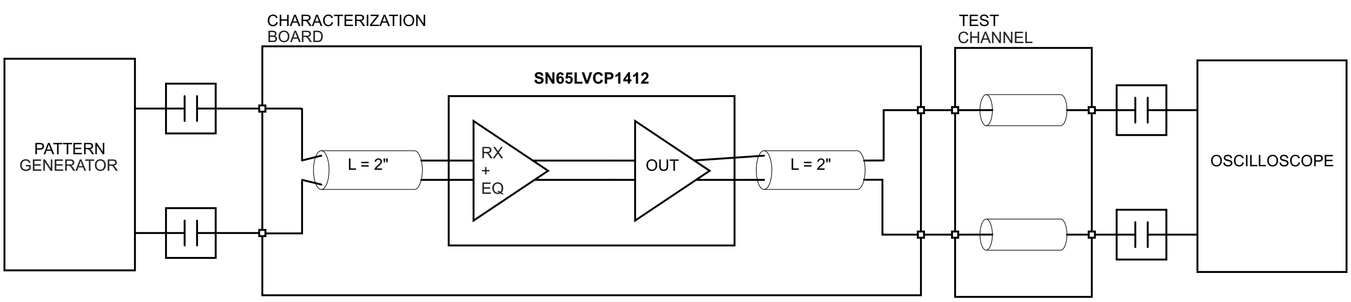


Figure 11. Transmit Side Performance Test Circuit

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

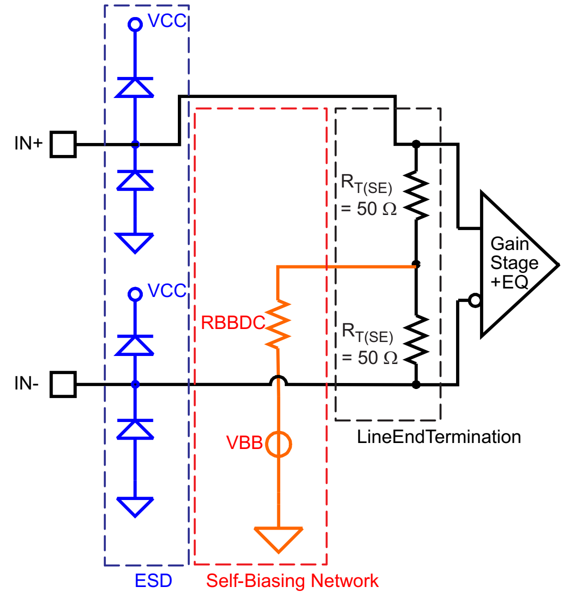


Figure 12. Equivalent Input Circuit Design

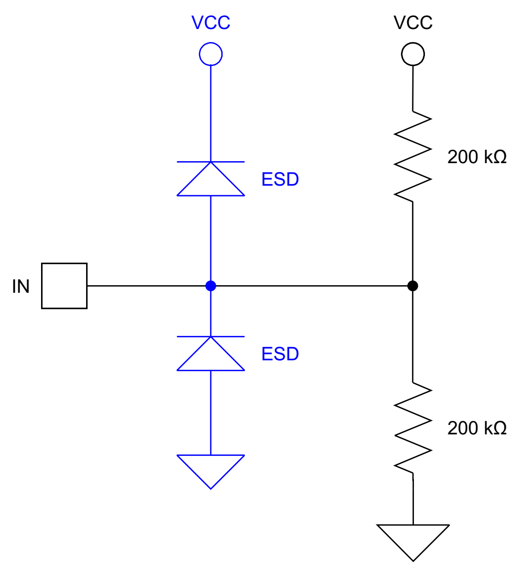


Figure 13. 3-Level Input Biasing Network

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

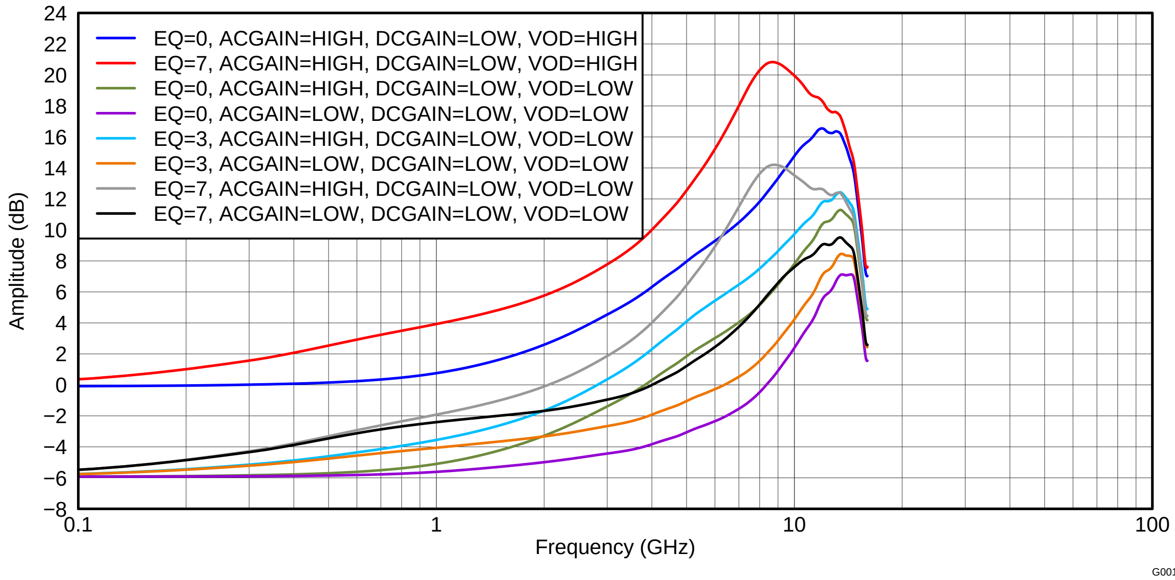


Figure 14. Typical EQ Gain Profile Curve

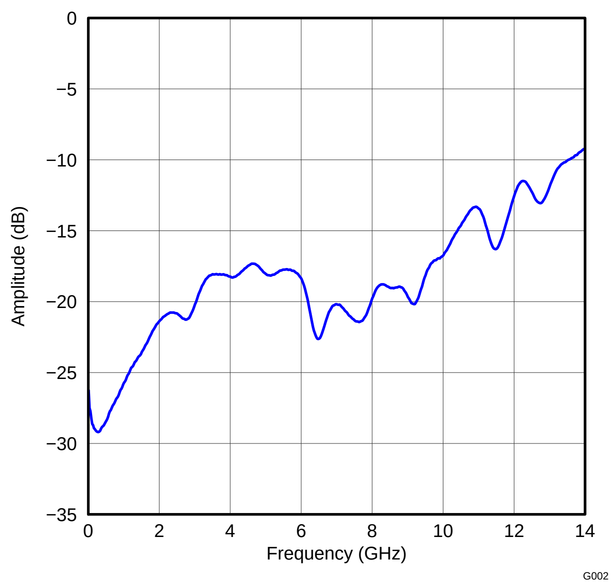


Figure 15. Differential Input Return Loss

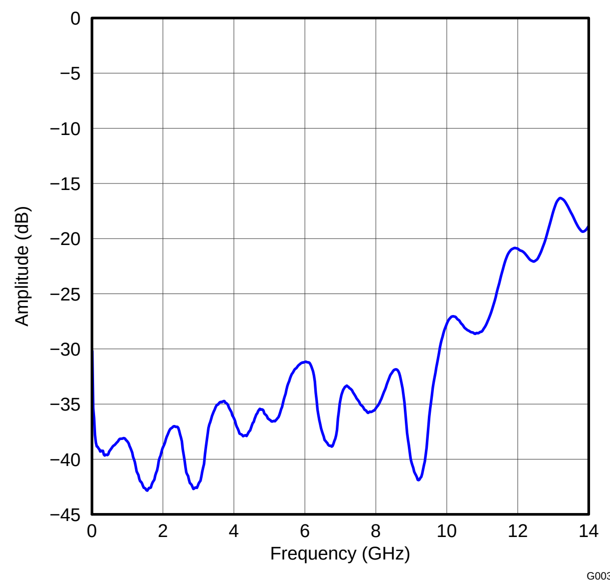


Figure 16. Differential to Common Mode Conversion

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

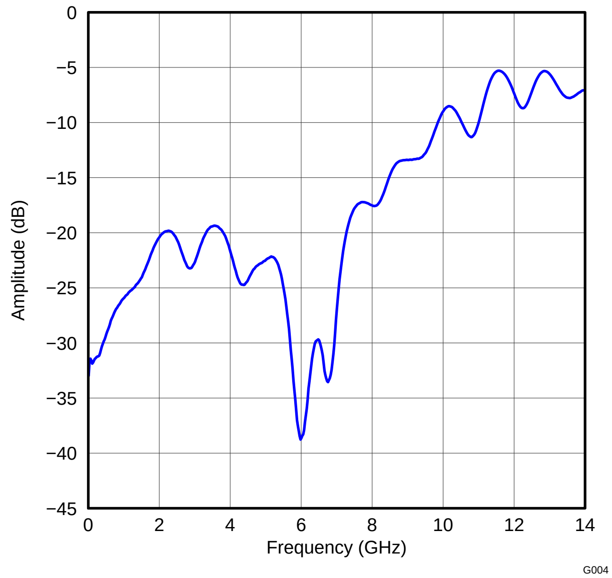


Figure 17. Differential Output Return Loss

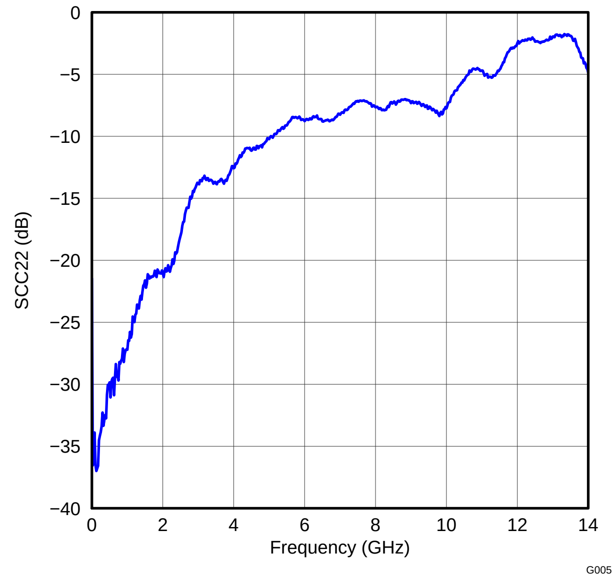
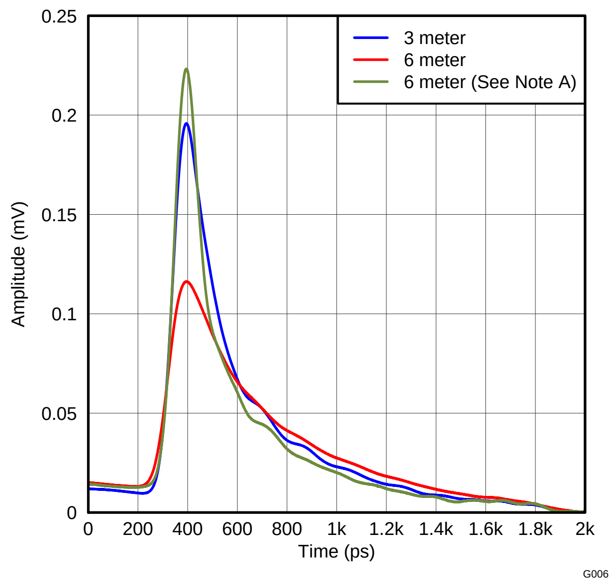
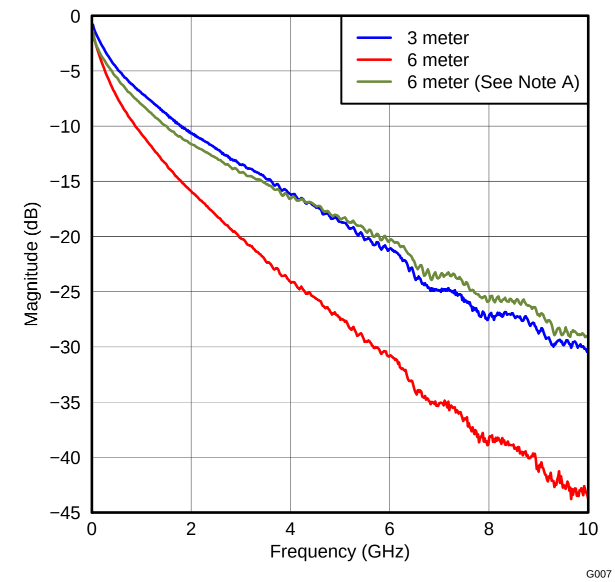


Figure 18. Common Mode Output Return Loss



A. With SN65LVCP1412 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 19. Cable Mode – Symbol Response

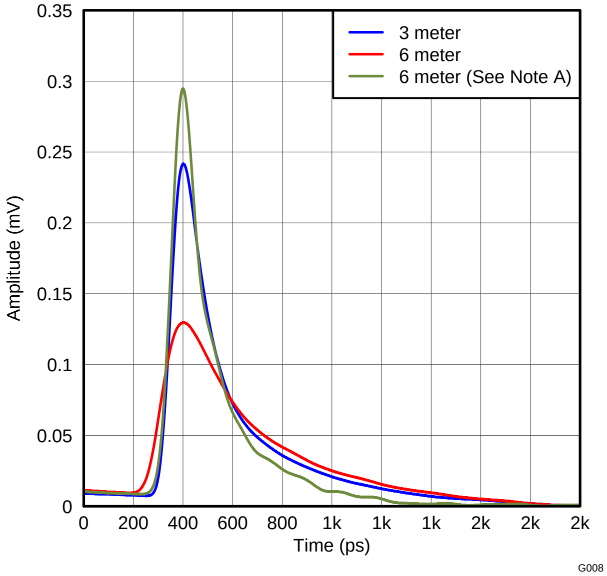


A. With SN65LVCP1412 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 20. Cable Mode – Frequency Domain

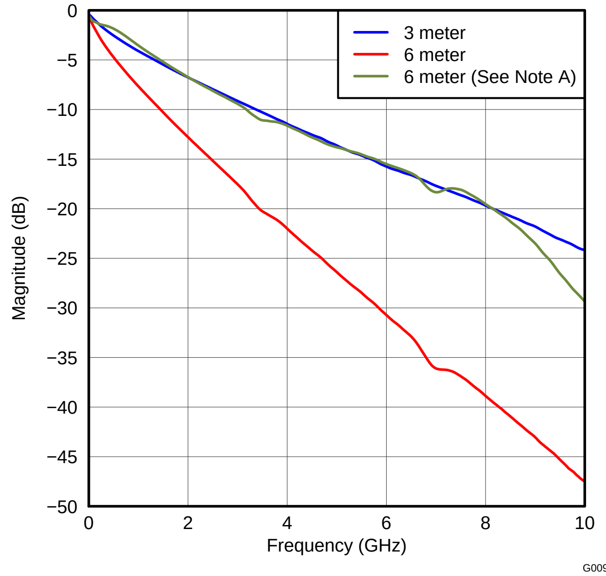
TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).



A. With SN65LVCP1412 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 21. Trace Mode – Symbol Response



A. With SN65LVCP1412 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 22. Trace Mode - Frequency Domain

Table 1. Control Settings Descriptions

MODE	DCGAIN	ACGAIN<1:0>	EQ<2:0>	DC GAIN (dB)	EQ GAIN (dB)	APPLICATION
0	0	00	000 to 111	–6	1 to 9	Short Input Trace; Large Input Swing
0	0	11	000 to 111	–6	7 to 17	Long Input Trace; Large Input Swing
0	1	01	000 to 111	0	1 to 9	Short Input Trace; Small Input Swing
0	1	11	000 to 111	0	2 to 10	Short Input Trace; Small Input Swing
1	0	00	000 to 111	–6	1 to 9	Short Input Cable; Large Input Swing
1	0	11	000 to 111	–6	7 to 17	Long Input Cable; Large Input Swing
1	1	01	000 to 111	0	1 to 9	Short Input Cable; Small Input Swing
1	1	11	000 to 111	0	2 to 10	Short Input Cable; Small Input Swing

Table 2. Control Settings Descriptions

GAIN	DC GAIN	ACGAIN<1:0>
Low	0	00
HighZ	0	11
High	1	01

TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

The SN65LVCP1412 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. The SDA and SCK pins require external 10kΩ pull-ups to VCC.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The SN65LVCP1412 is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0000ADD[2:0]) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7 bit slave address is 0000000.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the SN65LVCP1412 is I^2C compatible. The typical timing is shown in Figure 9 and a complete data transfer is shown in Figure 10. Parameters for Figure 9 are defined in Table 3.

Bus Idle: Both SDA and SCL lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

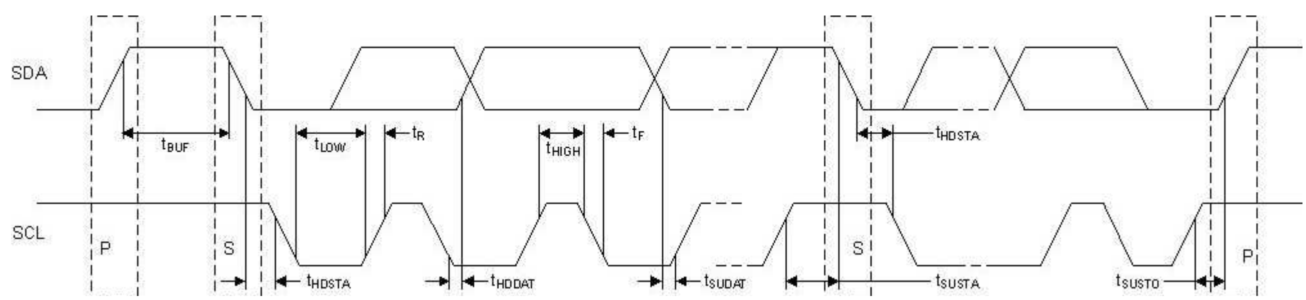


Figure 23. Two-wire Serial Interface Timing Diagram

Table 3. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		μs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		μs
t_{LOW}	Low period of the SCL clock	1.3		μs
t_{HIGH}	High period of the SCL clock	0.6		μs
t_{SUSTA}	Setup time for a repeated START condition	0.6		μs
t_{HDDAT}	Data HOLD time	0		μs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		μs

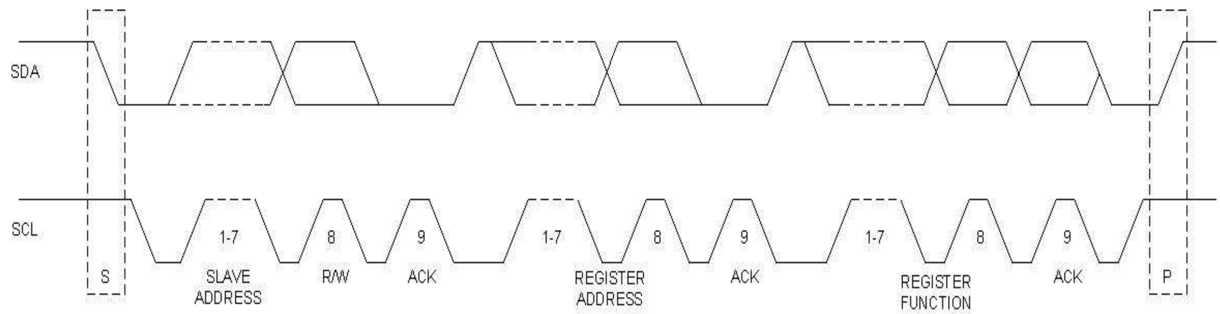


Figure 24. Two-wire Serial Interface Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 22 (0x18) are shown in Table 4. Table 5 describes the circuit functionality based on the register settings.

Table 4. SN65LVCP1412 Register Mapping Information

Register 0x00 (General Device Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	PWRDOWN	SYNC_01	RSVD	SYNC_ALL	EQ_MODE		RSVD
Register 0x01 (Channel Enable) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					LN_EN_CH1	LN_EN_CH0	
Register 0x05 (Channel 0 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x06 (Channel 0 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x08 (Channel 1 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x09 (Channel 1 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x0F Read Only							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Register 0x11 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	RSVD						
Register 0x12 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD							

Table 5. SN65LVCP1412 Register Description

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x00	7	RSVD	Fot TI use only	00000000
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Powerdown	
	5	SYNC_01	All settings from channel 1 will be used for channel 0 and 1: 0 = channel 0 tracking channel 1 settings 1 = no tracking tracking	
	4	RSVD	For TI use only	
	3	SYNC_ALL	All settings from channel 1 will be used on all channels: 0 = all channels tracking channel 1 1 = no channel tracking Overwrites SYNC_01	
	2	EQ_MD	Set EQ Mode: 0 = Cable Mode 1 = Trace Mode	
	1			
	0	RSVD	For TI use only	

Table 5. SN65LVCP1412 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x01	7			00000000
	6			
	5			
	4			
	3			
	2	LN_EN_CH1	Channel 1 Enable: 0 = Enable 1 = Disable	
	1	LN_EN_CH0	Channel 0 Enable: 0 = Enable 1 = Disable	
	0			
0x05 0x08	7	RSVD		00000000
	6	EQ2	Equalizer Adjustment Setting 000 = Minimum equalization setting 111 = Maximum equalization setting	
	5	EQ1		
	4	EQ0		
	3	VOD_CTRL	Channel [x] VOD control: 0 = low VOD range 1 = high VOD range	
	2	DC_GAIN_CTRL	Channel [x] EQ DC Gain: 0 = set EQ DC Gain to 0.5x 1 = set EQ DC Gain to 1x	
	1	AC_GAIN_CTRL1	AC Gain Control: 00 = Low 01 = HiZ 11 = High	
	0	AC_GAIN_CTRL0		
0x06 0x09	7			00000000
	6			
	5			
	4			
	3			
	2	DRV_PEAK	Channel [x] Driver Peaking: 0 = disables driver Peaking 1 = enables driver 6db AC Peaking	
	1	EQ_EN	Channel [x] EQ stage enable: 0 = Enable 1 = Disable	
	0	DRV_EN	Channel [x] Driver stage enable: 0 = Enable 1 = Disable	
0x0F	7	RSVD	For TI use only	00110000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	

Table 5. SN65LVCP1412 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x11	7			00000000
	6	RSVD	For TI use only	
	5			
	4			
	3			
	2			
	1			
	0			
0x12	7	RSVD	For TI use only	00000000
	6			
	5			
	4			
	3			
	2			
	1			
	0			

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVCP1412RLHR	ACTIVE	WQFN	RLH	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	LVCP 1412	Samples
SN65LVCP1412RLHT	ACTIVE	WQFN	RLH	24	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	LVCP 1412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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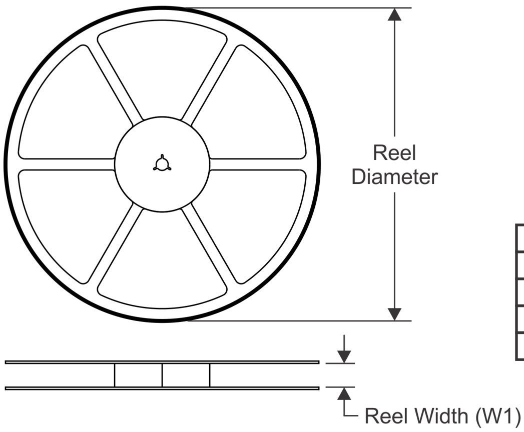
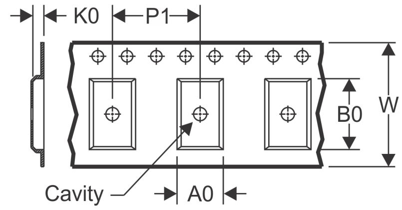
TAPE AND REEL INFORMATION

REEL DIMENSIONS

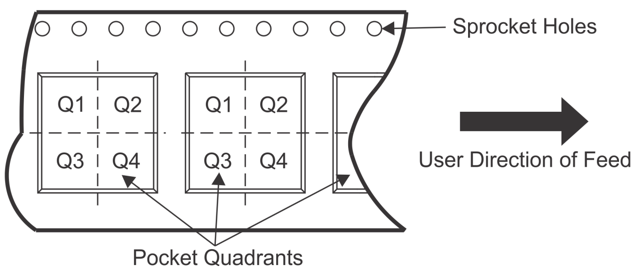


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

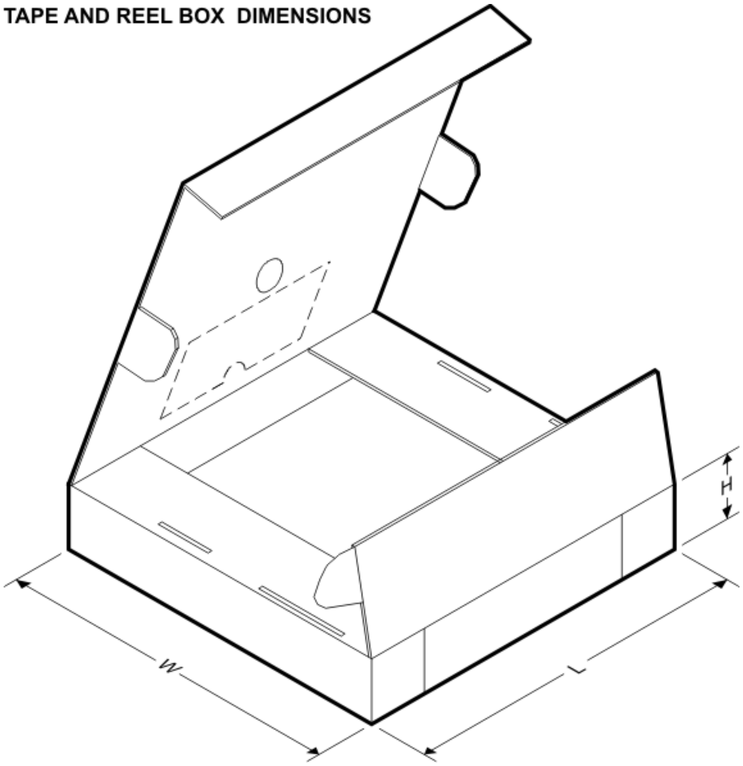
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP1412RLHR	WQFN	RLH	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
SN65LVCP1412RLHT	WQFN	RLH	24	250	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

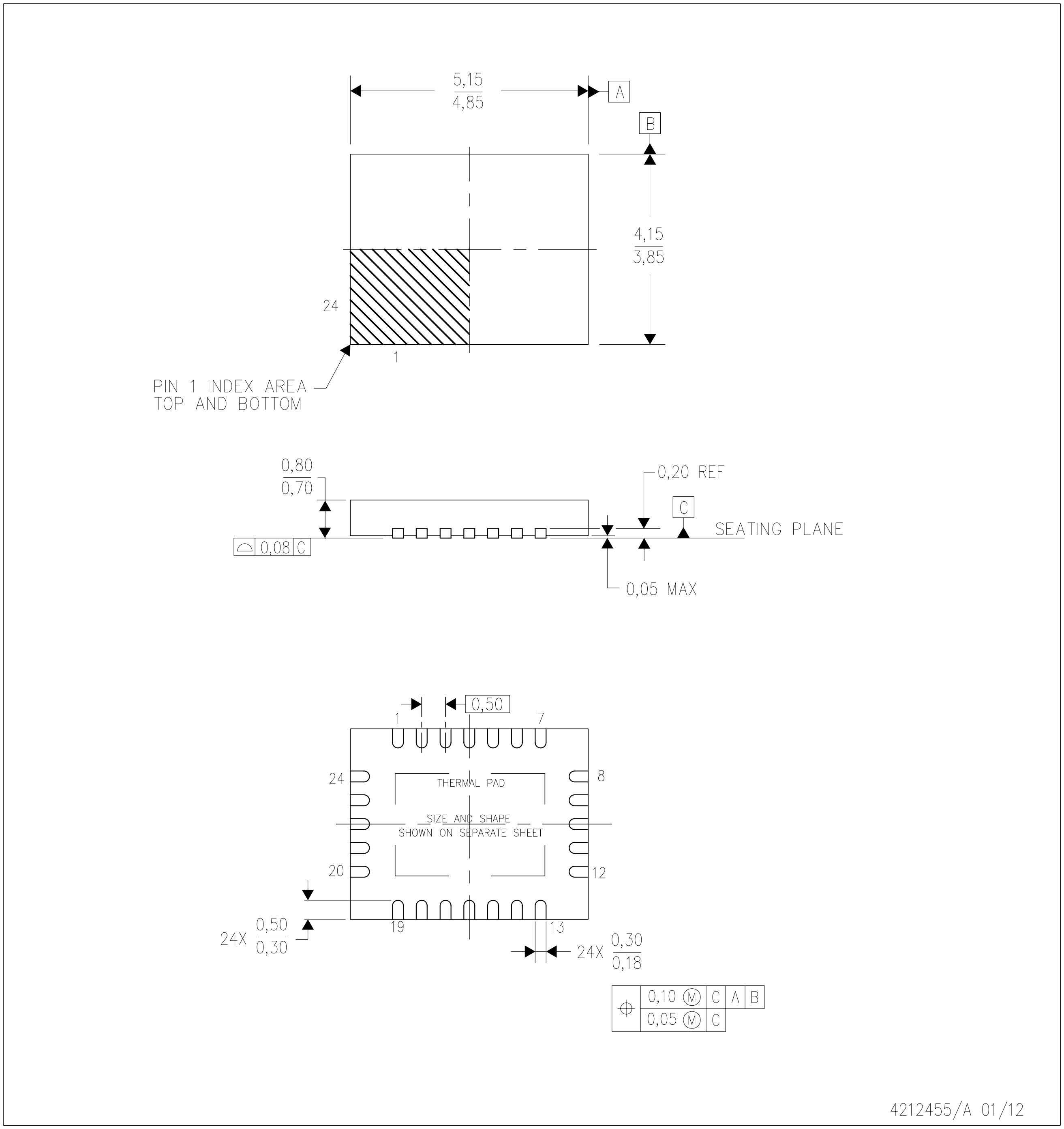
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP1412RLHR	WQFN	RLH	24	3000	338.1	338.1	20.6
SN65LVCP1412RLHT	WQFN	RLH	24	250	338.1	338.1	20.6

RLH (R–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

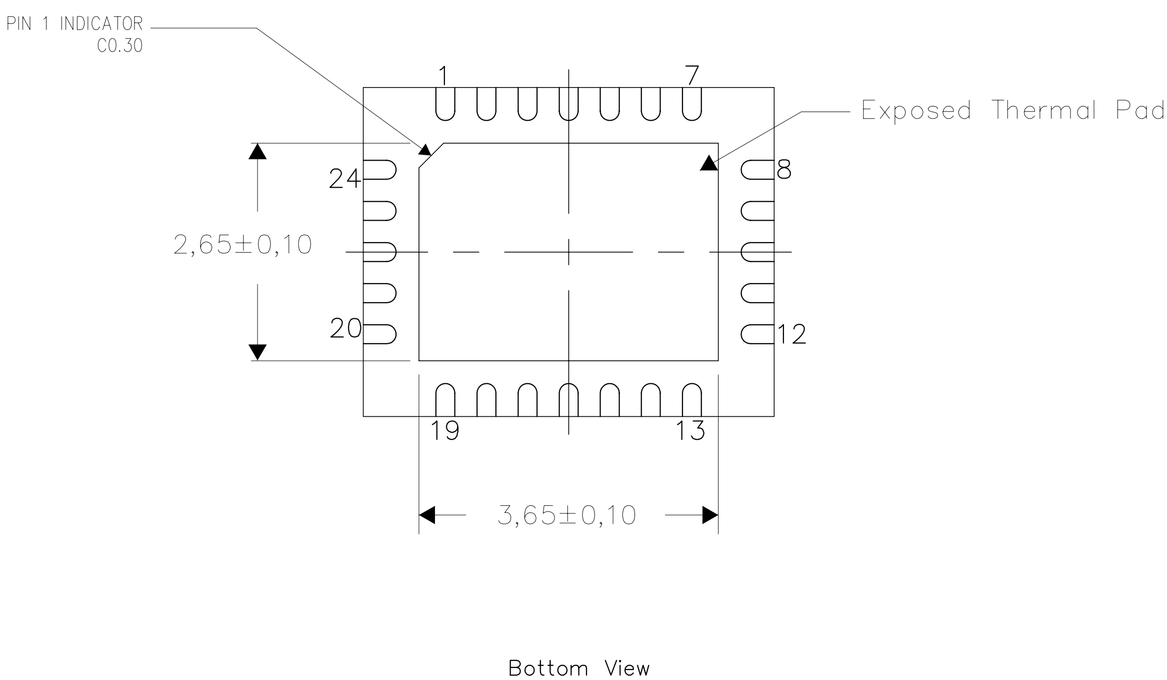
RLH (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

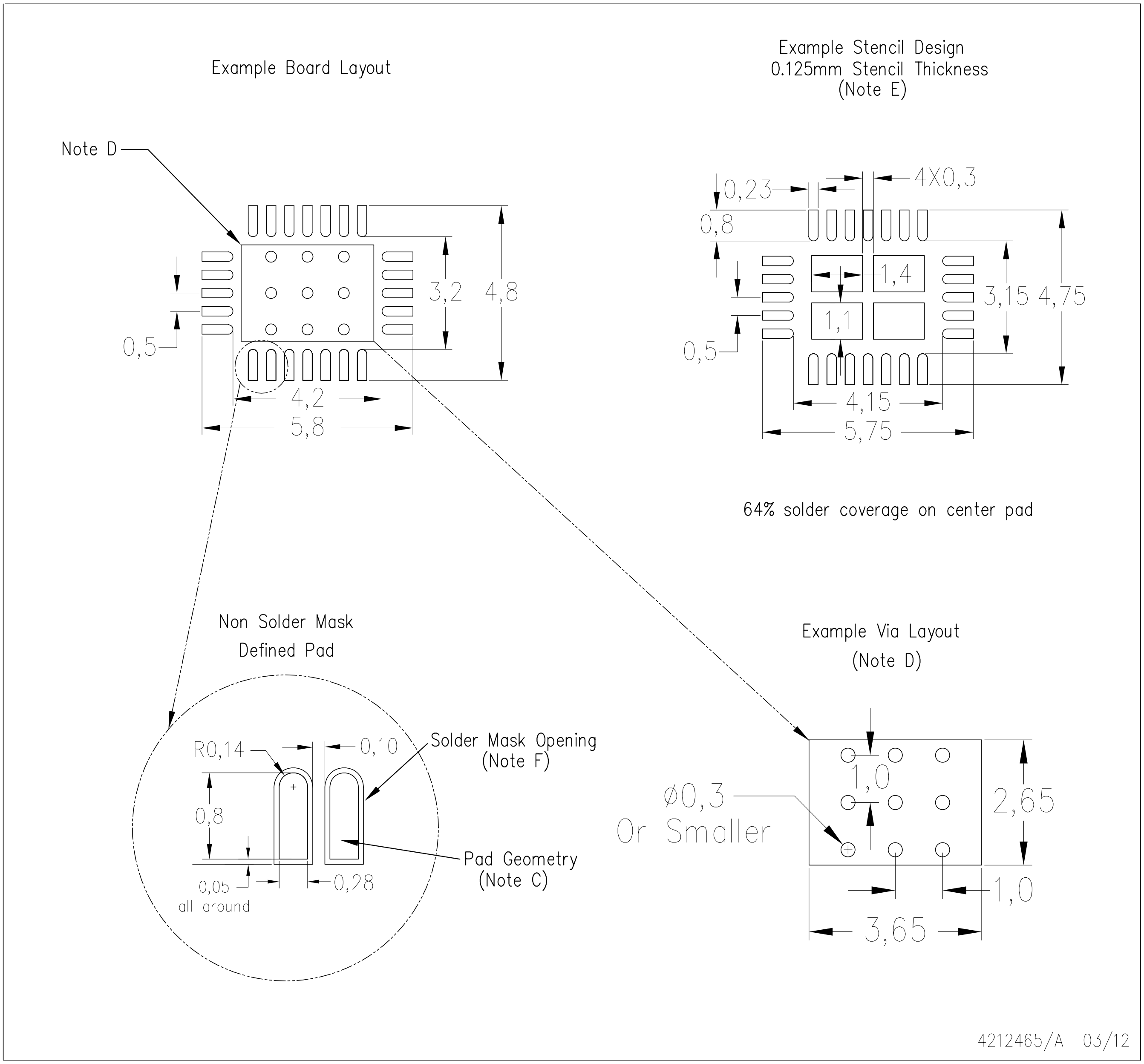


Exposed Thermal Pad Dimensions

4212464/A 03/12

NOTE: All linear dimensions are in millimeters

RLH (R−PVQFN−N24) PLASTIC QUAD FLATPACK NO−LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC−7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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