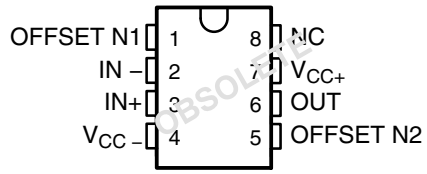
The TL087, TL088, and TL287 are obsolete and are no longer supplied.

TL087, TL088, TL287, TL288
JFET-INPUT OPERATIONAL AMPLIFIERS

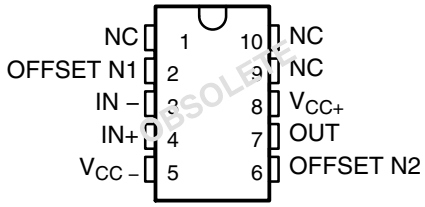
SLOS082B – MARCH 1979 REVISED – JULY 2004

- **Low Input Offset Voltage . . . 0.5 mV Max**
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 18 V/μs Typ**
- **Low Total Harmonic Distortion 0.003% Typ**

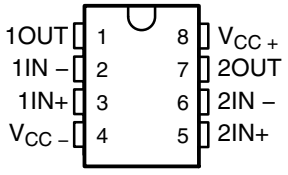
TL087, TL088
D, JG, OR P PACKAGE
(TOP VIEW)



TL088M
U PACKAGE
(TOP VIEW)

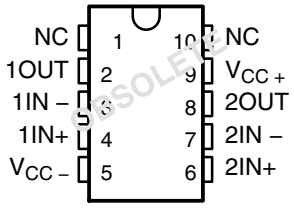


TL287, TL288
JG OR P PACKAGE
(TOP VIEW)



NC – No internal connection

TL288M
U PACKAGE
(TOP VIEW)



description/ordering information

These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset currents, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

The C-suffix devices are characterized for operation from 0°C to 70°C, and the I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

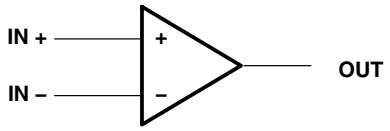
ORDERING INFORMATION

T_A	TYPE	V_{IO} MAX AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	Dual	1 mV	PDIP (P)	Tube of 50	TL288CP	TL288CP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

The TL087, TL088, and TL287 are obsolete and are no longer supplied.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, VCC+ (see Note 1)		18	18	18	V
Supply voltage, V_{CC}– (see Note 1)		–18	–18	–18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Input current, I_I (each Input)		±1	±1	±1	mA
Output current, I_O (each output)		±80	±80	±80	mA
Total V_{CC}+ terminal current		160	160	160	mA
Total V_{CC}– terminal current		–160	–160	–160	mA
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Maximum junction temperature, T_J			150	150	°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	P package		85	85	°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	300	°C
Storage temperature range, T_{stg}		–65 to 150	–65 to 150	–65 to 150	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
8. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
9. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

The TL087, TL088, and TL287 are obsolete and are no longer supplied.

recommended operating conditions

			C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		±5	±5	±5	±5	±5	±15	V
V_{IC}	Common-mode input voltage	$V_{CC\pm}$ = ±5 V	−1	4	−1	4	−1	4	V
		$V_{CC\pm}$ = ±15 V	−11	11	−11	11	−11	11	
V_I	Input voltage	$V_{CC\pm}$ = ±5 V	−1	4	−1	4	−1	4	V
		$V_{CC\pm}$ = ±15 V	−11	11	−11	11	−11	11	
T_A	Operating free-air temperature		0	70	−40	85	−55	125	°C

operating characteristics $V_{CC} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL088M, TL288M			TL087I, TL087C TL088I, TL088C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, A_{VD} = 1		18		8	18		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		55			55		ns
	Overshoot factor	C_L = 100 pF,	A_{VD} = 1		25			25		%
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		19			19		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL088M TL288M			TL087I TL088I TL287I TL288I			TL087C TL088C TL287C TL288C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, V_O = 0, T_A = 25°C	TL087, TL287					0.1	0.5		0.1	0.5	mV
			TL088, TL288		0.1	3		0.1	1		0.1	1	
		R_S = 50 Ω, V_O = 0, T_A = full range	TL087, TL287						2			1.5	
			TL088, TL288			6			3			2.5	
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = 25°C to MAX		10			8			8		µV/°C
I_{IO}	Input offset current	T_A = 25°C			5			5	100		5	100	pA
		T_A = full range				25			3			2	nA
I_{IB}	Input bias current‡	T_A = 25°C			30			30	200		30	200	pA
		T_A = full range				100			20			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		(V_{CC-}) +4 to (V_{CC+}) −4			(V_{CC-}) +4 to (V_{CC+}) −4			(V_{CC-}) +4 to (V_{CC+}) −4			V
$V_{O(PP)}$	Maximum-peak-to-peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq$ 10 kΩ	24			24			24			
			$R_L \geq$ 2 kΩ	20			20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, T_A = 25°C	V_O = ±10 V,	50	105		50	105		50	105		V/mV
		$R_L \geq$ 2 kΩ, T_A = full range	V_O = ±10 V,	25			25			25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common–mode rejection ratio	R_S = 50 Ω, $V_{IC} = V_{ICR}$ min, T_A = 25°C	V_O = 0 V,	80	93		80	93		80	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	R_S = 50 Ω, $V_{CC\pm}$ = ±9 V to ±15 V, T_A = 25°C	V_O = 0 V,	80	99		80	99		80	99		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0 V,		26	2.8		2.6	2.8		2.6	2.8	mA

† All characteristics are measured under open–loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is −55°C to 125°C for TL_88M; −40°C to 85°C for TL_8_I; and 0°C to 70°C for TL_8_C.

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

TEXAS INSTRUMENTS
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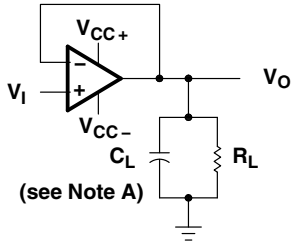
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

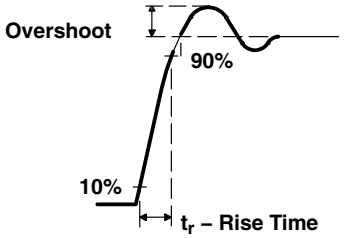


Figure 2. Rise Time and Overshoot Waveform

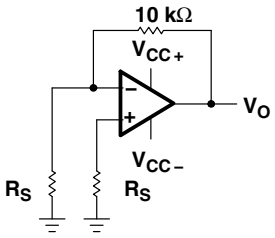
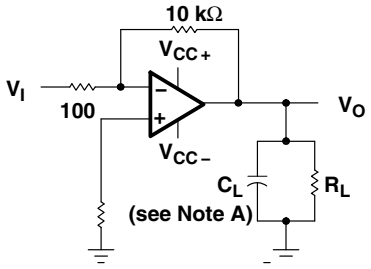


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Brandwidth and Phase Margin Test Circuit

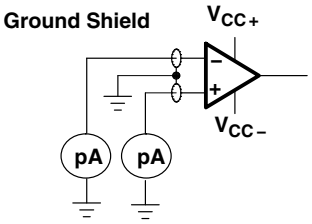


Figure 5. Input Bias and Offset Current Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of these JFET operational amplifiers, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device then is inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements then are subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	6, 7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Common-mode input voltage range limits	vs V_{CC} vs Temperature	10 11
V_{ID}	Differential input voltage	vs Output voltage	12
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	13 17 14, 15, 16 18
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	19 20 21
z_o	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	22 23
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	25
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	26 27 28
I_{CC}	Supply current	vs V_{CC} vs Temperature	29 30
SR	Slew rate	vs R_L vs Temperature	31 32
	Overshoot factor	vs C_L	33
V_n	Equivalent input noise voltage	vs Frequency	34
THD	Total harmonic distortion	vs Frequency	35
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	36 37
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	38 39 40
	Phase shift	vs Frequency	20
	Pulse response	Small-signal Large-signal	41 42

TYPICAL CHARACTERISTICS†

**DISTRIBUTION OF TL088
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

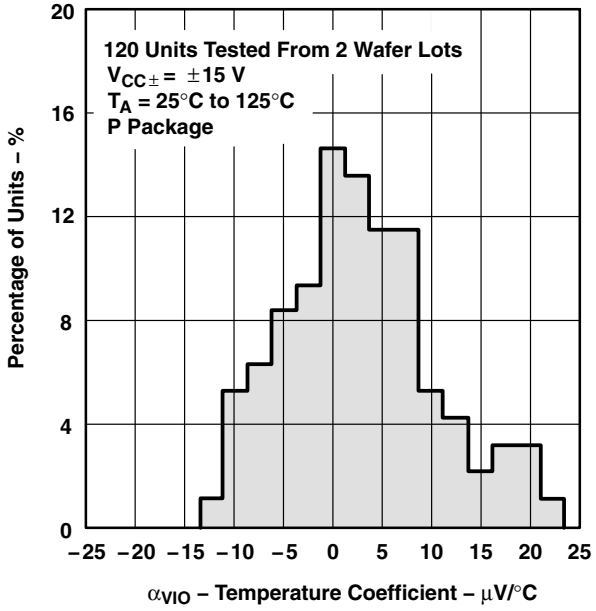


Figure 6

**DISTRIBUTION OF TL288
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

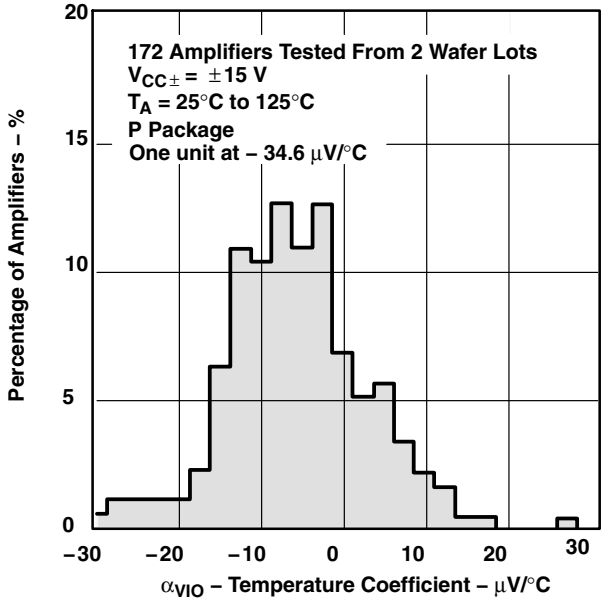


Figure 7

**INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

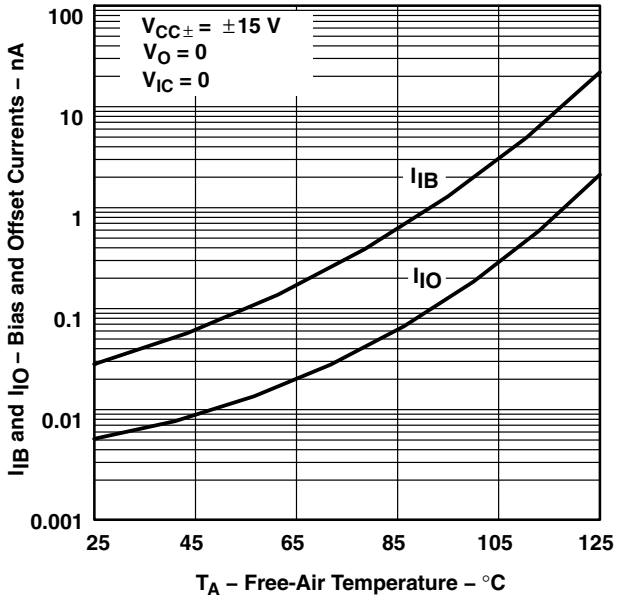


Figure 8

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

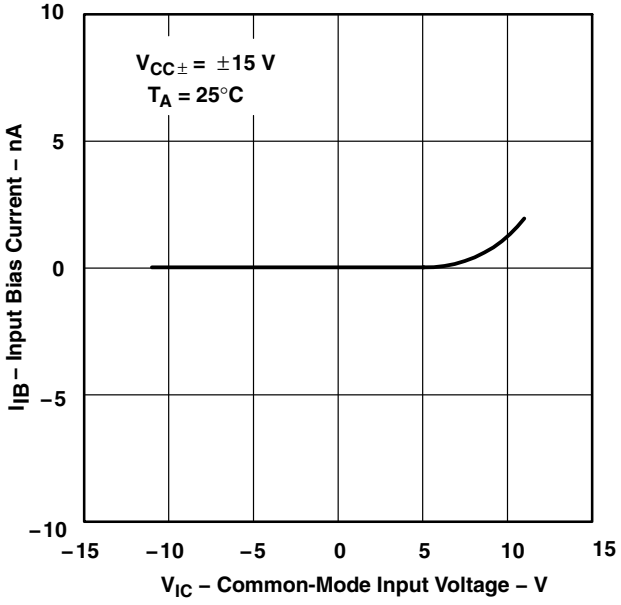


Figure 9

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs SUPPLY VOLTAGE

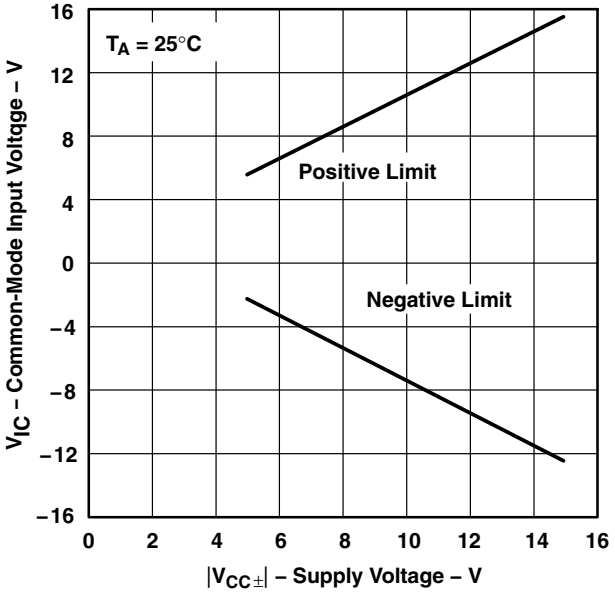


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs FREE-AIR TEMPERATURE

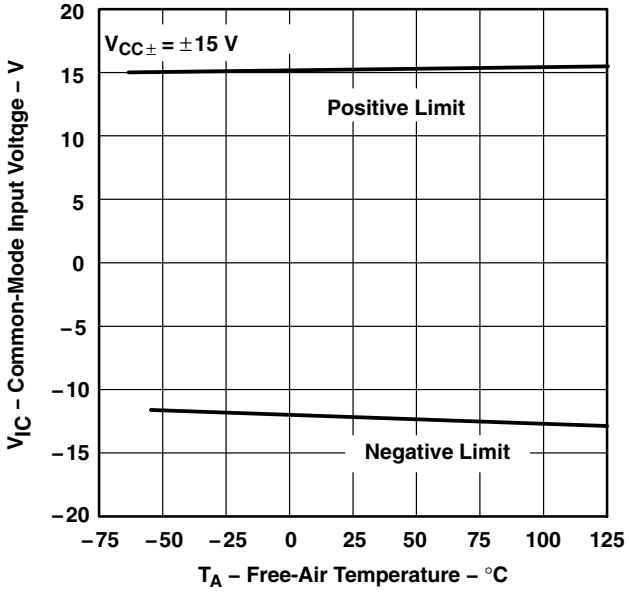


Figure 11

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

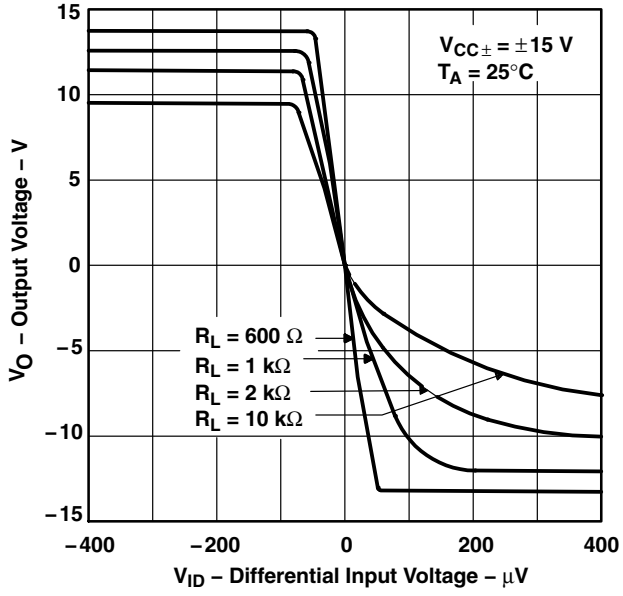


Figure 12

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

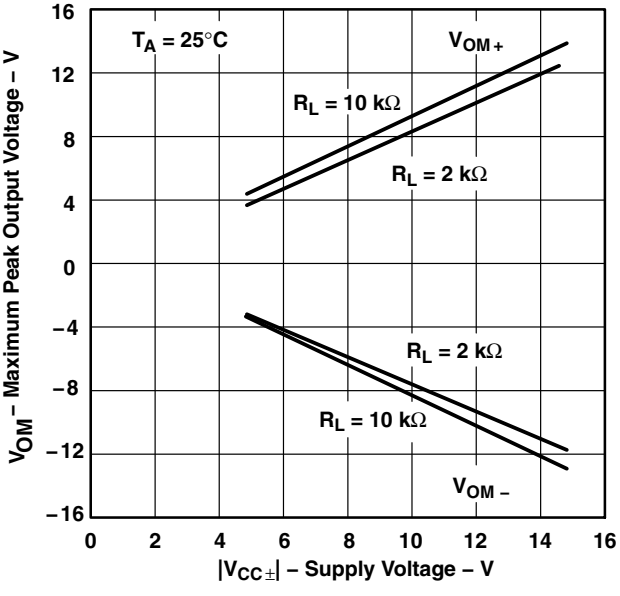


Figure 13

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

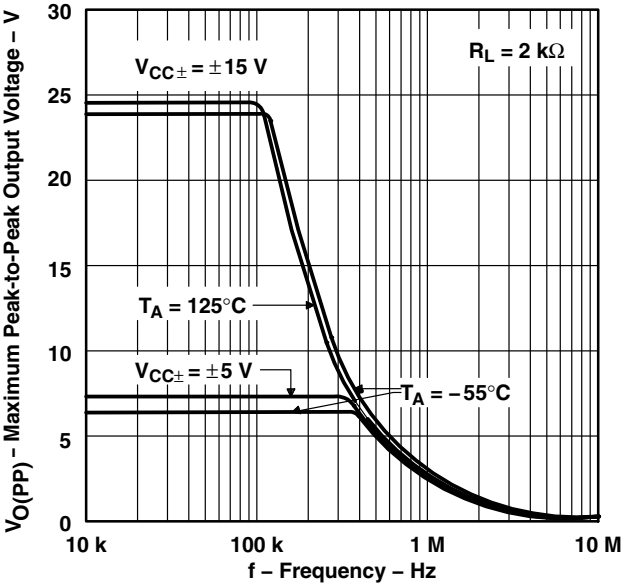


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

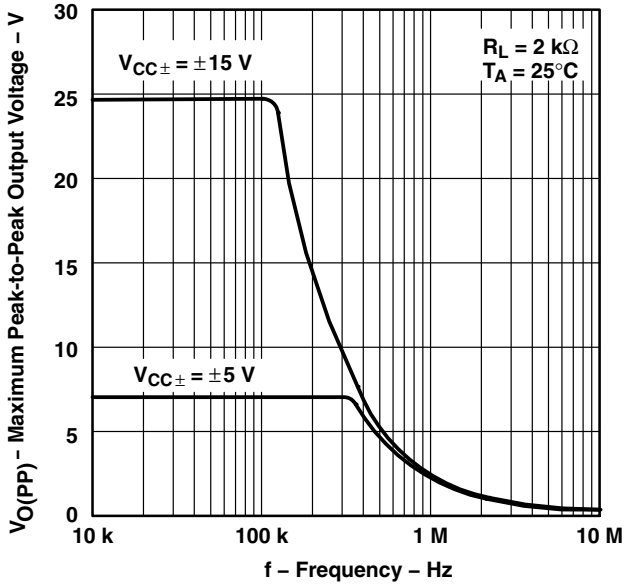


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

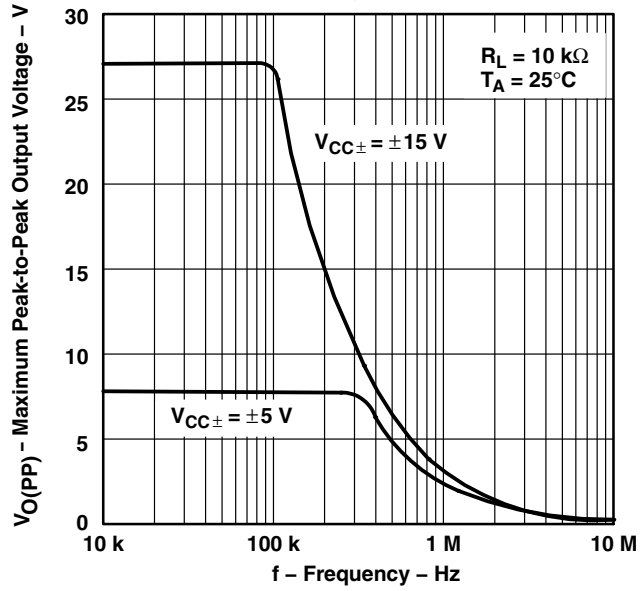


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

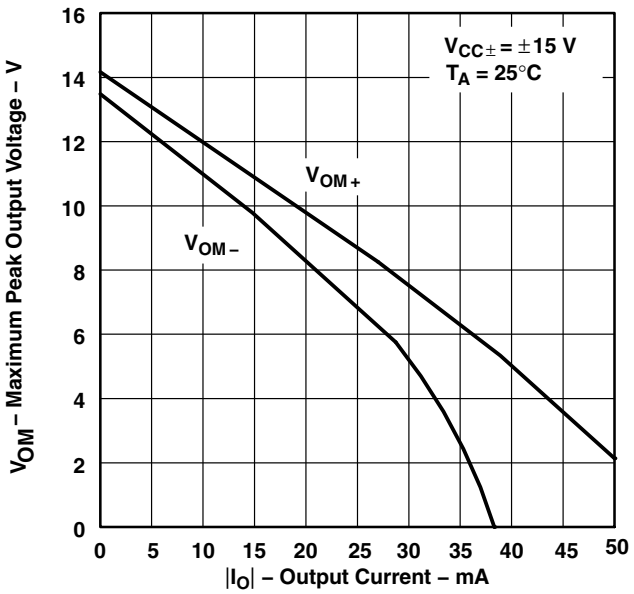


Figure 17

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

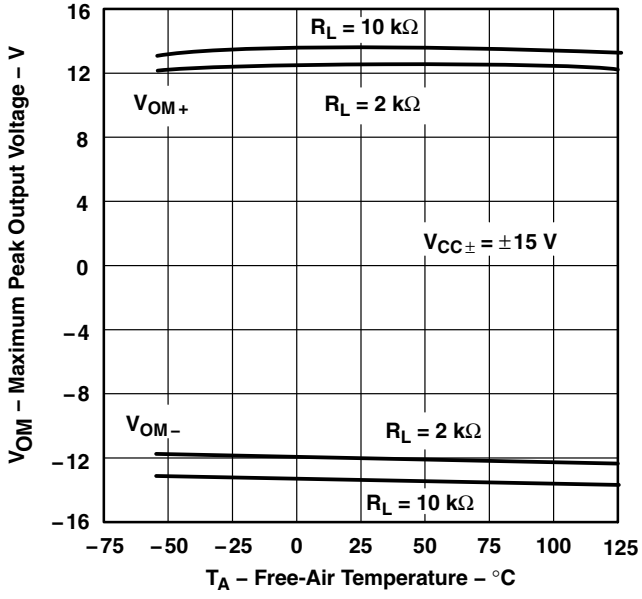


Figure 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

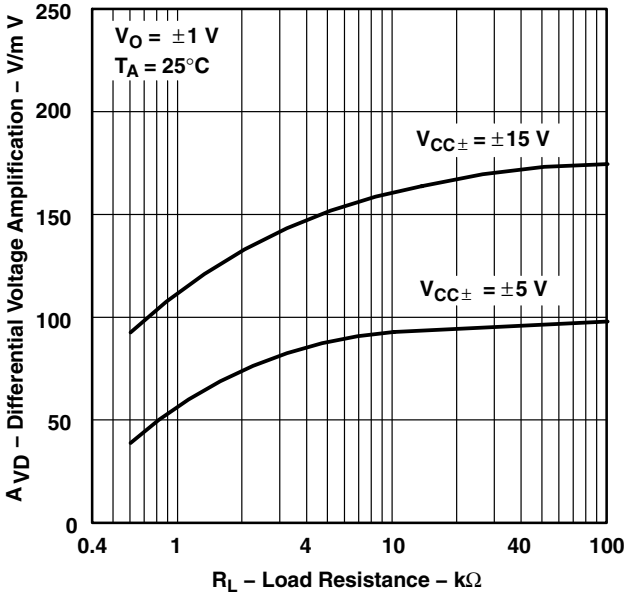


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

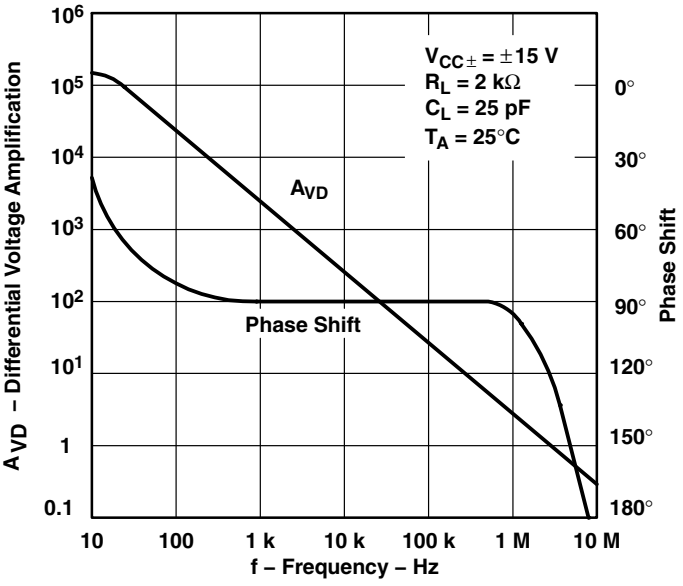


Figure 20

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

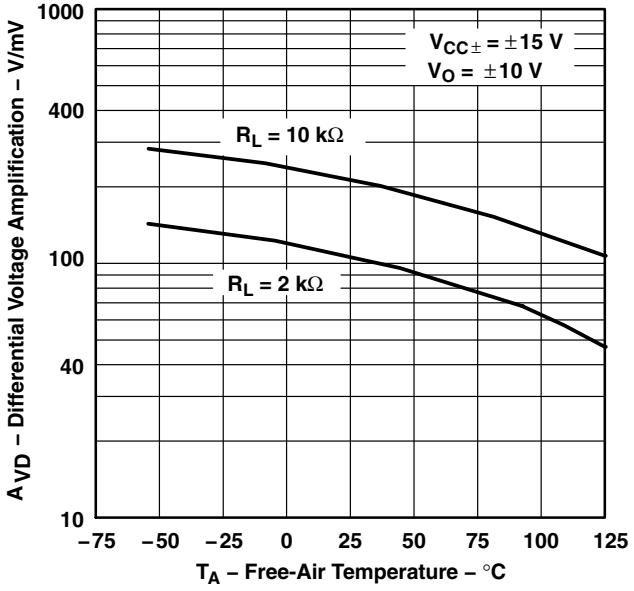


Figure 21

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

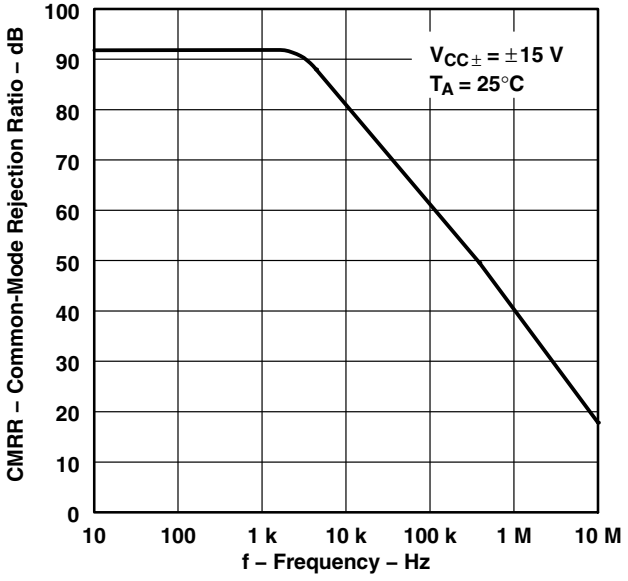


Figure 22

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

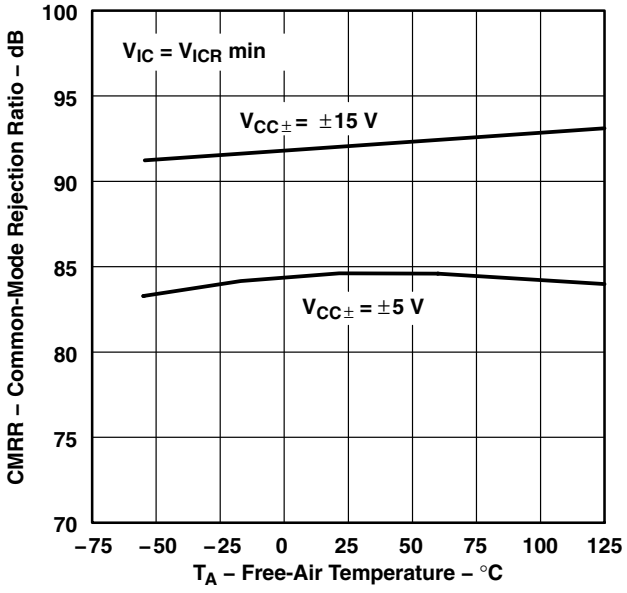


Figure 23

OUTPUT IMPEDANCE vs FREQUENCY

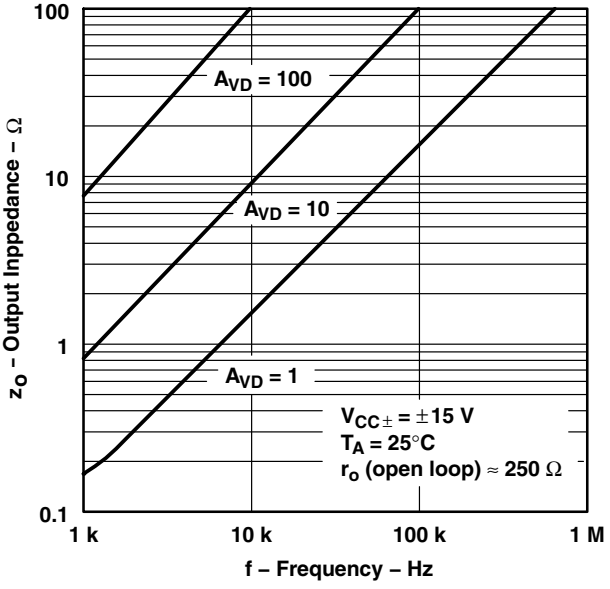


Figure 24

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

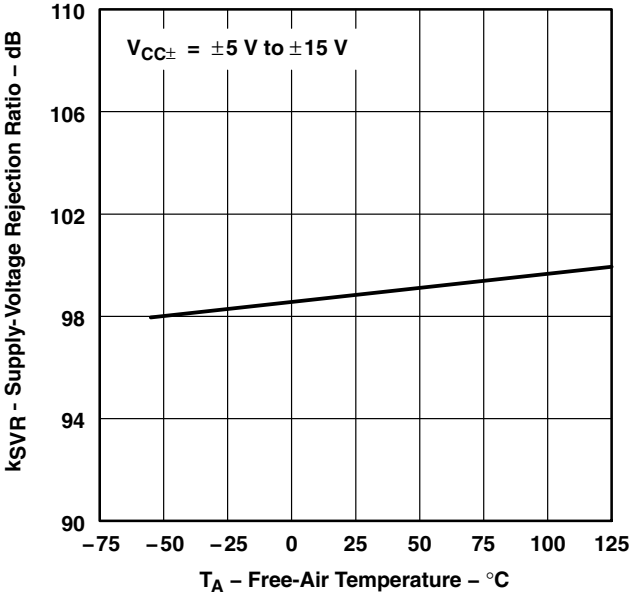


Figure 25

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

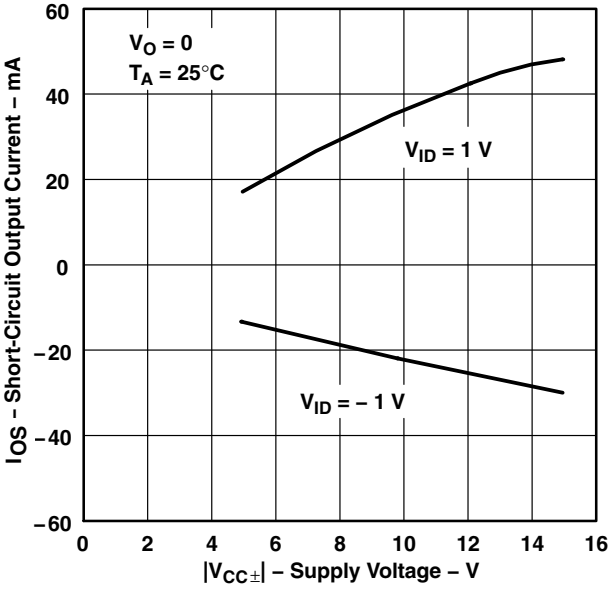


Figure 26

SHORT-CIRCUIT OUTPUT CURRENT vs TIME

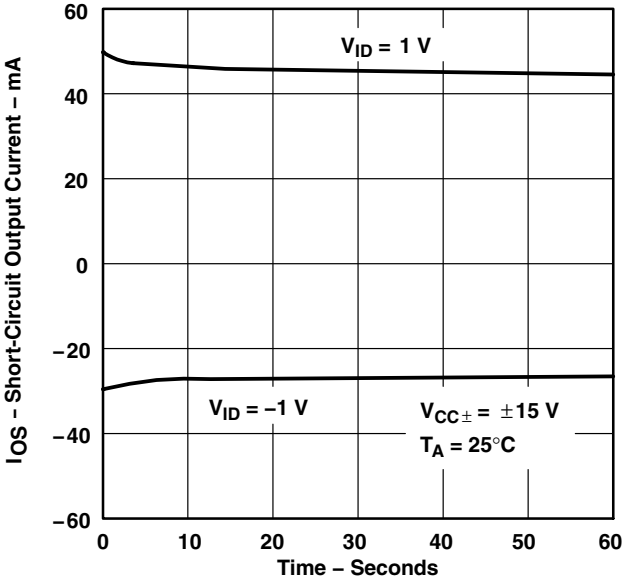


Figure 27

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

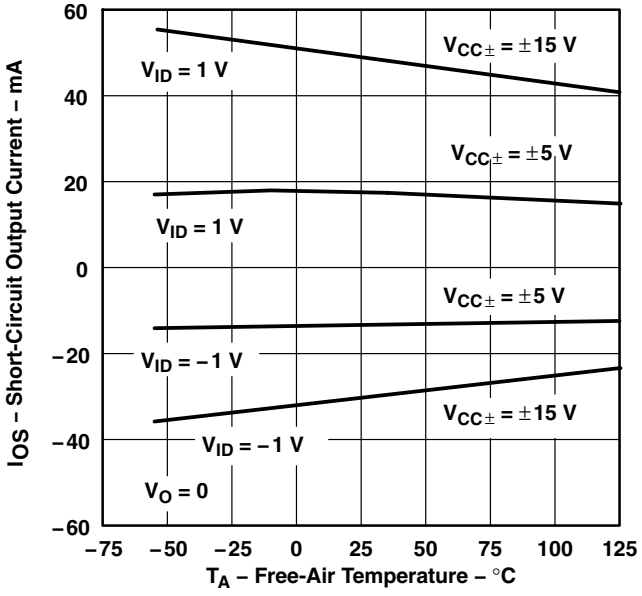


Figure 28

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

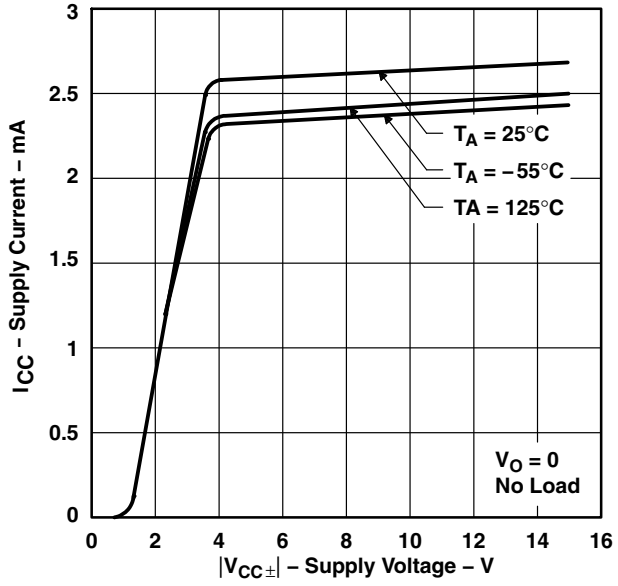


Figure 29

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

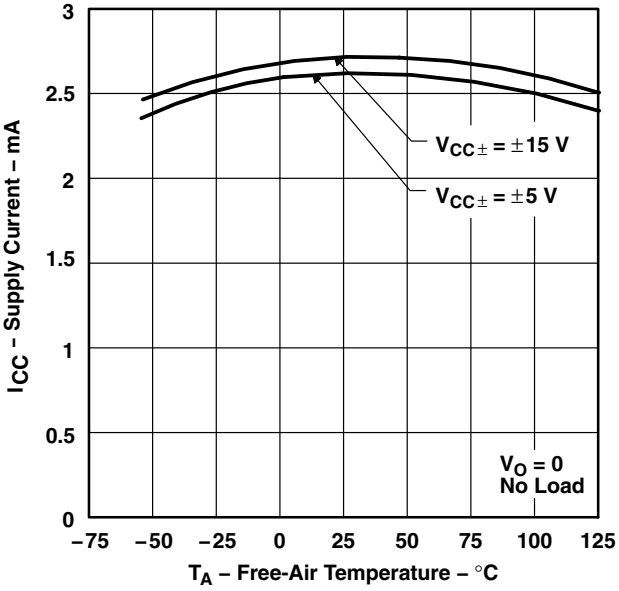


Figure 30

SLEW RATE vs LOAD RESISTANCE

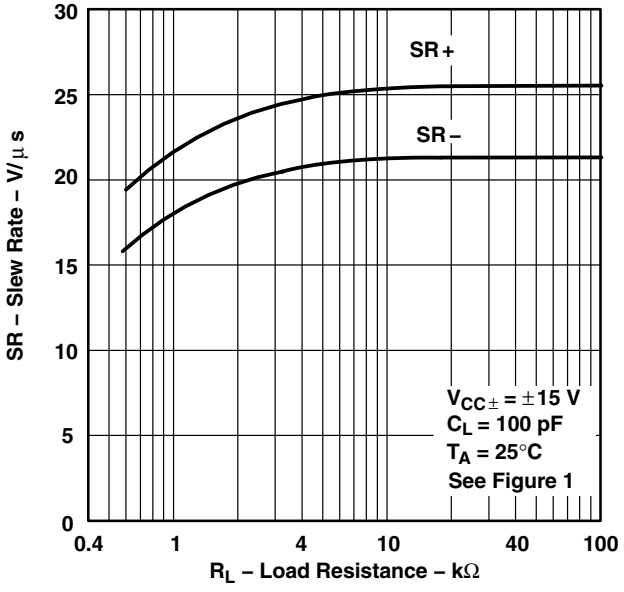


Figure 31

SLEW RATE vs FREE-AIR TEMPERATURE

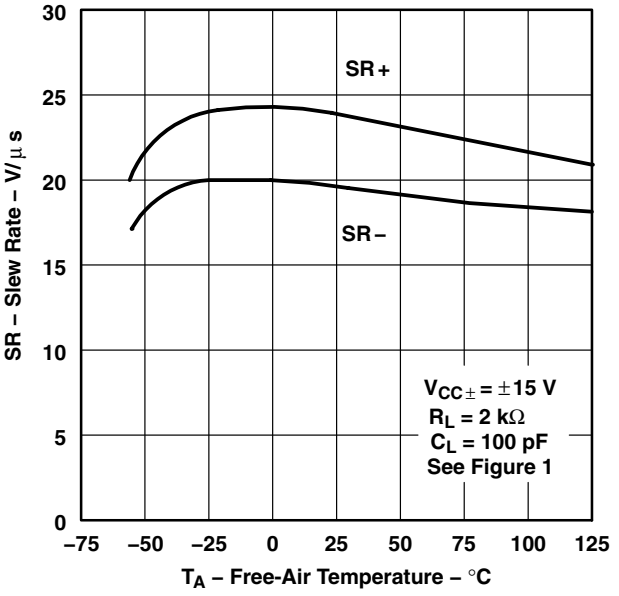


Figure 32

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OVERSHOOT FACTOR vs LOAD CAPACITANCE

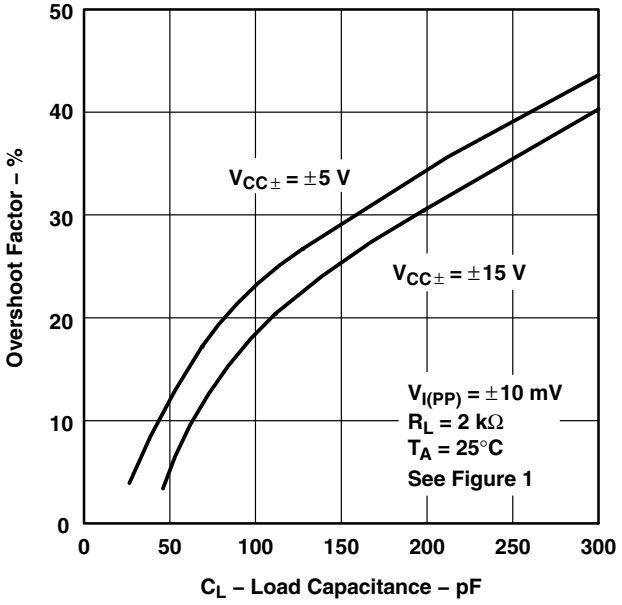


Figure 33

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

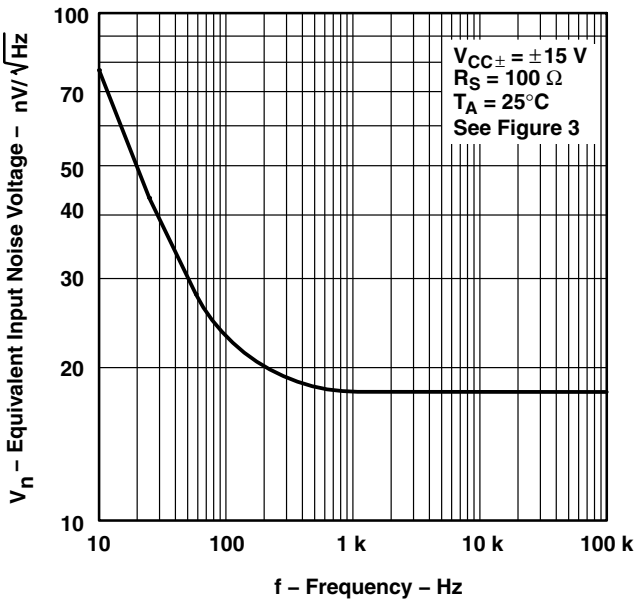


Figure 34

TOTAL HARMONIC DISTORTION vs FREQUENCY

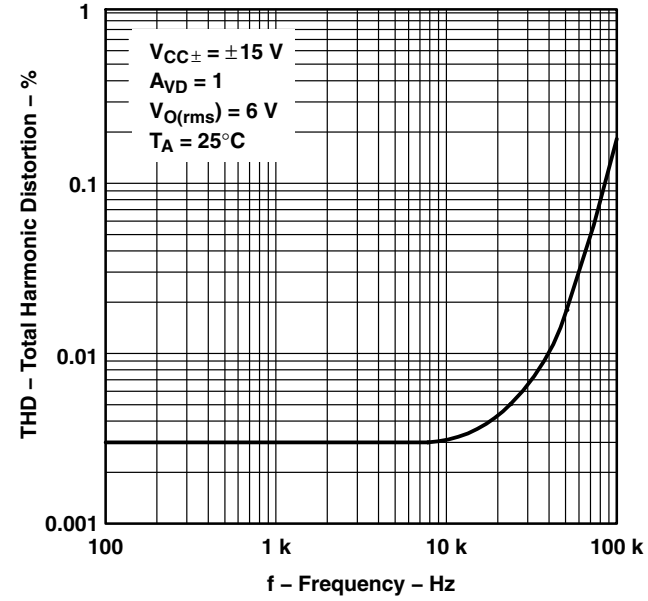


Figure 35

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

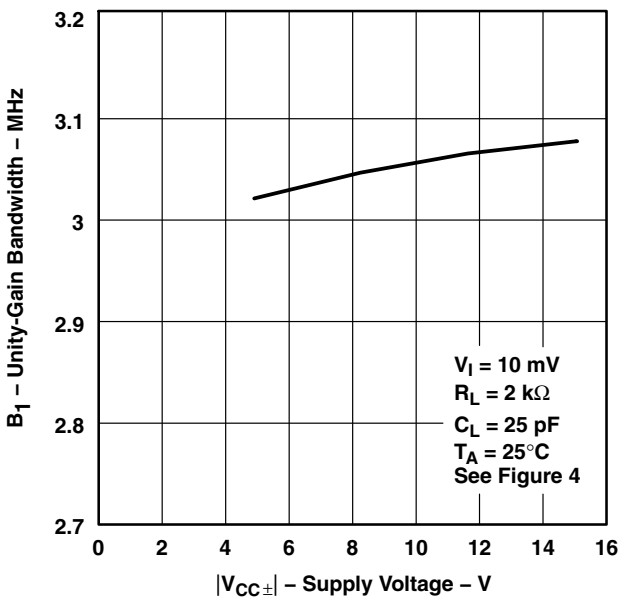


Figure 36

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

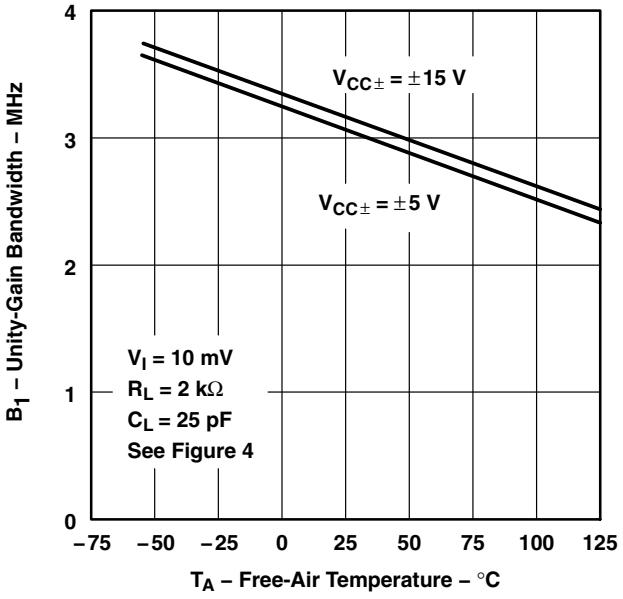


Figure 37

PHASE MARGIN vs SUPPLY VOLTAGE

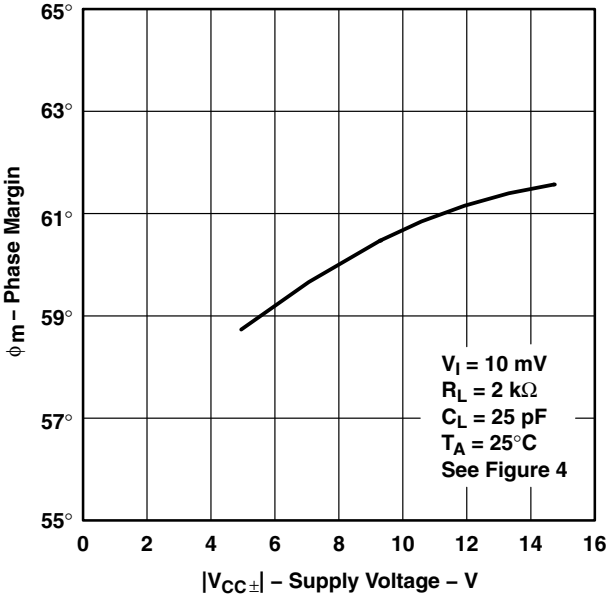


Figure 38

PHASE MARGIN vs LOAD CAPACITANCE

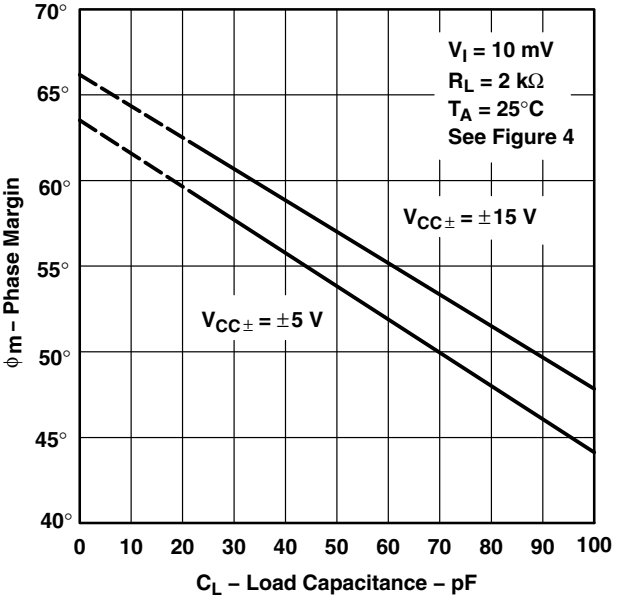


Figure 39

PHASE MARGIN vs FREE-AIR TEMPERATURE

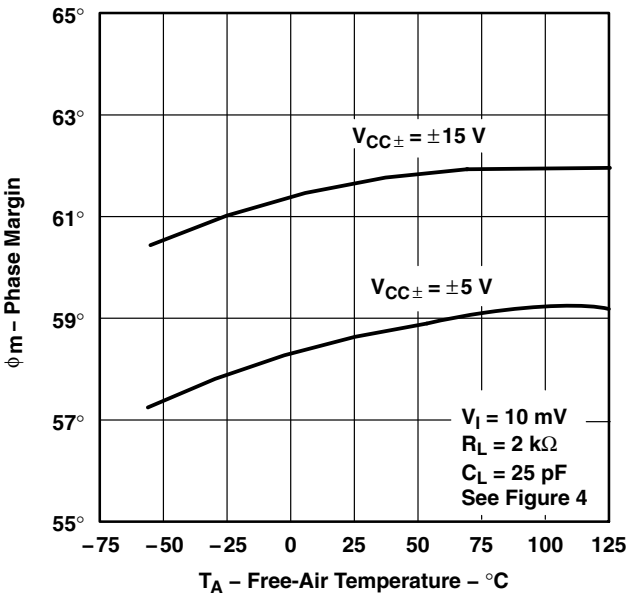


Figure 40

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

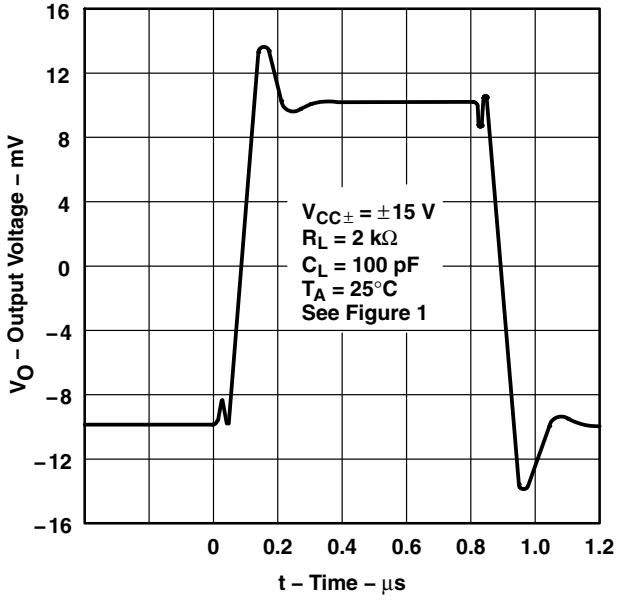


Figure 41

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

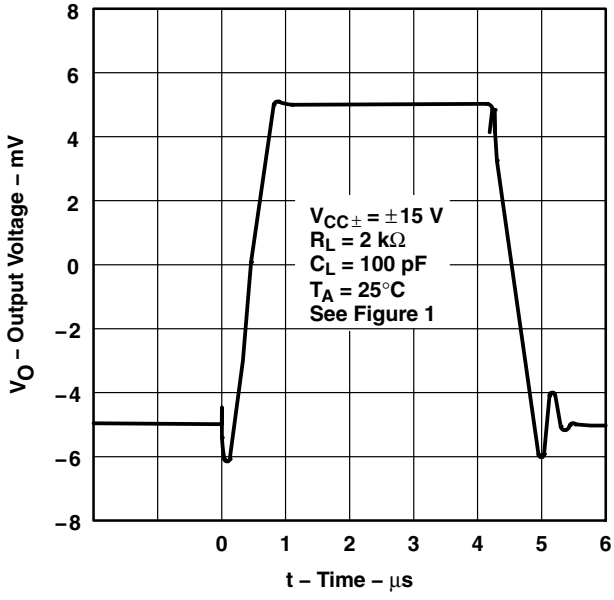
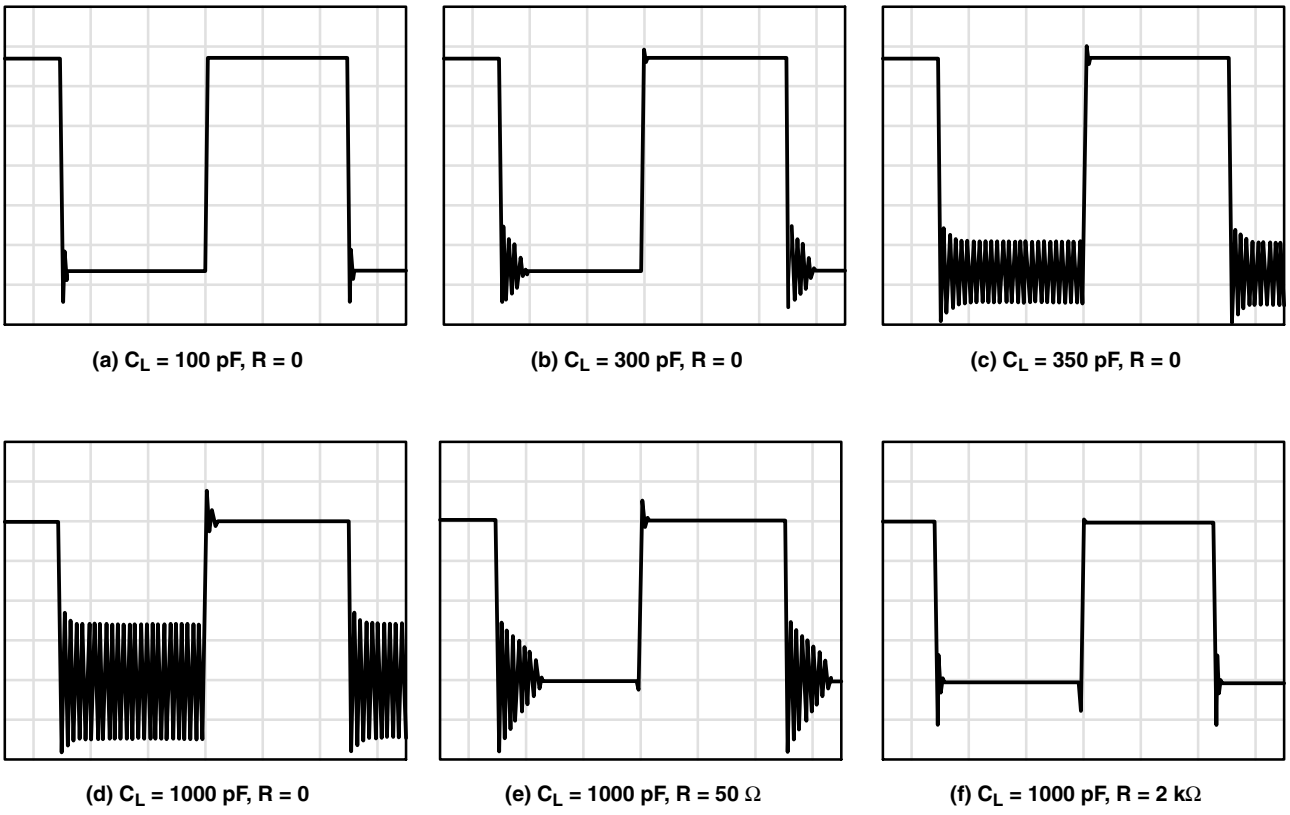


Figure 42

TYPICAL APPLICATION DATA

output characteristics

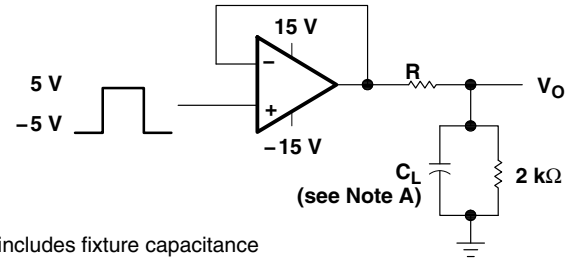
All operating characteristics are specified with 100-pF load capacitance. These amplifiers will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF, and larger, may be driven if enough resistance is added in series with the output (see Figure 43).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 43. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance

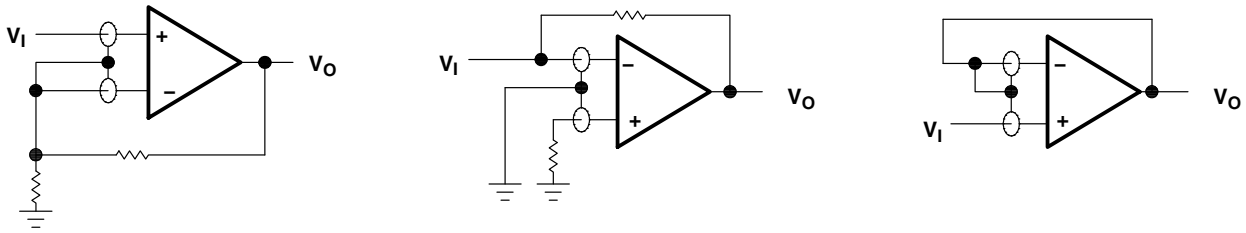
Figure 44. Test Circuit for Output Characteristics

TYPICAL APPLICATION DATA

input characteristics

These amplifiers are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, these amplifiers are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets easily can exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 45). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY–GAIN AMPLIFIER

Figure 45. Use of Guard Rings

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage diflferential amplifier. The low input bias current requirements of these amplifiers result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL288CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL288CP	Samples
TL288CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL288CP	Samples

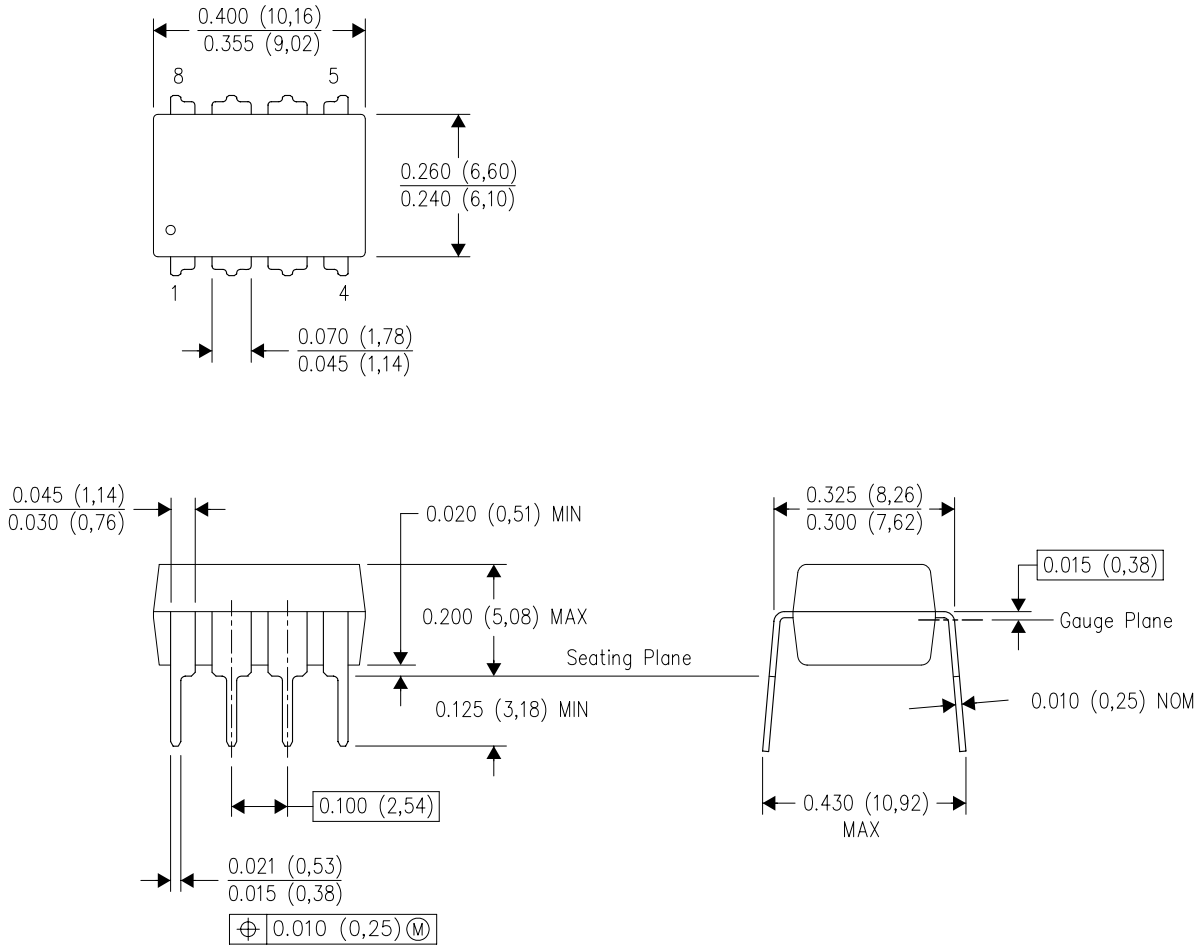
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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