1.8-V OPERATIONAL AMPLIFIERS WITH RAIL-TO-RAIL INPUT AND OUTPUT

Check for Samples: LMV932 DUAL, LMV934 QUAD, LMV931 SINGLE

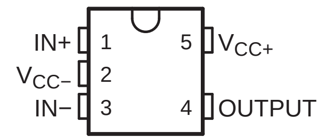
FEATURES

- **1.8-V, 2.7-V, and 5-V Specifications**
- **Rail-to-Rail Output Swing**
  - **600-Ω Load . . . 80 mV From Rail**
  - **2-kΩ Load . . . 30 mV From Rail**
- **V_{ICR} . . . 200 mV Beyond Rails**
- **Gain Bandwidth . . . 1.4 MHz**
- **Supply Current . . . 100 μA/Amplifier**
- **Max V_{IO} . . . 4 mV**
- **Space-Saving Packages**
  - **LMV931: SOT-23 and SC-70**
  - **LMV932: MSOP and SOIC**
  - **LMV934: SOIC and TSSOP**

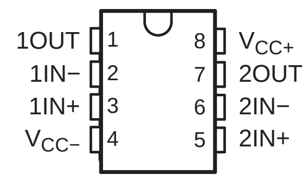
APPLICATIONS

- **Industrial (Utility/Energy Metering)**
- **Automotive**
- **Communications (Optical Telecom, Data/Voice Cable Modems)**
- **Consumer Electronics (PDAs, PCs, CDR/W, Portable Audio)**
- **Supply-Current Monitoring**
- **Battery Monitoring**

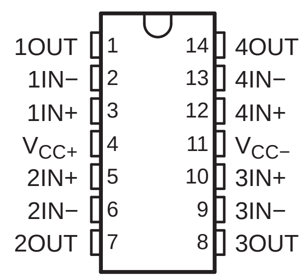
LMV931 . . . DBV (SOT-23-5) OR DCK (SC-70) PACKAGE (TOP VIEW)



LMV932 . . . D (SOIC) OR DGK (VSSOP/MSOP) PACKAGE (TOP VIEW)



LMV934 . . . D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T_A	PACKAGE[(1)]			ORDERABLE PART NUMBER	TOP-SIDE MARKING[(2)]
–40°C to 125°C	Single	SOT-23 – DBV	Reel of 3000	LMV931IDBVR	RBB_
			Reel of 250	LMV931IDBVT	PREVIEW
		SC-70 – DCK	Reel of 3000	LMV931IDCKR	RB_
			Reel of 250	LMV931IDCKT	PREVIEW
	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV932IDGKR	RD_
			Reel of 250	LMV932IDGKT	PREVIEW
		SOIC – D	Tube of 75	LMV932ID	MV932I
			Reel of 2500	LMV932IDR	
	Quad	SOIC – D	Tube of 50	LMV934ID	LMV934I
			Reel of 2500	LMV934IDR	
		TSSOP – PW	Tube of 90	LMV934IPW	MV934I
			Reel of 2000	LMV934IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The LMV93x devices are low-voltage low-power operational amplifiers that are well suited for today's low-voltage and/or portable applications. Specified for operation of 1.8 V to 5 V, they can be used in portable applications that are powered from a single-cell Li-ion or two-cell batteries. They have rail-to-rail input and output capability for maximum signal swings in low-voltage applications. The LMV93x input common-mode voltage extends 200 mV beyond the rails for increased flexibility. The output can swing rail-to-rail unloaded and typically can reach 80 mV from the rails, while driving a 600-Ω load (at 1.8-V operation).

During 1.8-V operation, the devices typically consume a quiescent current of 103 µA per channel, and yet they are able to achieve excellent electrical specifications, such as 101-dB open-loop DC gain and 1.4-MHz gain bandwidth. Furthermore, the amplifiers offer good output drive characteristics, with the ability to drive a 600-Ω load and 1000-pF capacitance with minimal ringing.

The LMV93x devices are offered in the latest packaging technology to meet the most demanding space-constraint applications. The LMV931 is offered in standard SOT-23 and SC-70 packages. The LMV932 is available in the traditional MSOP and SOIC packages. The LMV934 is available in the traditional SOIC and TSSOP packages.

The LMV93x devices are characterized for operation from –40°C to 125°C, making the part universally suited for commercial, industrial, and automotive applications.

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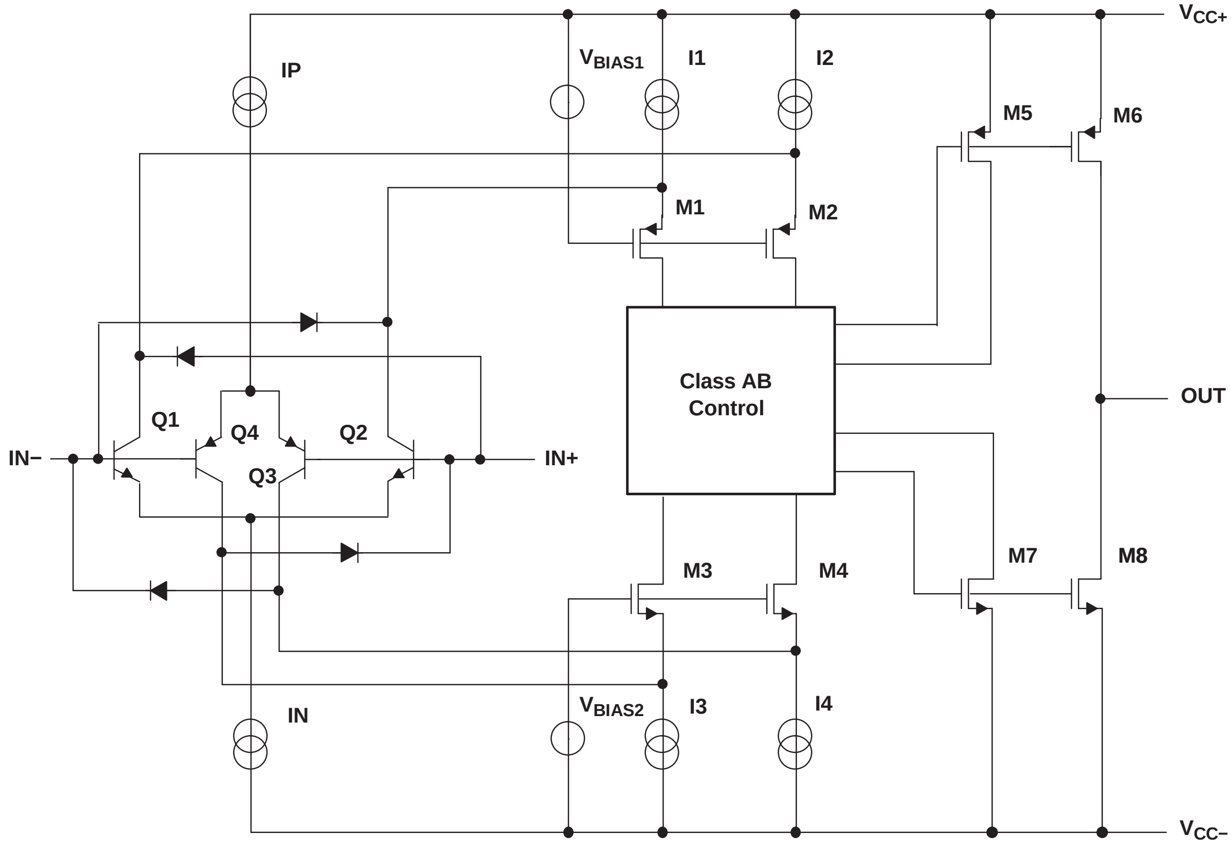
Figure 1. SIMPLIFIED SCHEMATIC



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Absolute Maximum Ratings[1]

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage[2]			5.5	V
V_{ID}	Differential input voltage[3]		Supply voltage		
V_I	Input voltage range, either input		$V_{CC–}$ – 0.2	V_{CC+} + 0.2	V
	Duration of output short circuit (one amplifier) to $V_{CC\pm}$ [4] [5]		Unlimited		
θ_{JA}	Package thermal impedance[5] [6]	D package (8 pin)		97	°C/W
		D package (14 pin)		86	
		DBV package		206	
		DCK package		252	
		DGK package		172	
		PW package		113	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.
(5) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage ($V_{CC+} – V_{CC–}$)	1.8	5	V
T_A	Operating free-air temperature	–40	125	°C

ESD Protection

	TYP	UNIT
Human-Body Model	2000	V
Machine Model	200	V

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Electrical Characteristics

V_{CC+} = 1.8 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		LMV931 (single)		25°C		1	4	mV
					Full range			6	
			LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
					Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				25°C		5.5		μV/°C
I_{IB}	Input bias current		V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
					25°C			65	
					Full range			75	
I_{IO}	Input offset current				25°C		13	25	nA
					Full range			40	
I_{CC}	Supply current (per channel)				25°C		103	185	μA
					Full range			205	
CMRR	Common-mode rejection ratio		0 ≤ V_{IC} ≤ 0.6 V, 1.4 V ≤ V_{IC} ≤ 1.8 V		25°C	60	78		dB
					–40°C to 85°C	55			
			0.2 ≤ V_{IC} ≤ 0.6 V, 1.4 V ≤ V_{IC} ≤ 1.6 V		–40°C to 125°C	55			
			–0.2 ≤ V_{IC} ≤ 0 V, 1.8 V ≤ V_{IC} ≤ 2 V		25°C	50	72		
k_{SVR}	Supply-voltage rejection ratio		1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
					Full range	70			
V_{ICR}	Common-mode input voltage range		CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 2.1	V_{CC+} + 0.2	V
					–40°C to 85°C	V_{CC-}		V_{CC+}	
					–40°C to 125°C	V_{CC-} + 0.2		V_{CC+} – 0.2	
A_V	Large-signal voltage gain	LMV931	V_O = 0.2 V to 1.6 V, V_{IC} = 0.5 V	R_L = 600 Ω to 0.9 V	25°C	77	101		dB
					Full range	73			
				R_L = 2 kΩ to 0.9 V	25°C	80	105		
					Full range	75			
		LMV932, LMV934		R_L = 600 Ω to 0.9 V	25°C	75	90		
					Full range	72			
				R_L = 2 kΩ to 0.9 V	25°C	78	100		
					Full range	75			
V_O	Output swing		R_L = 600 Ω to 0.9 V, V_{ID} = ±100 mV	High level	25°C	1.65	1.72		V
					Full range	1.63			
				Low level	25°C		0.077	0.105	
					Full range			0.120	
			R_L = 2 kΩ to 0.9 V, V_{ID} = ±100 mV	High level	25°C	1.75	1.77		
					Full range	1.74			
				Low level	25°C		0.024	0.035	
					Full range			0.040	
I_{OS}	Output short-circuit current		V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	4	8		mA
					Full range	3.3			
			V_O = 1.8 V, V_{ID} = –100 mV	Sinking	25°C	7	9		
					Full range	5			
GBW	Gain bandwidth product				25°C		1.4		MHz

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Electrical Characteristics (continued)

V_{CC+} = 1.8 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate[1]		25°C		0.35		V/μS
Φ_m	Phase margin		25°C		67		°
	Gain margin		25°C		7		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		60		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.06		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.023		%
	Amplifier-to-amplifier isolation[2]		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

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Electrical Characteristics

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	LMV931 (single)		25°C		1	4	mV
				Full range			6	
		LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
				Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage			25°C		5.5		μV/°C
I_{IB}	Input bias current	V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
				25°C			65	
				Full range			75	
I_{IO}	Input offset current			25°C		8	25	nA
				Full range			40	
I_{CC}	Supply current (per channel)			25°C		105	190	μA
				Full range			210	
CMRR	Common-mode rejection ratio	0 ≤ V_{IC} ≤ 1.5 V, 2.3 V ≤ V_{IC} ≤ 2.7 V		25°C	60	81		dB
				–40°C to 85°C	55			
		0.2 ≤ V_{IC} ≤ 1.5 V, 2.3 V ≤ V_{IC} ≤ 2.5 V		–40°C to 125°C	55			
		–0.2 ≤ V_{IC} ≤ 0 V, 2.7 V ≤ V_{IC} ≤ 2.9 V		25°C	50	74		
k_{SVR}	Supply-voltage rejection ratio	1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
				Full range	70			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 3	V_{CC+} + 0.2	V
				–40°C to 85°C	V_{CC-}		V_{CC+}	
				–40°C to 125°C	V_{CC-} + 0.2		V_{CC+} – 0.2	
A_V	Large-signal voltage gain — LMV931	V_O = 0.2 V to 2.5 V	R_L = 600 Ω to 1.35 V	25°C	87	104		dB
				Full range	86			
			R_L = 2 kΩ to 1.35 V	25°C	92	110		
				Full range	91			
	Large-signal voltage gain — LMV932, LMV934		R_L = 600 Ω to 1.35 V	25°C	78	90		
				Full range	75			
			R_L = 2 kΩ to 1.35 V	25°C	81	100		
				Full range	78			
V_O	Output swing	R_L = 600 Ω to 1.35 V, V_{ID} = ±100 mV	High level	25°C	2.55	2.62		V
				Full range	2.53			
			Low level	25°C		0.083	0.11	
				Full range			0.13	
		R_L = 2 kΩ to 1.35 V, V_{ID} = ±100 mV	High level	25°C	2.65	2.675		
				Full range	2.64			
			Low level	25°C		0.025	0.04	
				Full range			0.045	
I_{OS}	Output short-circuit current	V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	20	30		mA
				Full range	15			
		V_O = 2.7 V, V_{ID} = –100 mV	Sinking	25°C	18	25		
				Full range	12			
GBW	Gain bandwidth product			25°C		1.4		MHz

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Electrical Characteristics (continued)

V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate[1]		25°C		0.4		V/µS
Φ_m	Phase margin		25°C		70		°
	Gain margin		25°C		7.5		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		57		nV/$\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.082		pA/$\sqrt{Hz}$
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.022		%
	Amplifier-to-amplifier isolation[2]		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

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Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		LMV931 (single)		25°C		1	4	mV
					Full range			6	
			LMV932 (dual), LMV934 (quad)		25°C		1	5.5	
					Full range			7.5	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				25°C		5.5		μV/°C
I_{IB}	Input bias current		V_{IC} = V_{CC+} – 0.8 V		25°C		15	35	nA
					25°C			65	
					Full range			75	
I_{IO}	Input offset current				25°C		9	25	nA
					Full range			40	
I_{CC}	Supply current (per channel)				25°C		116	210	μA
					Full range			230	
CMRR	Common-mode rejection ratio		0 ≤ V_{IC} ≤ 3.8 V, 4.6 V ≤ V_{IC} ≤ 5 V		25°C	60	86		dB
					–40°C to 85°C	55			
			0.3 ≤ V_{IC} ≤ 3.8 V, 4.6 V ≤ V_{IC} ≤ 4.7 V		–40°C to 125°C	55			
			–0.2 ≤ V_{IC} ≤ 0 V, 5 V ≤ V_{IC} ≤ 5.2 V		25°C	50	78		
k_{SVR}	Supply-voltage rejection ratio		1.8 V ≤ V_{CC+} ≤ 5 V, V_{IC} = 0.5 V		25°C	75	100		dB
					Full range	70			
V_{ICR}	Common-mode input voltage range		CMRR ≥ 50 dB		25°C	V_{CC-} – 0.2	–0.2 to 5.3	V_{CC+} + 0.2	V
					–40°C to 85°C	V_{CC-}		V_{CC+}	
					–40°C to 125°C	V_{CC-} + 0.3		V_{CC+} – 0.3	
A_V	Large-signal voltage gain	LMV931	V_O = 0.2 V to 4.8 V	R_L = 600 Ω to 2.5 V	25°C	88	102		dB
					Full range	87			
				R_L = 2 kΩ to 2.5 V	25°C	94	113		
					Full range	93			
		LMV932, LMV934		R_L = 600 Ω to 2.5 V	25°C	81	90		
					Full range	78			
				R_L = 2 kΩ to 2.5 V	25°C	85	100		
					Full range	82			
V_O	Output swing		R_L = 600 Ω to 2.5 V, V_{ID} = ±100 mV	High level	25°C	4.855	4.89		V
					Full range	4.835			
				Low level	25°C		0.12	0.16	
					Full range			0.18	
			R_L = 2 kΩ to 2.5 V, V_{ID} = ±100 mV	High level	25°C	4.945	4.967		
					Full range	4.935			
				Low level	25°C		0.037	0.065	
					Full range			0.075	
I_{OS}	Output short-circuit current		V_O = 0 V, V_{ID} = 100 mV	Sourcing	25°C	80	100		mA
					Full range	68			
			V_O = 5 V, V_{ID} = –100 mV	Sinking	25°C	58	65		
					Full range	45			
GBW	Gain bandwidth product				25°C		1.5		MHz

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Electrical Characteristics (continued)

V_{CC+} = 5 V, V_{CC-} = 0 V, V_{IC} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate[1]		25°C		0.42		V/μS
Φ_m	Phase margin		25°C		71		°
	Gain margin		25°C		8		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V_{IC} = 0.5 V	25°C		50		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.07		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_{ID} = 1 V_{p-p}	25°C		0.022		%
	Amplifier-to-amplifier isolation[2]		25°C		123		dB

(1) Number specified is the slower of the positive and negative slew rates.
(2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

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TYPICAL CHARACTERISTICS

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

SUPPLY CURRENT vs SUPPLY VOLTAGE

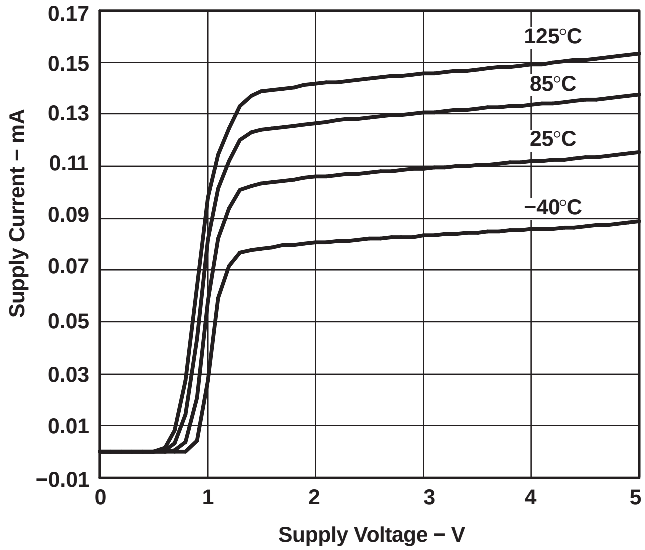

Figure 2.

SLEW RATE vs SUPPLY VOLTAGE

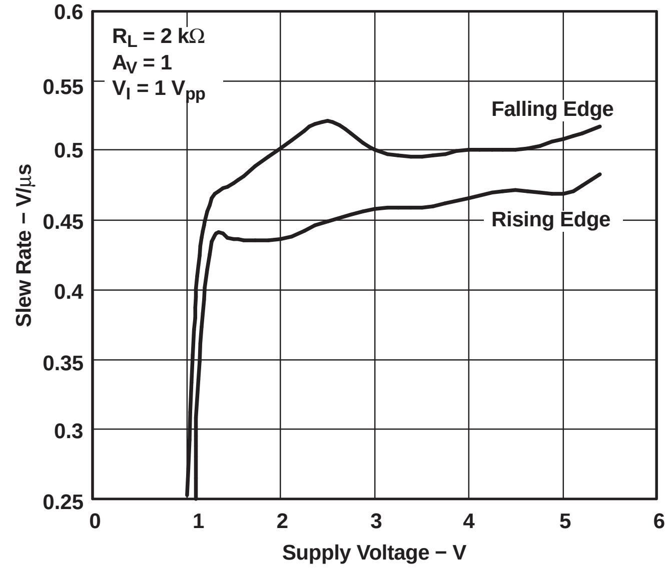

Figure 3.

SOURCE CURRENT vs OUTPUT VOLTAGE

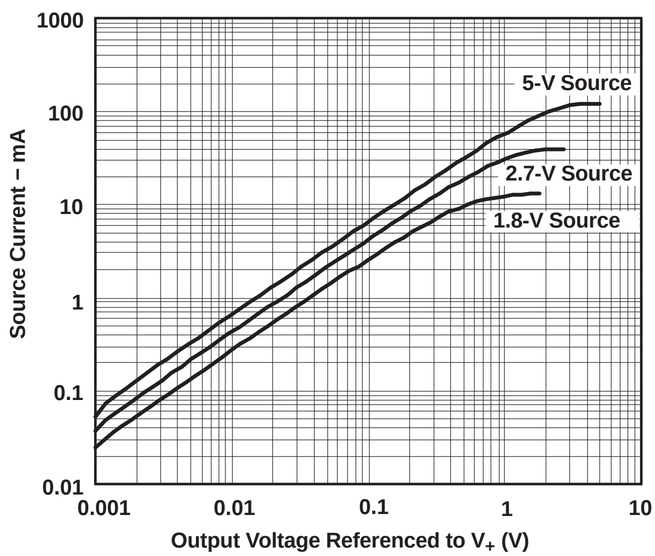

Figure 4.

SINK CURRENT vs OUTPUT VOLTAGE

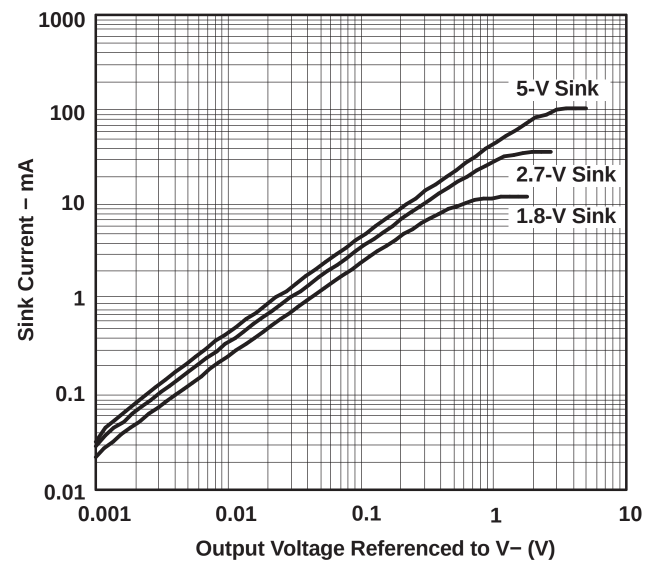

Figure 5.

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TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

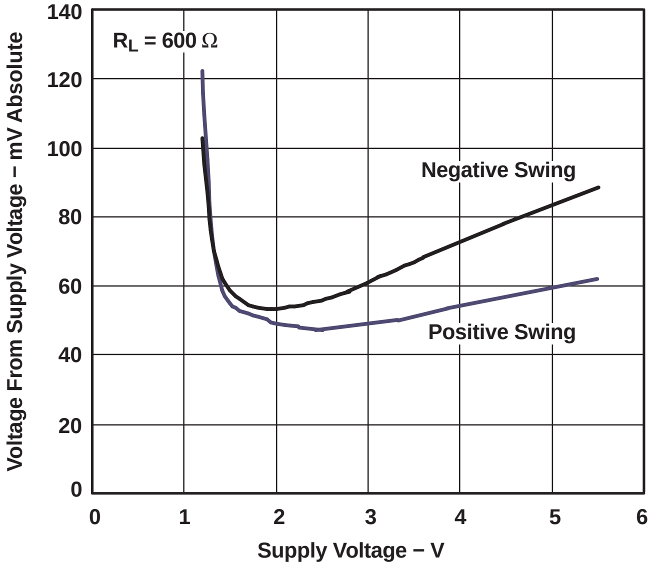

Figure 6.

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

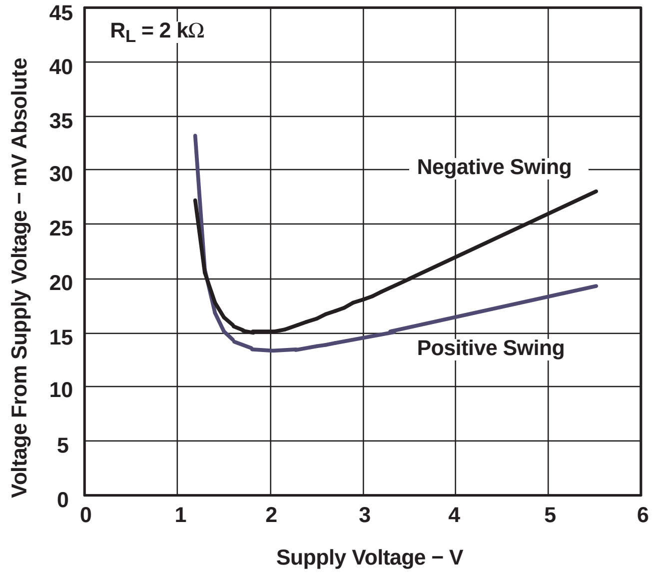

Figure 7.

SHORT-CIRCUIT CURRENT (SINK)
vs
TEMPERATURE

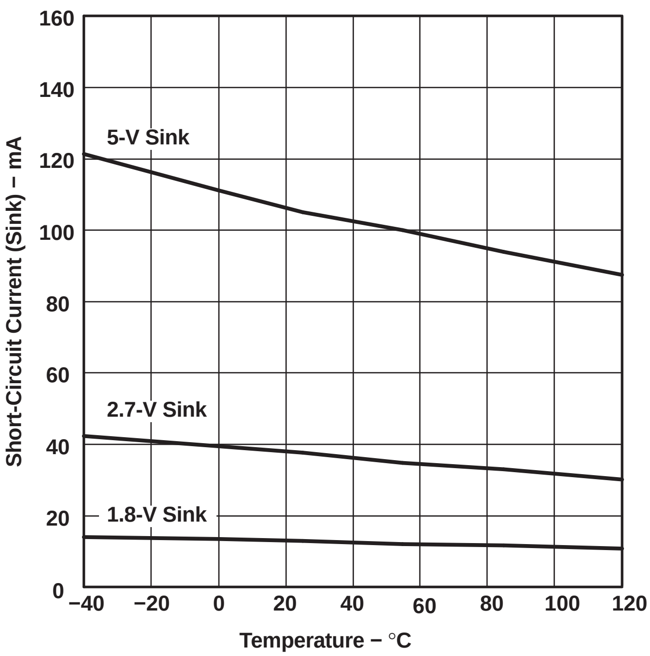

Figure 8.

SHORT-CIRCUIT CURRENT (SOURCE)
vs
TEMPERATURE

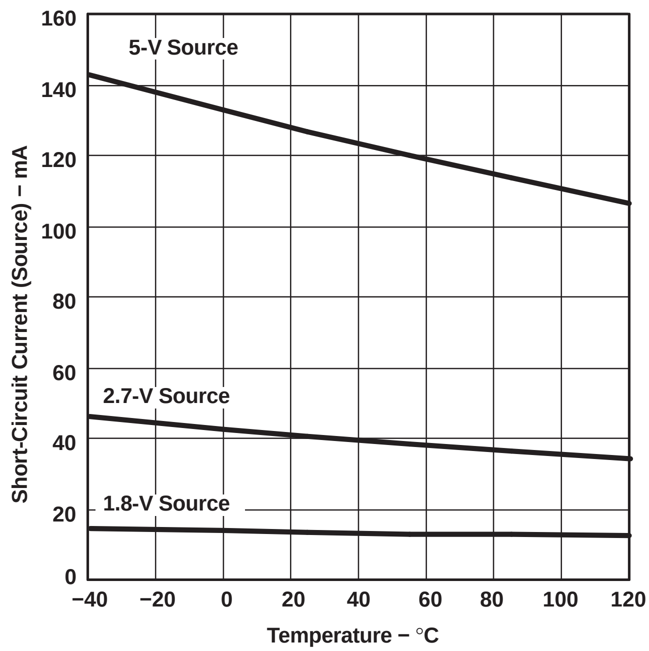

Figure 9.

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TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

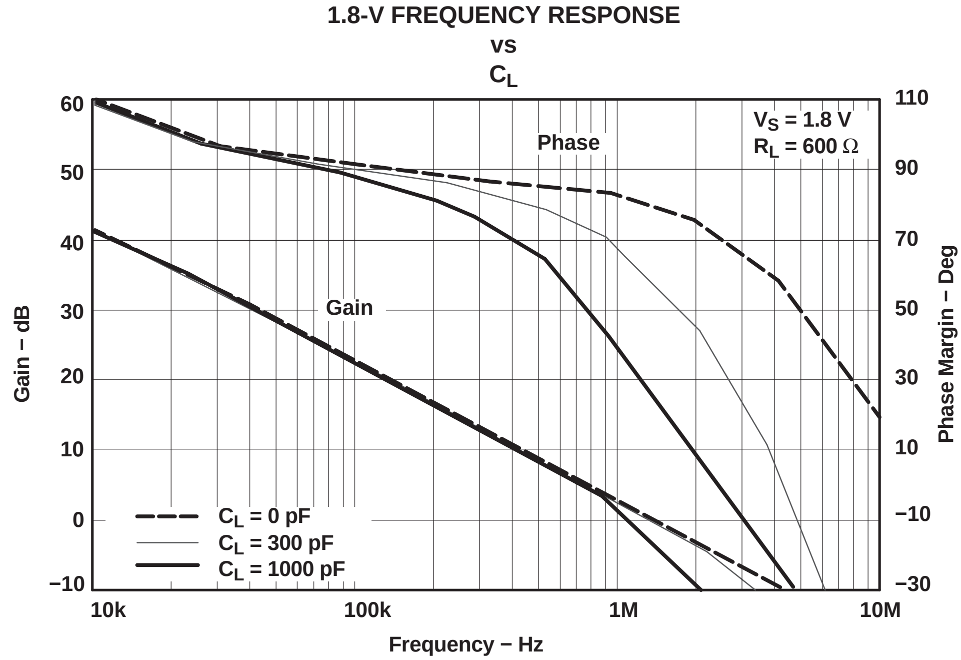

Figure 10.

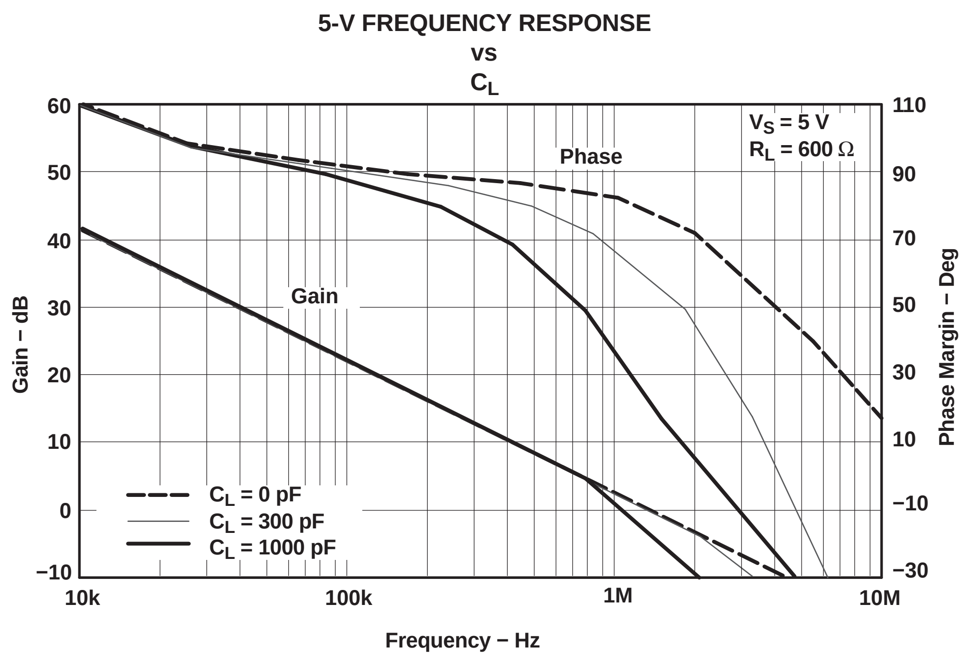

Figure 11.

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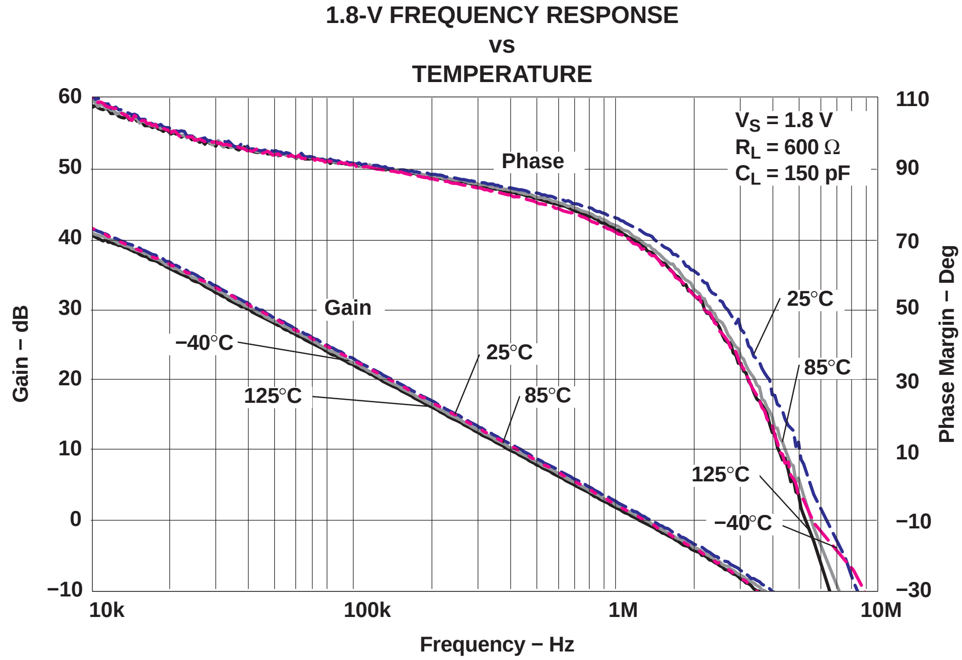
TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)



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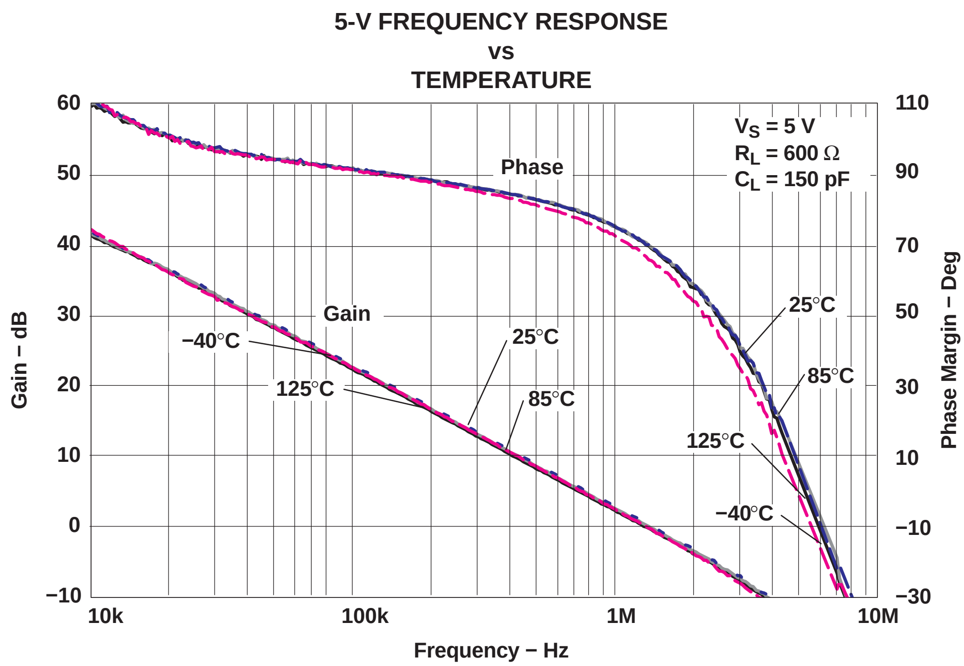

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

CMRR vs FREQUENCY

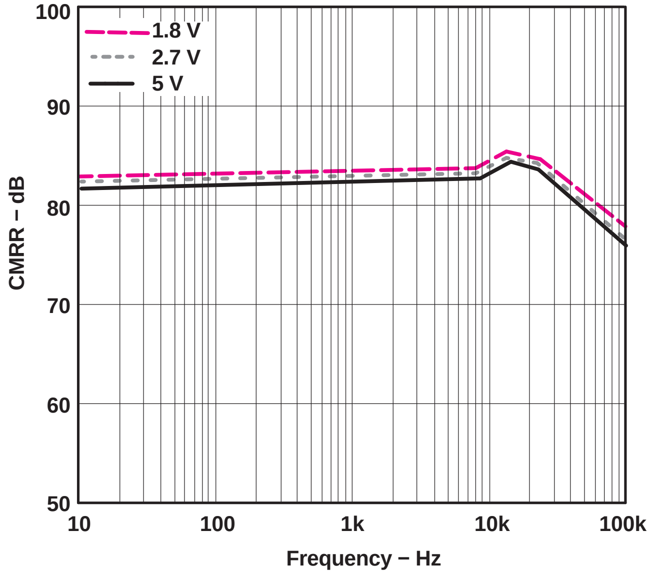

Figure 14.

PSRR vs FREQUENCY

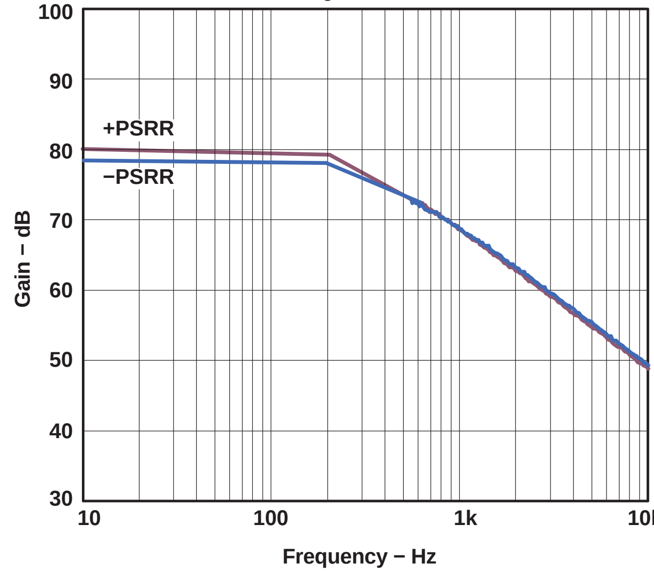

Figure 15.

THD vs FREQUENCY

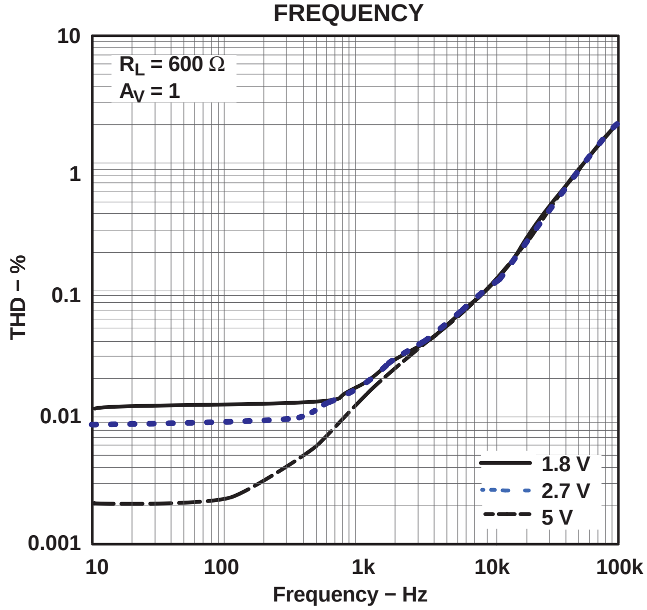

Figure 16.

THD vs FREQUENCY

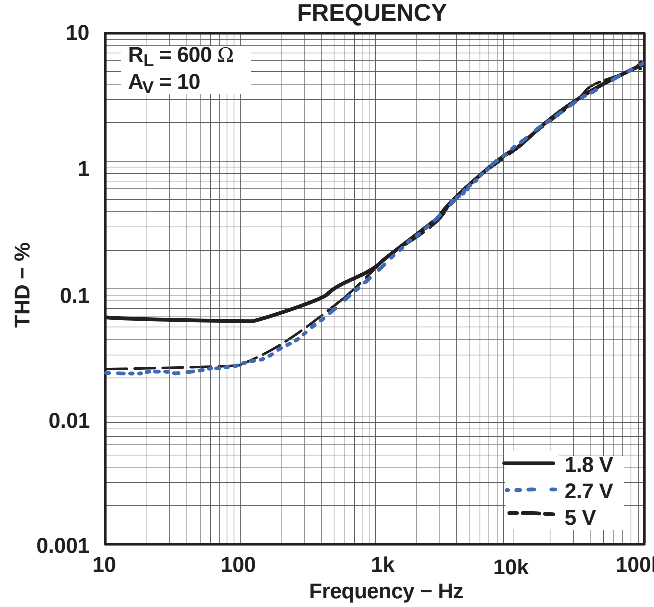

Figure 17.

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TYPICAL CHARACTERISTICS (continued)

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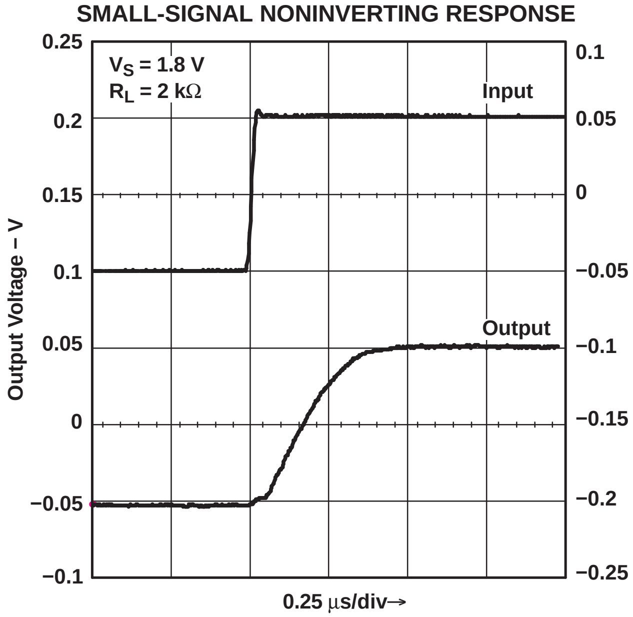
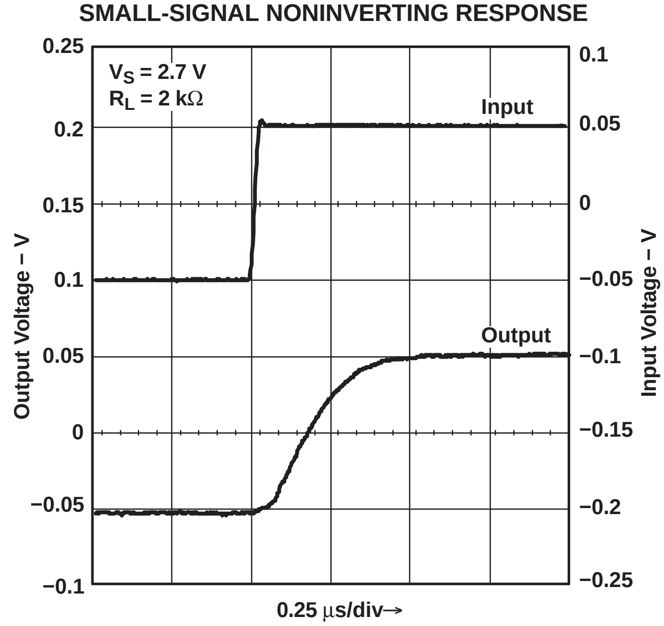


Figure 18.



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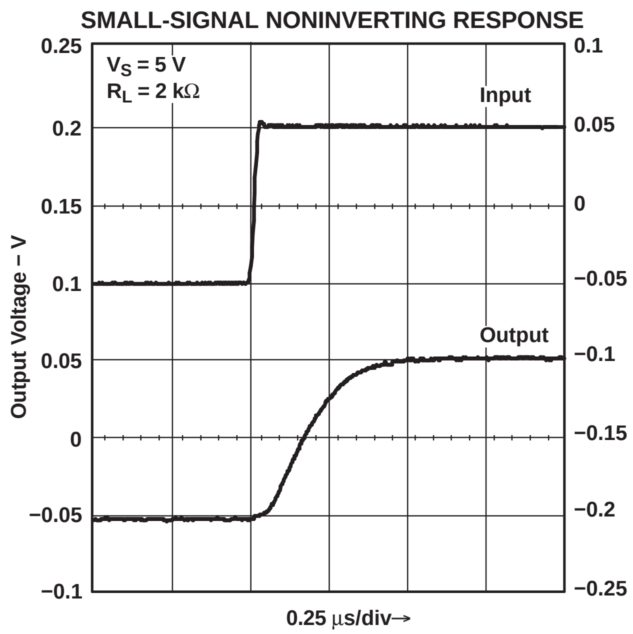

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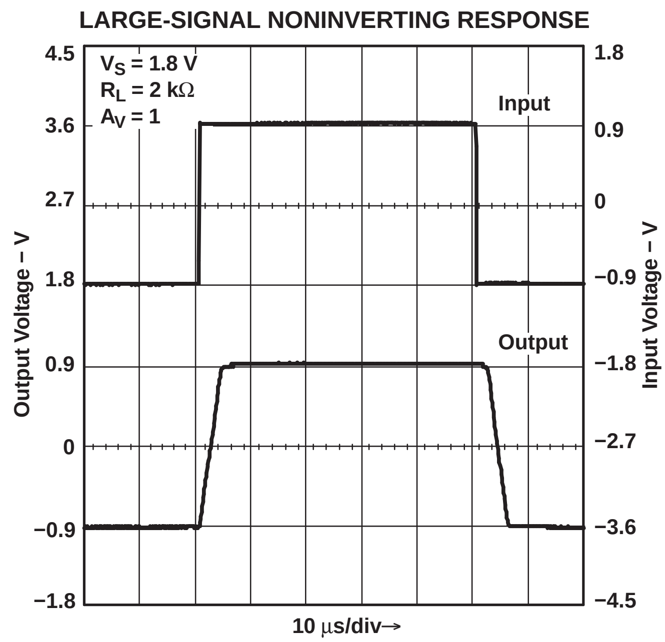

Figure 21.

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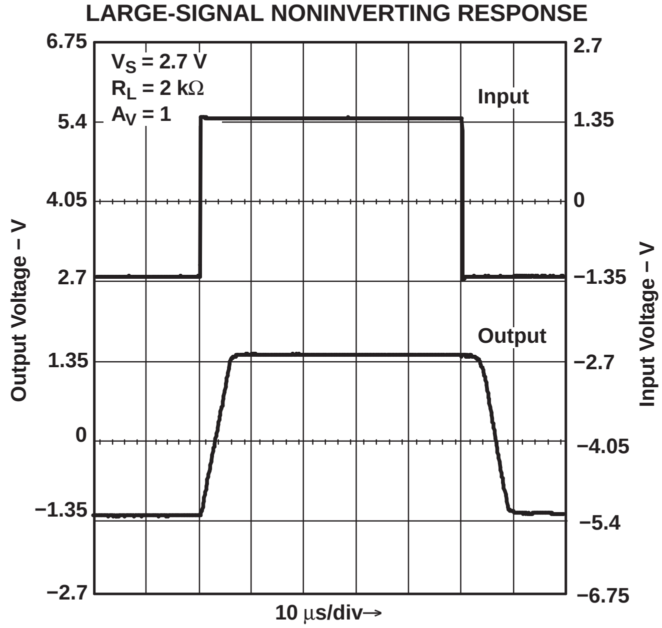
TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)



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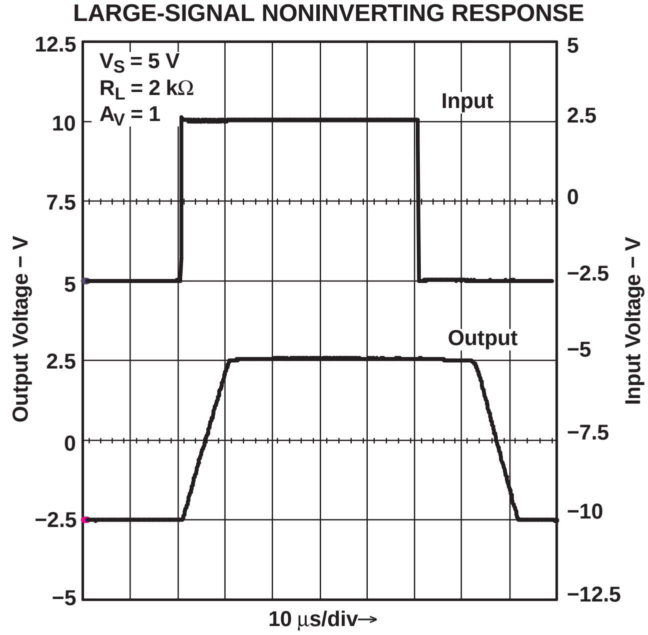
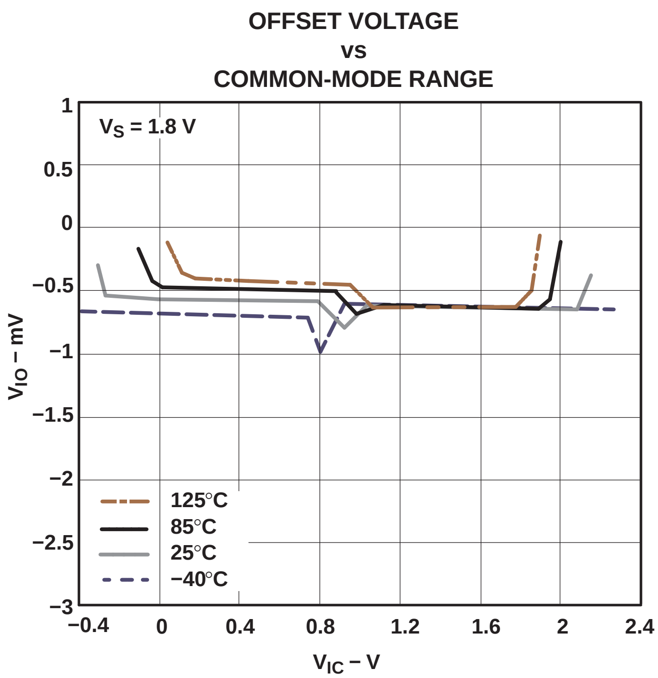


Figure 23.



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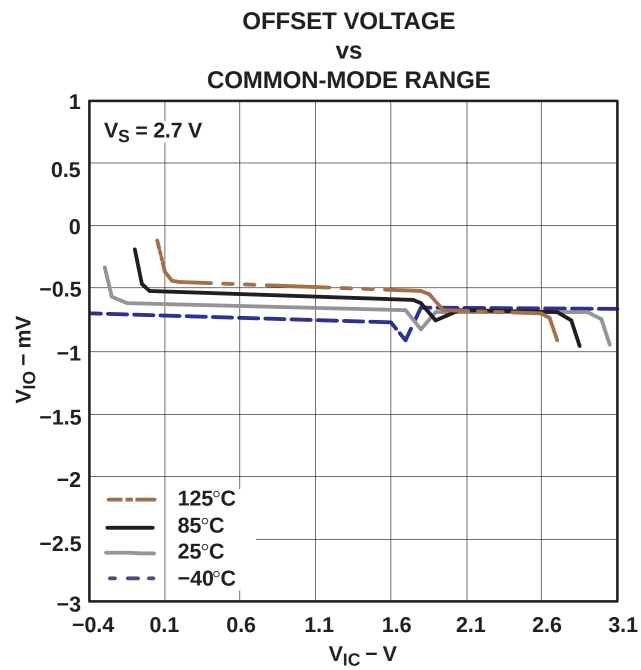

Figure 25.

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TYPICAL CHARACTERISTICS (continued)

V_{CC+} = 5 V, Single Supply, T_A = 25°C (unless otherwise specified)

OFFSET VOLTAGE vs COMMON-MODE RANGE

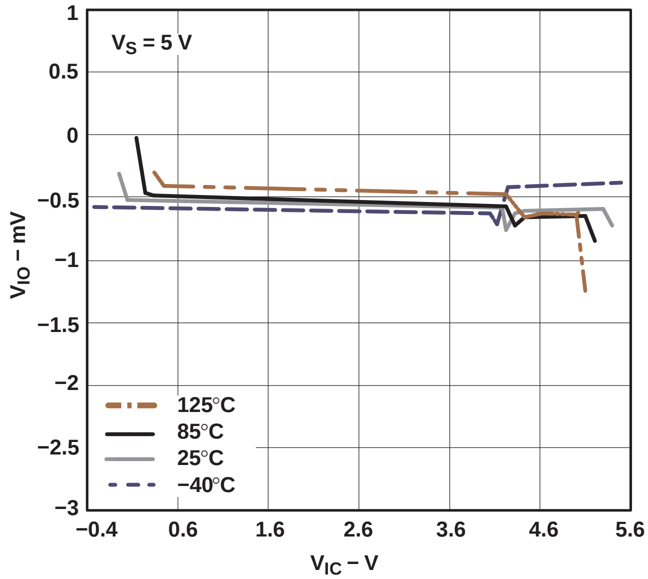

Figure 26.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV931IDBVR	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	(RBBB ~ RBBC ~ RBBI)	
LMV931IDBVRE4	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDBVRG4	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDCKR	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125	(RBB ~ RBC ~ RBI)	
LMV931IDCKRE4	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDCKRG4	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		
LMV932ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	MV932I	
LMV932IDE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDGKR	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	(RD6 ~ RDB)	
LMV932IDGKRG4	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	MV932I	
LMV932IDRE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDRG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV934ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LMV934I	
LMV934IDE4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LMV934I	
LMV934IDRE4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	MV934I	
LMV934IPWE4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWR	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	MV934I	
LMV934IPWRE4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWRG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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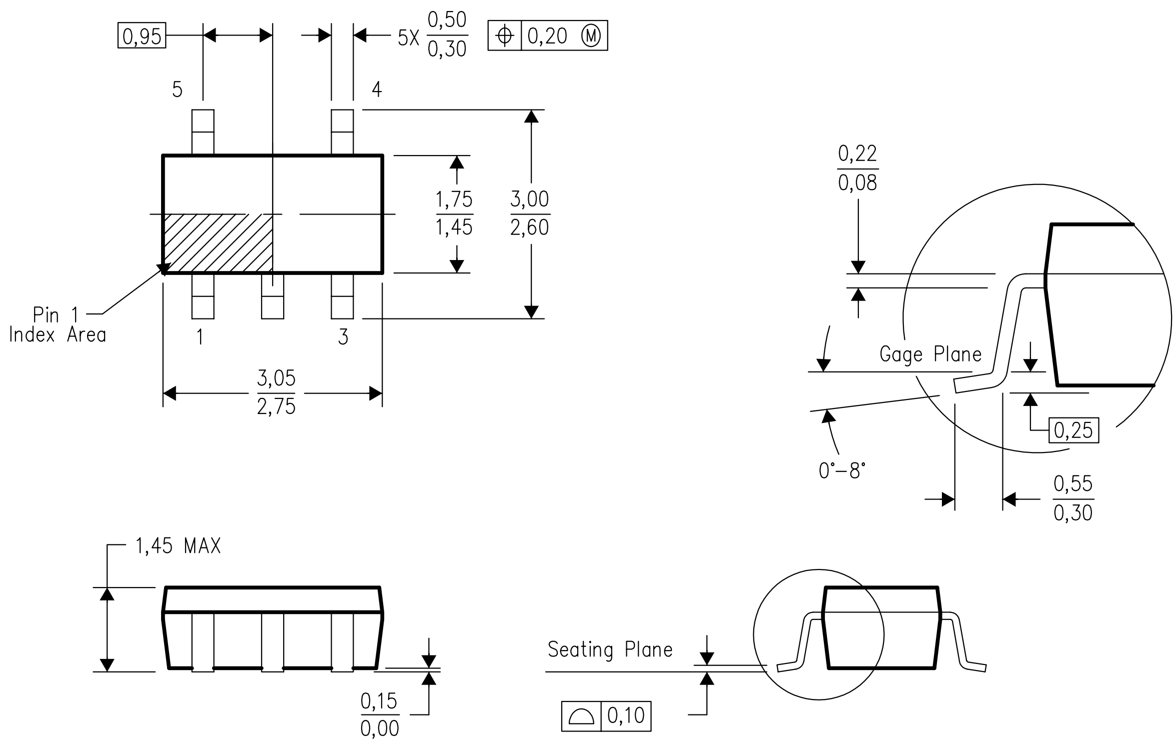
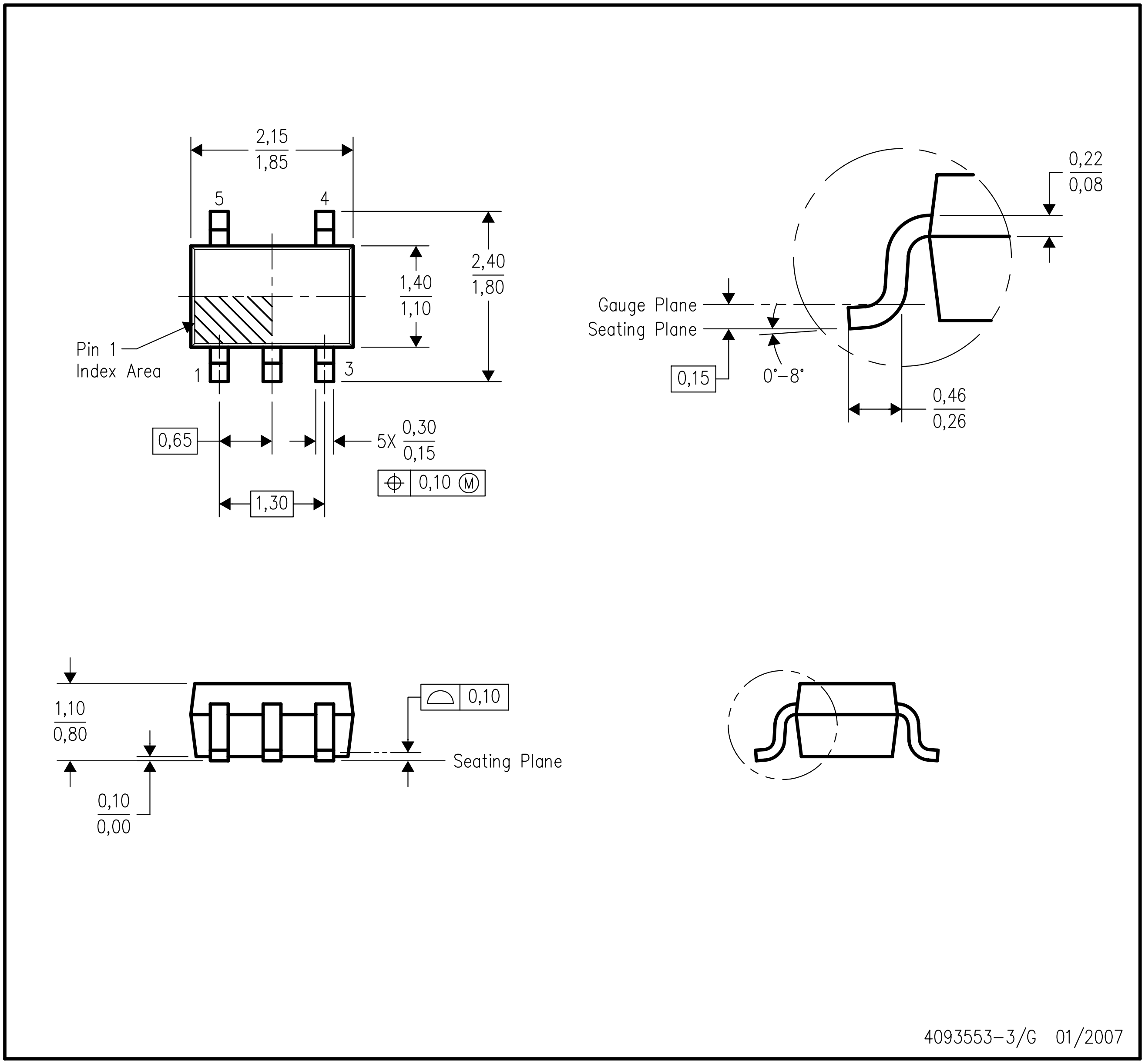
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

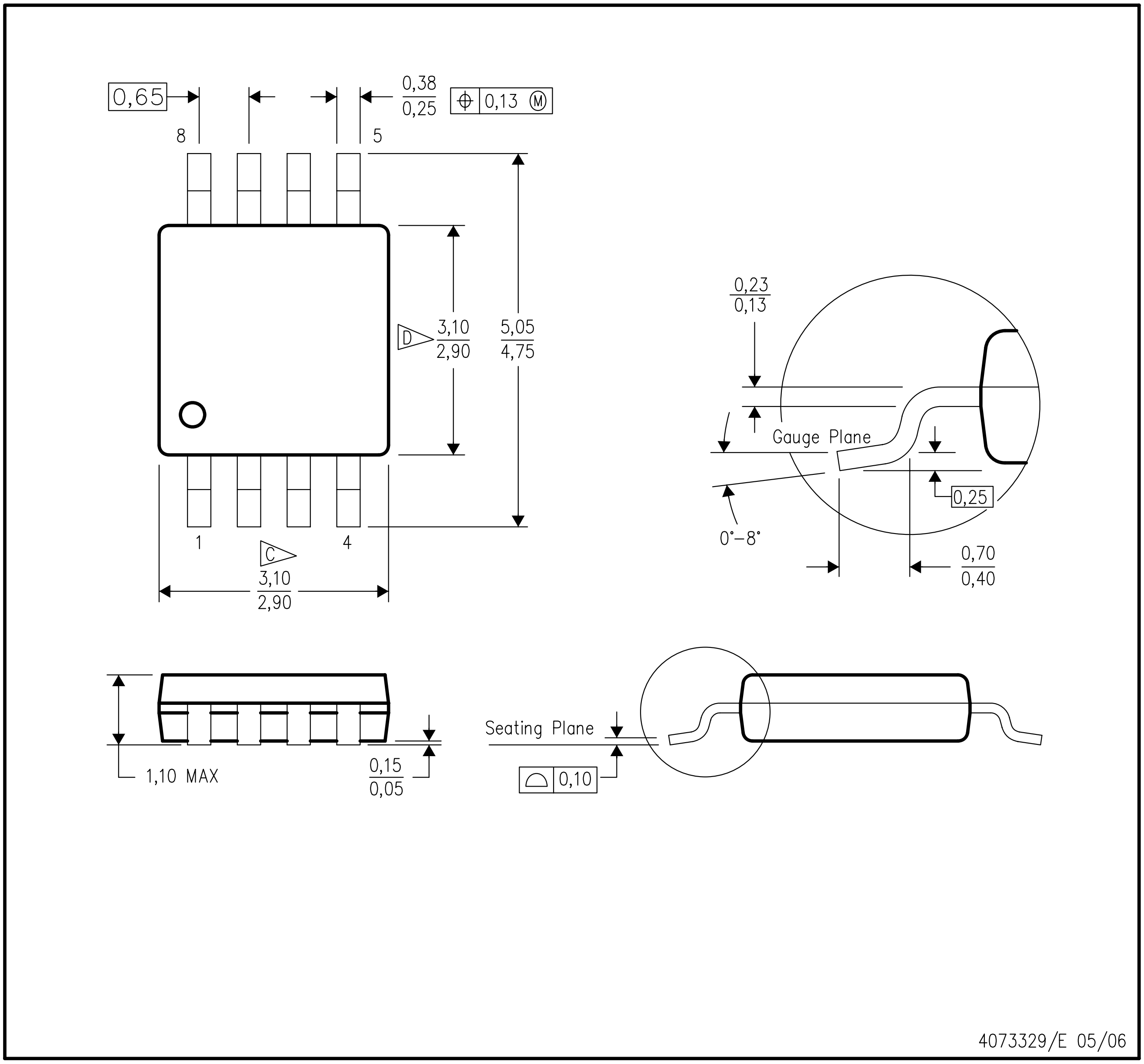
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



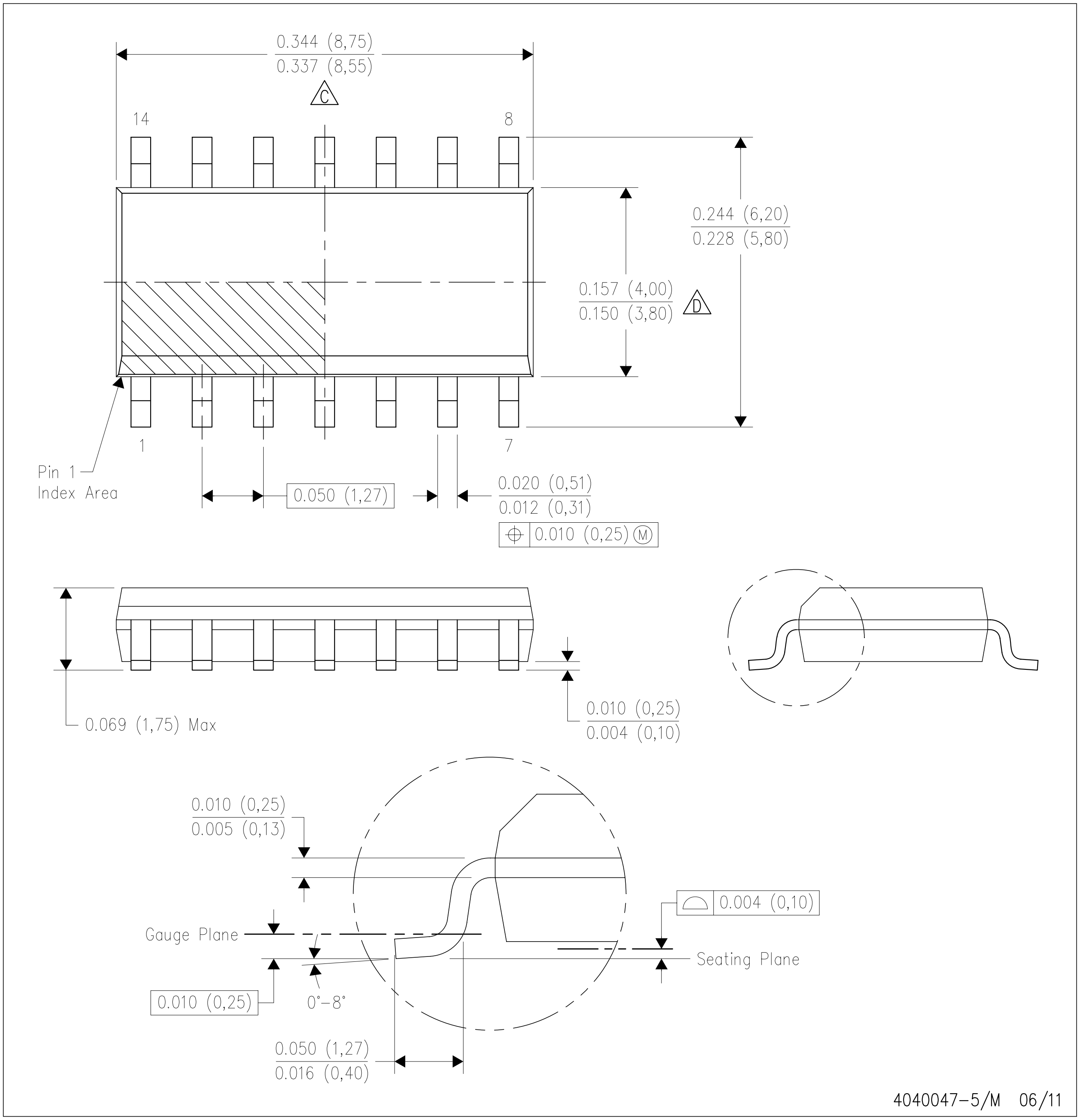
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



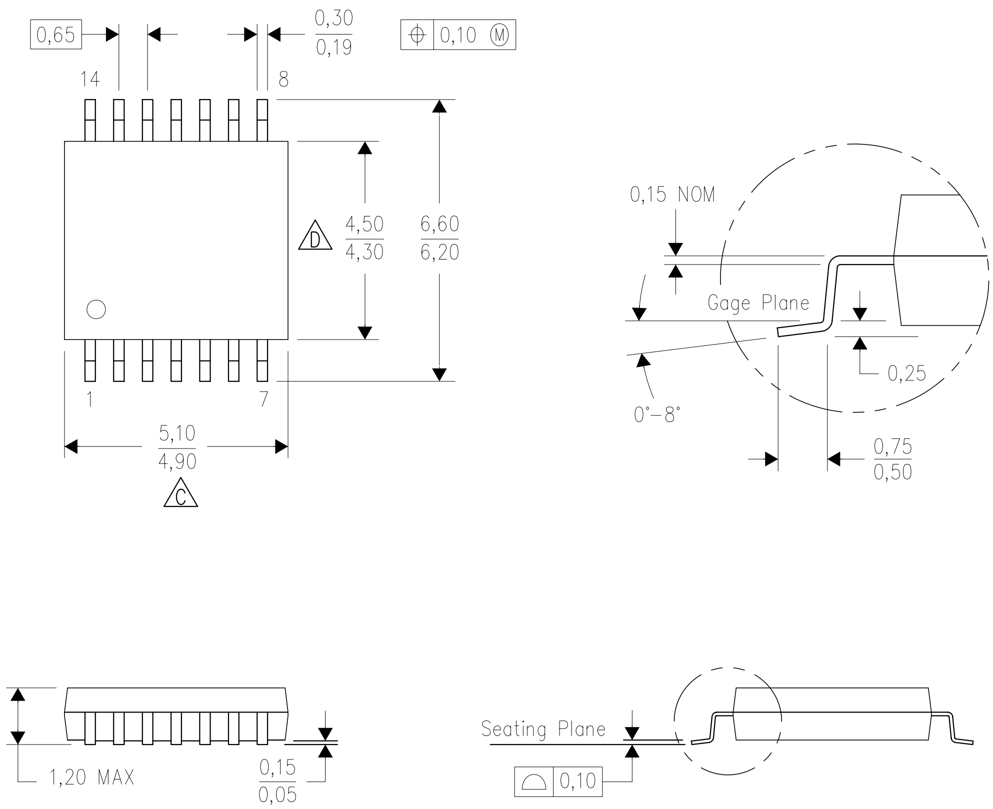
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

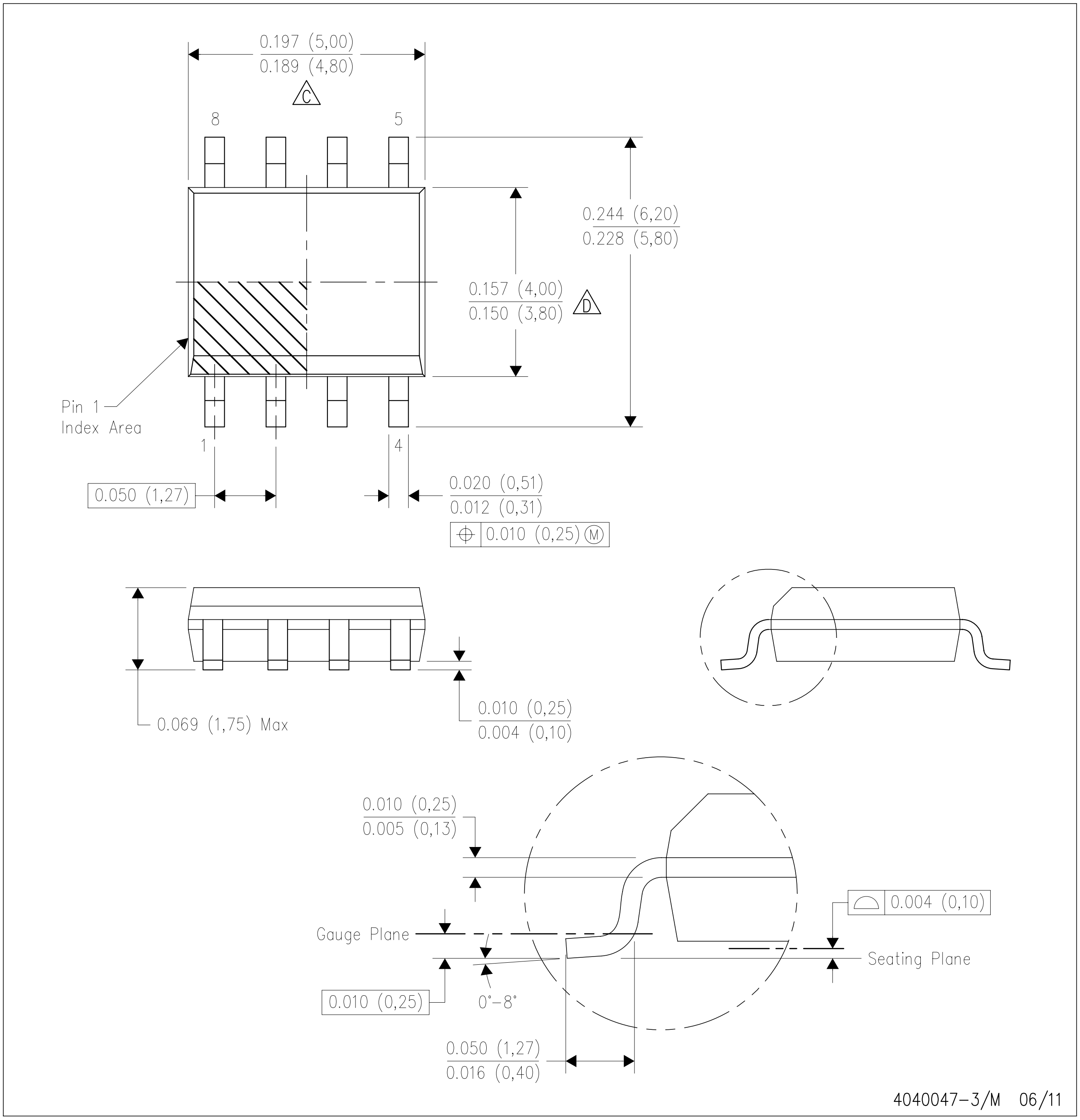
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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