OUTPUT RAIL-TO-RAIL VERY-LOW-NOISE OPERATIONAL AMPLIFIERS

Check for Samples: TL971, TL972, TL974

FEATURES

- **Rail-to-Rail Output Voltage Swing: ±2.4 V at V_{CC} = ±2.5 V**
- **Very Low Noise Level: 4 nV/√Hz**
- **Ultra-Low Distortion: 0.003%**
- **High Dynamic Features: 12 MHz, 5 V/µs**
- **Operating Range: 2.7 V to 12 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **1500-V Charged-Device Model (C101)**

APPLICATIONS

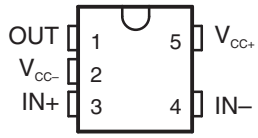
- **Portable Equipment (CD Players, PDAs)**
- **Portable Communications (Cell Phones, Pagers)**
- **Instrumentation and Sensors**
- **Professional Audio Circuits**

DESCRIPTION/ORDERING INFORMATION

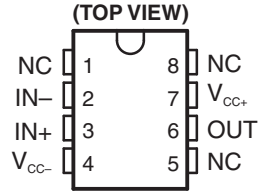
The TL97x family of operational amplifiers operates at voltages as low as ±1.35 V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm × 2.9 mm).

TL971...DBV PACKAGE
(TOP VIEW)

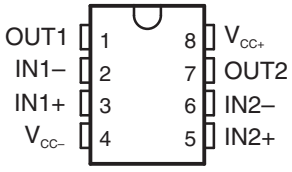


TL971...D PACKAGE
(TOP VIEW)

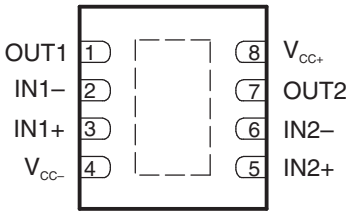


NC – No internal connection

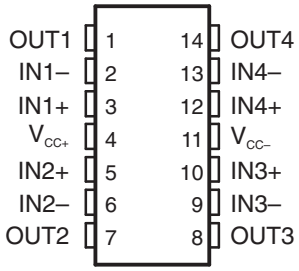
TL972...D, DGK, P, OR PW PACKAGE
(TOP VIEW)



TL972...DRG PACKAGE
(TOP VIEW)



TL974...D, N, OR PW PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]			ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 125°C	Single	SOIC – D	Reel of 2500	TL971IDR	Z971
			Tube of 75	TL971ID	
		SOT-23 – DBV	Reel of 3000	TL971IDBVR	PREVIEW
			Reel of 250	TL971IDBVT	
	Dual	MSOP – DGK	Reel of 2500	TL972IDGKR	TSA
		PDIP – P	Tube of 50	TL972IP	TL972IP
		QFN – DRG	Reel of 1000	TL972IDRGR	PREVIEW
		SOIC – D	Reel of 2500	TL972IDR	Z972
			Tube of 75	TL972ID	
		TSSOP – PW	Reel of 2000	TL972IPWR	Z972
			Tube of 150	TL972IPW	
	Quad	PDIP – N	Tube of 25	TL974IN	TL974IN
		SOIC – D	Reel of 2500	TL974IDR	TL974I
			Tube of 50	TL974ID	
		TSSOP – PW	Reel of 2000	TL974IPWR	Z974
			Tube of 90	TL974IPW	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range(2)			2.7 V to 15 V
V_{ID}	Differential input voltage(3)			±1 V
V_{IN}	Input voltage range(4)			V_{CC-} – 0.3 V to V_{CC+} + 0.3 V
θ_{JA}	Package thermal impedance, junction to free air	D package(5)	8 pin	97°C/W
			14 pin	86°C/W
		DBV package(5)		206°C/W
		DGK package(6)		172°C/W
		DRG package(6)		44°C/W
		N package(5)		80°C/W
		P package(5)		85°C/W
		PW package(5)	8 pin	149°C/W
			14 pin	113°C/W
T_J	Maximum junction temperature			150°C
T_{stg}	Storage temperature range			–65°C to 150°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000 V
		Machine Model (MM)		200 V
		Charged-Device Model (CDM)		1500 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
(4) The input and output voltages must never exceed V_{CC} + 0.3 V.
(5) Package thermal impedance is calculated in accordance with JESD 51-7.
(6) Package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	12	V
V_{ICM}	Common-mode input voltage	V_{CC-} + 1.15	V_{CC+} – 1.15	V
T_A	Operating free-air temperature	–40	125	°C

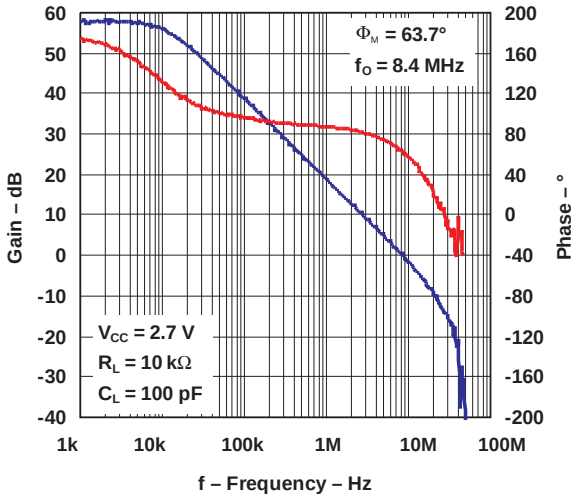
ELECTRICAL CHARACTERISTICS

V_{CC+} = 2.5 V, $V_{CC–}$ = –2.5 V, full-range T_A = –40°C to 125°C (unless otherwise noted)

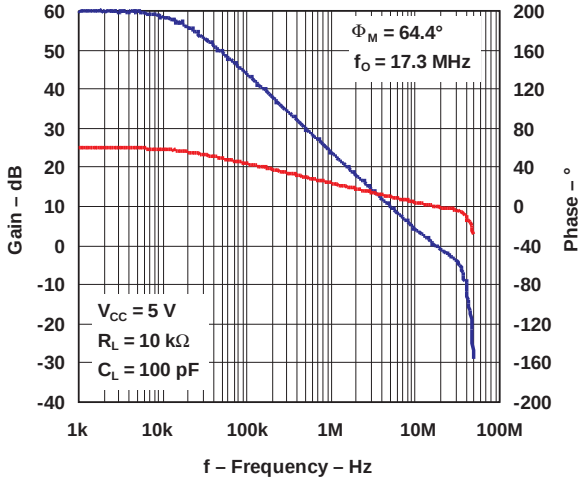
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1	4	mV
			Full range			6	
αV_{IO}	Input offset voltage drift	V_{ICM} = 0 V, V_O = 0 V	25°C		5		µV/°C
I_{IO}	Input offset current	V_{ICM} = 0 V, V_O = 0 V	25°C		10	150	nA
I_{IB}	Input bias current	V_{ICM} = 0 V, V_O = 0 V	25°C		200	750	nA
			Full range			1000	
V_{ICM}	Common-mode input voltage		25°C	–1.35		1.35	V
CMRR	Common-mode rejection ratio	V_{ICM} = ±1.35 V	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	V_{CC} = ±2 V to ±3 V	25°C	60	70		dB
A_{VD}	Large-signal voltage gain	R_L = 2 kΩ	25°C	70	80		dB
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	2	2.4		V
V_{OL}	Low-level output voltage	R_L = 2 kΩ	25°C		–2.4	–2	V
I_{source}	Output source current		25°C	1.2	1.4		mA
		V_{OUT} = ±2.5 V	Full range	1			
I_{sink}	Output sink current		25°C	50	80		mA
		V_{OUT} = ±2.5 V	Full range	25			
I_{CC}	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	8.5	12		MHz
SR	Slew rate	A_V = 1, V_{IN} = ±1 V	25°C	2.8	5		V/µs
			Full range	2.8			
Φm	Phase margin at unity gain	R_L = 2 kΩ, C_L =100 pF	25°C		60		°
Gm	Gain margin	R_L = 2 kΩ, C_L =100 pF	25°C		10		dB
V_n	Equivalent input noise voltage	f = 100 kHz	25°C		4		nV/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –1, R_L = 10 kΩ	25°C		0.003		%

TYPICAL CHARACTERISTICS

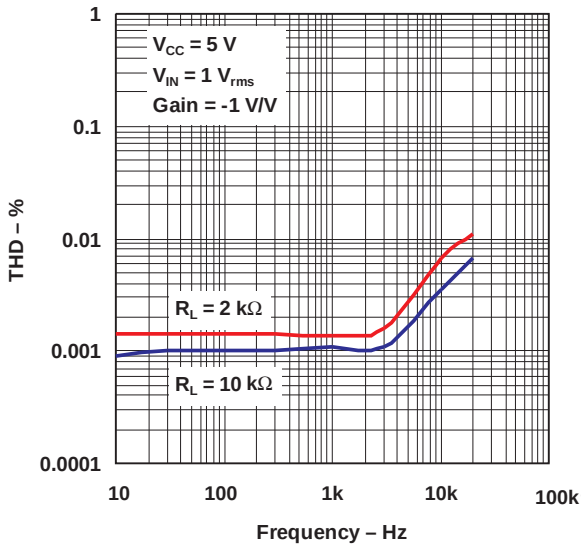
GAIN AND PHASE vs FREQUENCY



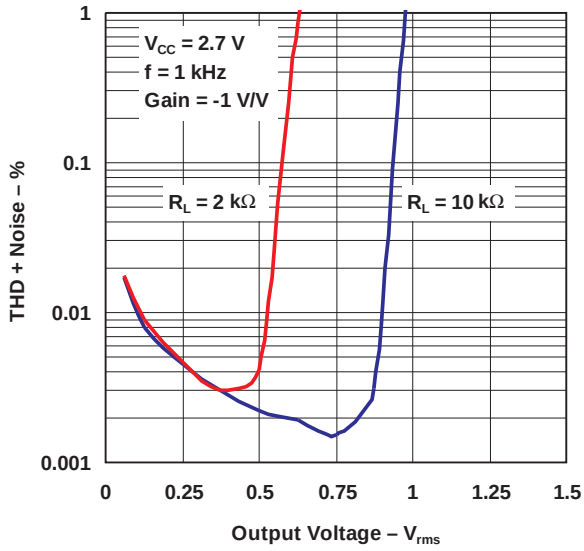
GAIN AND PHASE vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

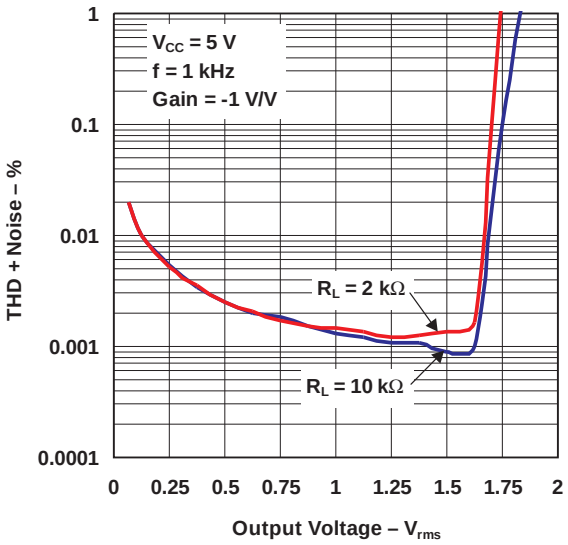


TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

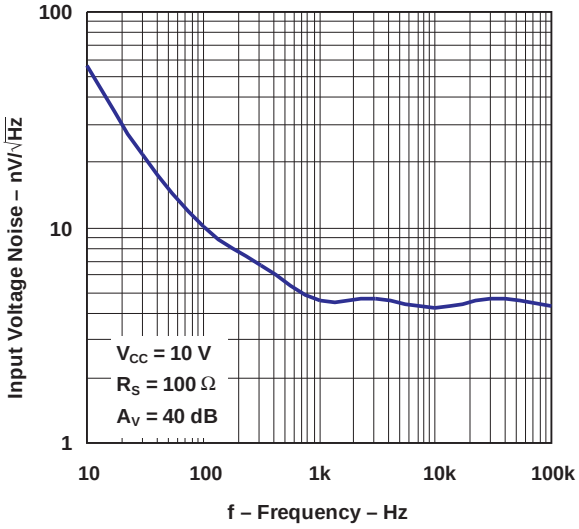


TYPICAL CHARACTERISTICS (continued)

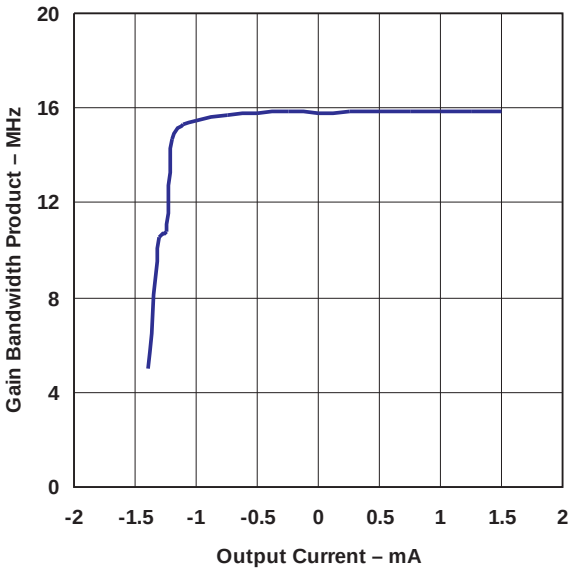
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



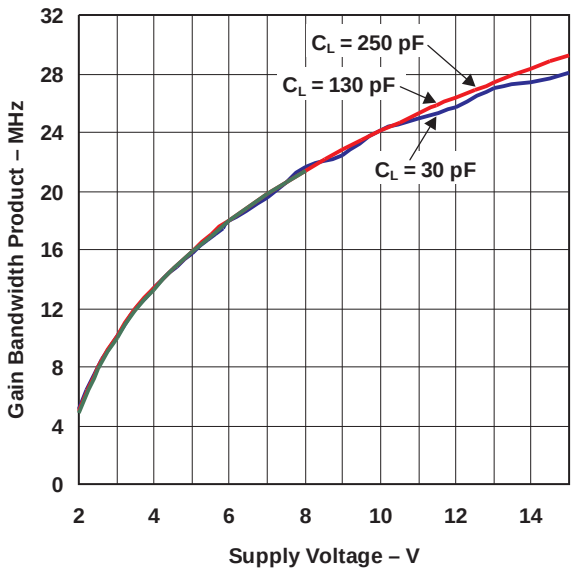
INPUT VOLTAGE NOISE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs OUTPUT CURRENT

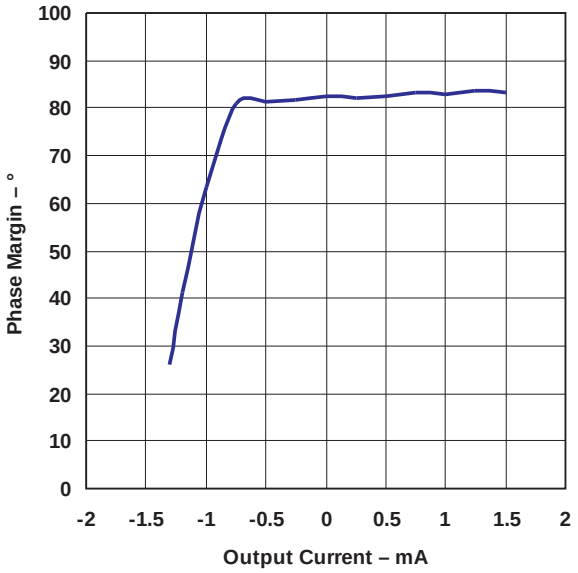


GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

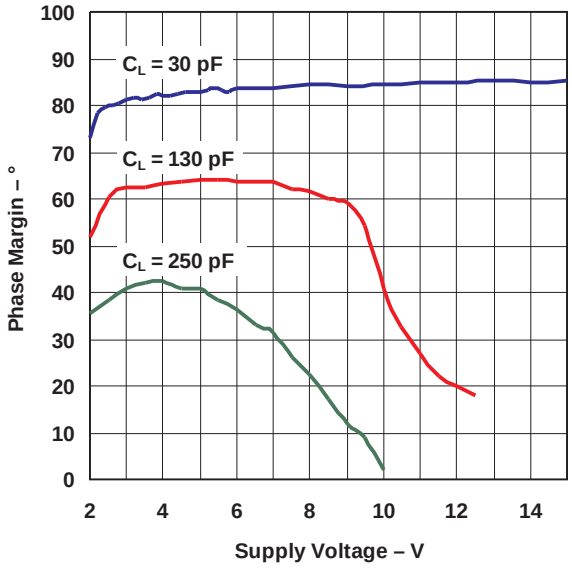


TYPICAL CHARACTERISTICS (continued)

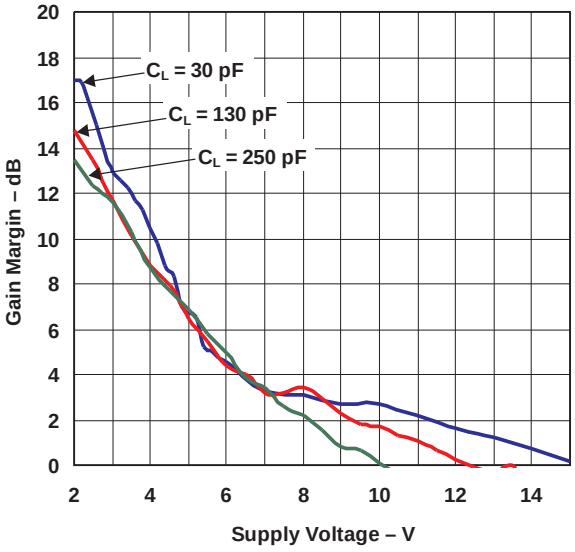
PHASE MARGIN vs OUTPUT CURRENT



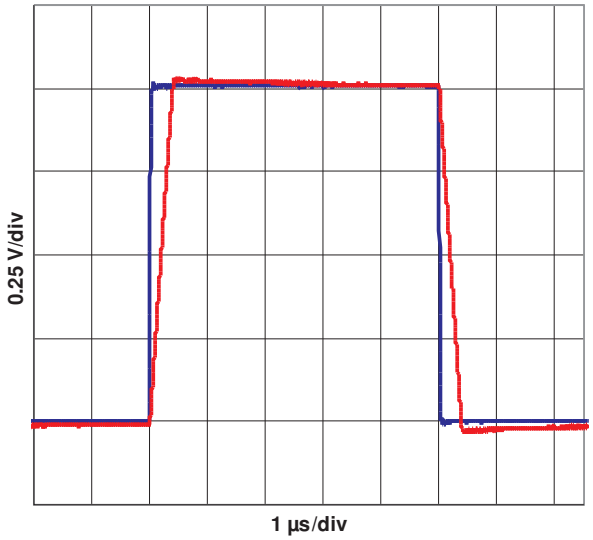
PHASE MARGIN vs SUPPLY VOLTAGE



GAIN MARGIN vs SUPPLY VOLTAGE

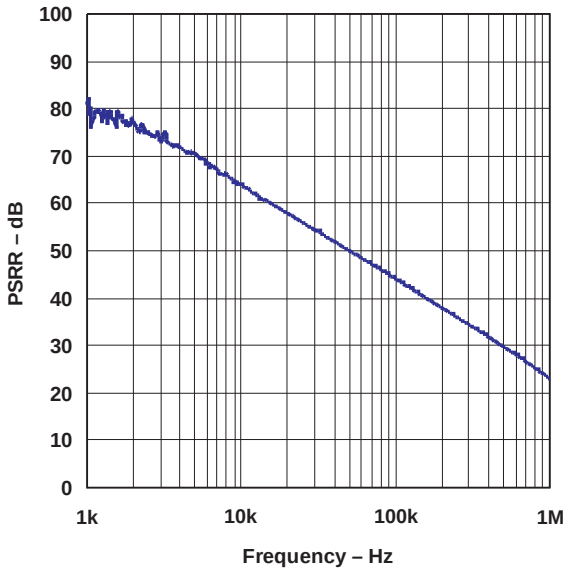


INPUT RESPONSE

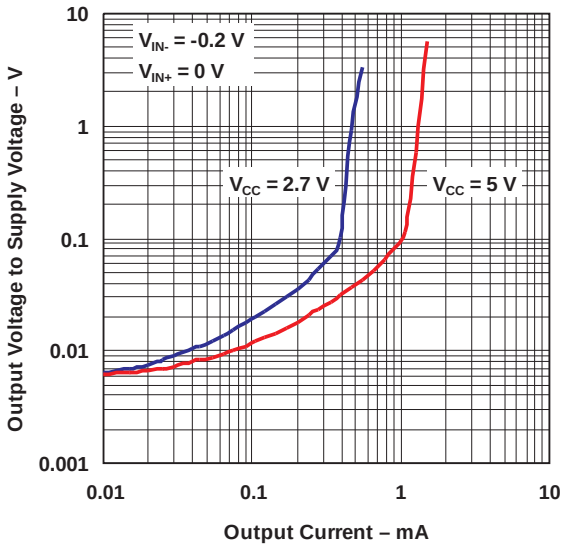


TYPICAL CHARACTERISTICS (continued)

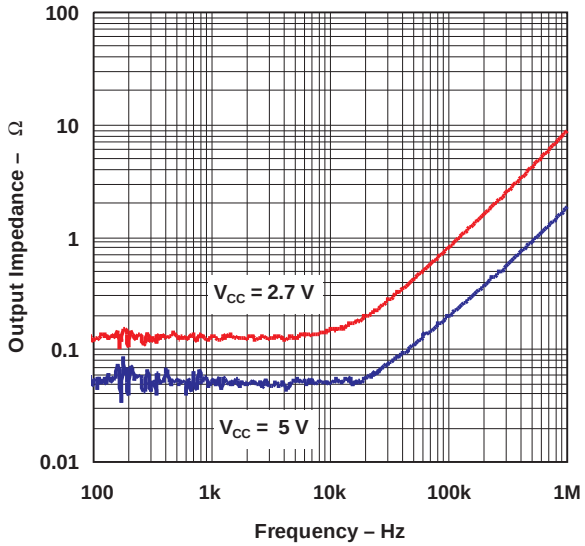
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY



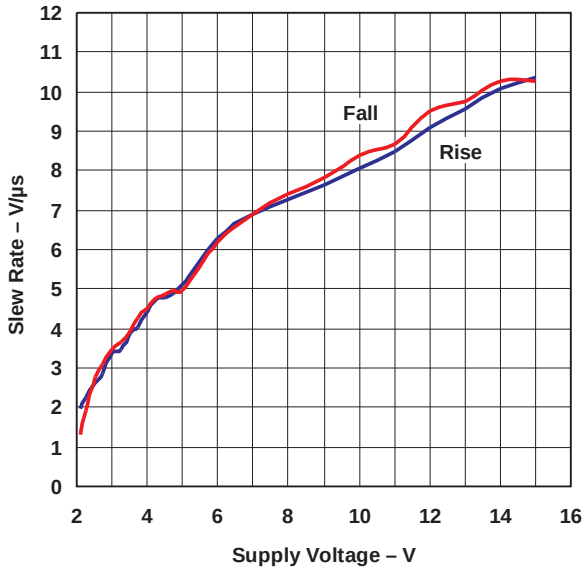
OUTPUT VOLTAGE vs OUTPUT CURRENT



OUTPUT IMPEDANCE vs FREQUENCY



SLEW RATE vs SUPPLY VOLTAGE



REVISION HISTORY

Changes from Revision F (December 2009) to Revision G	Page
• Changed slew rate MIN value.	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL971ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	Samples
TL971IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	Samples
TL971IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	Samples
TL971IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971	Samples
TL972ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSA	Samples
TL972IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL972IP	Samples
TL972IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL972IP	Samples
TL972IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL972IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972	Samples
TL974ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	Samples
TL974IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL974IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	Samples
TL974IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I	Samples
TL974IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL974IN	Samples
TL974INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TL974IN	Samples
TL974IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	Samples
TL974IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	Samples
TL974IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	Samples
TL974IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF TL971, TL972, TL974 :

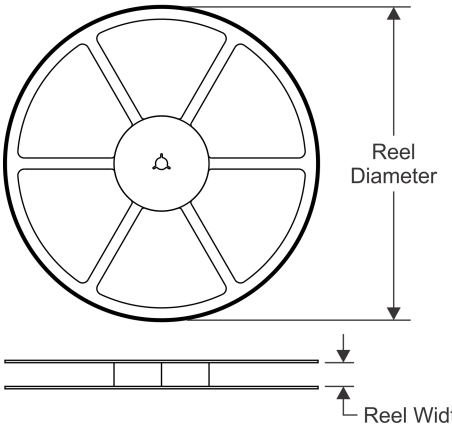
- Automotive: TL971-Q1, TL972-Q1, TL974-Q1

NOTE: Qualified Version Definitions:

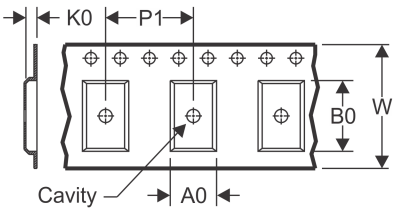
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

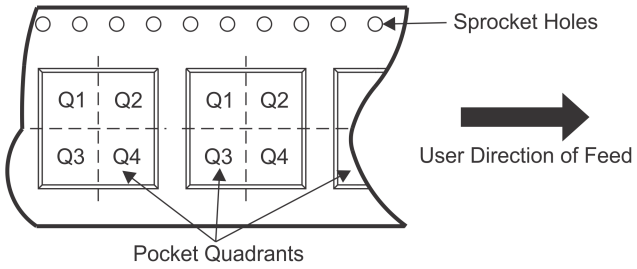


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

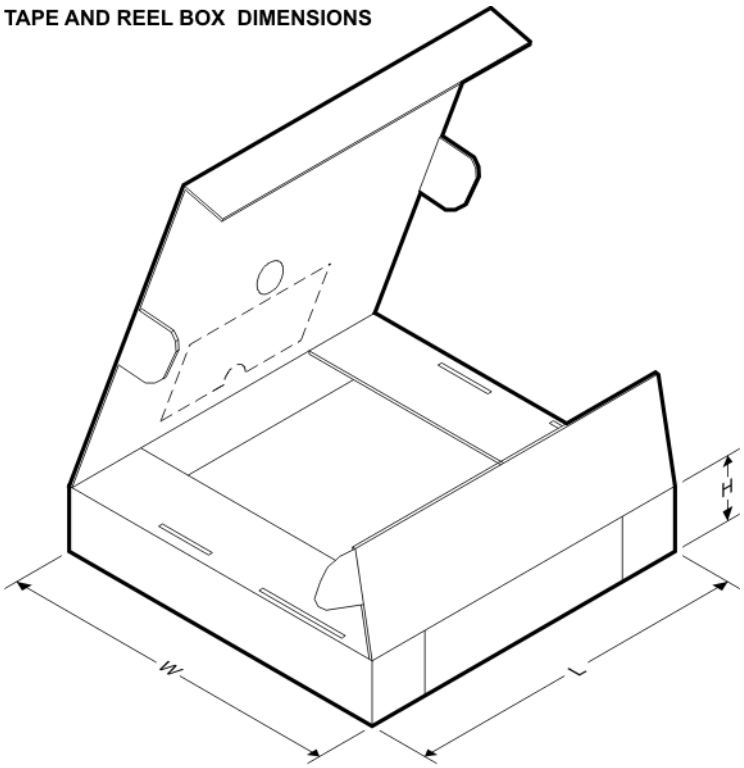
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

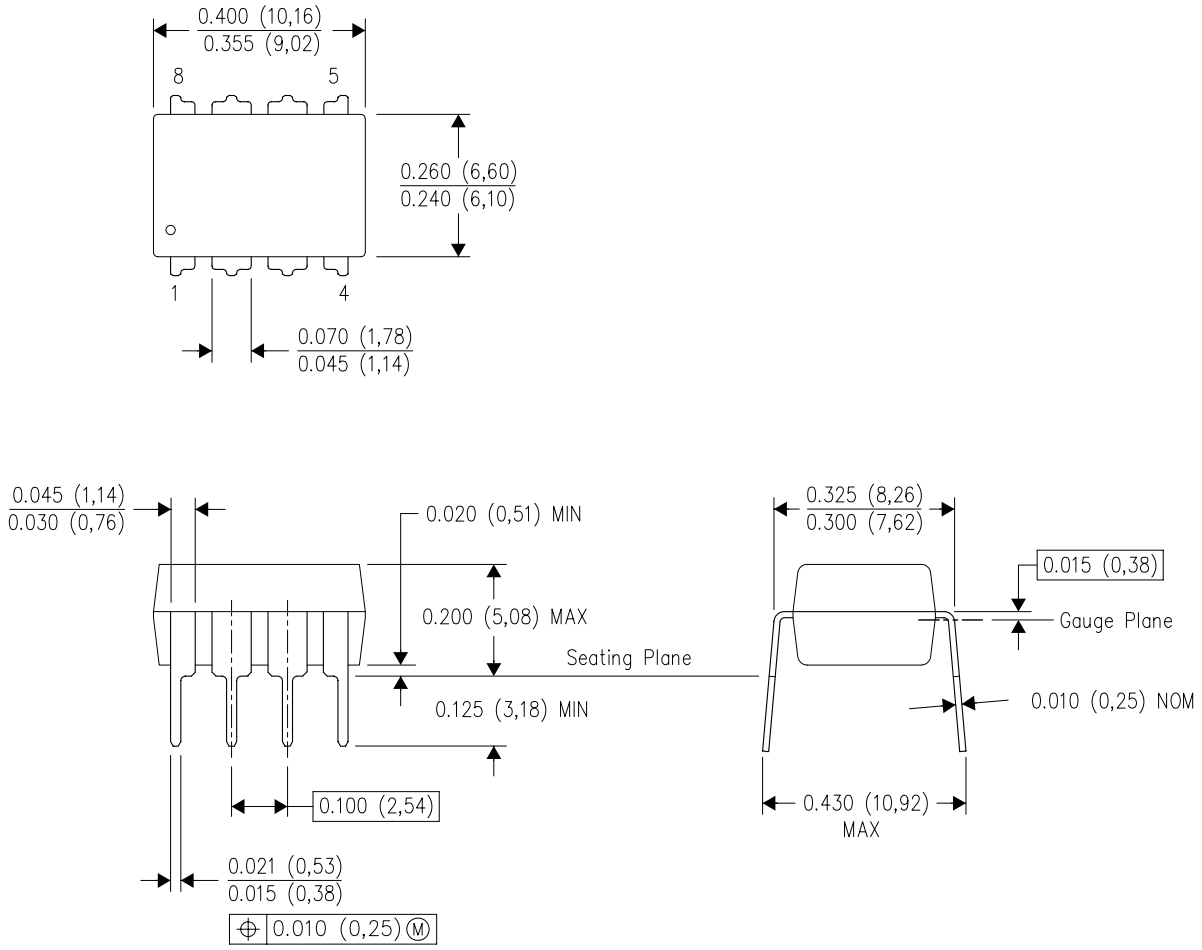
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL971IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TL972IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL974IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL974IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

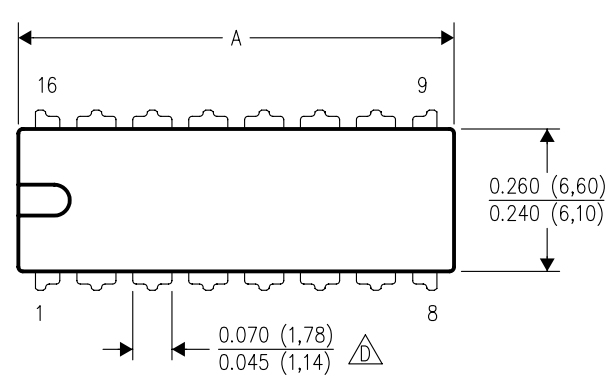


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

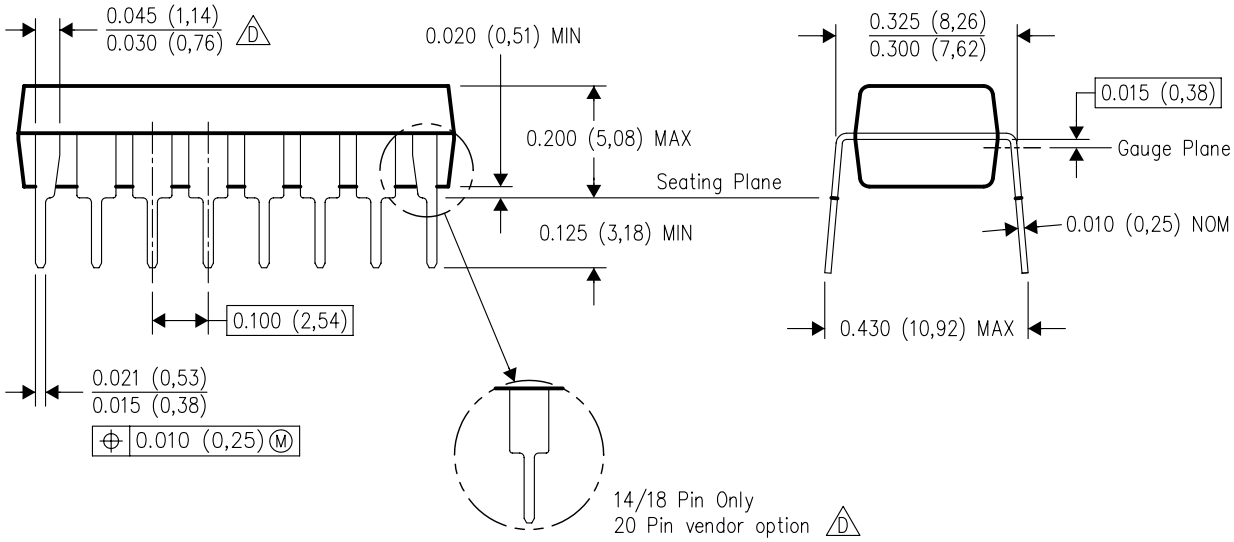
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



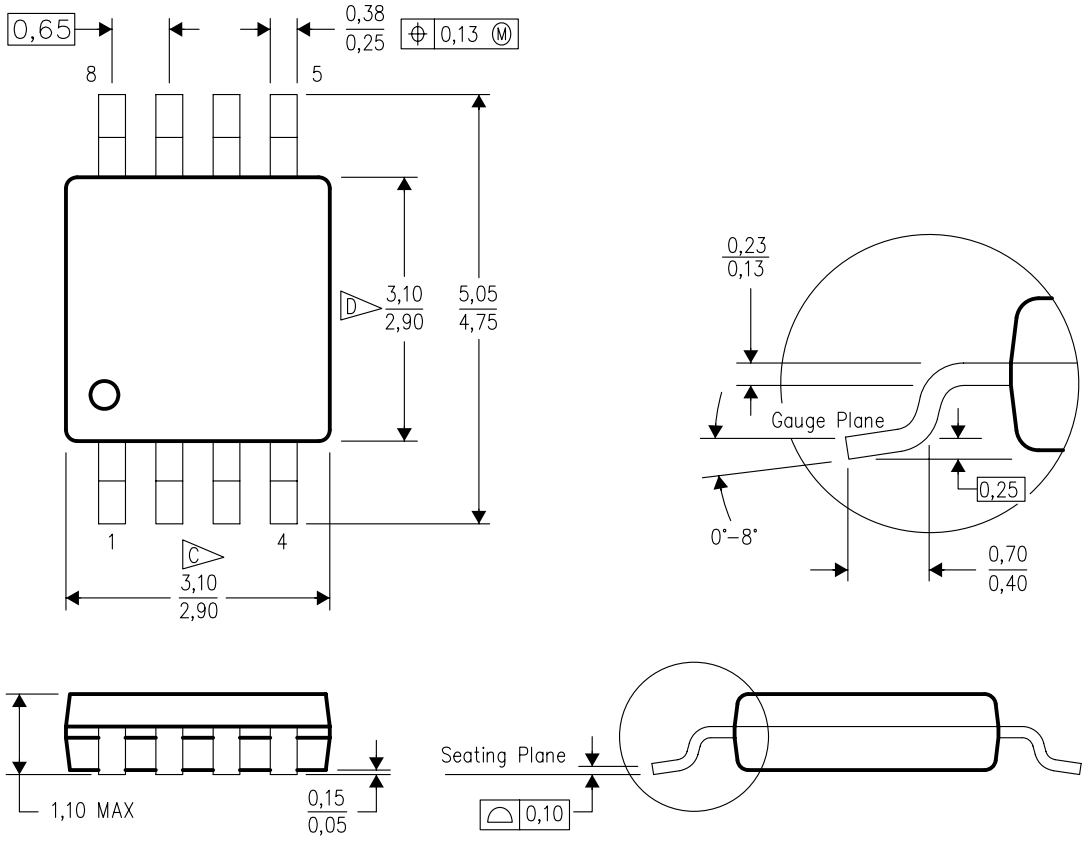
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

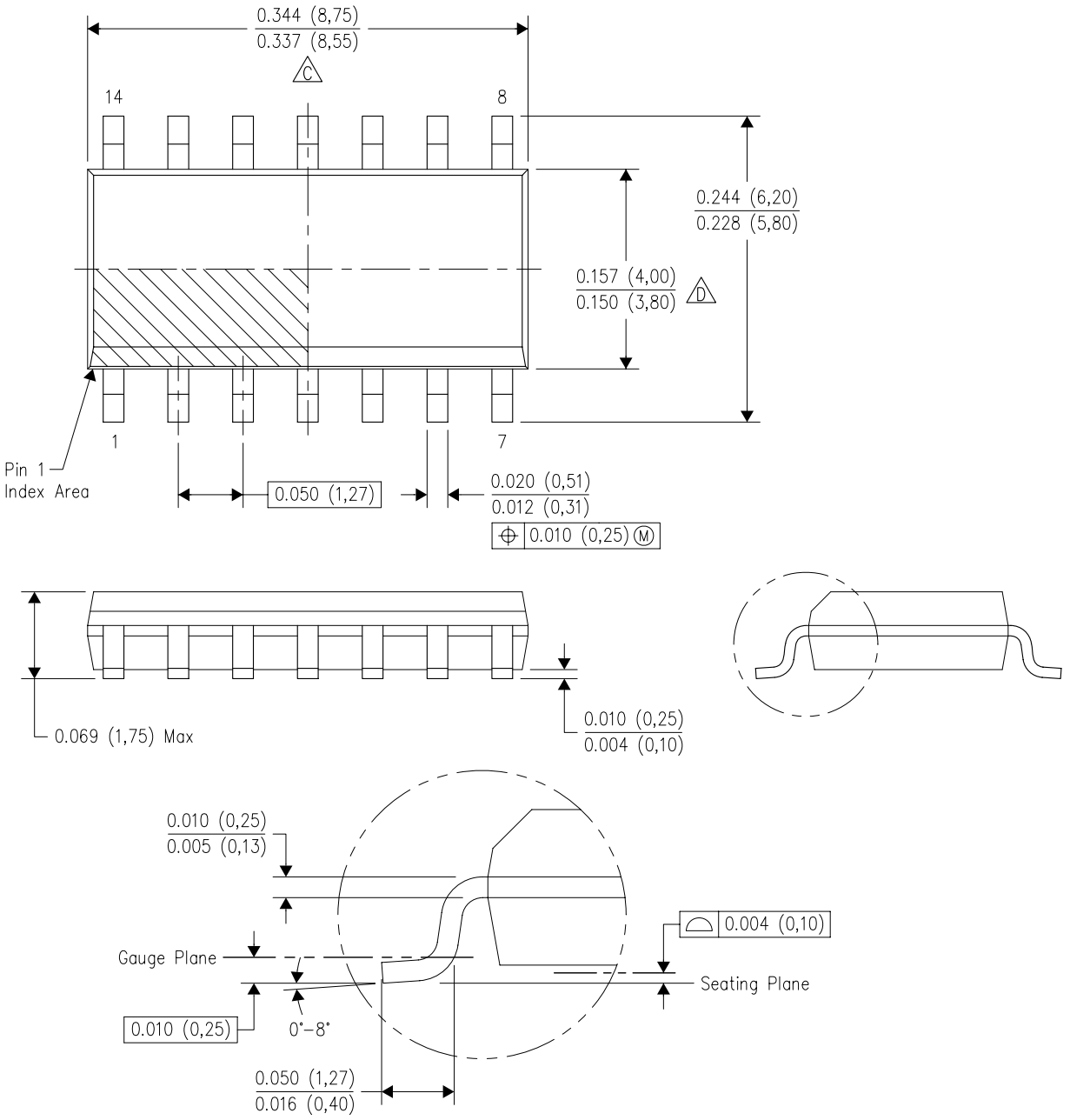
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

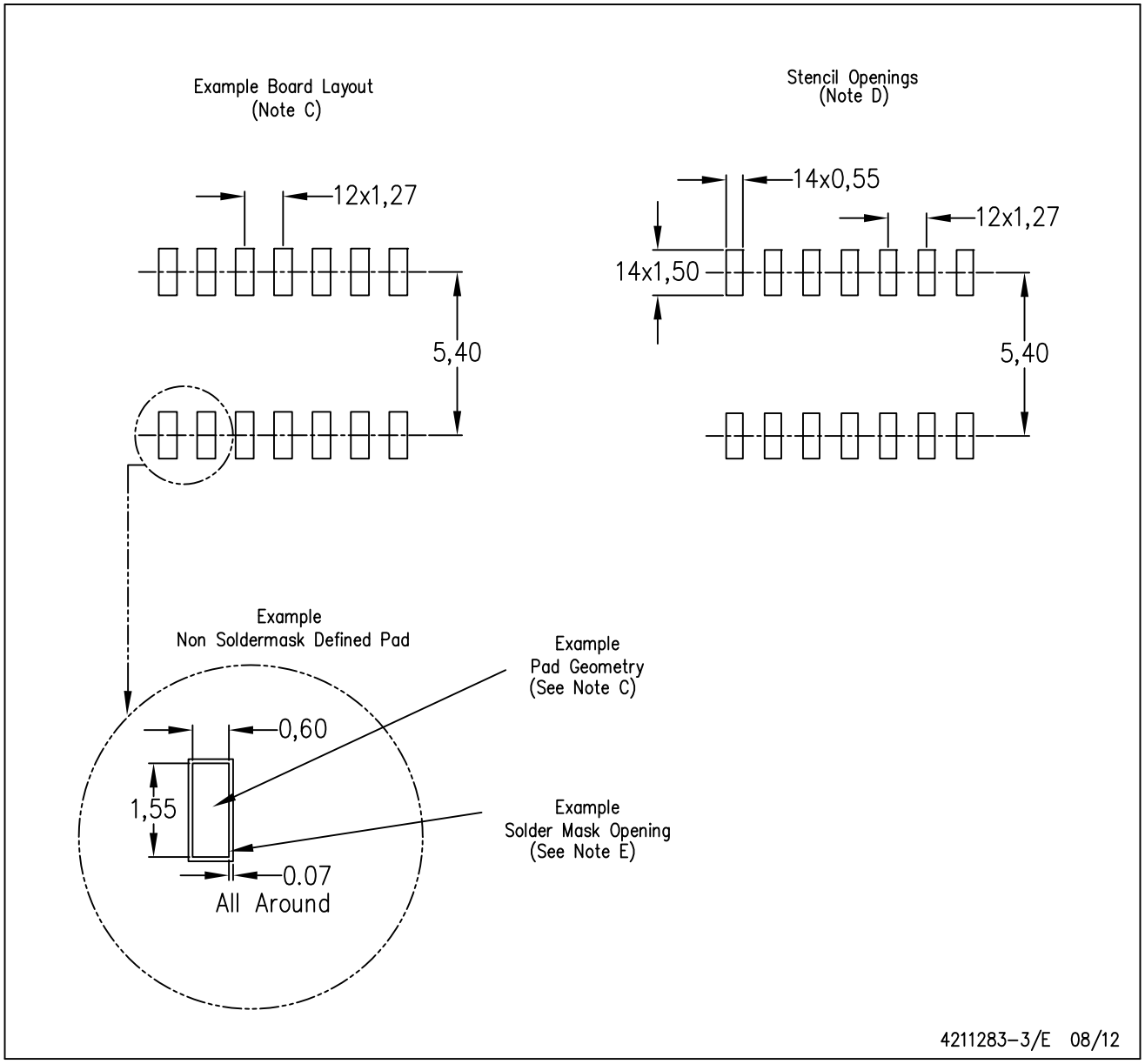
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

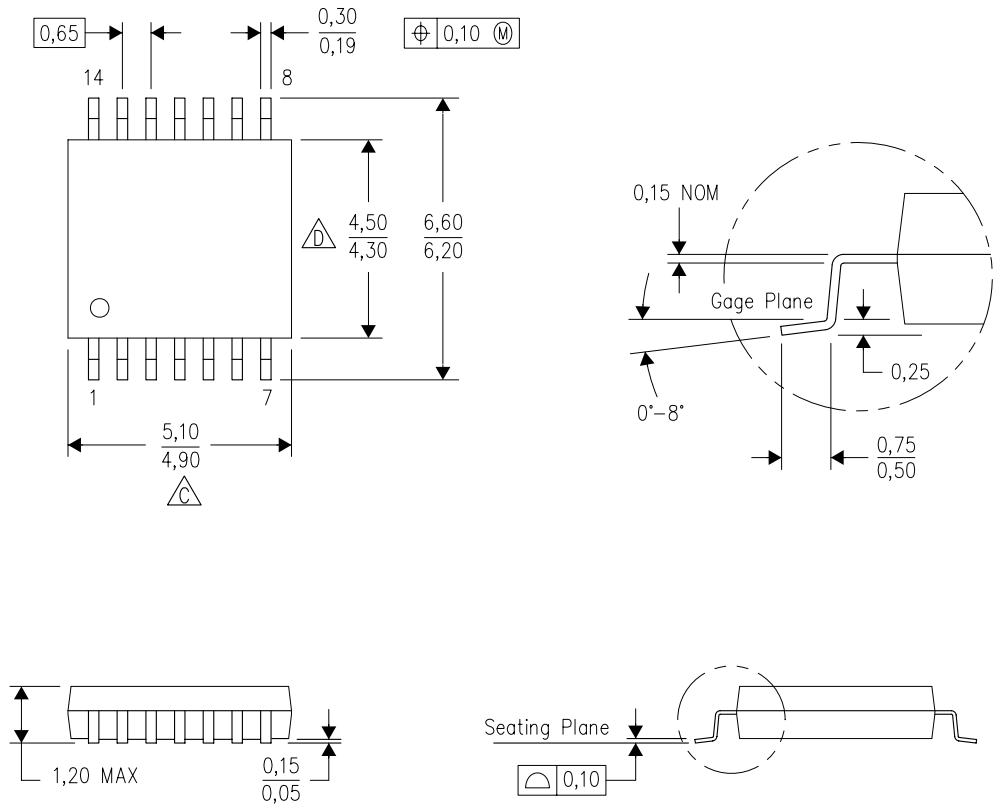
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

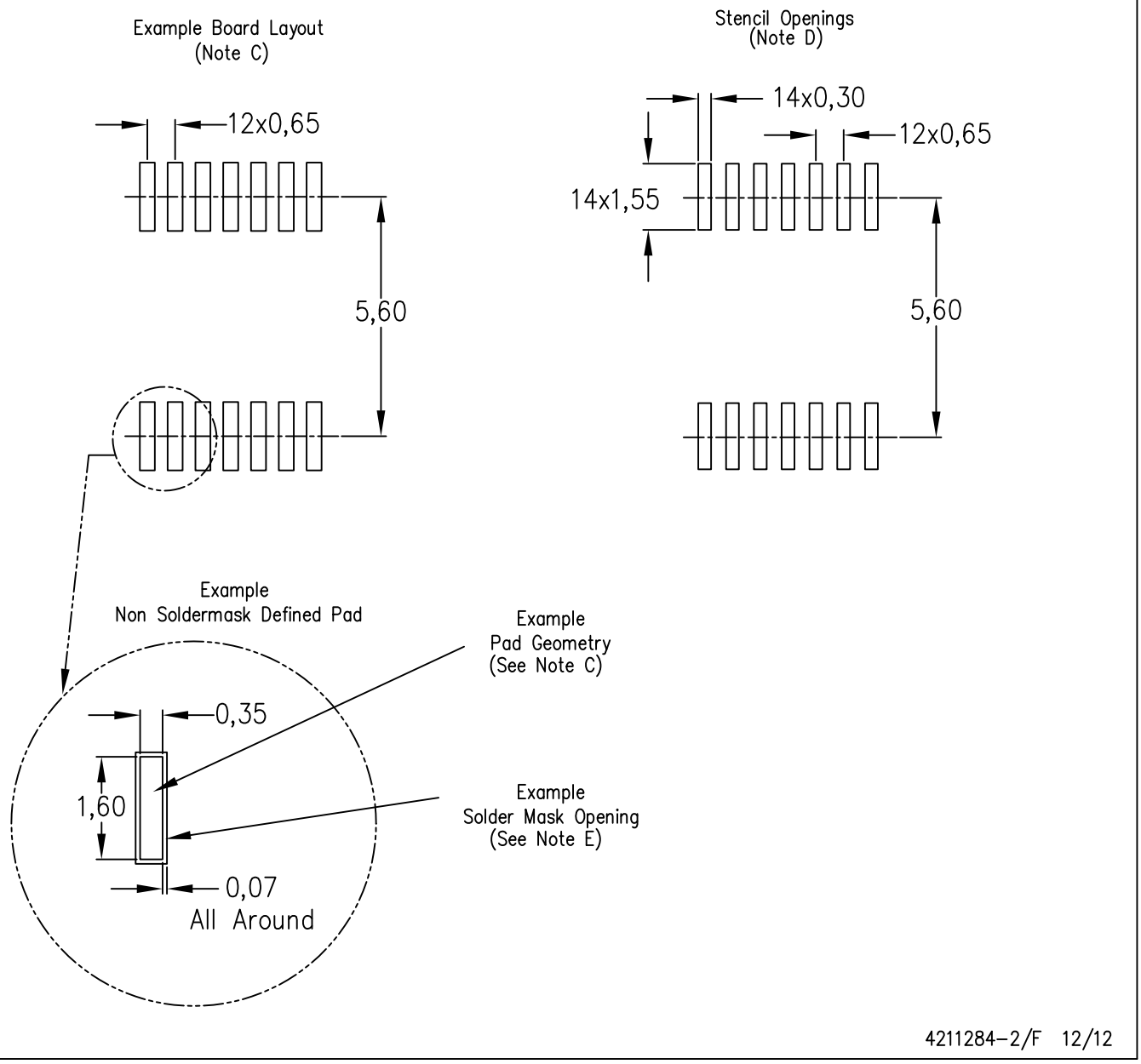
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

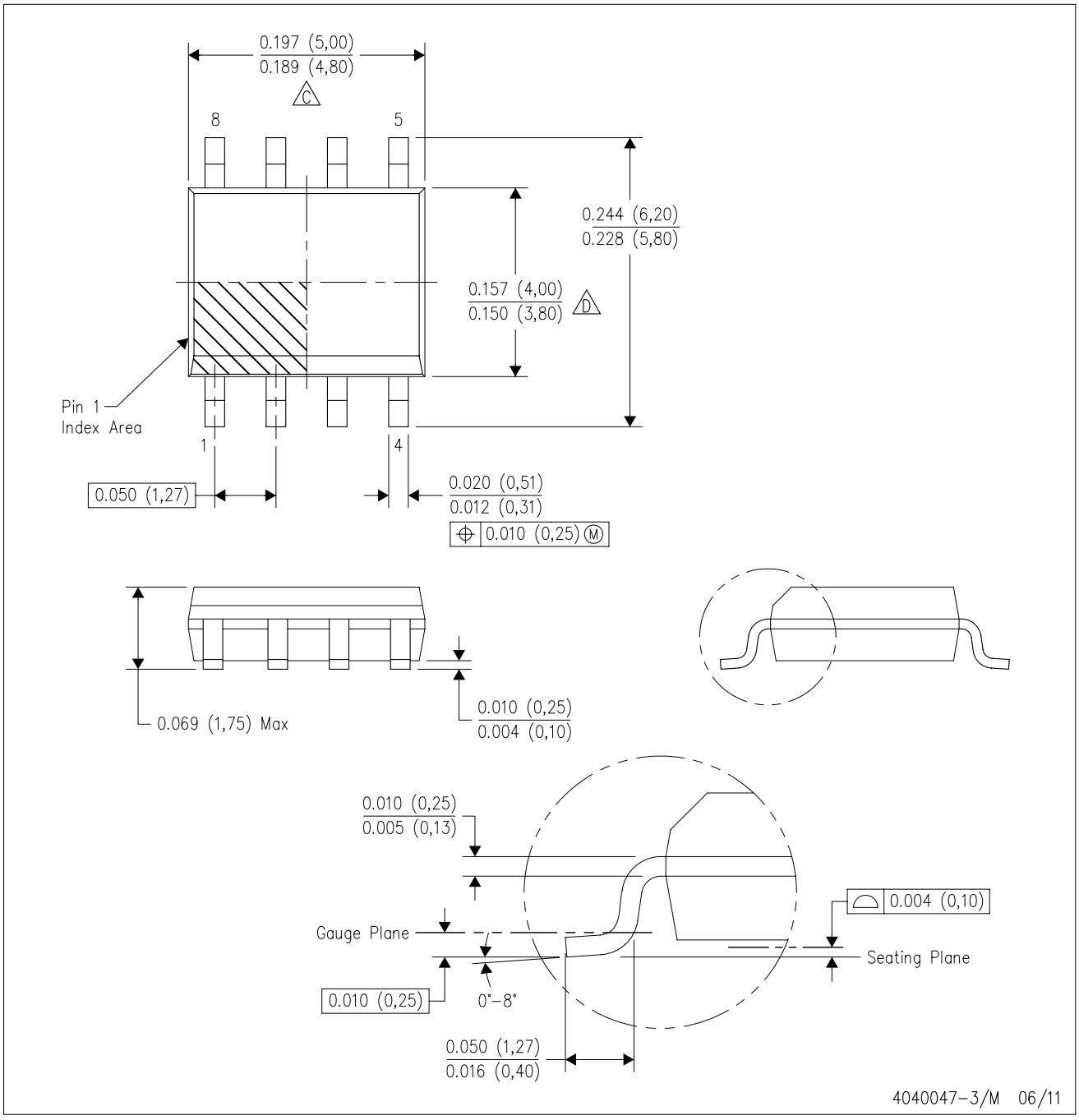
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



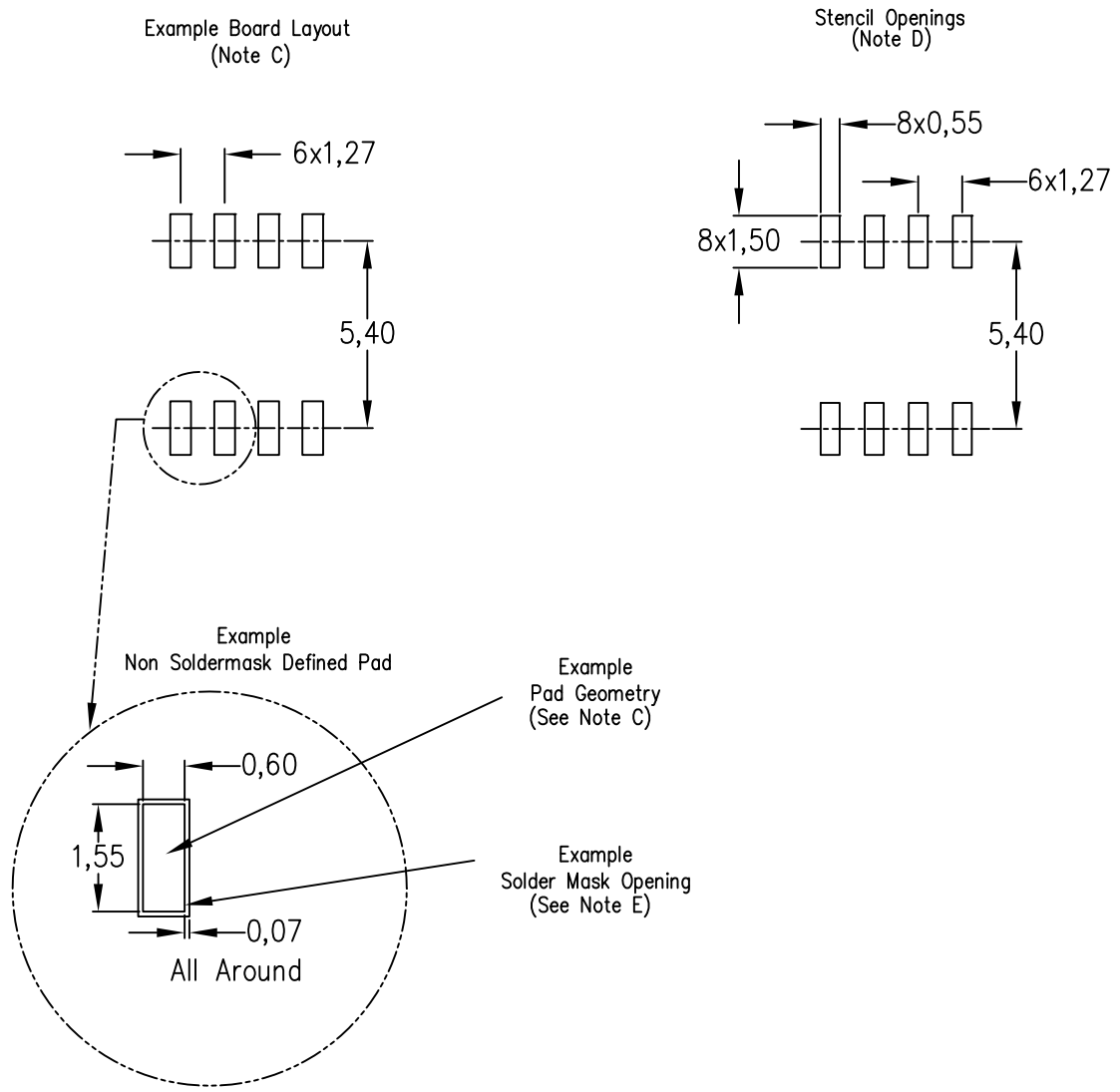
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



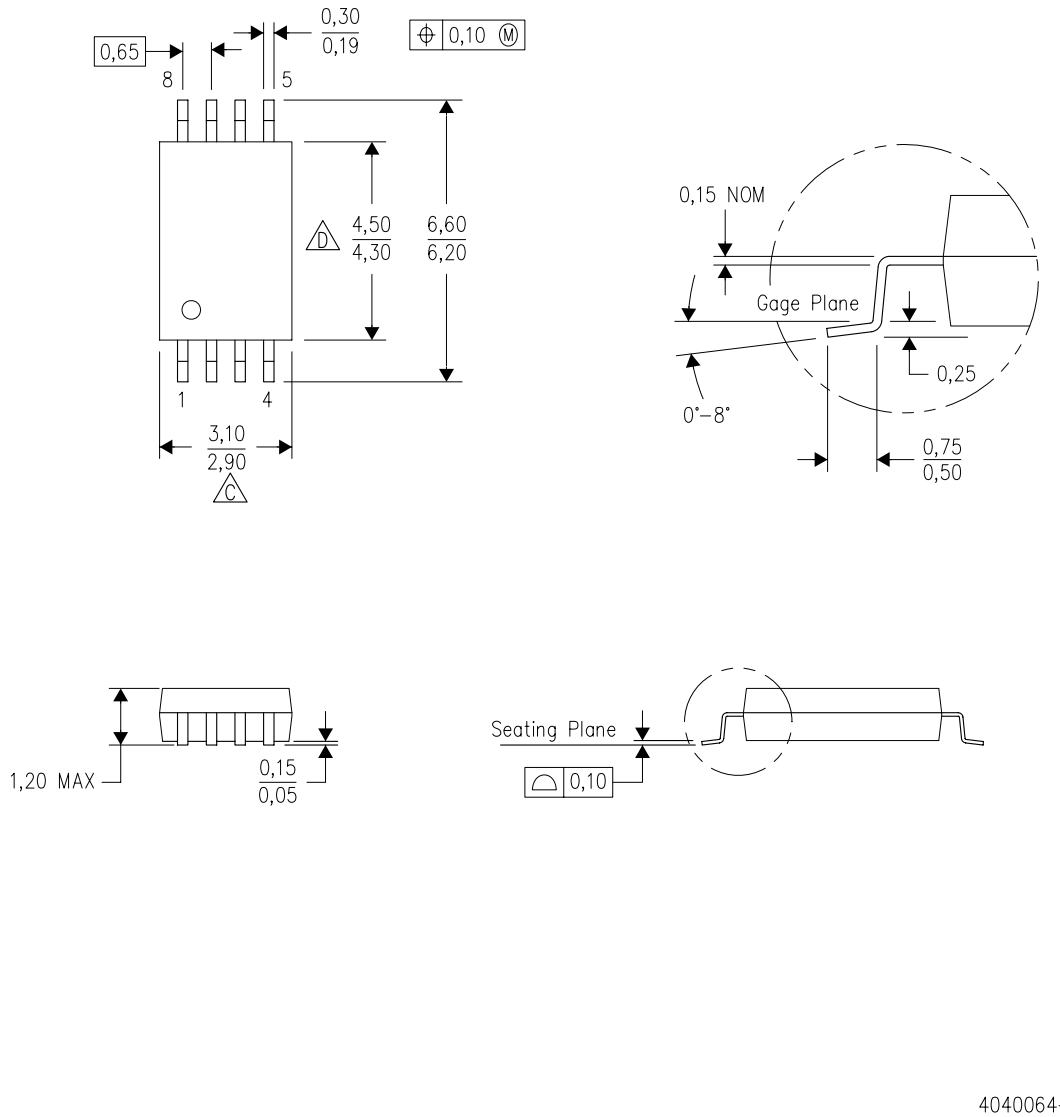
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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