# 138-mW DIRECTPATH™ STEREO HEADPHONE AMPLIFIER WITH I²C VOLUME CONTROL

## FEATURES

- **DirectPath™ Ground-Referenced Outputs**
  - **Eliminates Output DC Blocking Capacitors**
  - **Reduces Board Area**
  - **Reduces Component Height and Cost**
  - **Full Bass Response Without Attenuation**
- **Power Supply Voltage Range: 2.5 V to 5.5 V**
- **64 Step Audio Taper Volume Control**
- **High Power Supply Rejection Ratio (>100 dB PSRR)**
- **Differential Inputs for Maximum Noise Rejection (68 dB CMRR)**
- **High-Impedance Outputs When Disabled**
- **Advanced Pop and Click Suppression Circuitry**

- **Digital I²C Bus Control**
  - **Per Channel Mute and Enable**
  - **Software Shutdown**
  - **Multi-Mode Support: Stereo HP, Dual Mono HP, and Single-Channel BTL Operation**
  - **Amplifier Status**
- **Space Saving Packages**
  - **20 Pin, 4 mm x 4 mm QFN**
  - **16 ball, 2 mm x 2 mm WCSP**
- **ESD Protection of 8 kV HBM and IEC Contact**

## APPLICATIONS
- **Mobile Phones**
- **Portable Media Players**
- **Notebook Computers**
- **High Fidelity Applications**

## DESCRIPTION

The TPA6130A2 is a stereo DirectPath™ headphone amplifier with I²C digital volume control. The TPA6130A2 has minimal quiescent current consumption, with a typical $I_{DD}$ of 4 mA, making it optimal for portable applications. The I²C control allows maximum flexibility with a 64 step audio taper volume control, channel independent enables and mutes, and the ability to configure the outputs into stereo, dual mono, or a single receiver speaker BTL amplifier that drives 300 mW of power into 16 Ω loads.

The TPA6130A2 is a high fidelity amplifier with an SNR of 98 dB. A PSRR greater than 100 dB enables direct-to-battery connections without compromising the listening experience. The output noise of 9 μVrms (typical *A-weighted*) provides a minimal noise background during periods of silence. Configurable differential inputs and high CMRR allow for maximum noise rejection in the noisy environment of a mobile device.

TPA6130A2 packaging includes a 2 by 2 mm chip-scale package, and a 4 by 4 mm QFN package.
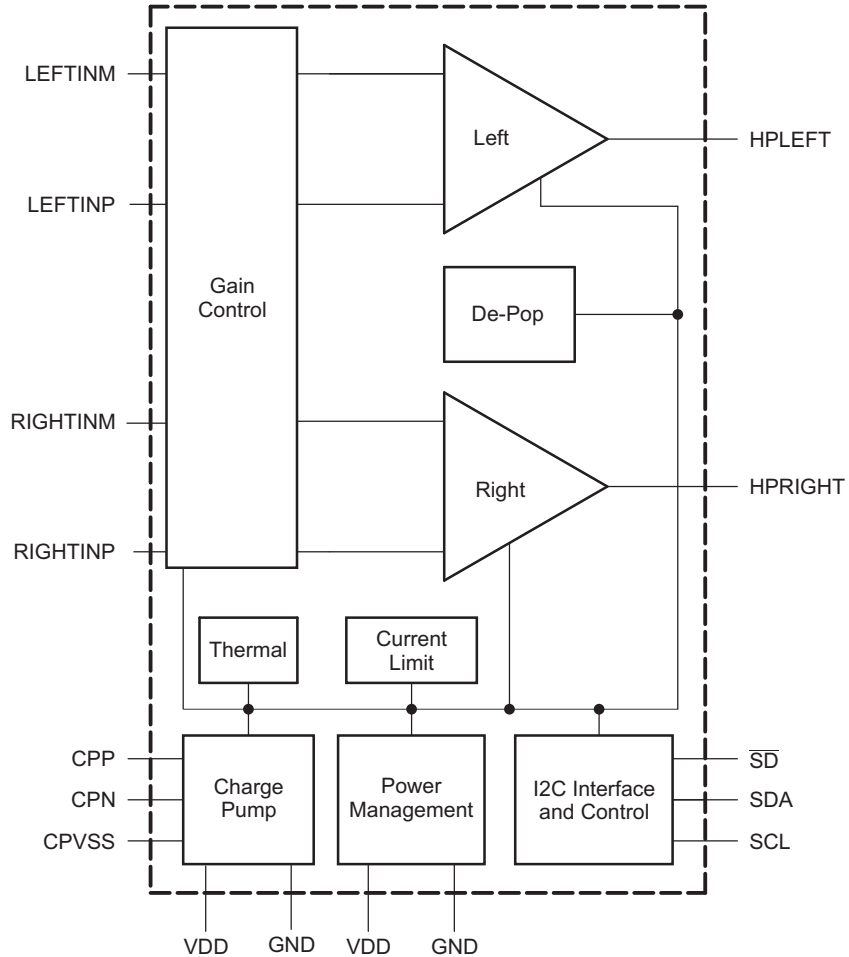
## SIMPLIFIED APPLICATION DIAGRAM
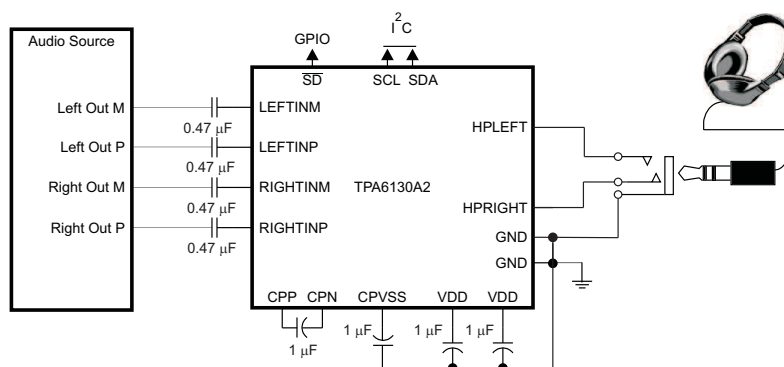
# TPA6130A2

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTIONAL BLOCK DIAGRAM

Headphone channels are independently enabled and muted. The I$^2$C interface controls channel gain, device modes, and charge pump activation. The charge pump generates a negative supply voltage for the output amplifiers. This allows a 0 V bias at the outputs, eliminating the need for bulky output capacitors. The thermal block detects faults and shuts down the device before damage occurs. The I$^2$C register records thermal fault conditions. The current limit block prevents the output current from getting high enough to damage the device. The De-Pop block eliminates audible pops during power-up, power-down, and amplifier enable and disable events.

Product Folder Link(s): *TPA6130A2*
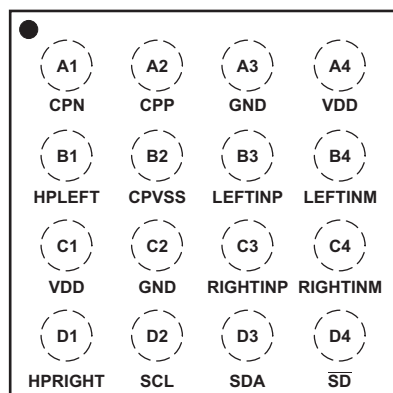
Top (Symbol Side) View WCSP Package (YZH)
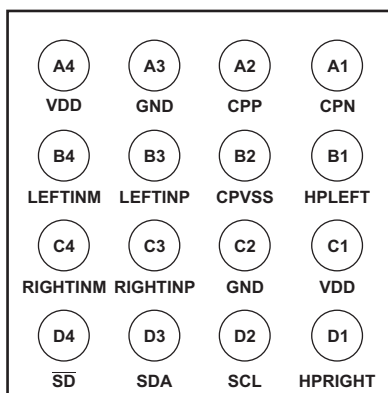
Bottom (Ball Side) View WCSP Package (YZH)
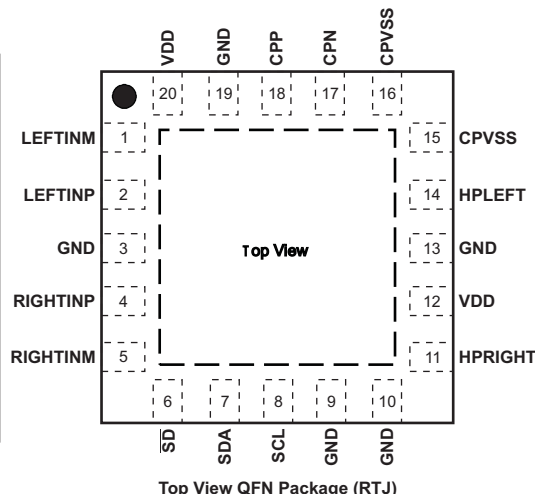
Top View QFN Package (RTJ)

## TERMINAL FUNCTIONS

| TERMINAL | | | INPUT/ OUTPUT/ POWER (I/O/P) | DESCRIPTION |
|---|---|---|---|---|
| NAME | BALL WCSP | PIN QFN | | |
| $V_{DD}$ | A4 | 20 | P | Charge pump voltage supply. $V_{DD}$ must be connected to the common $V_{DD}$ voltage supply. Decouple to GND (pin 19 on the QFN) with its own 1 μF capacitor. |
| GND | A3 | 19 | P | Charge pump ground. GND must be connected to common supply GND. It is recommended that this pin be decoupled to the $V_{DD}$ of the charge pump pin (pin 20 on the QFN). |
| CPP | A2 | 18 | P | Charge pump flying capacitor positive terminal. Connect one side of the flying capacitor to CPP. |
| CPN | A1 | 17 | P | Charge pump flying capacitor negative terminal. Connect one side of the flying capacitor to CPN. |
| LEFTINM | B4 | 1 | I | Left channel negative differential input. Impedance must be matched to LEFTINP. Connect the left input to LEFTINM when using single-ended inputs. |
| LEFTINP | B3 | 2 | I | Left channel positive differential input. Impedance must be matched to LEFTINM. AC ground LEFTINP near signal source while maintaining matched impedance to LEFTINM when using single-ended inputs. |
| CPVSS | B2 | 15, 16 | P | Negative supply generated by the charge pump. Decouple to pin 19 on the QFN or a GND plane. Use a 1 μF capacitor. |
| HPLEFT | B1 | 14 | O | Headphone left channel output. Connect to left terminal of headphone jack. |
| RIGHTINM | C4 | 5 | I | Right channel negative differential input. Impedance must be matched to RIGHTINP. Connect the right input to RIGHTINM when using single-ended inputs. |
| RIGHTINP | C3 | 4 | I | Right channel positive differential input. Impedance must be matched to RIGHTINM. AC ground RIGHTINP near signal source while maintaining matched impedance to RIGHTINM when using single-ended inputs. |
| GND | C2 | 3, 9, 10, 13 | P | Analog ground. Must be connected to common supply GND. It is recommended that this pin be used to decouple $V_{DD}$ for analog. Use pin 13 to decouple pin 12 on the QFN package. |
| $V_{DD}$ | C1 | 12 | P | Analog $V_{DD}$. $V_{DD}$ must be connected to common $V_{DD}$ supply. Decouple with its own 1-μF capacitor to analog ground (pin 13 on the QFN). |
| $\overline{SD}$ | D4 | 6 | I | Shutdown. Active low logic. 5V tolerant input. |
| SDA | D3 | 7 | I/O | SDA - I²C Data. 5V tolerant input. |
| SCL | D2 | 8 | I | SCL - I²C Clock. 5V tolerant input. |
| HPRIGHT | D1 | 11 | O | Headphone light channel output. Connect to the right terminal of the headphone jack. |
| Thermal pad | N/A | Die Pad | P | Solder the thermal pad on the bottom of the QFN package to the GND plane of the PCB. It is required for mechanical stability and will enhance thermal performance. |

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## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range, $T_A$ = 25°C (unless otherwise noted)

| | | | VALUE / UNIT |
|---|---|---|---|
| | Supply voltage, $V_{DD}$ | | −0.3 V to 6.0 V |
| $V_I$ | Input voltage | RIGHTINx, LEFTINx | −2.7 V to 3.6 V |
| | | $\overline{SD}$, SCL, SDA | −0.3 V to 7 V |
| | Output continuous total power dissipation | | See Dissipation Rating Table |
| $T_A$ | Operating free-air temperature range | | −40°C to 85°C |
| $T_J$ | Operating junction temperature range | | −40°C to 125°C |
| $T_{stg}$ | Storage temperature range | | −65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |
| | ESD Protection | HBM Output Pins | 8 kV |
| | | HBM All Other Pins | 3.5 kV |
| | IEC Contact ESD Protection[2] | No External Protection | 8 kV |
| | | V14MLA0603 Varistors Used for External Protection | 15 kV |
| | Minimum Load Impedance | | 12.8 Ω |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested to IEC 61000-4-2 standards on a TPA6130A2 EVM.

## DISSIPATION RATINGS TABLE

| PACKAGE | $T_A ≤ 25°C$ POWER RATING | DERATING FACTOR[1] [2] | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| RTJ | 4100 mW | 41 mW/°C | 2250 mW | 1640 mW |
| YZH | 970 mW | 9.7 mW/°C | 530 mW | 390 mW |

(1) Derating factor measured with JEDEC High K board: 1S2P - One signal layer and two plane layers.
(2) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. Please see JEDEC document page for downloadable copies: http://www.jedec.org/download/default.cfm.

## AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICES[1] | PART NUMBER | SYMBOL |
|---|---|---|---|
| −40°C to 85°C | 20-pin, 4 mm × 4 mm QFN | TPA6130A2RTJ[2] | BSG |
| | 16-ball, 1,98 mm × 1.98 mm (+0,01mm, −0,09 mm) | TPA6130A2YZH | BRU |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The RTJ package is only available taped and reeled. To order, add the suffix "R" to the end of the part number for a reel of 3000, or add the suffix "T" to the end of the part number for a reel of 250 (e.g., TPA6130A2RTJR).

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | Supply voltage, $V_{DD}$ | | 2.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | SCL, SDA, $\overline{SD}$ | 1.3 | | V |
| $V_{IL}$ | Low-level input voltage | SCL, SDA | | 0.6 | V |
| | | $\overline{SD}$ | | 0.35 | V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

Product Folder Link(s): *TPA6130A2*

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| |VOS| | Output offset voltage | $V_{DD}$ = 2.5 V to 5.5 V, inputs grounded | | | 150 | 400 | μV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 2.5 V to 5.5 V, inputs grounded | | | −109 | −90 | dB |
| CMRR | Common mode rejection ratio | $V_{DD}$ = 2.5 V to 5.5 V | | | −68 | | dB |
| $|I_{IH}|$ | High-level input current | $V_{DD}$ = 5.5 V, $V_I$ = $V_{DD}$ | SCL, SDA | | | 1 | μA |
| | | | $\overline{SD}$ | | | 10 | |
| $|I_{IL}|$ | Low-level input current | $V_{DD}$ = 5.5 V, $V_I$ = 0 V | SCL, SDA, $\overline{SD}$ | | | 1 | μA |
| $I_{DD}$ | Supply current | $V_{DD}$ = 2.5 V to 5.5 V, $\overline{SD}$ = $V_{DD}$ | | | 4 | 6 | mA |
| | | Shutdown mode, $V_{DD}$ = 2.5V to 5.5 V, $\overline{SD}$ = 0 V | | | 0.4 | 1 | μA |
| | | SW Shutdown mode, $V_{DD}$ = 2.5V to 5.5 V, SWS = 1 | | | 25 | 75 | μA |
| | | Both HP amps disabled, $V_{DD}$ = 2.5V to 5.5 V, SWS = 0, Charge Pump enabled, $\overline{SD}$ = $V_{DD}$ | | | 1.4 | 2.5 | mA |

## TIMING CHARACTERISTICS[1][2]

For I²C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | No wait states | | | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | | 0.6 | | | μs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 1.3 | | | μs |
| $t_{su1}$ | Setup time, SDA to SCL | | 300 | | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | | 10 | | | ns |
| $t_{(buf)}$ | Bus free time between stop and start condition | | 1.3 | | | μs |
| $t_{su2}$ | Setup time, SCL to start condition | | 0.6 | | | μs |
| $t_{h2}$ | Hold time, start condition to SCL | | 0.6 | | | μs |
| $t_{su3}$ | Setup time, SCL to stop condition | | 0.6 | | | μs |

(1)    $V_{Pull-up}$ = $V_{DD}$
(2)    A pull-up resistor ≤2 kΩ is required for a 5 V I²C bus voltage.
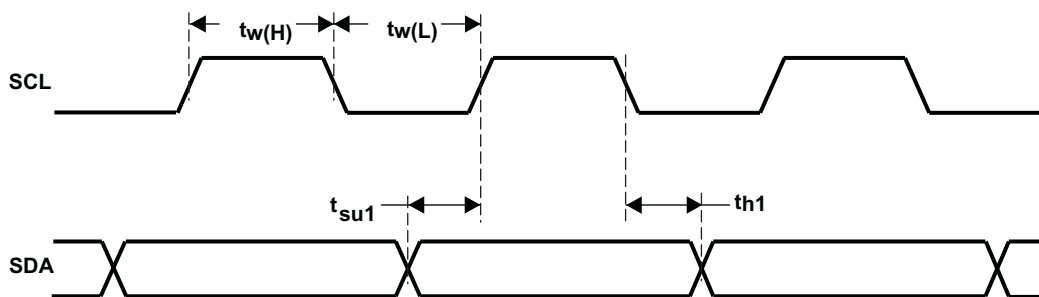


**Figure 1. SCL and SDA Timing**

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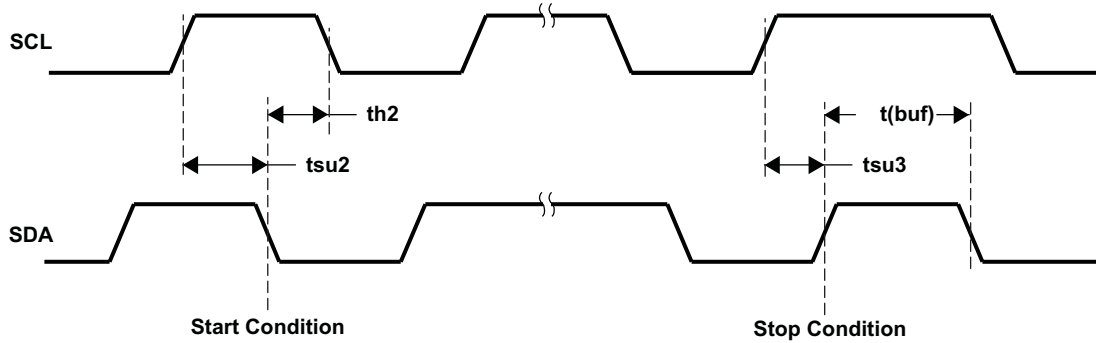


Figure 2. Start and Stop Conditions Timing

## OPERATING CHARACTERISTICS

$V_{DD}$ = 3.6 V , $T_A$ = 25°C, $R_L$ = 16 Ω (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $P_O$ | Output power | Stereo, Outputs out of phase, THD = 1%, f = 1 kHz, Gain = 0.1 dB | $V_{DD}$ = 2.5V | | 60 | | mW |
| | | | $V_{DD}$ = 3.6V | | 127 | | |
| | | | $V_{DD}$ = 5V | | 138 | | |
| | | Bridge-tied load, THD = 1%, f = 1 kHz, Gain = 0.1 dB | $V_{DD}$ = 2.5V | | 110 | | |
| | | | $V_{DD}$ = 3.6V | | 230 | | |
| | | | $V_{DD}$ = 5V | | 290 | | |
| THD+N | Total harmonic distortion plus noise | $P_O$ = 35 mW | f = 100 Hz | | 0.0029% | | |
| | | | f = 1 kHz | | 0.0055% | | |
| | | | f = 20 kHz | | 0.0027% | | |
| $k_{SVR}$ | Supply ripple rejection ratio | 200 mV$_{pp}$ ripple, f = 217 Hz | | | -97 | -90 | dB |
| | | 200 mV$_{pp}$ ripple, f = 1 kHz | | | -93 | | |
| | | 200 mV$_{pp}$ ripple, f = 20 kHz | | | -76 | | |
| $\Delta A_v$ | Gain matching | | | | 1% | | |
| | Slew rate | | | | 0.3 | | V/µs |
| $V_n$ | Noise output voltage | $V_{DD}$ = 3.6V, A-weighted, Gain = 0.1 dB | | | 9 | | µV$_{RMS}$ |
| $f_{osc}$ | Charge pump switching frequency | | | 300 | 400 | 500 | kHz |
| | Start-up time from shutdown | | | | 5 | | ms |
| | Differential input impedance | See Figure 33 | | | | | |
| SNR | Signal-to-noise ratio | $P_o$ = 35 mW | | | 98 | | dB |
| | Thermal shutdown | Threshold | | | 180 | | °C |
| | | Hysteresis | | | 35 | | °C |
| $Z_O$ | Tri-state HP output impedance | HiZ left and right bits set. HP amps disabled. DC value. | | | 25 | | MΩ |
| $C_O$ | Output capacitance | | | | 80 | | pF |

Product Folder Link(s): TPA6130A2

# TYPICAL CHARACTERISTICS

$C_{(PUMP, DECOUPLE, ,BYPASS, CPVSS)}$ = 1 μF, $C_I$ = 2.2μF.
All THD + N graphs taken with outputs out of phase (unless otherwise noted).

## Table of Graphs

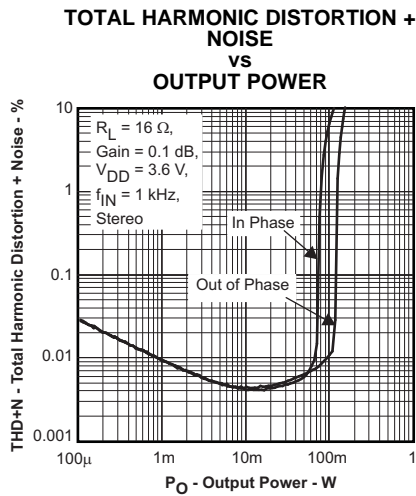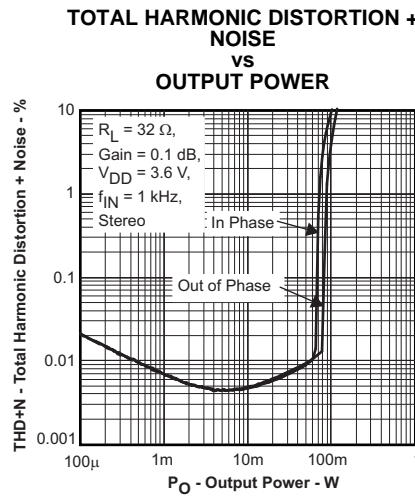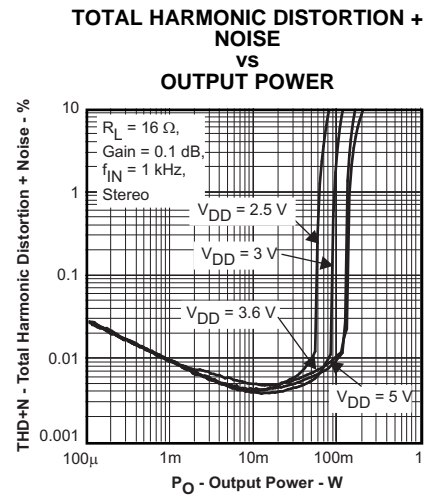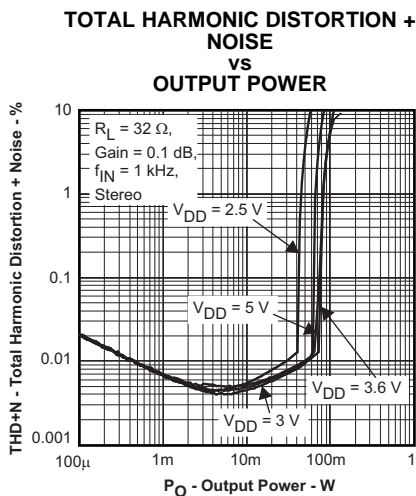| | | FIGURE |
|---|---|---|
| Total harmonic distortion + noise | vs Output power | 3–8 |
| Total harmonic distortion + noise | vs Frequency | 9–22 |
| Supply voltage rejection ratio | vs Frequency | 23-25 |
| Common mode rejection ratio | vs Frequency | 26-27 |
| Output power | vs Load | 28-29 |
| Output voltage | vs Load | 30-31 |
| Power Dissipation | vs Output power | 32 |
| Differential Input Impedance | vs Gain | 33 |
| Shutdown time | | 34 |
| Startup time | | 35 |



Figure 3.



Figure 4.



Figure 5.



Figure 6.



Figure 7.



Figure 8.

# TPA6130A2

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 16 Ω,
$V_{DD}$ = 2.5 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 20 mW

$P_O$ = 1 mW

$P_O$ = 4 mW

**Figure 9.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 16 Ω,
$V_{DD}$ = 3 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 40 mW

$P_O$ = 20 mW

$P_O$ = 5 mW

**Figure 10.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 16 Ω,
$V_{DD}$ = 3.6 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 70 mW

$P_O$ = 35 mW

$P_O$ = 5 mW

**Figure 11.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 16 Ω,
$V_{DD}$ = 5 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 50 mW

$P_O$ = 80 mW

$P_O$ = 5 mW

**Figure 12.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 32 Ω,
$V_{DD}$ = 2.5 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 20 mW

$P_O$ = 1 mW

$P_O$ = 4 mW

**Figure 13.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 32 Ω,
$V_{DD}$ = 3 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 20 mW

$P_O$ = 40 mW

$P_O$ = 5 mW

**Figure 14.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 32 Ω,
$V_{DD}$ = 3.6 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 35 mW

$P_O$ = 70 mW

$P_O$ = 5 mW

**Figure 15.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 32 Ω,
$V_{DD}$ = 5 V,
Gain = 0.1 dB,
Stereo

$P_O$ = 50 mW

$P_O$ = 70 mW

$P_O$ = 5 mW

**Figure 16.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**

$R_L$ = 16 Ω,
$V_{DD}$ = 2.5 V,
Gain = 6.1 dB,
BTL

$P_O$ = 100 mW

$P_O$ = 5 mW

$P_O$ = 25 mW

**Figure 17.**

All graphs: THD+N - Total Harmonic Distortion + Noise - % vs f - Frequency - Hz

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**TOTAL HARMONIC DISTORTION +
NOISE
vs
FREQUENCY**



**Figure 18.**

**TOTAL HARMONIC DISTORTION +
NOISE
vs
FREQUENCY**
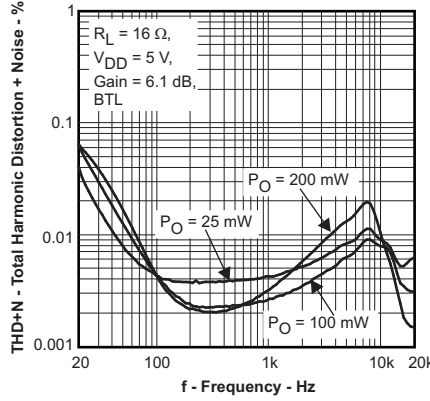


**Figure 19.**

**TOTAL HARMONIC DISTORTION +
NOISE
vs
FREQUENCY**
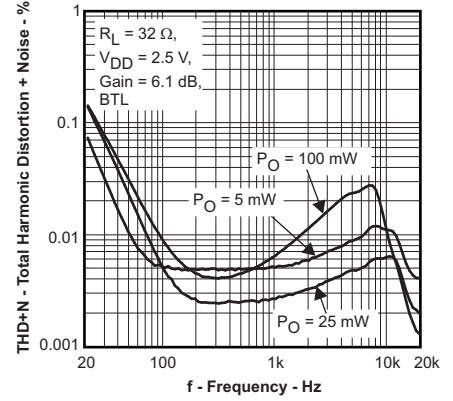


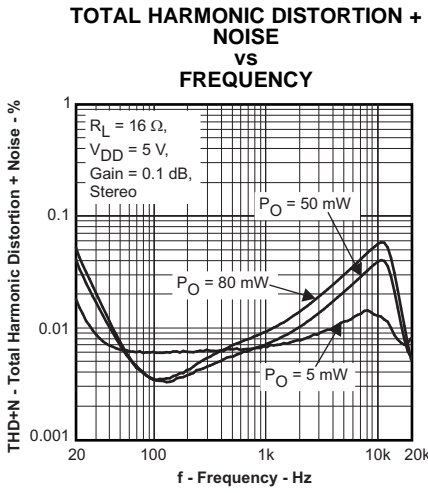**Figure 20.**
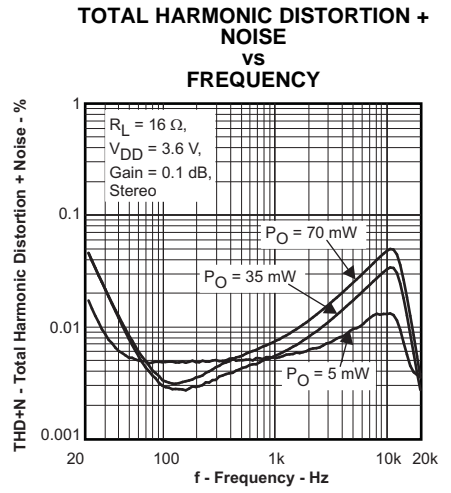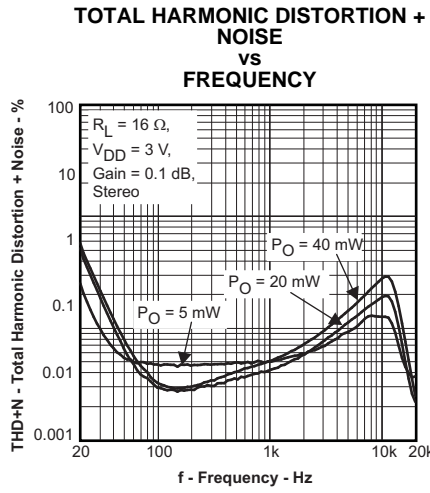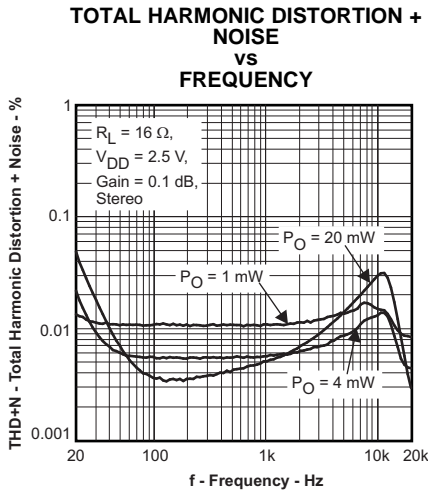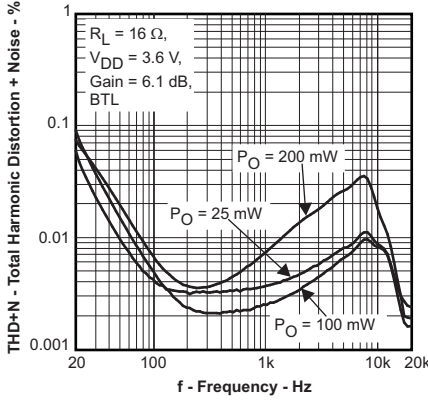
**TOTAL HARMONIC DISTORTION +
NOISE
vs
FREQUENCY**



**Figure 21.**
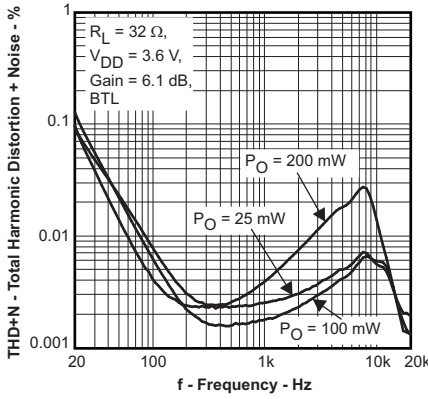
**TOTAL HARMONIC DISTORTION +
NOISE
vs
FREQUENCY**
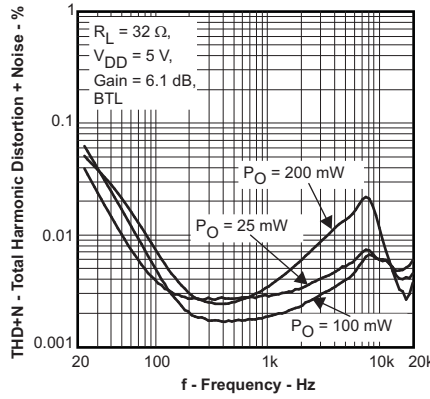


**Figure 22.**

**SUPPLY VOLTAGE REJECTION
RATIO
vs
FREQUENCY**
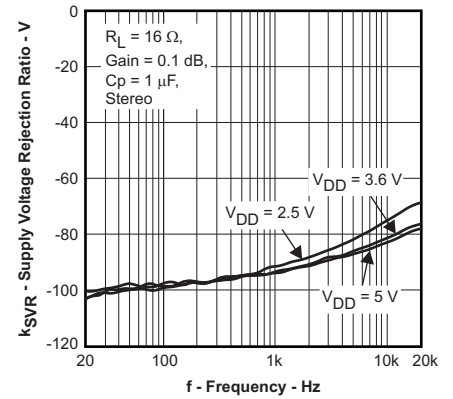


**Figure 23.**

**SUPPLY VOLTAGE REJECTION
RATIO
vs
FREQUENCY**
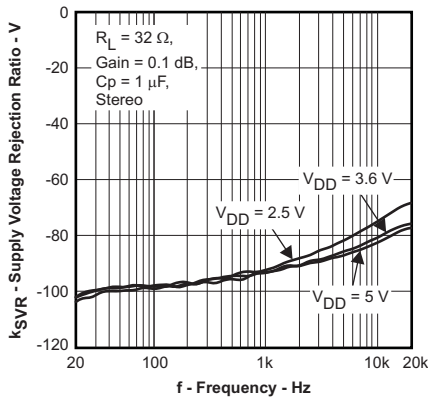


**Figure 24.**

**SUPPLY VOLTAGE REJECTION
RATIO
vs
FREQUENCY**
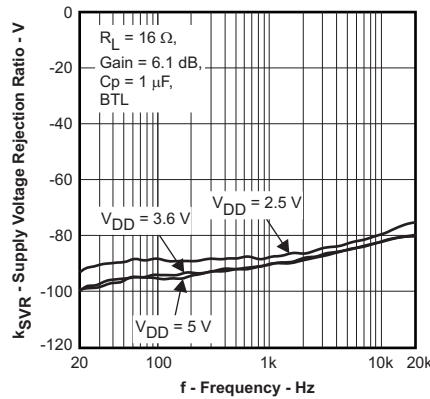


**Figure 25.**

**COMMON MODE REJECTION RATIO
vs
FREQUENCY**



**Figure 26.**

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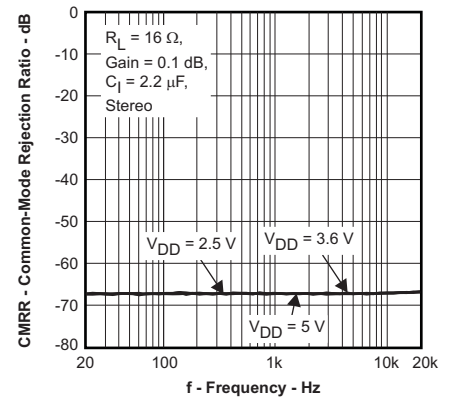
**COMMON MODE REJECTION RATIO**
**vs**
**FREQUENCY**
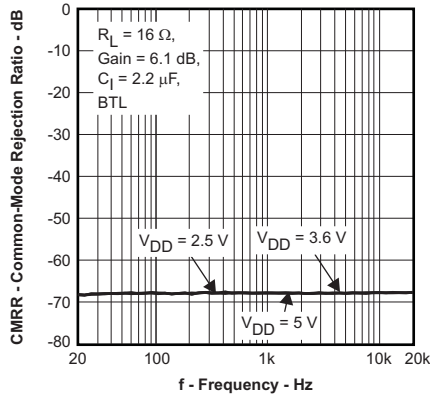


Figure 27.

**OUTPUT POWER**
**vs**
**LOAD**
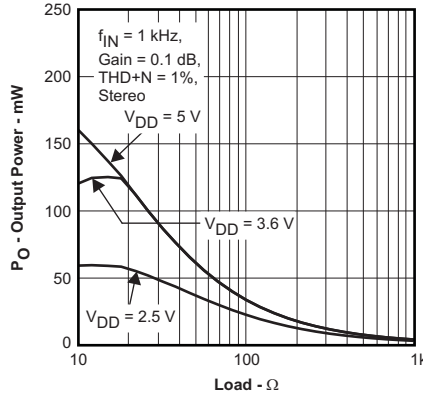


Figure 28.

**OUTPUT POWER**
**vs**
**LOAD**
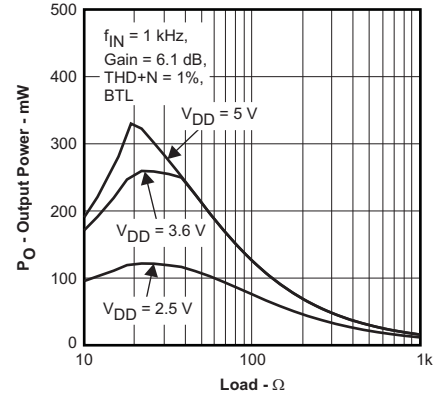


Figure 29.

**OUTPUT VOLTAGE**
**vs**
**LOAD**
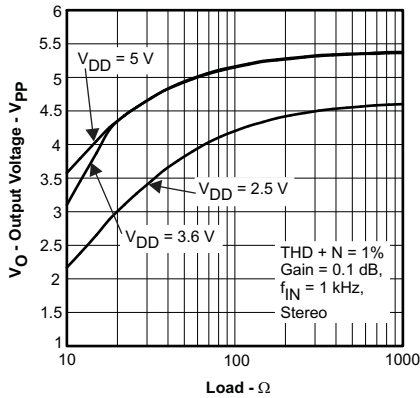


Figure 30.

**OUTPUT VOLTAGE**
**vs**
**LOAD**
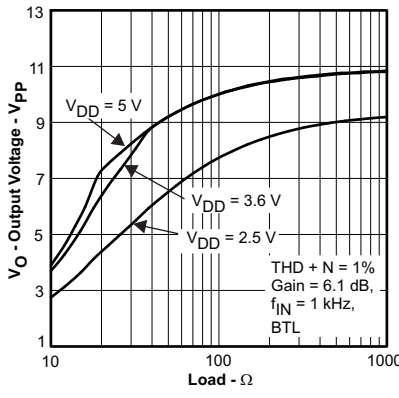


Figure 31.

**POWER DISSIPATION**
**vs**
**OUTPUT POWER**
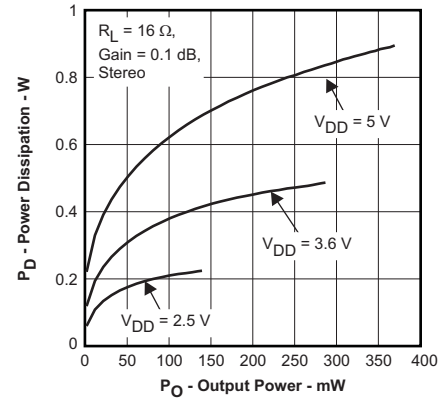


Figure 32.

**DIFFERENTIAL INPUT IMPEDANCE**
**vs**
**GAIN**



Figure 33.

Product Folder Link(s): *TPA6130A2*
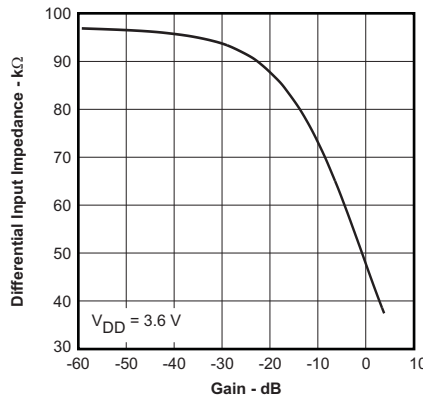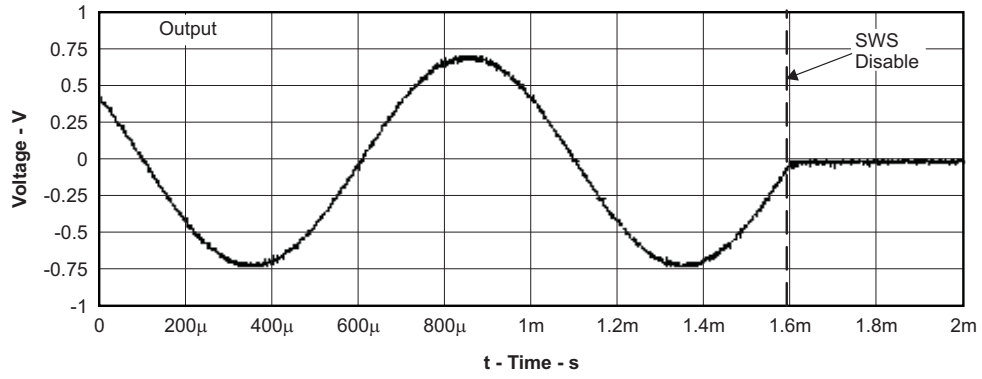
**Figure 34. Shutdown Time**



**Figure 35. Startup Time**

Product Folder Link(s): *TPA6130A2*
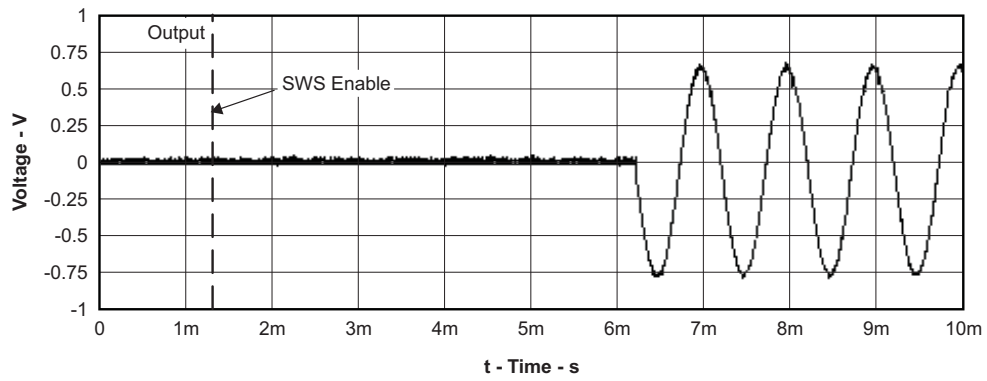
## APPLICATION INFORMATION

### SIMPLIFIED APPLICATIONS CIRCUIT
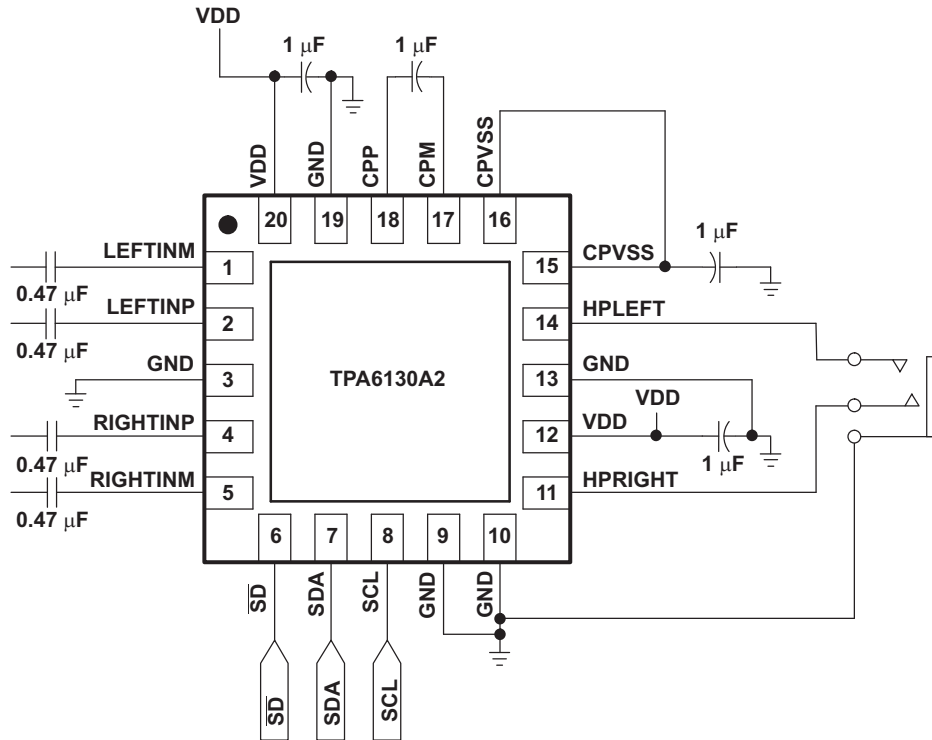


### Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The top drawing in Figure 36 illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive values of 16 Ω or 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance ($R_L$), the capacitor ($C_O$), and the cutoff frequency ($f_C$).

$$f_c = \frac{1}{2\pi R_L C_O}$$

(1)

$C_O$ can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c}$$

(2)

If $f_c$ is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The Capless amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is

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connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in Figure 36.

**Conventional**

**Capless**
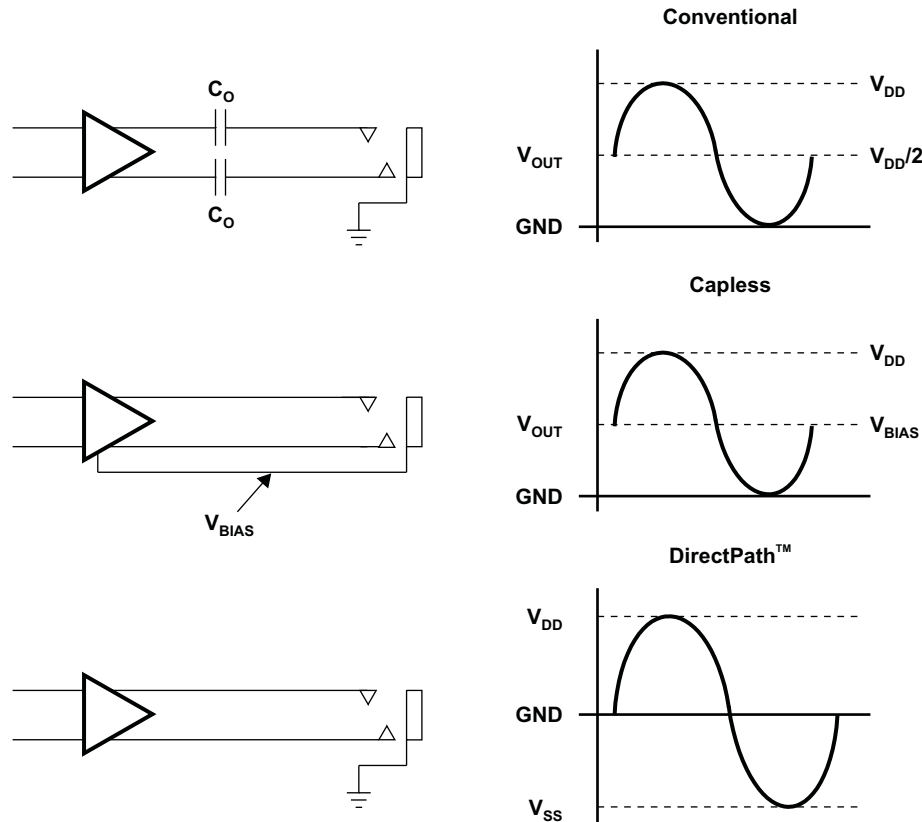
**DirectPath™**

**Figure 36. Amplifier Applications**

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors, and does not place any voltage on the sleeve. The bottom block diagram and waveform of Figure 36 illustrate the ground-referenced headphone architecture. This is the architecture of the TPA6130A2.

### Input-Blocking Capacitors

DC input-blocking capacitors block the dc portion of the audio source, and allow the inputs to properly bias. Maximum performance is achieved when the inputs of the TPA6130A2 are properly biased. Performance issues such as pop are optimized with proper input capacitors.

The dc input-blocking capacitors may be removed provided the inputs are connected differentially and within the input common mode range of the amplifier, the audio signal does not exceed ±3 V, and pop performance is sufficient.

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$C_{IN}$ is a theoretical capacitor used for mathematical calculations only. Its value is the series combination of the dc input-blocking capacitors, $C_{(DCINPUT-BLOCKING)}$. Use Equation 3 to determine the value of $C_{(DCINPUT-BLOCKING)}$. For example, if $C_{IN}$ is equal to 0.22 µF, then $C_{(DCINPUT-BLOCKING)}$ is equal to about 0.47 µF.

$$C_{IN} = \frac{1}{2}\ C_{(DCINPUT-BLOCKING)}$$

(3)

The two $C_{(DCINPUT-BLOCKING)}$ capacitors form a high-pass filter with the input impedance of the TPA6130A2. Use Equation 3 to calculate $C_{IN}$, then calculate the cutoff frequency using $C_{IN}$ and the differential input impedance of the TPA6130A2, $R_{IN}$, using Equation 4. Note that the differential input impedance changes with gain. See Figure 33 for input impedance values. The frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi\ R_{IN}\ C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi\ fc_{IN}\ R_{IN}}$$

(4)

If a high pass filter with a -3 dB point of no more than 20 Hz is desired over all gain settings, the minimum impedance would be used in the above equation. Figure 33 shows this to be 37 kΩ. The capacitor value by the above equation would be 0.215 µF. However, this is $C_{IN}$, and the desired value is for $C_{(DCINPUT-BLOCKING)}$. Multiplying $C_{IN}$ by 2 yields 0.43 µF, which is close to the standard capacitor value of 0.47 µF. Place 0.47 µF capacitors at each input terminal of the TPA6130A2 to complete the filter.

## Charge Pump Flying Capacitor and CPVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The $CP_{VSS}$ capacitor must be at least equal to the flying capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 µF is typical.

## Decoupling Capacitors

The TPA6130A2 is a DirectPath™ headphone amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. Use good low equivalent-series-resistance (ESR) ceramic capacitors, typically 1.0 µF. Find the smallest package possible, and place as close as possible to the device $V_{DD}$ lead. Placing the decoupling capacitors close to the TPA6130A2 is important for the performance of the amplifier. Use a 10 µF or greater capacitor near the TPA6130A2 to filter lower frequency noise signals. The high PSRR of the TPA6130A2 will make the 10 µF capacitor unnecessary in most applications.

## Layout Recommendations

### Exposed Pad On TPA6130A2RTJ Package Option

Solder the exposed metal pad on the TPA6130A2RTJ QFN package to the a pad on the PCB. *The pad on the PCB may be grounded or may be allowed to float (not be connected to ground or power).* If the pad is grounded, it must be connected to the same ground as the GND pins (3, 9, 10, 13, and 19). See the layout and mechanical drawings at the end of the datasheet for proper sizing. Soldering the thermal pad improves mechanical reliability, improves grounding of the device, and enhances thermal conductivity of the package.

### GND Connections

The GND pin for charge pump should be decoupled to the charge pump $V_{DD}$ pin, and the GND pin adjacent to the Analog $V_{DD}$ pin should be separately decoupled to each other.

## I²C CONTROL INTERFACE DETAILS

### Addressing the TPA6130A2

The device operates only as a slave device whose address is 1100000 binary.

## GENERAL I²C OPERATION

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 37. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TPA6130A2 holds SDA low during acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. When the bus level is 5 V, pull-up resistors between 1 kΩ and 2 kΩ in value must be used.
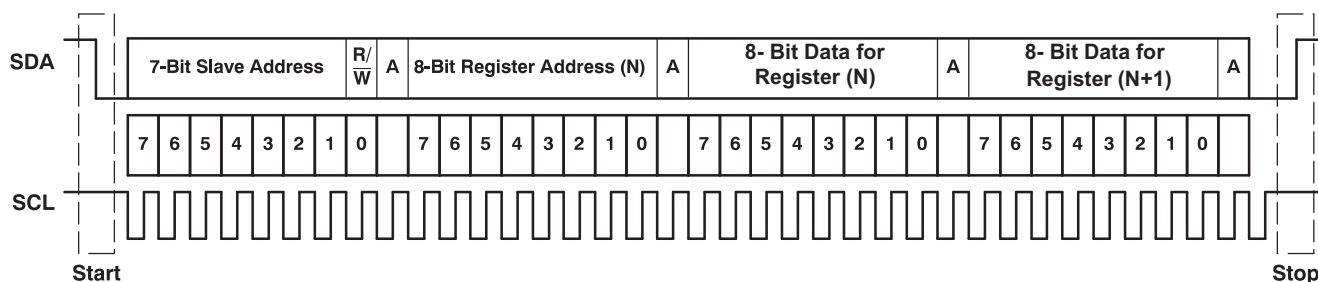


**Figure 37. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 37.

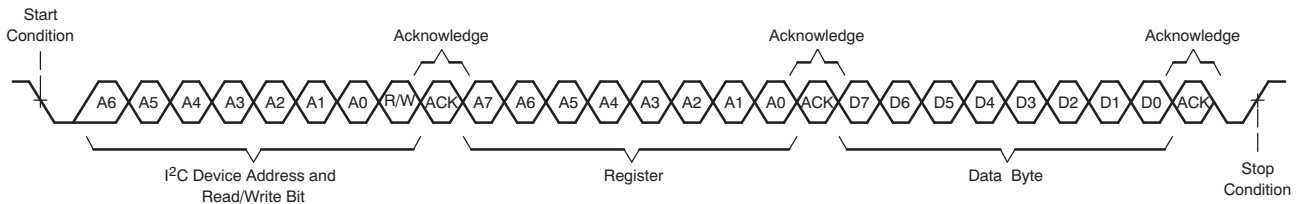## SINGLE-AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA6130A2 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TPA6130A2 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.
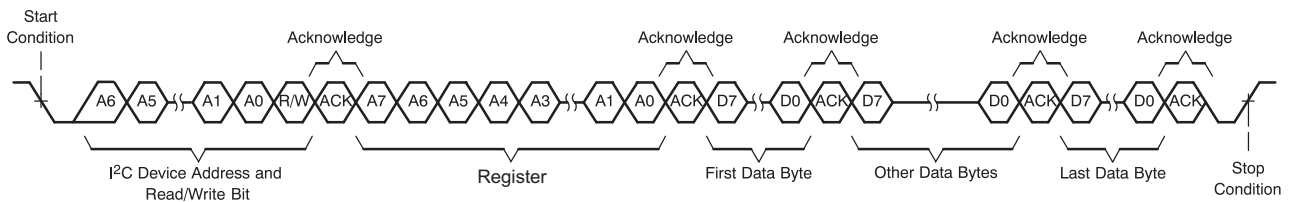
## SINGLE-BYTE WRITE

As shown in Figure 38, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA6130A2 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA6130A2 internal memory address being accessed. After receiving the register byte, the TPA6130A2 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TPA6130A2 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

**Figure 38. Single-Byte Write Transfer**

## MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA6130A2 as shown in Figure 39. After receiving each data byte, the TPA6130A2 responds with an acknowledge bit.
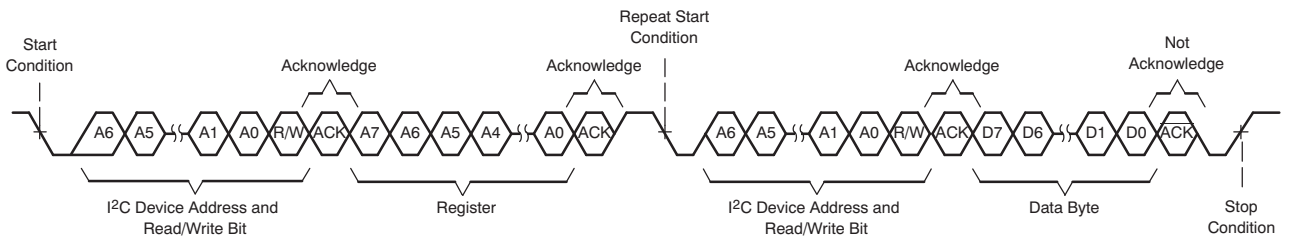


**Figure 39. Multiple-Byte Write Transfer**

## SINGLE-BYTE READ

As shown in Figure 40, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA6130A2 address and the read/write bit, the TPA6130A2 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA6130A2 issues an acknowledge bit. The master device transmits another start condition followed by the TPA6130A2 address and the read/write bit again. This time the read/write bit is set to 1, indicating a read transfer. Next, the TPA6130A2 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.
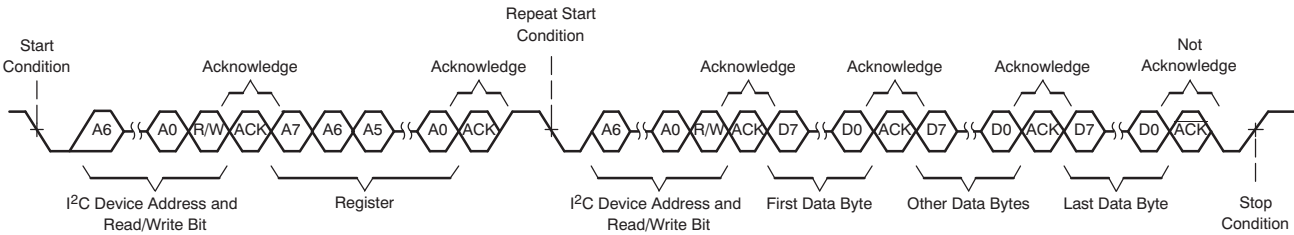


**Figure 40. Single-Byte Read Transfer**

## MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA6130A2 to the master device as shown in Figure 41. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

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**Figure 41. Multiple-Byte Read Transfer**

## Register Map

**Table 1. Register Map**

| Register | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| 1 | HP_EN_L | HP_EN_R | Mode[1] | Mode[0] | Reserved | Reserved | Thermal | SWS |
| 2 | Mute_L | Mute_R | Volume[5] | Volume[4] | Volume[3] | Volume[2] | Volume[1] | Volume[0] |
| 3 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HiZ_L | HiZ_R |
| 4 | Reserved | Reserved | RFT | RFT | Version[3] | Version[2] | Version[1] | Version[0] |
| 5 | RFT | RFT | RFT | RFT | RFT | RFT | RFT | RFT |
| 6 | RFT | RFT | RFT | RFT | RFT | RFT | RFT | RFT |
| 7 | RFT | RFT | RFT | RFT | RFT | RFT | RFT | RFT |
| 8 | RFT | RFT | RFT | RFT | RFT | RFT | RFT | RFT |

Bits labeled "Reserved" are reserved for future enhancements. They may not be written to. When read, they will show a "0" value.

Bits labeled "RFT" are reserved for TI testing. Under no circumstances must any data be written to these registers. Writing to these bits may change the function of the device, or cause complete failure. If read, these bits may assume any value.

### Control Register (Address: 1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | HP_EN_L | HP_EN_R | Mode[1] | Mode[0] | Reserved | Reserved | Thermal | SWS |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| HP_EN_L | Enable bit for the left-channel amplifier. Amplifier is active when bit is high. |
| HP_EN_R | Enable bit for the right-channel amplifier. Amplifier is active when bit is high. |
| Mode[1:0] | Mode bits Mode[1] and Mode[0] select one of three modes of operation. 00 is stereo headphone mode. 01 is dual mono headphone mode. 10 is bridge-tied load mode. |
| Reserved | These bits are reserved for future enhancements. They may not be written to. When read they will read as zero. |
| Thermal | A 1 on this bit indicates a thermal shutdown was initiated by the hardware. When the temperature drops to safe levels, the device will start to operate again, regardless of bit status. This bit is clear-on-read. |
| SWS | Software shutdown control. When the bit is one, the device is in software shutdown. When the bit is low, the charge-pump is active. SWS must be low for normal operation. |

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## Volume and Mute Register (Address: 2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | Mute_L | Mute_R | Volume[5] | Volume[4] | Volume[3] | Volume[2] | Volume[1] | Volume[0] |
| Reset Value | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Mute_L      Left channel mute. If this bit is High the left channel is muted.

Mute_R      Right channel mute. If this bit is High the right channel is muted.

Volume[5:0]      Six bits for volume control. 111111 indicates the highest gain and 000000 indicates the lowest gain.

## Output Impedance Register (Address: 3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | HiZ_L | HiZ_R |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reserved      These bits are reserved for future enhancements. They may not be written to. When read they will read as zero. All writes to these bits will be ignored.

HiZ_L      Puts left-channel amplifier output in tri-state high impedance mode.

HiZ_R      Puts right-channel amplifier output in tri-state high impedance mode.

## I$^2$C address and Version Register (Address: 4)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | Reserved | Reserved | RFT | RFT | Version[3] | Version[2] | Version[1] | Version[0] |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reserved      These bits are reserved for future enhancements. They may not be written to. When read they will read as zero.

Version[3:0]      The version bits track the revision of the silicon. Valid values are 0010 for released TPA6130A2.

RFT      Reserved for Test. Do NOT write to these registers.

## Reserved for test registers (Addresses: 5-8)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | RFT | RFT | RFT | RFT | RFT | RFT | RFT | RFT |
| Reset Value | x | x | x | x | x | x | x | x |

RFT      Reserved for Test. Do NOT write to these registers.

**Modes of Operation**

The TPA6130A2 supports numerous modes of operation.

**Hardware Shutdown**

Hardware shutdown occurs when the $\overline{SD}$ pin is set to logic 0. The device is completely shutdown in this mode, drawing minimal current. This mode overrides all other modes. All information programmed into the registers is lost. When the device starts up again, the registers go back to their default state.

**Software Shutdown**

Software shutdown is set by placing a logic 1 in register 1, bit 0. That is the SWS bit. The software shutdown places the device in a low power state, although the current draw is higher than that of hardware shutdown (see the Electrical Characteristics Table for values). Engaging software shutdown turns off the charge pump and disables the outputs. The device is awakened by placing a logic 0 in the SWS bit.

Note that when the device is in SWS mode, register 1, bits 7 and 6 will be cleared to reflect the disabled state of the amplifier. All other registers maintain their values. Re-enable the amplifer by placing a logic 0 in the SWS bit. It is necessary to reset the entire register because a full word must be used when writing just one bit.

**Charge Pump Enabled, HP Amplifiers Disabled**

The output amplifiers of the TPA6130A2 are enabled by placing a logic 1 in register 1, bits 6 and 7. Place a logic 0 in register 1, bits 6 and 7 to disable the output amplifiers. The left and right outputs can be enabled and disabled individually. When the output amplifiers are disabled, the charge-pump remains on.

**HiZ State**

HiZ is enabled by placing a logic 1 in register 3, bits 0 and 1. Place a logic 0 in register 3, bits 0 and 1 to disable the HiZ state of the outputs. The left and right outputs can be placed into a HiZ state individually.

The HiZ state puts the outputs into a state of high impedance. Use this configuration when the outputs of the TPA6130A2 share traces with other devices whose outputs may be active.

Note that to use the HiZ mode, the TPA6130A2 MUST be active (not in SWS or hardware shutdown). Furthermore, the output amplifiers must NOT be enabled.

**Stereo Headphone Drive**

The device is in this mode when the MODE bits in register 1 are 00 and both headphone enable bits are enabled. The two amplifier channels operate independently. This mode is appropriate for stereo playback.

**Dual Mono Headphone Drive**

The device is in this mode when the MODE bits in register 1 are 01 and both headphone enable bits are enabled. The left channel is the active input. It is amplified and distributed to both the left and right headphone outputs.

**Bridge-Tied Load Receiver Drive**

The device is in this mode when the MODE bits in register 1 are 10 and both headphone enable bits are enabled. In this mode, the device will take the left channel input and drive a single load connected between HPLEFT and HPRIGHT in a bridge-tied fashion. The minimum load for bridge-tied mode is the same as for stereo mode (see table entitled "Absolute Maximum Ratings").

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## Default Mode

The TPA6130A2 starts up with the following conditions:

- SWS = Off, CHARGE PUMP = On
- HP ENABLES = Off
- HiZ = Off
- MODE = Stereo
- HP MUTES = On, VOLUME = -59.5 dB,

## VOLUME CONTROL

The TPA6130A2 volume control is set through the I²C interface. The six volume control register bits are decoded to 64 volume settings that employ an audio taper. See Table 2 for the gain table. The values listed in this table are typical. Each gain step has a different input impedance. See Figure 33.

### Table 2. Audio Taper Gain Values

| Gain Control Word (Binary) Mute [7:6], V[5:0] | Nominal Gain (dB) | Nominal Gain (V/V) | Gain Control Word (Binary) Mute [7:6], V[5:0] | Nominal Gain (dB) | Nominal Gain (V/V) |
|---|---|---|---|---|---|
| 11XXXXXX | −100 | 0.00001 | 00100000 | −10.9 | 0.283 |
| 00000000 | −59.5 | 0.001 | 00100001 | −10.3 | 0.305 |
| 00000001 | −53.5 | 0.002 | 00100010 | −9.7 | 0.329 |
| 00000010 | −50.0 | 0.003 | 00100011 | −9.0 | 0.353 |
| 00000011 | −47.5 | 0.004 | 00100100 | −8.5 | 0.379 |
| 00000100 | −45.5 | 0.005 | 00100101 | −7.8 | 0.405 |
| 00000101 | −43.9 | 0.007 | 00100110 | −7.2 | 0.433 |
| 00000110 | −41.4 | 0.009 | 00100111 | −6.7 | 0.462 |
| 00000111 | −39.5 | 0.012 | 00101000 | −6.1 | 0.493 |
| 00001000 | −36.5 | 0.015 | 00101001 | −5.6 | 0.524 |
| 00001001 | −35.3 | 0.018 | 00101010 | −5.1 | 0.557 |
| 00001010 | −33.3 | 0.022 | 00101011 | −4.5 | 0.591 |
| 00001011 | −31.7 | 0.026 | 00101100 | −4.1 | 0.627 |
| 00001100 | −30.4 | 0.031 | 00101101 | −3.5 | 0.664 |
| 00001101 | −28.6 | 0.037 | 00101110 | −3.1 | 0.702 |
| 00001110 | −27.1 | 0.043 | 00101111 | −2.6 | 0.742 |
| 00001111 | −26.3 | 0.050 | 00110000 | −2.1 | 0.783 |
| 00010000 | −24.7 | 0.057 | 00110001 | −1.7 | 0.825 |
| 00010001 | −23.7 | 0.065 | 00110010 | −1.2 | 0.870 |
| 00010010 | −22.5 | 0.074 | 00110011 | −0.8 | 0.915 |
| 00010011 | −21.7 | 0.084 | 00110100 | −0.3 | 0.962 |
| 00010100 | −20.5 | 0.093 | 00110101 | 0.1 | 1.010 |
| 00010101 | −19.6 | 0.104 | 00110110 | 0.5 | 1.061 |
| 00010110 | −18.8 | 0.116 | 00110111 | 0.9 | 1.112 |
| 00010111 | −17.8 | 0.129 | 00111000 | 1.4 | 1.165 |
| 00011000 | −17.0 | 0.142 | 00111001 | 1.7 | 1.220 |
| 00011001 | −16.2 | 0.156 | 00111010 | 2.1 | 1.277 |
| 00011010 | −15.2 | 0.172 | 00111011 | 2.5 | 1.335 |
| 00011011 | −14.5 | 0.188 | 00111100 | 2.9 | 1.395 |
| 00011100 | −13.7 | 0.205 | 00111101 | 3.3 | 1.456 |
| 00011101 | −13.0 | 0.223 | 00111110 | 3.6 | 1.520 |
| 00011110 | −12.3 | 0.242 | 00111111 | 4.0 | 1.585 |
| 00011111 | −11.6 | 0.262 | | | |

Product Folder Link(s): TPA6130A2

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA6130A2RTJR | ACTIVE | QFN | RTJ | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSG | Samples |
| TPA6130A2RTJRG4 | ACTIVE | QFN | RTJ | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSG | Samples |
| TPA6130A2RTJT | ACTIVE | QFN | RTJ | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSG | Samples |
| TPA6130A2RTJTG4 | ACTIVE | QFN | RTJ | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSG | Samples |
| TPA6130A2YZHR | ACTIVE | DSBGA | YZH | 16 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BRU | Samples |
| TPA6130A2YZHT | ACTIVE | DSBGA | YZH | 16 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BRU | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|---------------------|---------------------|---------|---------|---------|---------|--------|---------------|
| TPA6130A2RTJR | QFN | RTJ | 20 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPA6130A2RTJT | QFN | RTJ | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPA6130A2YZHR | DSBGA | YZH | 16 | 3000 | 180.0 | 8.4 | 2.07 | 2.07 | 0.81 | 4.0 | 8.0 | Q1 |
| TPA6130A2YZHT | DSBGA | YZH | 16 | 250 | 180.0 | 8.4 | 2.07 | 2.07 | 0.81 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA6130A2RTJR | QFN | RTJ | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPA6130A2RTJT | QFN | RTJ | 20 | 250 | 210.0 | 185.0 | 35.0 |
| TPA6130A2YZHR | DSBGA | YZH | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| TPA6130A2YZHT | DSBGA | YZH | 16 | 250 | 210.0 | 185.0 | 35.0 |

RTJ (S−PWQFN−N20)                    PLASTIC QUAD FLATPACK NO−LEAD
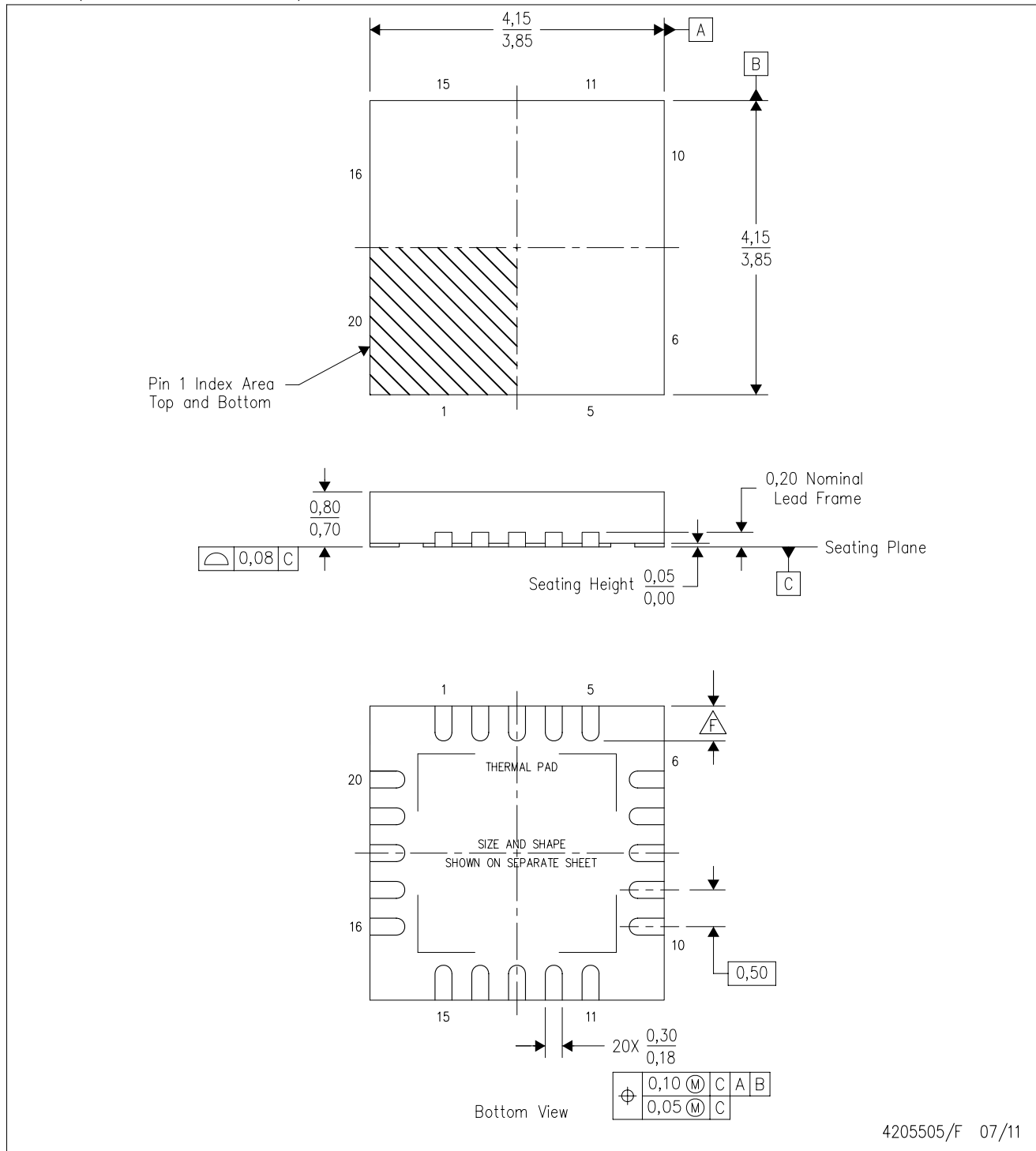


4205505/F  07/11

NOTES:  A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5−1994.
        B.  This drawing is subject to change without notice.
        C.  QFN (Quad Flatpack No−Lead) package configuration.
        D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E.  See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F.  Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

RTJ (S-PWQFN-N20)                    PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C = 0,30

$20X \dfrac{0,50}{0,30}$

2,70±0,10

2,70±0,10

Exposed Thermal Pad
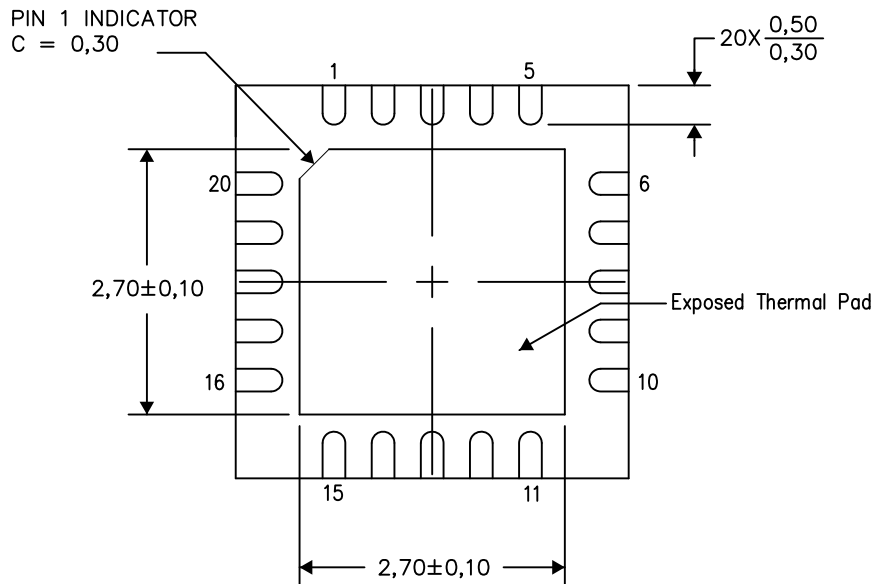
Bottom View

Exposed Thermal Pad Dimensions

4206256-2/R  11/12

NOTE:   All linear dimensions are in millimeters
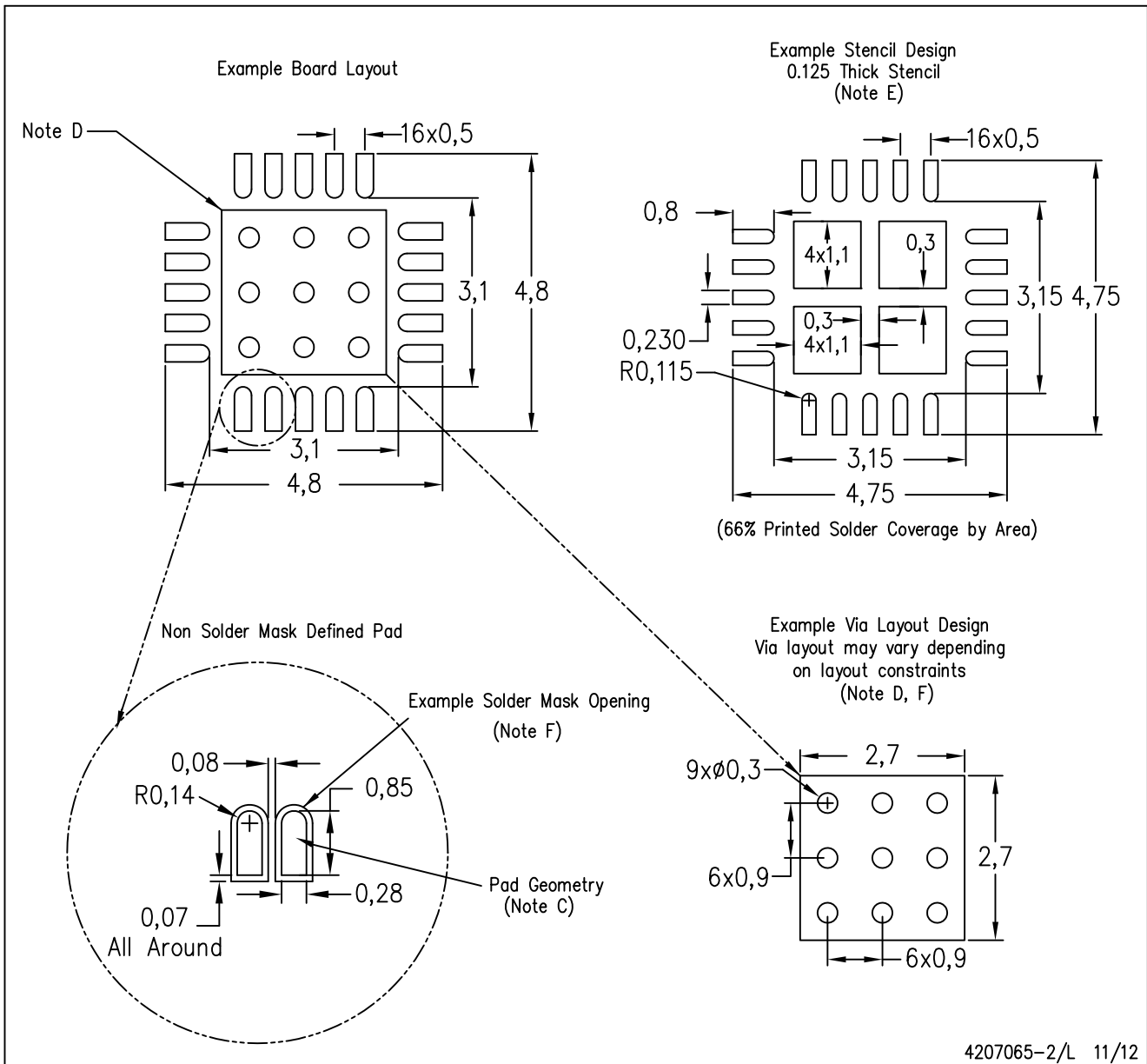
TEXAS
INSTRUMENTS
www.ti.com

RTJ (S−PWQFN−N20)          PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

16x0,5

3,1  4,8

3,1

4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

16x0,5

0,8

4x1,1    0,3

0,3
4x1,1

0,230

R0,115

3,15  4,75

3,15

4,75

(66% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

9x⌀0,3

6x0,9

2,7

2,7

6x0,9

4207065−2/L  11/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
             Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout.  These documents are available at
             www.ti.com <http://www.ti.com>.
         E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
         F.  Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
             recommendations for vias placed in the thermal pad.

YZH (S−XBGA−N16)  DIE−SIZE BALL GRID ARRAY
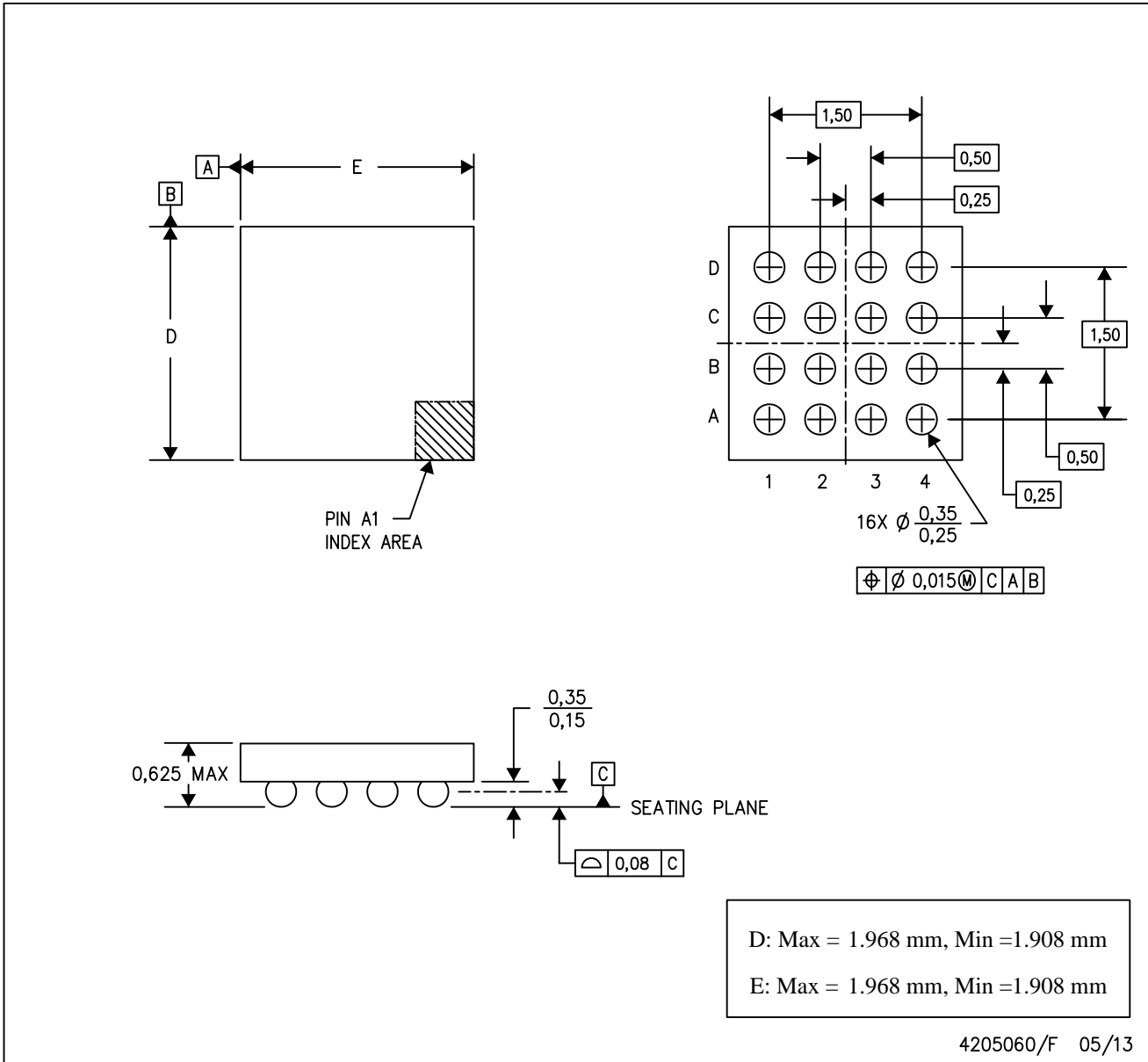


PIN A1
INDEX AREA

1,50

0,50

0,25

D
C
B
A

1  2  3  4

16X Ø 0,35 / 0,25

⊕ Ø 0,015 Ⓜ C A B

1,50

0,50

0,25

0,35 / 0,15

0,625 MAX

SEATING PLANE

⌴ 0,08 C

D: Max = 1.968 mm, Min =1.908 mm

E: Max = 1.968 mm, Min =1.908 mm

4205060/F   05/13

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  NanoFree™ package configuration.

# IMPORTANT NOTICE

| Products | | Applications | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
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