RAIL-TO-RAIL OUTPUT, VERY LOW-NOISE OPERATIONAL AMPLIFIERS

Check for Samples: TL971-Q1, TL972-Q1, TL974-Q1

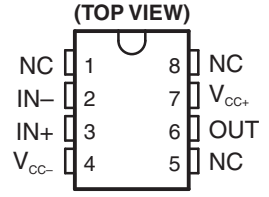
FEATURES

- **Qualified for Automotive Applications**
- **Rail-to-Rail Output Voltage Swing: ±2.4 V at V_{CC} = ±2.5 V**
- **Very Low Noise Level: 4 nV/√Hz**
- **Ultra-Low Distortion: 0.003%**
- **High Dynamic Features: 12 MHz, 5 V/µs**
- **Operating Range: 2.7 V to 12 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **200-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**

APPLICATIONS

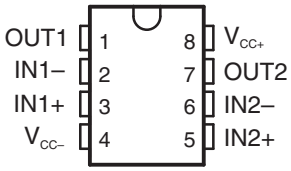
- **Portable Equipment (CD Players, PDAs)**
- **Portable Communications (Cell Phones, Pagers)**
- **Instrumentation and Sensors**
- **Professional Audio Circuits**

TL971...D PACKAGE
(TOP VIEW)

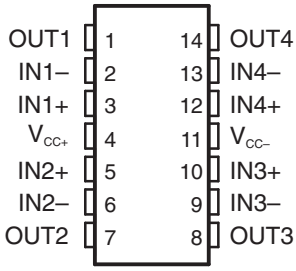


NC – No internal connection

TL972...D OR PW PACKAGE
(TOP VIEW)



TL974...PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TL97x family of operational amplifiers operates at voltages as low as ±1.35 V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

ORDERING INFORMATION(1)(2)

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TL971QDRQ1	TL971Q
	TL972QDRQ1	TL972Q
	TL972QPWRQ1	TL972Q
	TL974QPWRQ1	TL974Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range(2)			2.7 V to 15 V
V_{ID}	Differential input voltage(3)			±1 V
V_{IN}	Input voltage range(4)			V_{CC-} – 0.3 V to V_{CC+} + 0.3 V
θ_{JA}	Package thermal impedance, junction to free air	D package(5)	8 pin	97°C/W
		PW package(5)	8 pin	149°C/W
			14 pin	113°C/W
T_J	Maximum junction temperature			150°C
T_{lead}	Maximum lead temperature	Soldering, 10 seconds		260°C
T_{stg}	Storage temperature range			–65°C to 150°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000 V
		Machine Model (MM)		200 V
		Charged-Device Model (CDM)		1500 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
(4) The input and output voltages must never exceed V_{CC} + 0.3 V.
(5) Package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	12	V
V_{ICM}	Common-mode input voltage	V_{CC-} + 1.15	V_{CC+} – 1.15	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

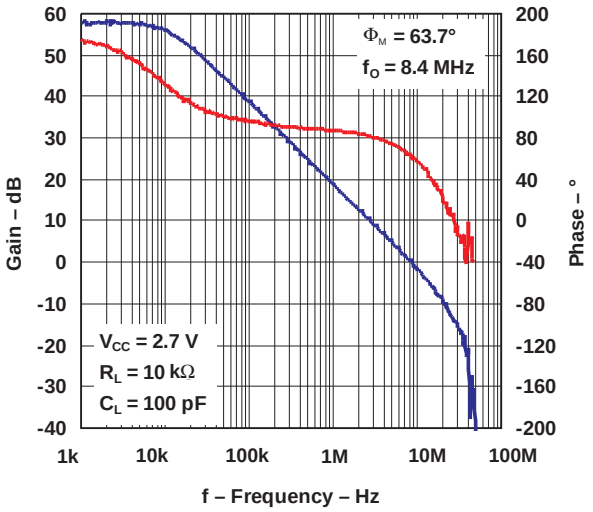
V_{CC+} = 2.5 V, $V_{CC–}$ = –2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1	4	mV
			Full range			6	
αV_{IO}	Input offset voltage drift	V_{ICM} = 0 V, V_O = 0 V	25°C		5		µV/°C
I_{IO}	Input offset current	V_{ICM} = 0 V, V_O = 0 V	25°C		10	150	nA
I_{IB}	Input bias current	V_{ICM} = 0 V, V_O = 0 V	25°C		200	750	nA
			Full range			1000	
V_{ICM}	Common-mode input voltage		25°C	–1.35		1.35	V
CMRR	Common-mode rejection ratio	V_{ICM} = ±1.35 V	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	V_{CC} = ±2 V to ±3 V	25°C	60	70		dB
A_{VD}	Large-signal voltage gain	R_L = 2 kΩ	25°C	70	80		dB
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	2	2.4		V
V_{OL}	Low-level output voltage	R_L = 2 kΩ	25°C		–2.4	–2	V
I_{source}	Output source current		25°C	1.2	1.4		mA
		V_{OUT} shorted to –2.5 V	Full range	1			
I_{sink}	Output sink current		25°C	50	80		mA
		V_{OUT} shorted to +2.5 V	Full range	25			
I_{CC}	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	8.5	12		MHz
SR	Slew rate	A_V = 1, V_{IN} = ±1 V	25°C	3.5	5		V/µs
			Full range	3			
Φm	Phase margin at unity gain	R_L = 2 kΩ, C_L =100 pF	25°C		60		°
Gm	Gain margin	R_L = 2 kΩ, C_L =100 pF	25°C		10		dB
V_n	Equivalent input noise voltage	f = 100 kHz	25°C		4		nV/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –1, R_L = 10 kΩ	25°C		0.003		%

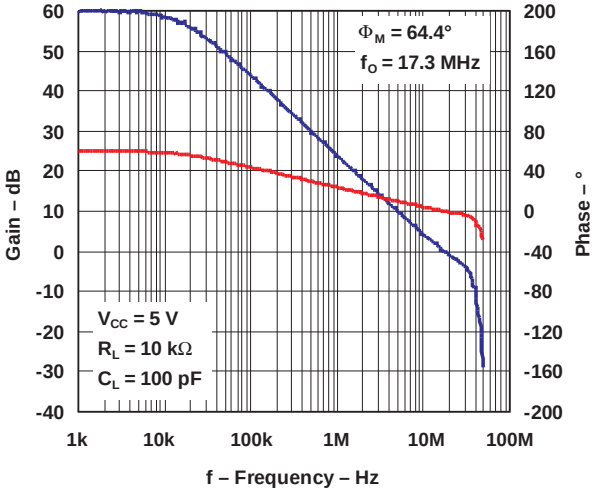
(1) Full range T_A = –40°C to 125°C

TYPICAL CHARACTERISTICS

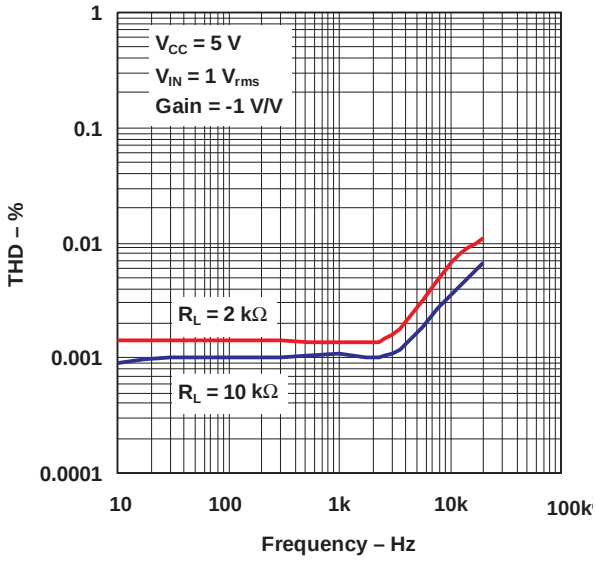
GAIN AND PHASE vs FREQUENCY



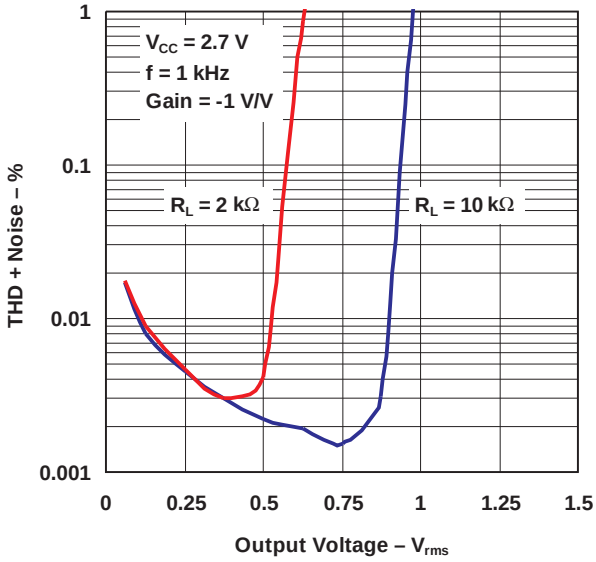
GAIN AND PHASE vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

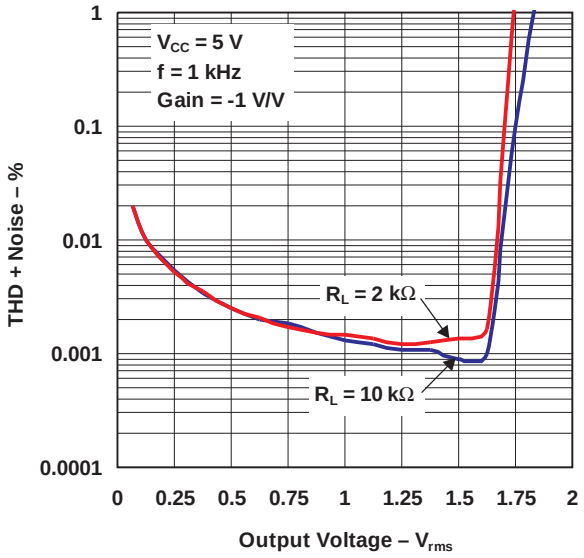


TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

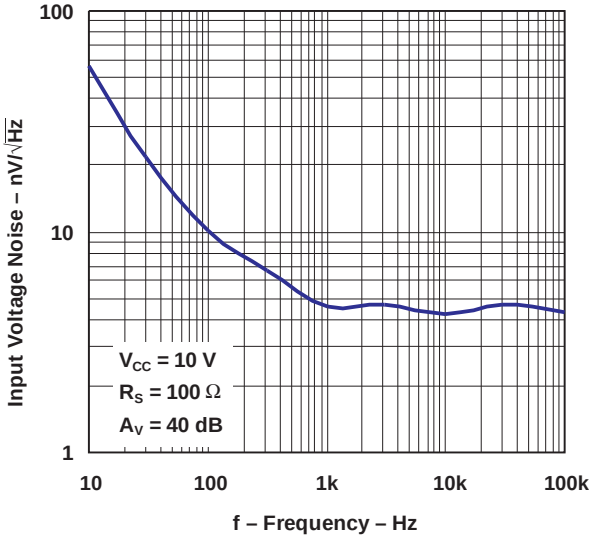


TYPICAL CHARACTERISTICS (continued)

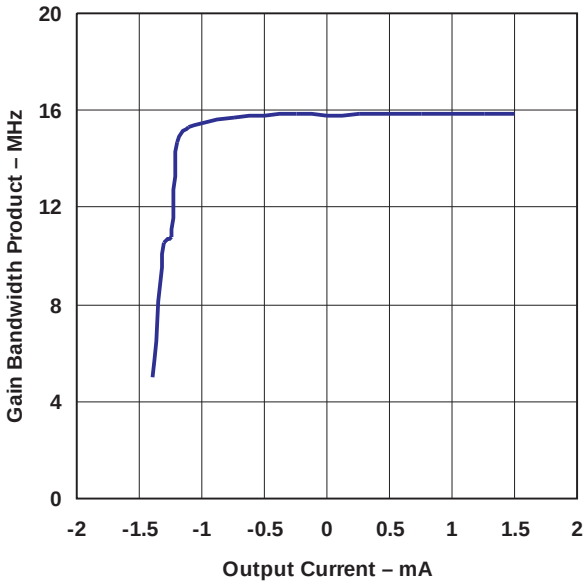
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



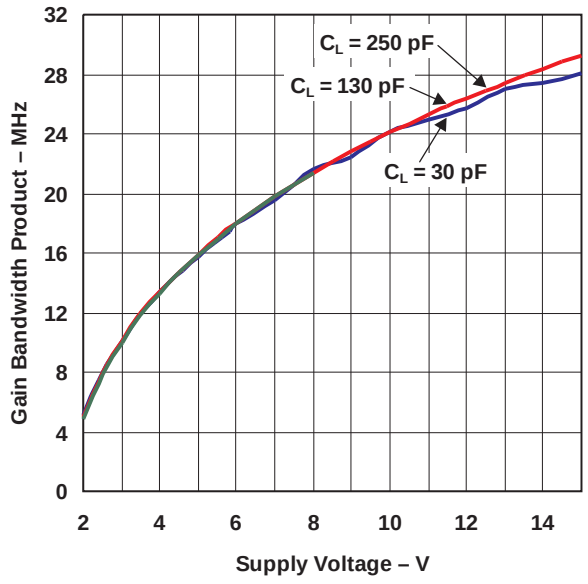
INPUT VOLTAGE NOISE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs OUTPUT CURRENT

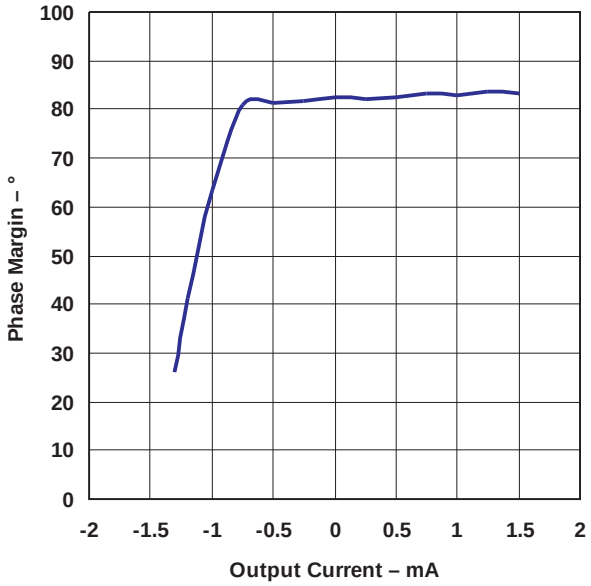


GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

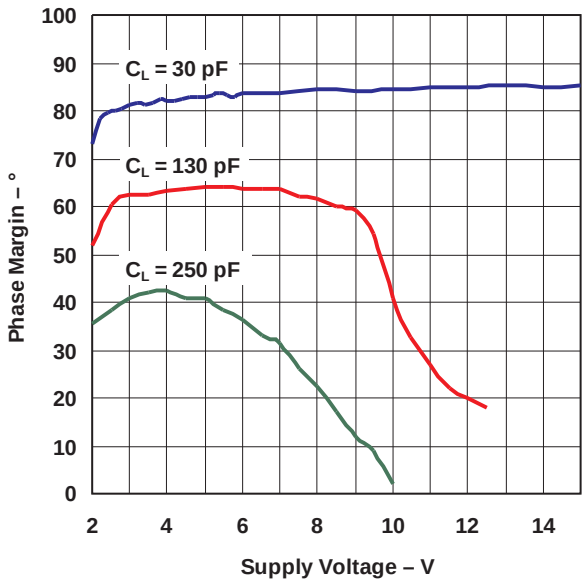


TYPICAL CHARACTERISTICS (continued)

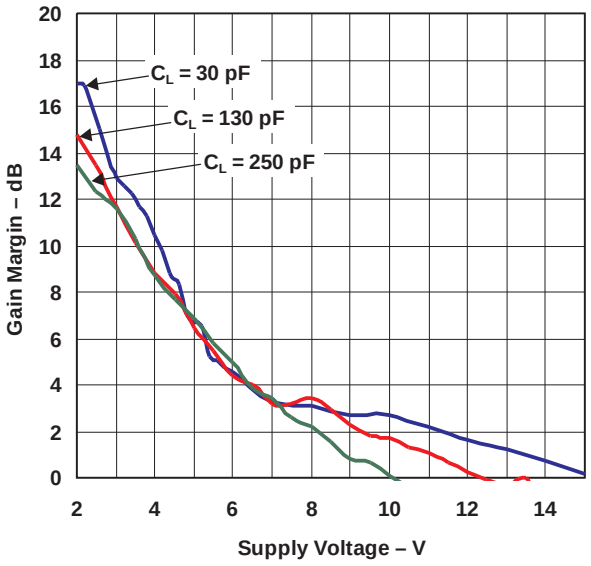
PHASE MARGIN vs OUTPUT CURRENT



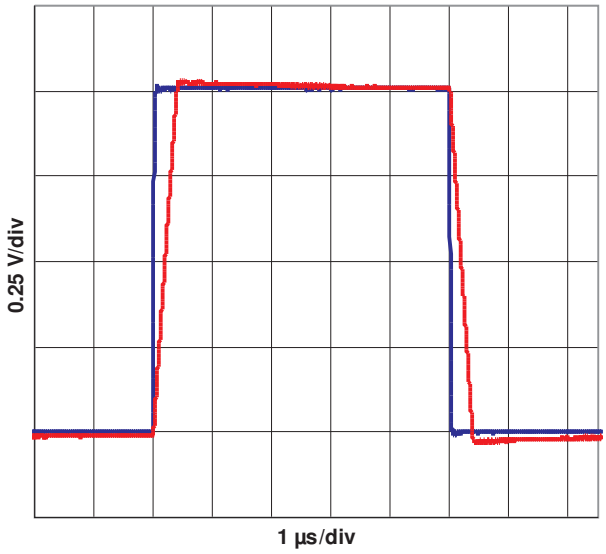
PHASE MARGIN vs SUPPLY VOLTAGE



GAIN MARGIN vs SUPPLY VOLTAGE

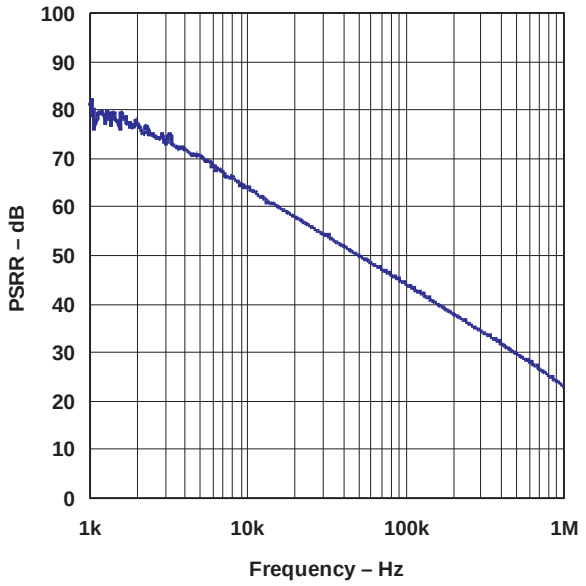


INPUT RESPONSE

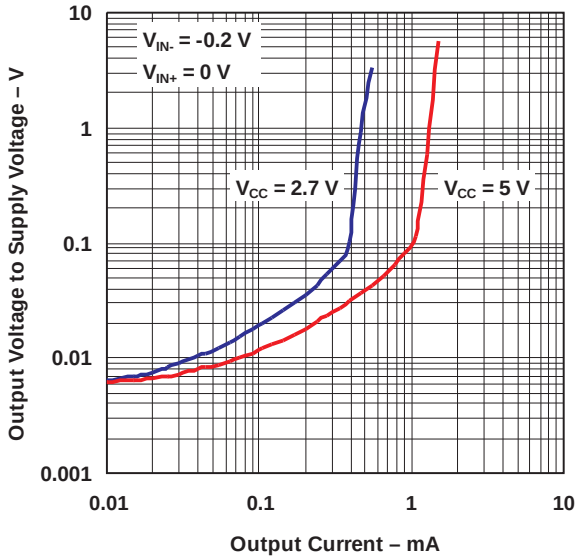


TYPICAL CHARACTERISTICS (continued)

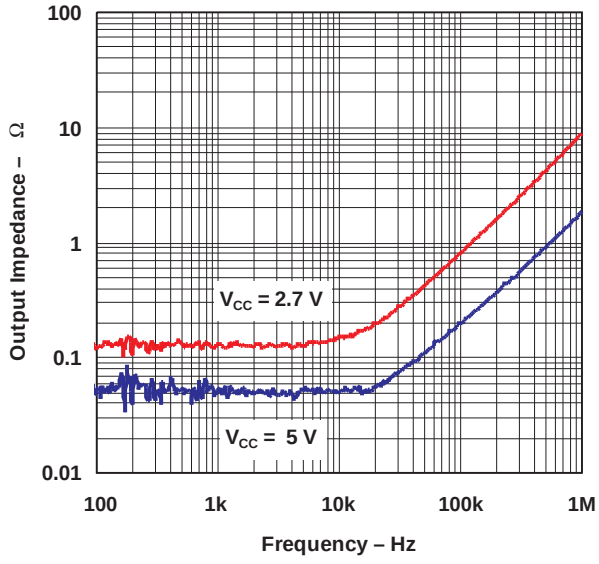
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY



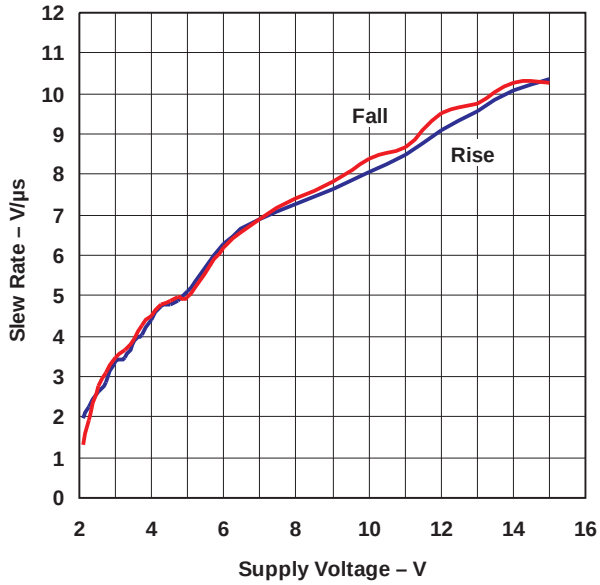
OUTPUT VOLTAGE vs OUTPUT CURRENT



OUTPUT IMPEDANCE vs FREQUENCY



SLEW RATE vs SUPPLY VOLTAGE



REVISION HISTORY

Changes from Original (March 2009) to Revision A **Page**

- Removed packaging column from the ordering information table. 1
- Changed V_{OUT} = ±2.5 V to V_{OUT} shorted to -2.5 V for I_{source}, and changed V_{OUT} = ±2.5 V to V_{OUT} shorted to +2.5 V for I_{sink}. 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL971QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL971Q	Samples
TL972QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL972Q	Samples
TL972QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL972Q	Samples
TL974QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF TL971-Q1, TL972-Q1, TL974-Q1 :

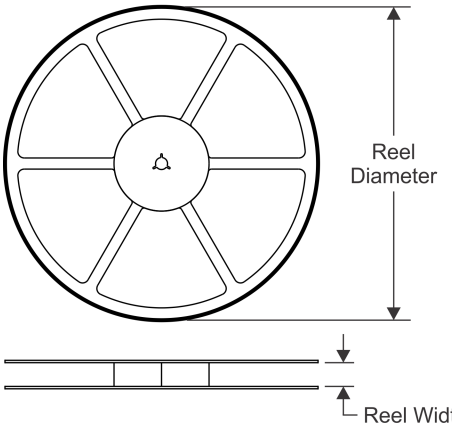
- Catalog: TL971, TL972, TL974

NOTE: Qualified Version Definitions:

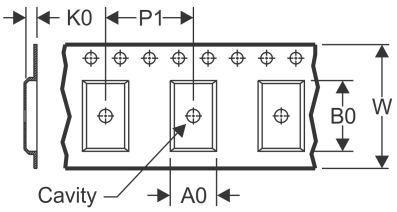
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

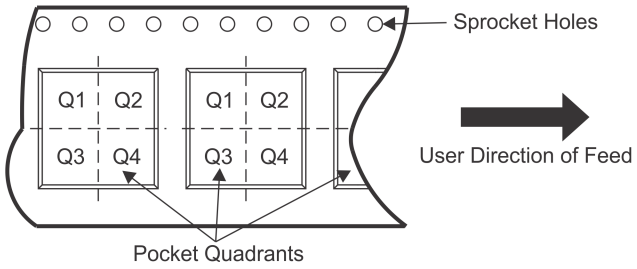


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

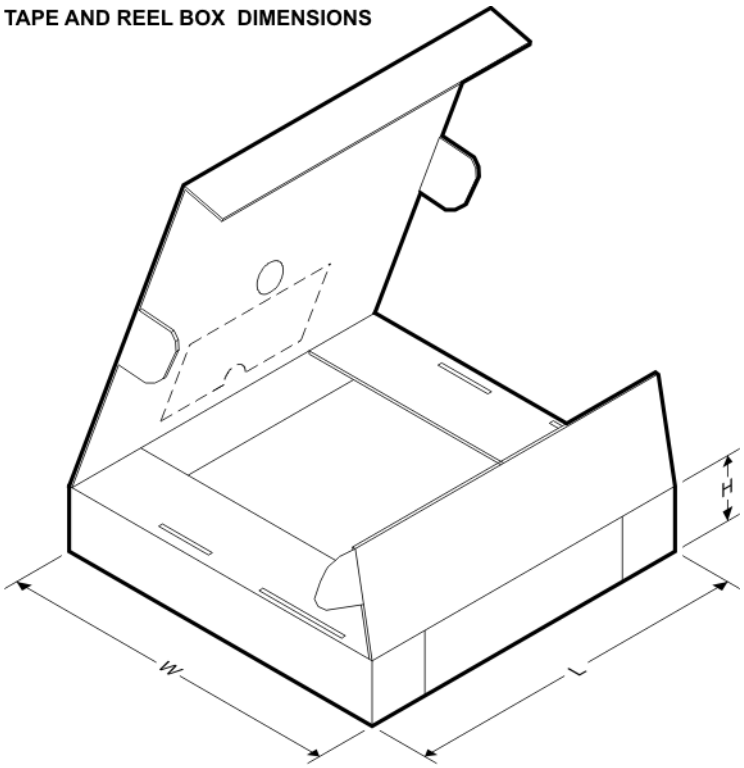
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL972QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL974QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

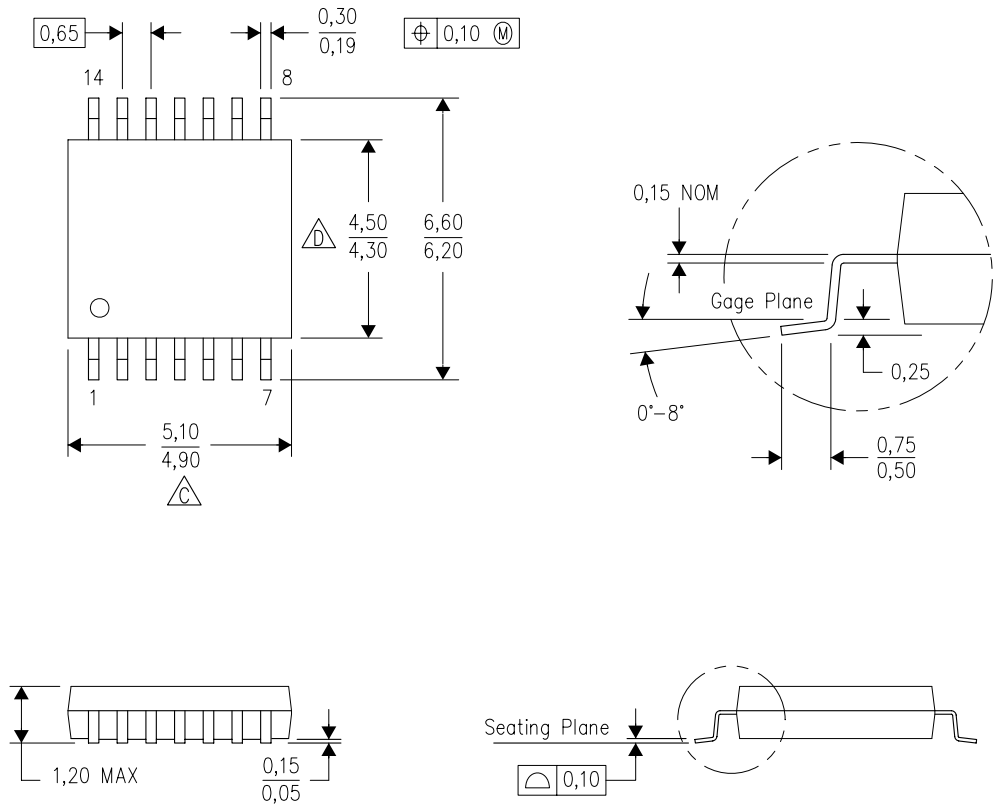
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL972QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
TL974QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

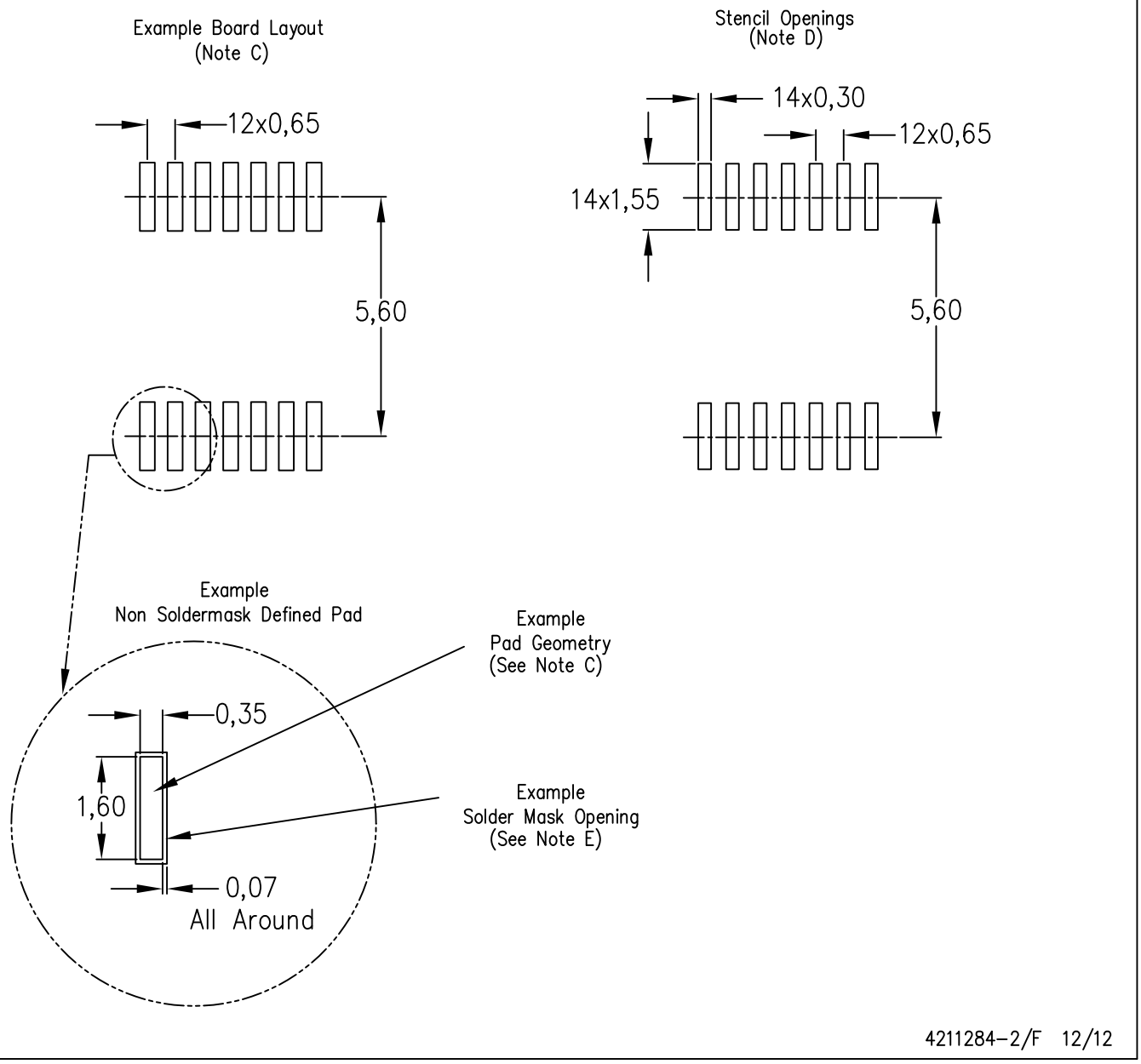
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

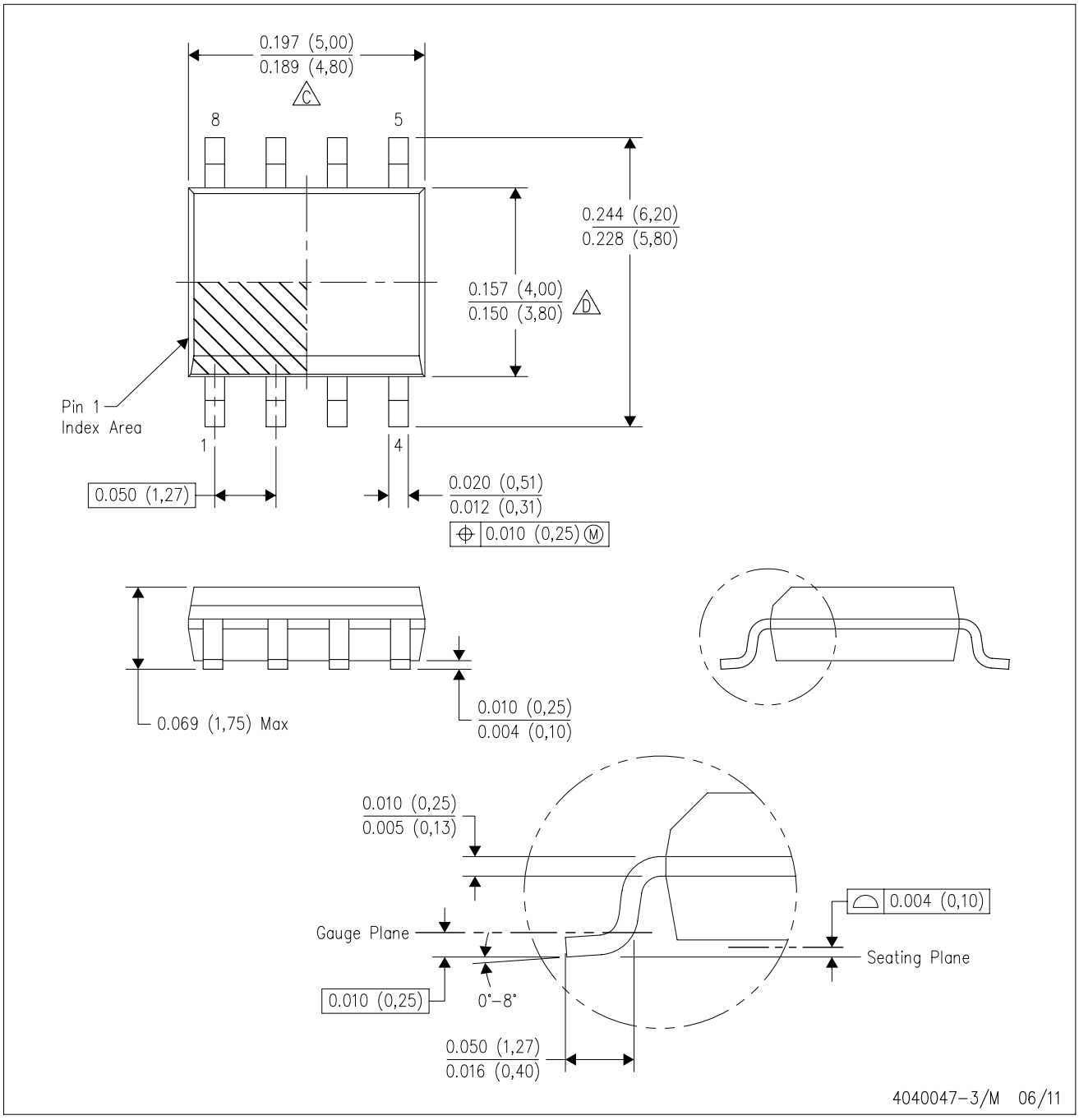
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



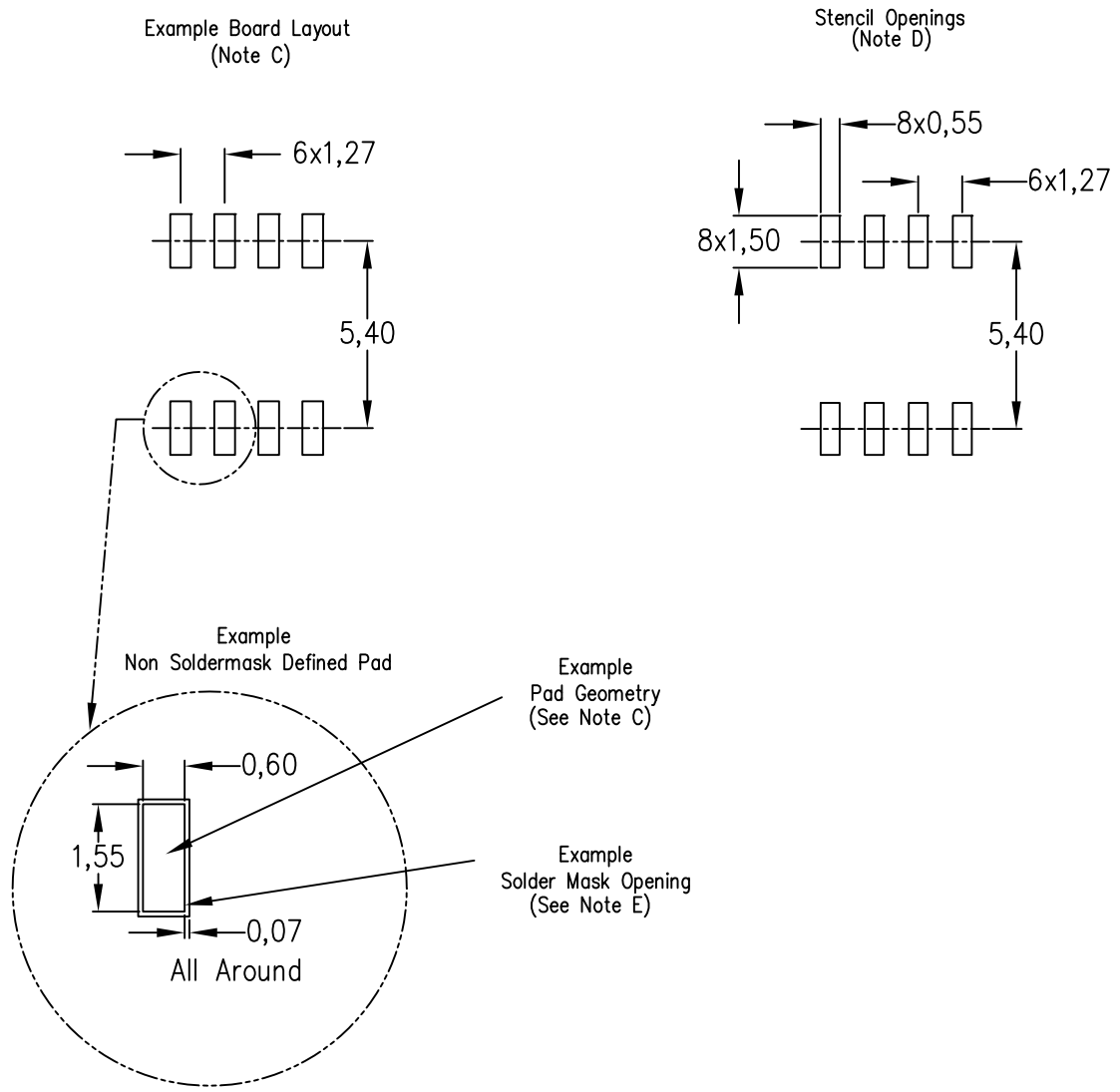
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



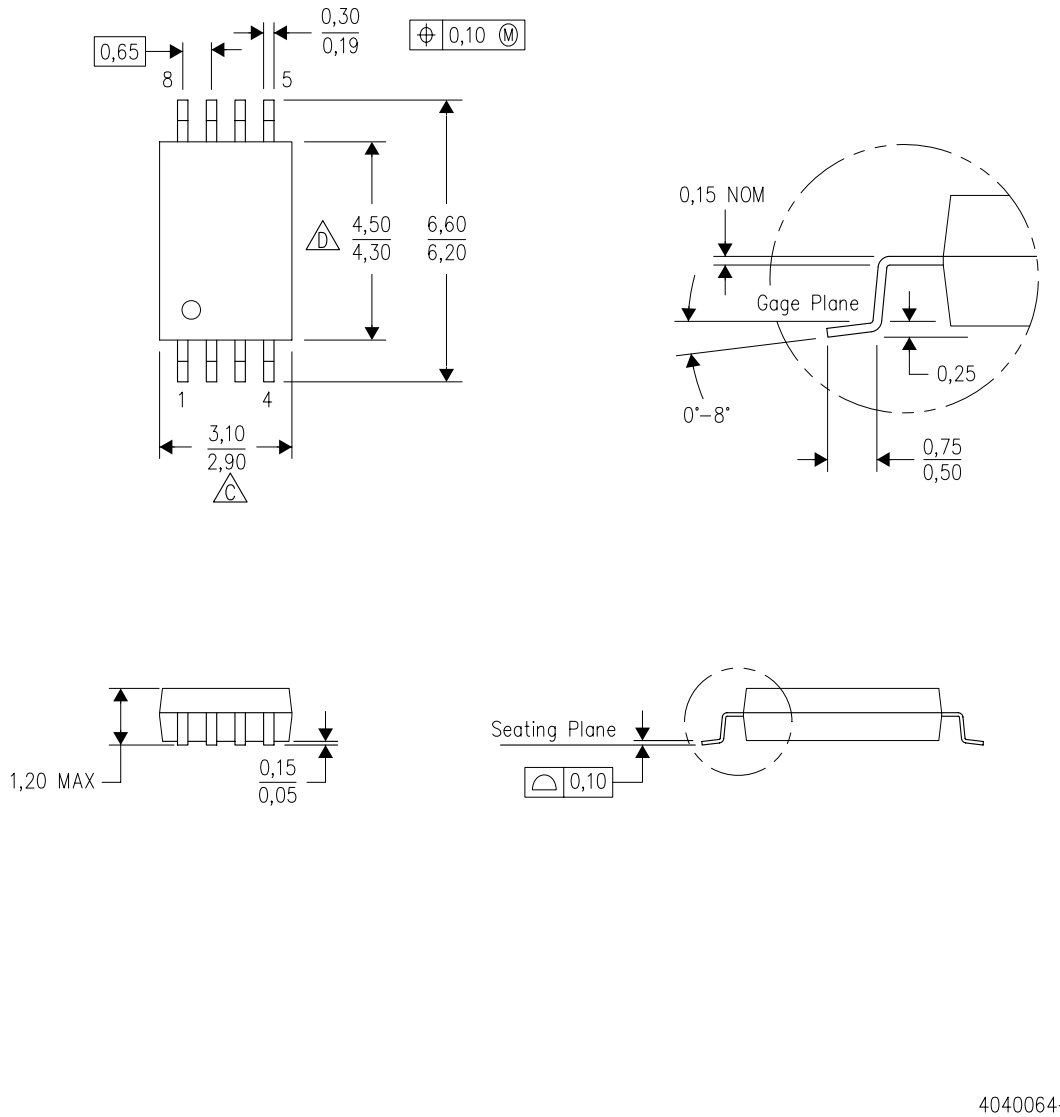
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE

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