Ultra Low-Power, Rail-to-Rail Out, Negative Rail In, VFB Op Amp

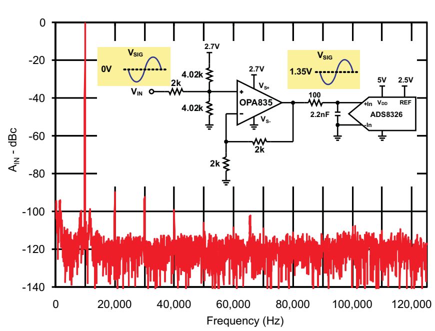
Check for Samples: OPA835, OPA2835

FEATURES

- **Ultra Low Power**
  - **Supply Voltage: 2.5 V to 5.5 V**
  - **Quiescent Current: 250 μA (typ)**
  - **Power Down Mode: 0.5 μA (typ)**
- **Bandwidth: 56 MHz**
- **Slew Rate: 160 V/μs**
- **Rise Time: 10 ns (2 V_{STEP})**
- **Settling Time: 45 ns (2V_{STEP})**
- **Overdrive Recovery Time: 195ns**
- **SNR: 0.00015% (–116.4dBc) at 1 kHz (1V $_{RMS}$)**
- **THD: 0.00003% (–130 dBc) at 1 kHz (1 V_{RMS})**
- **HD_2/HD_3: –70 dBc/–73 dBc at 1 MHz (2 Vpp)**
- **Input Voltage Noise: 9.3 nV/rtHz (f = 100 kHz)**
- **Input Offset Voltage: 100 μV (500 μV max)**
- **CMRR: 113 dB**
- **Output Current Drive: 40 mA**
- **RRO – Rail-to-Rail Output**
- **Input Voltage Range: –0.2 V to 3.9 V (5 V supply)**
- **Operating Temperature Range: –40°C–125°C**

APPLICATIONS

- **Low Power Signal Conditioning**
- **Audio ADC Input Buffer**
- **Low Power SAR and ΔΣ ADC Driver**
- **Portable Systems**
- **Low Power Systems**
- **High Density Systems**
- **Ultrasonic Flow Meter**



DESCRIPTION

Fabricated using the industry-leading BiCom-3x (SiGe complimentary bipolar) process, the OPA835 and OPA2835 are single and dual ultra low-power, rail-to-rail output, negative rail input, voltage-feedback operational amplifiers designed to operate over a power supply range of 2.5 V to 5.5 V Single Supply and ±1.25 V to ±2.75 V dual supply. Consuming only 250 μA per channel and a unity gain bandwidth of 56MHz, these amplifiers set an industry leading power-to-performance ratio for rail-to-rail amplifiers.

For battery powered portable applications where power is of key importance, the OPA835's and OPA2835's low power consumption and high frequency performance offers designers performance versus power not attainable in other devices. Coupled with a power savings mode to reduce current to <1.5 μA, the device offers an attractive solution for high frequency amplifiers in battery powered applications.

The OPA835 and OPA2835 are offered in following package options:

- OPA835 Single: SOT23-6 (DBV), and 10 pin WQFN (RUN) with integrated gain resistors.
- OPA2835 Dual: SOIC-8 (D), VSSOP (MSOP) -10 (DGS), and 10 pin WQFN (RUN).

The OPA835 RUN package option includes integrated gain setting resistors for smallest possible footprint on a printed circuit board (≈ 2mm x 2mm). By adding circuit traces on the PCB, gains of +1, -1, -1.33, +2, +2.33, -3, +4, -4, +5, -5.33, +6.33, -7, +8 and inverting attenuations of -0.1429, -0.1875, -0.25, -0.33, -0.75 can be achieved. See Application Information section for details.

The devices are characterized for operation over the extended industrial temperature range –40°C to 125°C.

OPA835 Related Products

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail	—	OPA2830	—	OPA4830
Rail-to-Rail, Low Power	OPA836	OPA2836	—	—
Rail-to-Rail, Fixed Gain	OPA832	OPA2832	OPA3832	—
General-Purpose, High Slew Rate	OPA690	OPA2690	OPA3690	—
Low-Noise, DC Precision	OPA820	OPA2822	—	OPA4820

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	CHANNEL COUNT	PACKAGE – LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA835	1	SOT23-6	DBV	–40°C to 125°C	QUM	OPA835IDBVT	TAPE and REEL, 250
OPA835	1	SOT23-6	DBV	–40°C to 125°C	QUM	OPA835IDBVR	TAPE and REEL, 3000
OPA835	1	WQFN-10	RUN	–40°C to 125°C	835	OPA835IRUNT	TAPE and REEL, 250
OPA835	1	WQFN-10	RUN	–40°C to 125°C	835	OPA835IRUNR	TAPE and REEL, 3000
OPA2835	2	SOIC-8	D	–40°C to 125°C	2835	OPA2835ID	RAIL, 75
OPA2835	2	SOIC-8	D	–40°C to 125°C	2835	OPA2835IDR	TAPE and REEL, 2500
OPA2835	2	VSSOP-10	DGS	–40°C to 125°C	2835	OPA2835IDGS	RAIL, 80
OPA2835	2	VSSOP-10	DGS	–40°C to 125°C	2835	OPA2835IDGSR	TAPE and REEL, 2500
OPA2835	2	WQFN-10	RUN	–40°C to 125°C	2835	OPA2835IRUNT	TAPE and REEL, 250
OPA2835	2	WQFN-10	RUN	–40°C to 125°C	2835	OPA2835IRUNR	TAPE and REEL, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

			UNITS
V_{S-} to V_{S+}	Supply voltage		5.5
V_I	Input voltage		V_{S-} - 0.7V to V_{S+} + 0.7V
V_{ID}	Differential input voltage		1 V
I_I	Continuous input current		0.85 mA
I_O	Continuous output current		60 mA
	Continuous power dissipation		See Thermal Characteristics Specification
T_J	Maximum junction temperature		150°C
T_A	Operating free-air temperature range		–40°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD ratings	HBM	6 kV
		CDM	1 kV
		MM	200 V

THERMAL INFORMATION

THERMAL METRIC(1)		OPA835	OPA835	OPA2835	OPA2835	OPA2835	UNITS
		SOT23-6 (DBV)	WQFN-10 (RUN)	SOT23-6 (D)	VSSOP (MSOP) - 10 (DGS)	WQFN-10 (RUN)	
		6 PINS	10 PINS	8 PINS	10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	194	145.8	150.1	206	145.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	129.2	75.1	83.8	75.3	75.1	
θ_{JB}	Junction-to-board thermal resistance	39.4	38.9	68.4	96.2	38.9	
ψ_{JT}	Junction-to-top characterization parameter	25.6	13.5	33.0	12.9	13.5	
ψ_{JB}	Junction-to-board characterization parameter	38.9	104.5	67.9	94.6	104.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

SPECIFICATIONS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL[(1)]
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		51		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		22.5		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		7.2		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		3		MHz	C
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		30		MHz	C
Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 1		24		MHz	C
Bandwidth for 0.1dB flatness	V_{OUT} = 1 V_{PP}, G = 2		4		MHz	C
Slew rate, Rise/Fall	V_{OUT} = 1V_{STEP}, G = 2		110/130		V/µs	C
Rise/Fall time	V_{OUT} = 1V_{STEP}, G = 2		9.5/9		ns	C
Settling time to 1%, Rise/Fall	V_{OUT} = 1V_{STEP}, G = 2		35/30		ns	C
Settling time to 0.1%, Rise/Fall	V_{OUT} = 1V_{STEP}, G = 2		60/65		ns	C
Settling time to 0.01%, Rise/Fall	V_{OUT} = 1V_{STEP}, G = 2		120/90		ns	C
Overshoot/Undershoot	V_{OUT} = 1V_{STEP}, G = 2		0.5/0.2		%	C
2nd Order Harmonic Distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5V		-133		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5V		-110		dBc	C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5V		-73		dBc	C
3rd Order Harmonic Distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5V		-137		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5V		-125		dBc	C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5V		-78		dBc	C
2nd Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5V		-75		dBc	C
3rd Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5V		-81		dBc	C
Input voltage noise	f = 100 KHz		9.3		nV/√Hz	C
Voltage Noise 1/f corner frequency			147		Hz	C
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current Noise 1/f corner frequency			14.7		kHz	C
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		140/125		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel to channel crosstalk (OPA2835)	f = 10 kHz		-120		dB	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

SPECIFICATIONS: V_{S+} = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	120		dB	A
Input referred offset voltage	T_A = 25°C		±100	±500	μV	A
	T_A = 0°C to 70°C			±880		B
	T_A = –40°C to 85°C			±1040		
	T_A = –40°C to 125°C			±1850		
Input offset voltage drift(2)	T_A = 0°C to 70°C		±1.4	±8.5	μV/°C	B
	T_A = –40°C to 85°C		±1.5	±9		
	T_A = –40°C to 125°C		±2.25	±13.5		
Input bias current	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410		B
	T_A = –40°C to 85°C	45		425		
	T_A = –40°C to 125°C	45		530		
Input bias current drift(2)	T_A = 0°C to 70°C		±0.25	±1.4	nA/°C	B
	T_A = –40°C to 85°C		±0.175	±1.05		
	T_A = –40°C to 125°C		±0.185	±1.1		
Input offset current	T_A = 25°C		±13	±100	nA	A
	T_A = 0°C to 70°C		±13	±100		B
	T_A = –40°C to 85°C		±13	±100		
	T_A = –40°C to 125°C		±13	±100		
Input offset current drift(2)	T_A = 0°C to 70°C		±0.205	±1.230	nA/°C	B
	T_A = –40°C to 85°C		±0.155	±0.940		
	T_A = –40°C to 125°C		±0.155	±0.940		
INPUT						
Common-mode input range low	T_A = 25°C, <3dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, <3dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, <3dB degradation in CMRR limit	1.5	1.6		V	A
	T_A = –40°C to 125°C, <3dB degradation in CMRR limit	1.5	1.6		V	B
Common-mode rejection ratio		88	110		dB	A
Input impedance common mode			200‖1.2		kΩ ‖ pF	C
Input impedance differential mode			200‖1		kΩ ‖ pF	C
OUTPUT						
Linear output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Linear output voltage high	T_A = 25°C, G = 5	2.45	2.5		V	A
	T_A = –40°C to 125°C, G = 5	2.45	2.5		V	B
Output saturation voltage, High / Low	T_A = 25°C, G = 5		45/13		mV	C
Linear output current drive	T_A = 25°C	±25	±35		mA	A
	T_A = –40°C to 125°C	±20			mA	B

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

SPECIFICATIONS: V_{S+} = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL[1]
GAIN SETTING RESISTORS (OPA835IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	2376	2400	2424	Ω	A
Resistor FB2 to FB3	DC resistance	1782	1800	1818	Ω	A
Resistor FB3 to FB4	DC resistance	594	600	606	Ω	A
Resistor Tolerance	DC resistance			±1	%	A
Resistor Temperature Coefficient	DC resistance		<10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifer	T_A = 25°C	175	245	340	µA	A
	T_A = –40°C to 125°C	135		345	µA	B
Power supply rejection (±PSRR)		88	105		dB	A
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified "on" above V_{S-}+ 2.1 V		1.4	2.1	V	A
Disable voltage threshold	Specified "off" below V_{S-}+ 0.7 V	0.7	1.4		V	A
Powerdown pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Powerdown quiescent current	$\overline{PD}$ = 0.5 V		0.5	1.5	µA	A
Turn-on time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		250		ns	C
Turn-off time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		50		ns	C

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		56		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		22.5			
	V_{OUT} = 100 mV_{PP}, G = 5		7.4			
	V_{OUT} = 100 mV_{PP}, G = 10		3.1			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		31		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		31		MHz	C
Bandwidth for 0.1dB flatness	V_{OUT} = 2 V_{PP}, G=2		14.5		MHz	C
Slew rate, Rise/Fall	V_{OUT} = 2 V Step, G = 2		160/260		V/µs	C
Rise/Fall time			10/7		ns	C
Settling time to 1%, Rise/Fall			45/45		ns	C
Settling time to 0.1%, Rise/Fall			50/55		ns	C
Settling time to 0.01%, Rise/Fall			82/85		ns	C
Overshoot/Undershoot			2.5/1.5		%	C
2nd Order Harmonic Distortion	f = 10 kHz		–135		dBc	C
	f = 100 kHz		–105			C
	f = 1 MHz		-70			C
3rd Order Harmonic Distortion	f = 10 kHz		–139		dBc	C
	f = 100 kHz		–122			C
	f = 1 MHz		-73			C
2nd Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 2 V_{PP}		–70		dBc	C
3rd Order Intermodulation Distortion			–83		dBc	C
Signal to Noise Ratio, SNR	f = 1kHz, V_{OUT} = 1 V_{RMS}, 22kHz bandwidth		0.00015		%	C
			-116.4		dBc	
Total Harmonic Distortion, THD	f = 1kHz, V_{OUT} = 1 V_{RMS}		0.00003		%	C
			-130		dBc	C
Input voltage noise	f = 100 KHz		9.3		nV/√Hz	C
Voltage Noise 1/f corner frequency			147		Hz	C
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current Noise 1/f corner frequency			14.7		Hz	C
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		195/135		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel to channel crosstalk (OPA2835)	f = 10 kHz		-120		dB	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5 V, V_{S-} = 0 V, V_O = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	120		dB	A
Input referred offset voltage	T_A = 25°C		±100	±500	µV	A
	T_A = 0°C to 70°C			±880	µV	B
	T_A = –40°C to 85°C			±1040	µV	B
	T_A = –40°C to 125°C			±1850	µV	B
Input offset voltage drift(2)	T_A = 0°C to 70°C		±1.4	±8.5	µV/°C	B
	T_A = –40°C to 85°C		±1.5	±9	µV/°C	B
	T_A = –40°C to 125°C		±2.25	±13.5	µV/°C	B
Input bias current	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410	nA	B
	T_A = –40°C to 85°C	45		425	nA	B
	T_A = –40°C to 125°C	45		530	nA	B
Input bias current drift(2)	T_A = 0°C to 70°C		±0.25	±1.4	nA/°C	B
	T_A = –40°C to 85°C		±0.175	±1.05	nA/°C	B
	T_A = –40°C to 125°C		±0.185	±1.1	nA/°C	B
Input offset current	T_A = 25°C		±13	±100	nA	A
	T_A = 0°C to 70°C		±13	±100	nA	B
	T_A = –40°C to 85°C		±13	±100	nA	B
	T_A = –40°C to 125°C		±13	±100	nA	B
Input offset current drift(2)	T_A = 0°C to 70°C		±0.205	±1.23	nA/°C	B
	T_A = –40°C to 85°C		±0.155	±0.94	nA/°C	B
	T_A = –40°C to 125°C		±0.155	±0.94	nA/°C	B
INPUT						
Common-mode input range low	T_A = 25°C, <3dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, <3dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, <3dB degradation in CMRR limit	3.8	3.9		V	A
	T_A = –40°C to 125°C, <3dB degradation in CMRR limit	3.8	3.9		V	B
Common-mode rejection ratio		91	113		dB	A
Input impedance common mode			200‖1.2		kΩ ‖ pF	C
Input impedance differential mode			200‖1		kΩ ‖ pF	C
OUTPUT						
Linear output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Linear output voltage high	T_A = 25°C, G = 5	4.75	4.8		V	A
	T_A = –40°C to 125°C, G = 5	4.75	4.8		V	B
Output saturation voltage, High / Low	T_A = 25°C, G = 5		70/25		mV	C
Linear output current drive	T_A = 25°C	±30	±40		mA	A
	T_A = –40°C to 125°C	±25			mA	B

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

SPECIFICATIONS: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5 V, $V_{S–}$ = 0 V, V_O = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

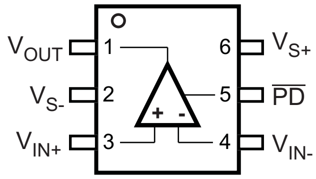
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL (1)
GAIN SETTING RESISTORS (OPA835IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	2376	2400	2424	Ω	A
Resistor FB2 to FB3	DC resistance	1782	1800	1818	Ω	A
Resistor FB3 to FB4	DC resistance	594	600	606	Ω	A
Resistor Tolerance	DC resistance			±1	%	A
Resistor Temperature Coefficient	DC resistance		<10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	200	250	350	µA	A
	T_A = –40°C to 125°C	150		365	µA	B
Power supply rejection (±PSRR)		90	110		dB	A
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified "on" above $V_{S–}$+ 2.1 V		1.4	2.1	V	A
Disable voltage threshold	Specified "off" below $V_{S–}$+ 0.7 V	0.7	1.4		V	A
Powerdown pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Powerdown quiescent current	$\overline{PD}$ = 0.5 V		0.5	1.5	µA	A
Turn-on time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		200		ns	C
Turn-off time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		60		ns	C

DEVICE INFORMATION

PIN CONFIGURATIONS

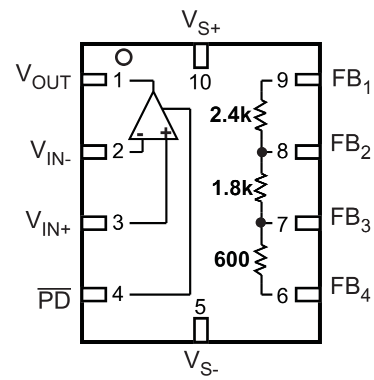
OPA835 (TOP VIEW)

SOT23-6 (DBV)



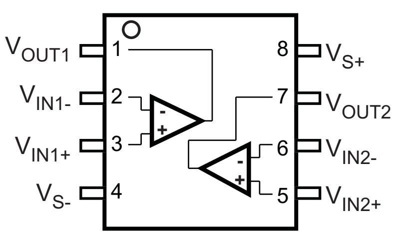
OPA835 (TOP VIEW)

WFQN-10 (RUN)



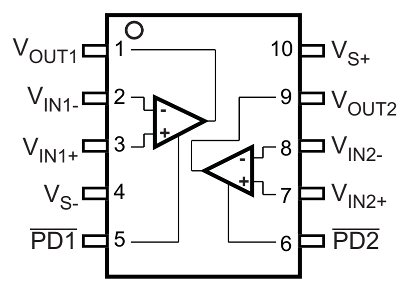
OPA2835 (TOP VIEW)

SOIC-8 (D)



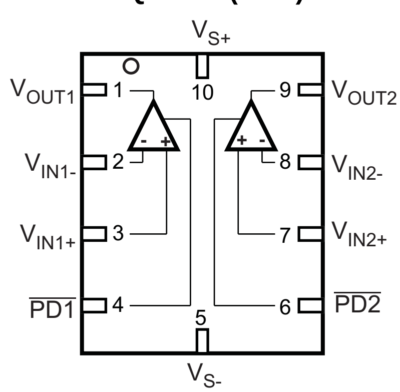
OPA2835 (TOP VIEW)

VSSOP (MSOP) -10 (DGS)



OPA2835 (TOP VIEW)

WQFN-10 (RUN)



PIN FUNCTIONS

PIN		DESCRIPTION
NUMBER	NAME	
OPA835 DBV PACKAGE		
1	V_{OUT}	Amplifier output
2	V_{S-}	Negative power supply input
3	V_{IN+}	Amplifier non-inverting input
4	V_{IN-}	Amplifier inverting input
5	$\overline{PD}$	Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
6	V_{S+}	Positive power supply input
OPA835 RUN PACKAGE		
1	V_{OUT}	Amplifier output
2	V_{IN-}	Amplifier inverting input
3	V_{IN+}	Amplifier non-inverting input
4	$\overline{PD}$	Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
5	V_{S-}	Negative power supply input
6	FB_4	Connection to bottom of 250 Ω internal gain setting resistors
7	FB_3	Connection to junction of 750 and 250 Ω internal gain setting resistors
8	FB_2	Connection to junction of 1k and 750 Ω internal gain setting resistors
9	FB_1	Connection to top of 1kΩ internal gain setting resistors
10	V_{S+}	Positive power supply input
OPA2835 D PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	V_{S-}	Negative power supply input
5	V_{IN2+}	Amplifier 2 non-inverting input
6	V_{IN2-}	Amplifier 2 inverting input
7	V_{OUT2}	Amplifier 2 output
8	V_{S+}	Positive power supply input
OPA2835 DSG PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	V_{S-}	Negative power supply input
5	$\overline{PD1}$	Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
6	$\overline{PD2}$	Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
7	V_{IN2+}	Amplifier 2 non-inverting input
8	V_{IN2-}	Amplifier 2 inverting input
9	V_{OUT2}	Amplifier 2 output
10	V_{S+}	Positive power supply input
OPA2835 RUN PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	$\overline{PD1}$	Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
5	V_{S-}	Negative power supply input
6	$\overline{PD2}$	Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
7	V_{IN2+}	Amplifier 2 non-inverting input

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NUMBER	NAME	
8	V_{IN2-}	Amplifier 2 inverting input
9	V_{OUT2}	Amplifier 2 output
10	V_{S+}	Positive power supply input

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

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Input Offset Current		Figure 24
Input Offset Current	vs Free-Air Temperature	Figure 25
Input Offset Current Drift		Figure 26

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V

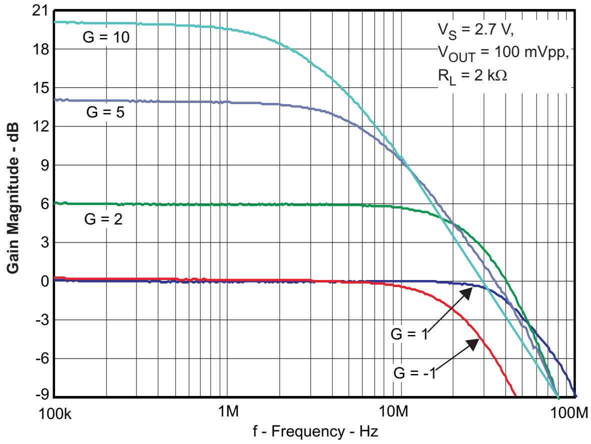

Figure 1. Small Signal Frequency Response

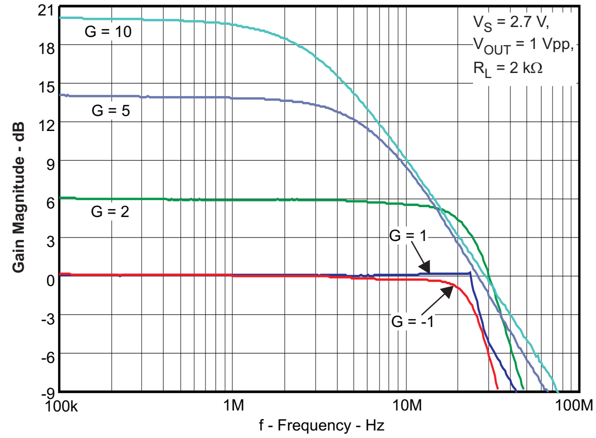

Figure 2. Large Signal Frequency Response

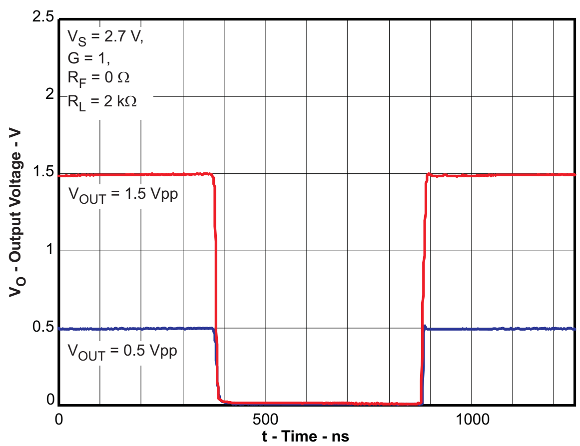

Figure 3. Noninverting Pulse Response

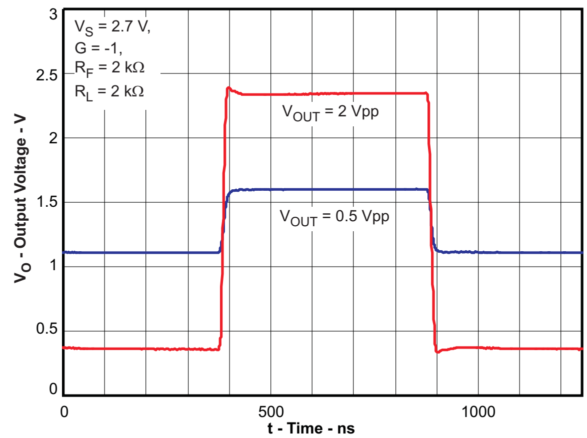

Figure 4. Inverting Pulse Response

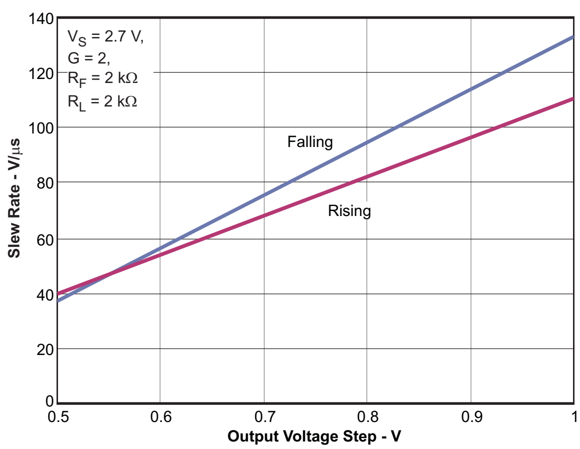

Figure 5. Slew Rate vs Output Voltage Step

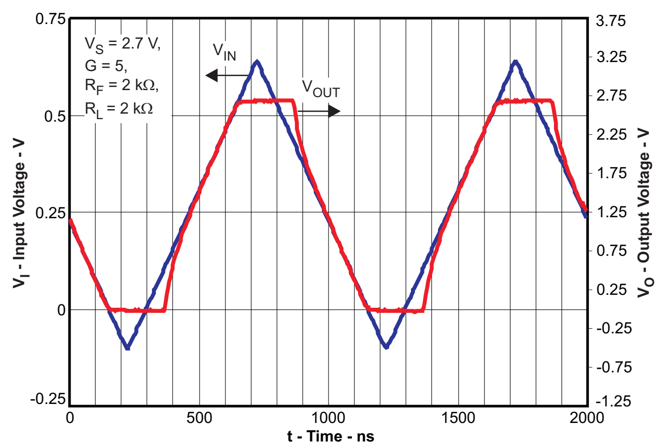

Figure 6. Output Overdrive Recovery

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

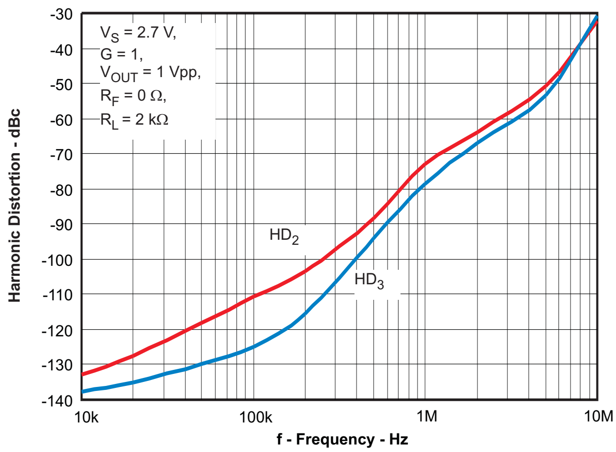

Figure 7. Harmonic Distortion vs Frequency

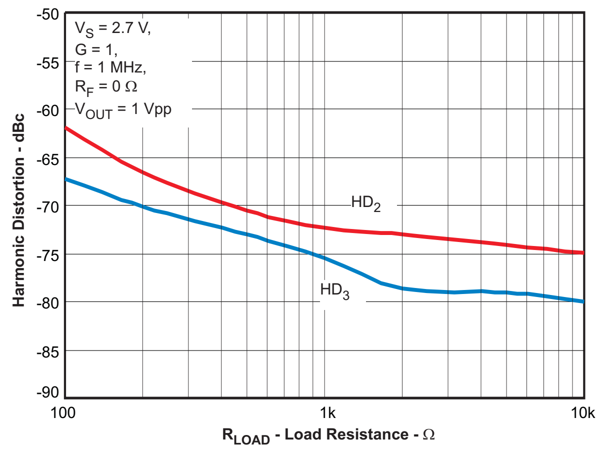

Figure 8. Harmonic Distortion vs Load Resistance

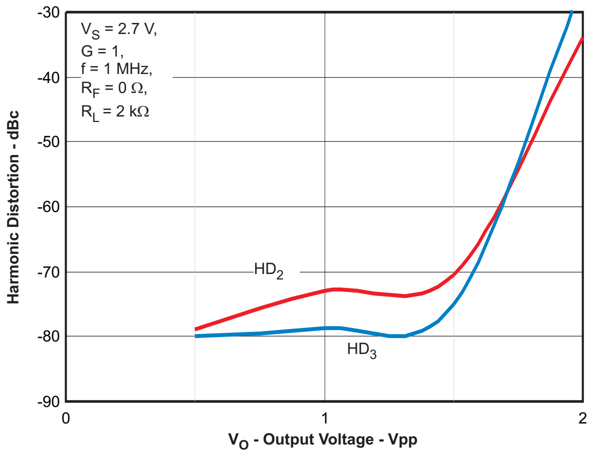

Figure 9. Harmonic Distortion vs Output Voltage

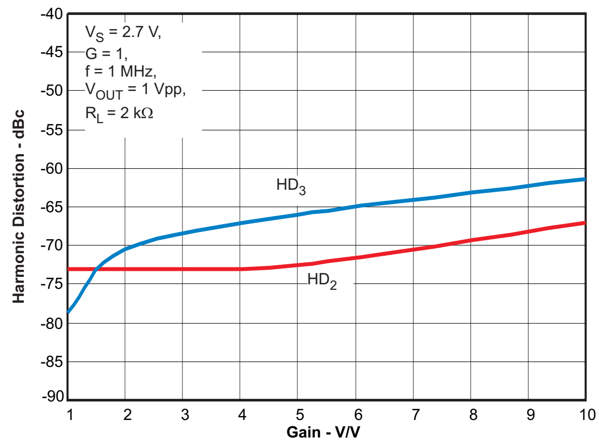

Figure 10. Harmonic Distortion vs Gain

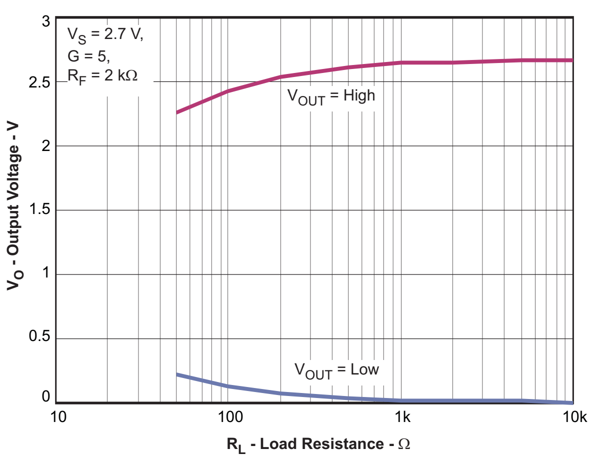

Figure 11. Output Voltage Swing vs Load Resistance

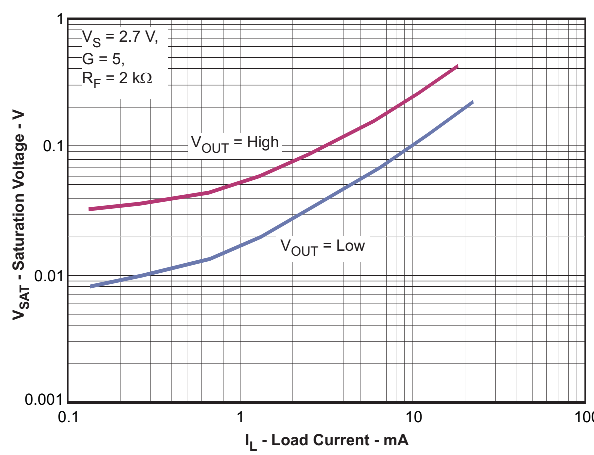

Figure 12. Output Saturation Voltage vs Load Current

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

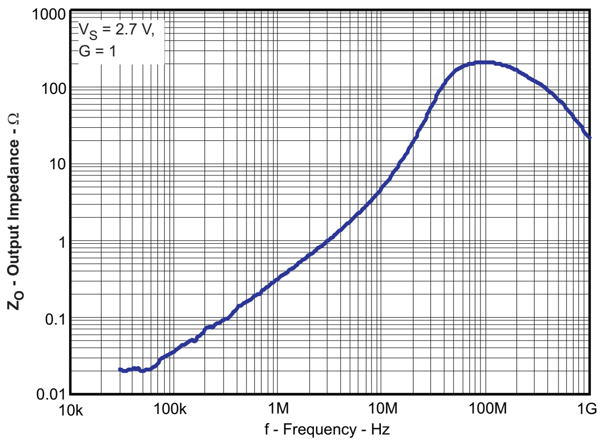

Figure 13. Output Impedance vs Frequency

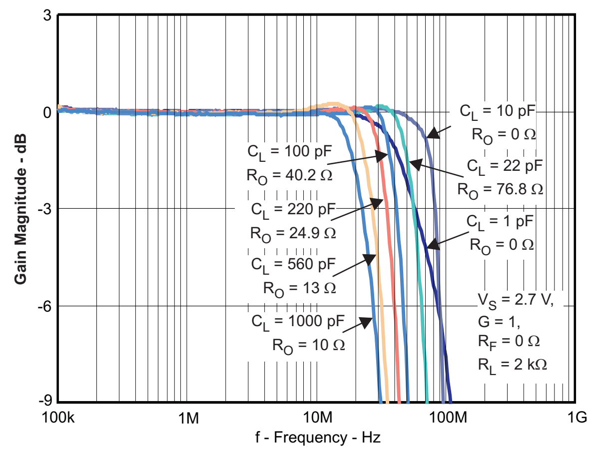

Figure 14. Frequency Response with Capacitive Load

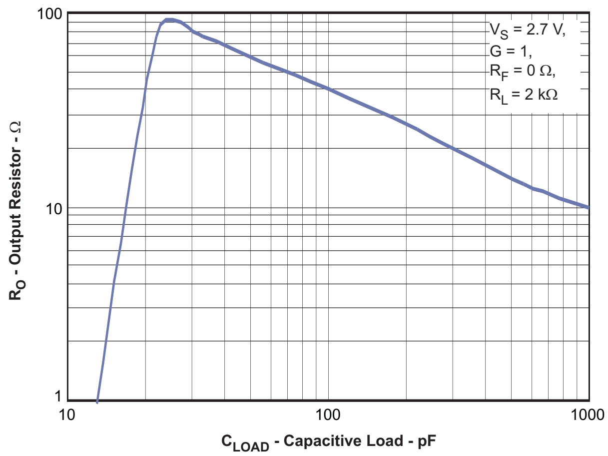

Figure 15. Series Output Resistor vs Capacitive Load

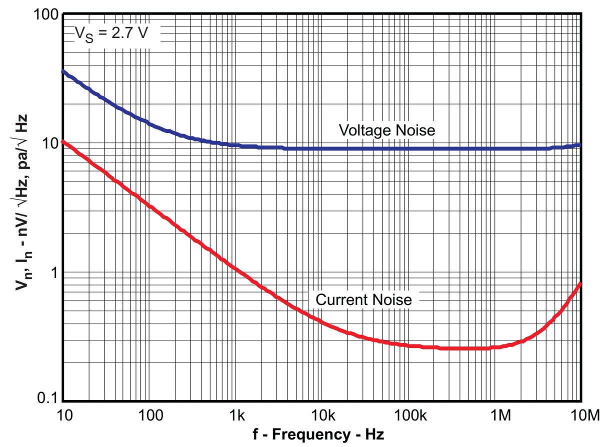

Figure 16. Input Referred Noise vs Frequency

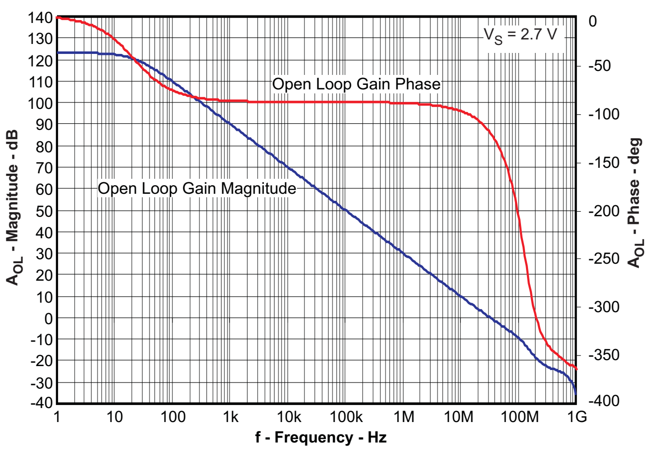

Figure 17. Open Loop Gain vs Frequency

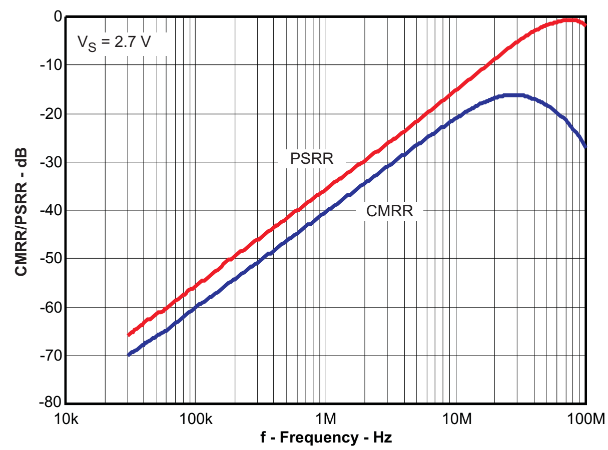

Figure 18. Common Mode/Power Supply Rejection Ratios vs Frequency

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

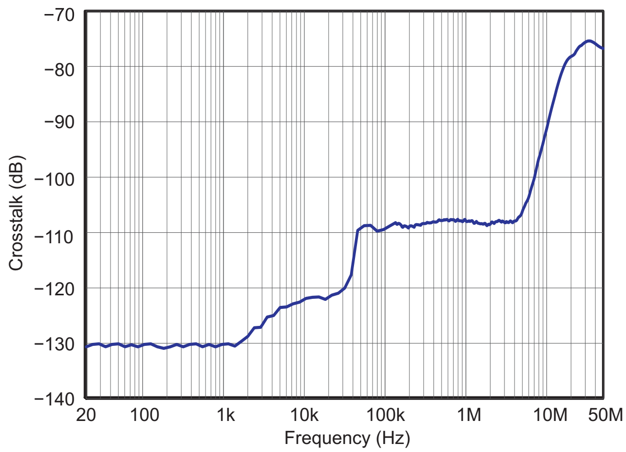

Figure 19. Crosstalk vs Frequency

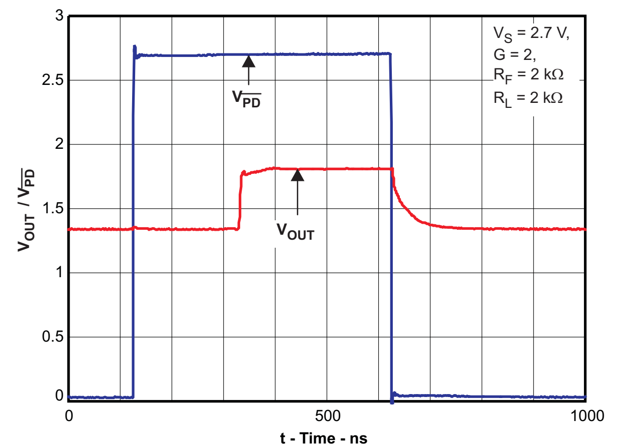

Figure 20. Power Down Response

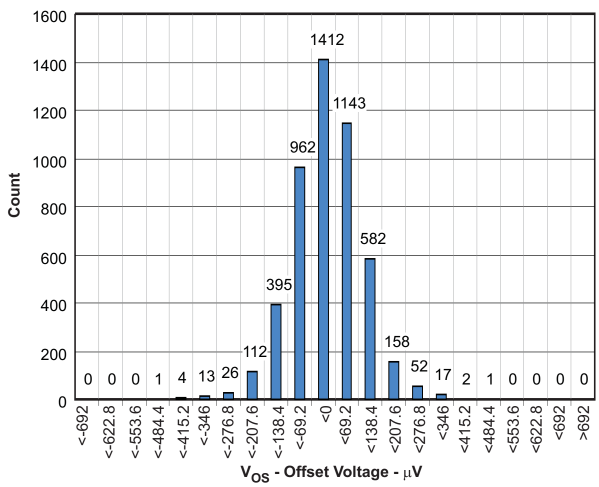

Figure 21. Input Offset Voltage

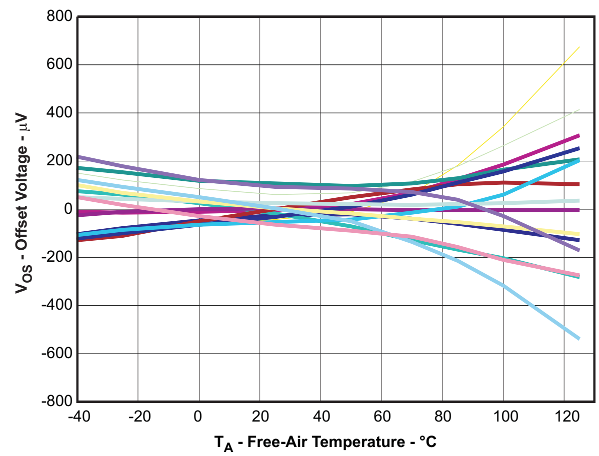

Figure 22. Input Offset Voltage vs Free-Air Temperature

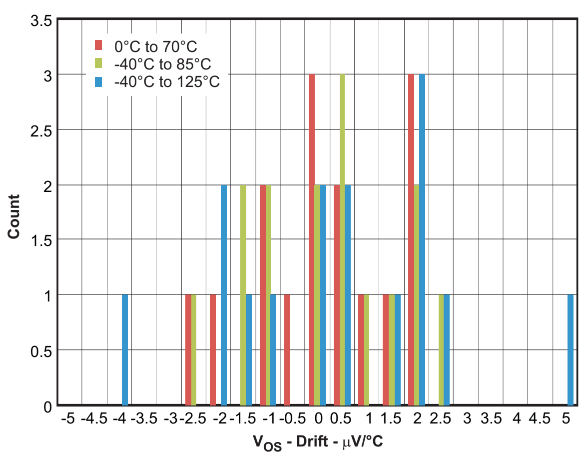

Figure 23. Input Offset Voltage Drift

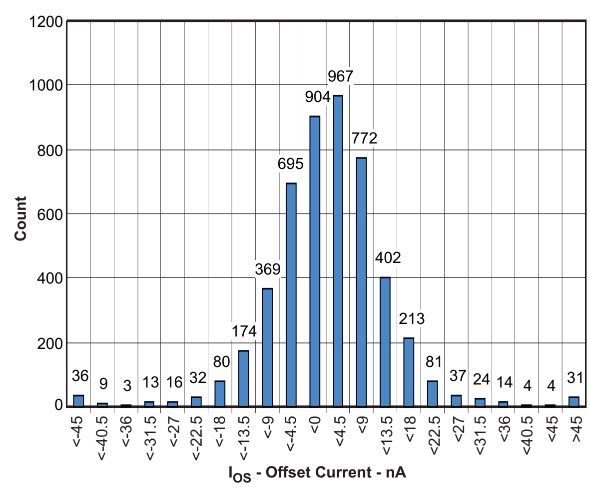

Figure 24. Input Offset Current

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

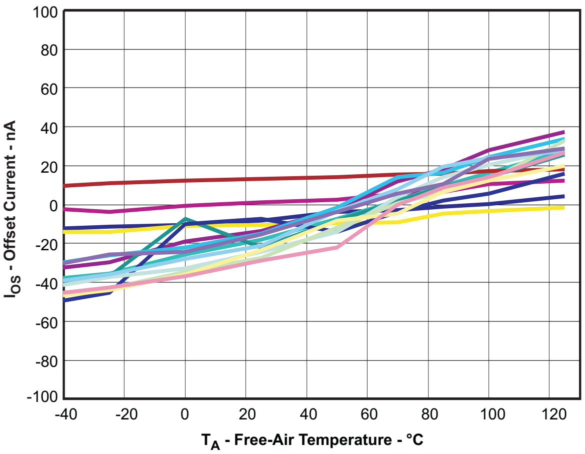

Figure 25. Input Offset Current vs Free-Air Temperature

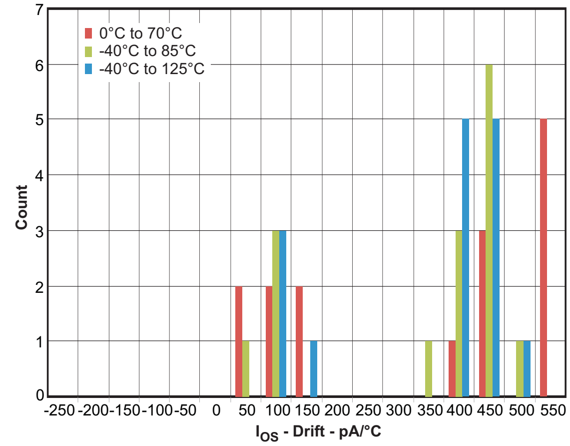

Figure 26. Input Offset Current Drift

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

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Input Offset Current	vs Free-Air Temperature	Figure 51
Input Offset Current Drift		Figure 52

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V

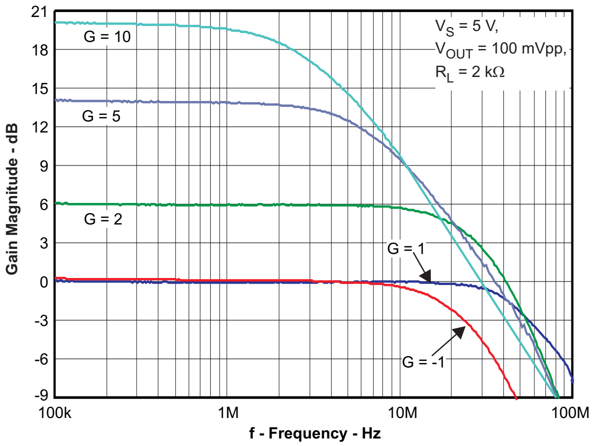

Figure 27. Small Signal Frequency Response

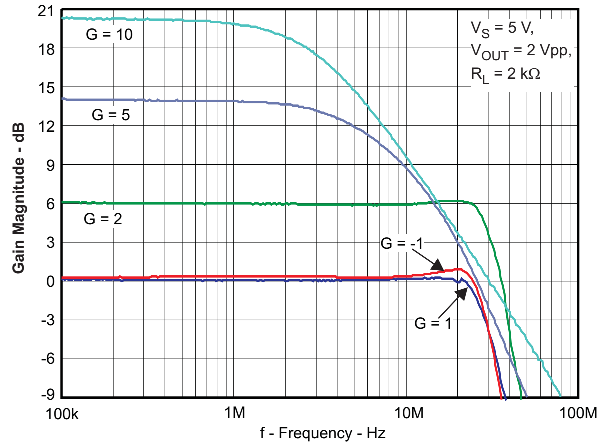

Figure 28. Large Signal Frequency Response

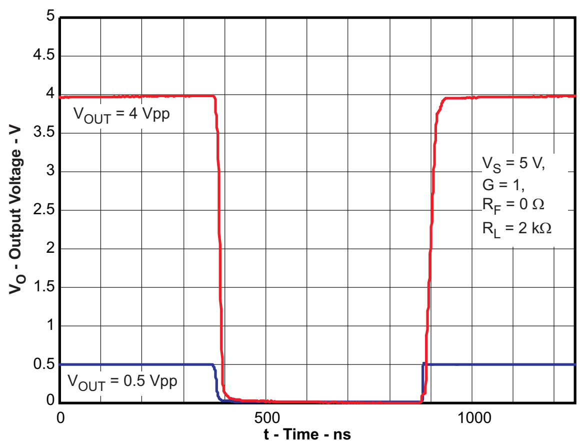

Figure 29. Noninverting Pulse Response

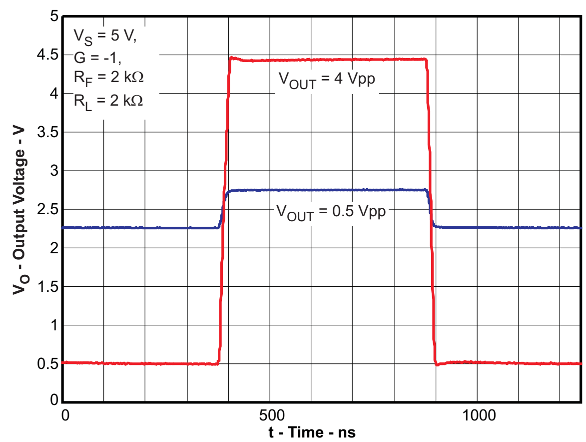

Figure 30. Inverting Pulse Response

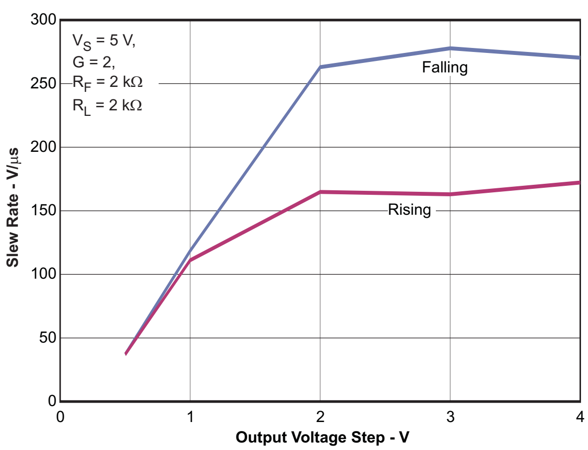

Figure 31. Slew Rate vs Output Voltage Step

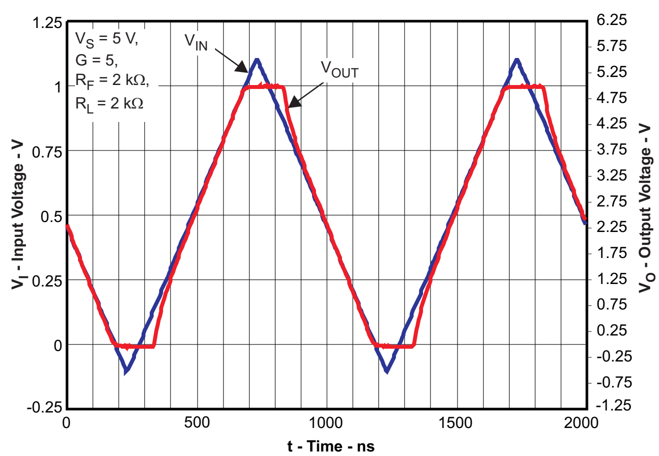

Figure 32. Output Overdrive Recovery

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

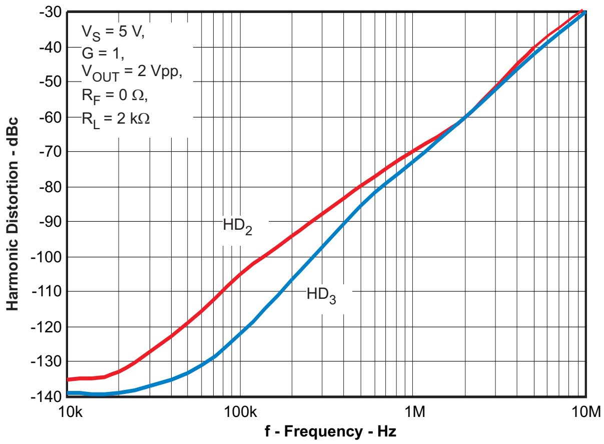

Figure 33. Harmonic Distortion vs Frequency

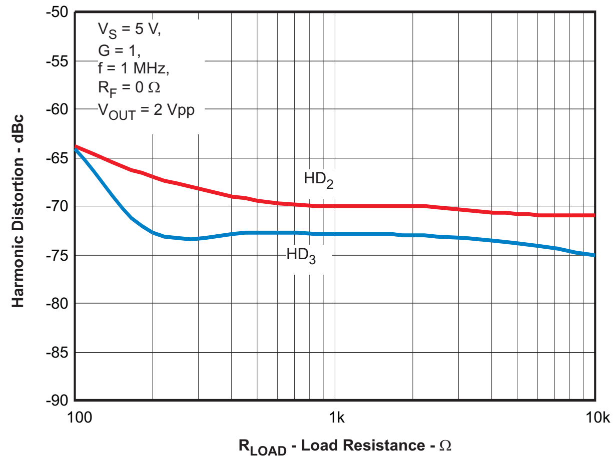

Figure 34. Harmonic Distortion vs Load Resistance

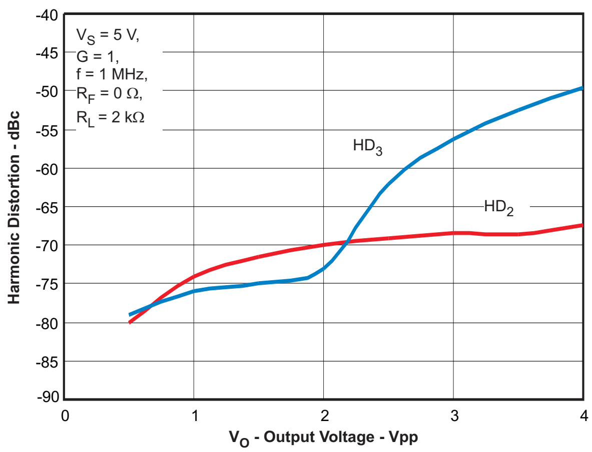

Figure 35. Harmonic Distortion vs Output Voltage

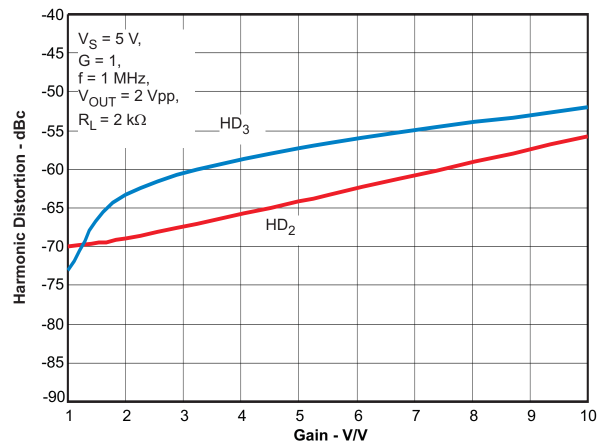

Figure 36. Harmonic Distortion vs Gain

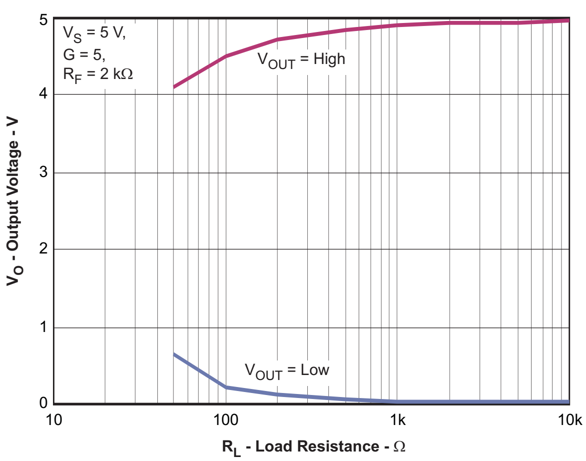

Figure 37. Output Voltage Swing vs Load Resistance

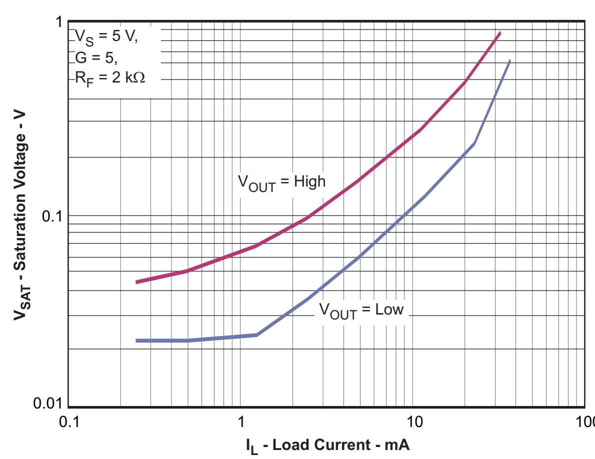

Figure 38. Output Saturation Voltage vs Load Current

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

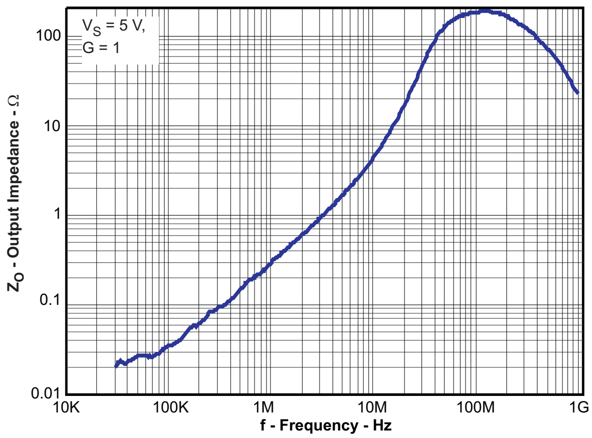

Figure 39. Output Impedance vs Frequency

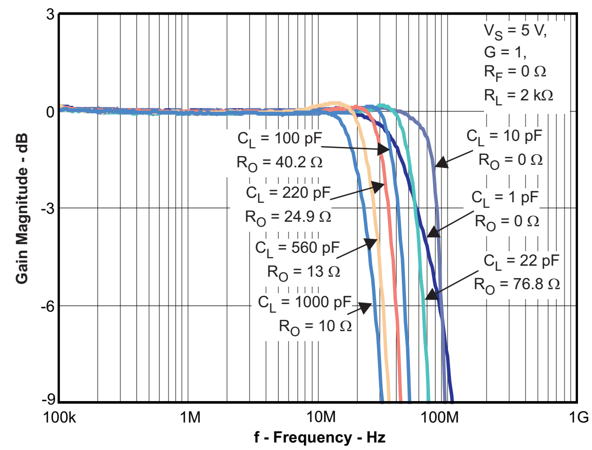

Figure 40. Frequency Response with Capacitive Load

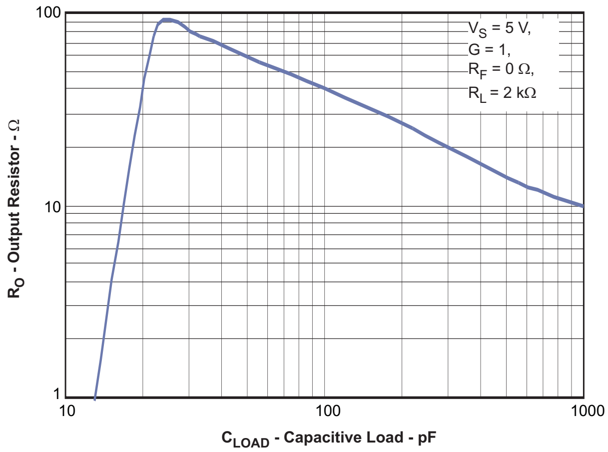

Figure 41. Series Output Resistor vs Capacitive Load

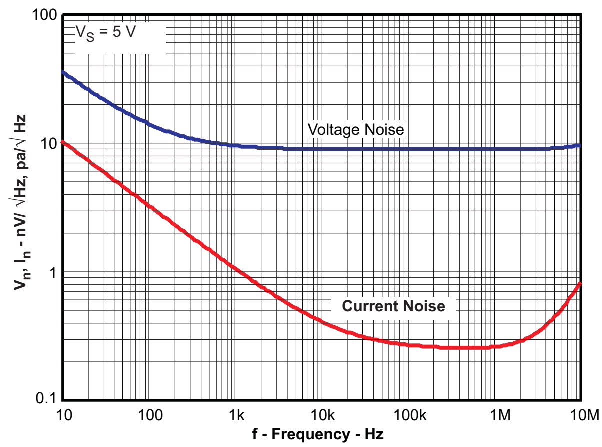

Figure 42. Input Referred Noise vs Frequency

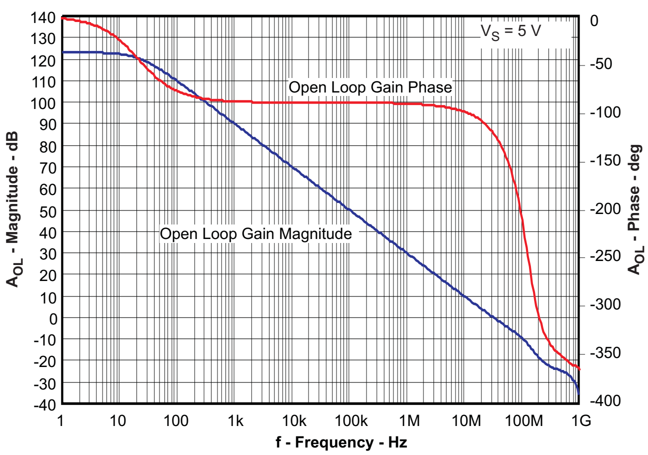

Figure 43. Open Loop Gain vs Frequency

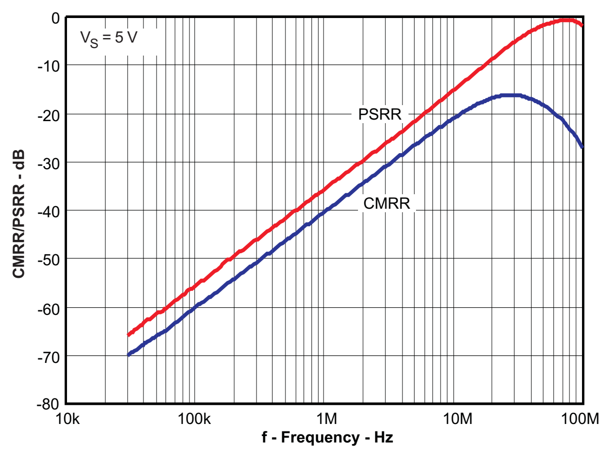

Figure 44. Common Mode/Power Supply Rejection Ratios vs Frequency

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

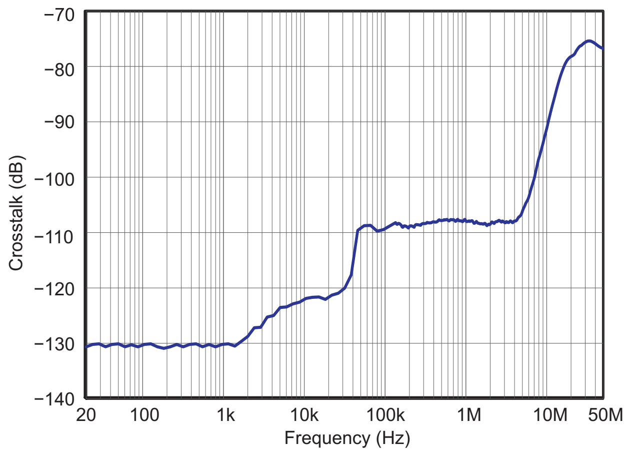

Figure 45. Crosstalk vs Frequency

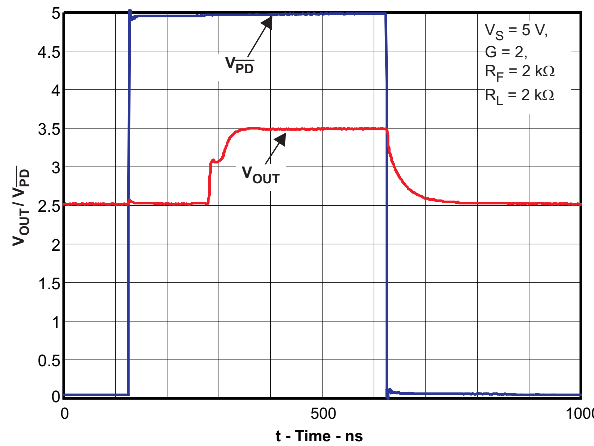

Figure 46. Power Down Response

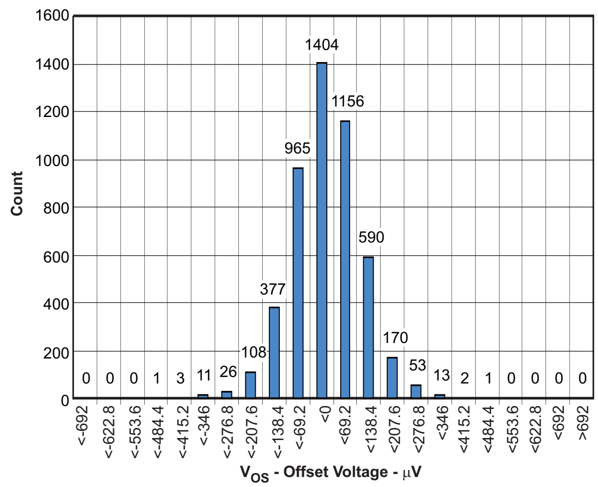

Figure 47. Input Offset Voltage

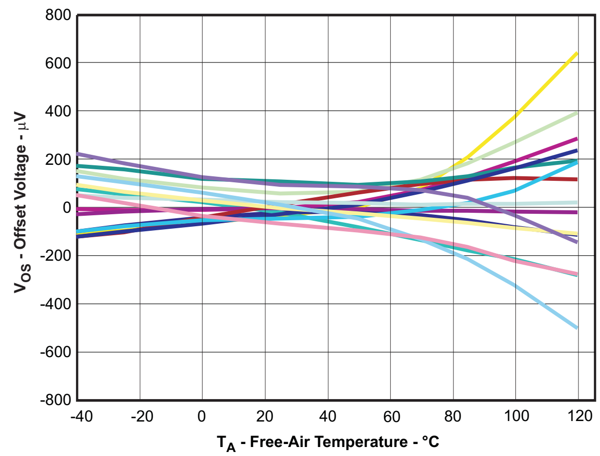

Figure 48. Input Offset Voltage vs Free-Air Temperature

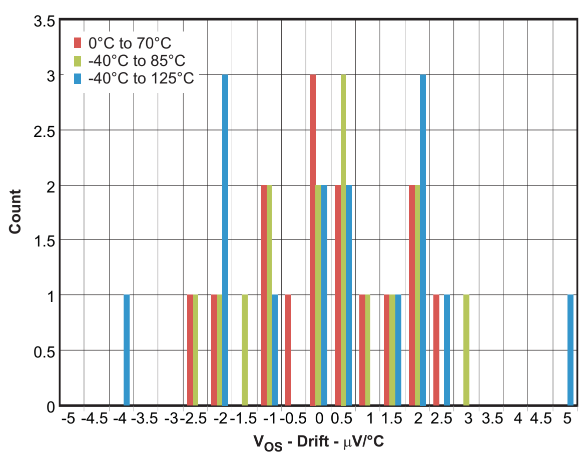

Figure 49. Input Offset Voltage Drift

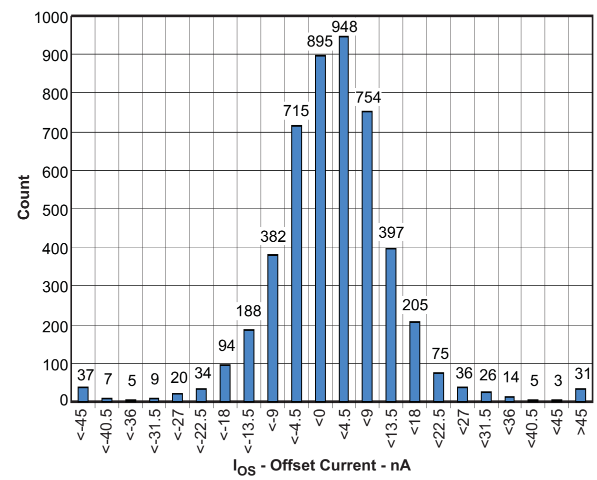

Figure 50. Input Offset Current

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

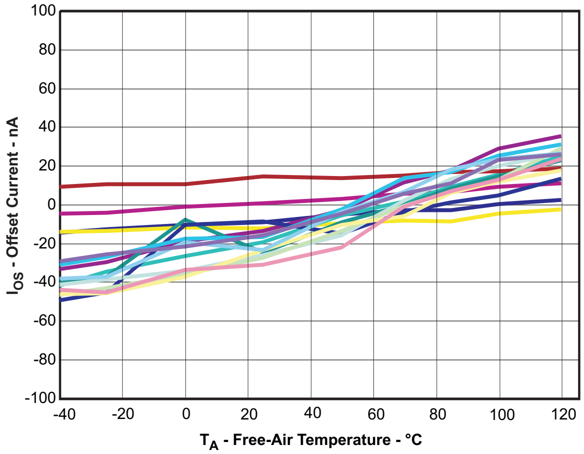

Figure 51. Input Offset Current vs Free-Air Temperature

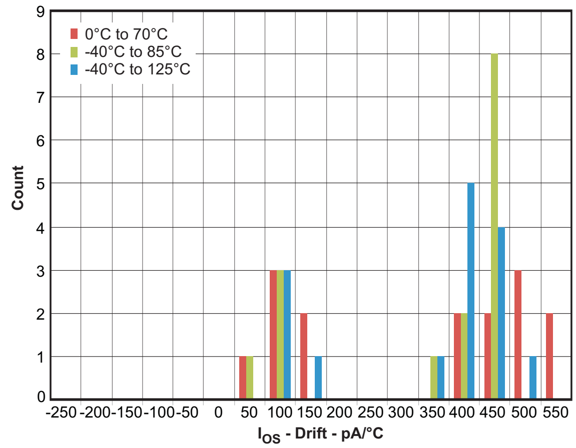

Figure 52. Input Offset Current Drift

APPLICATION INFORMATION

The following circuits show application information for the OPA835 and OPA2835. For simplicity, power supply decoupling capacitors are not shown in these diagrams.

Non-Inverting Amplifier

The OPA835 and OPA2835 can be used as non-inverting amplifiers with signal input to the non-inverting input, V_{IN+}. A basic block diagram of the circuit is shown in Figure 53.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by: $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA835 and OPA2835 are designed for the nominal value of R_F to be 2kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 2kΩ should be used as a default unless other design goals require changing to other values All test circuits used to collect data for this data sheet had R_F = 2kΩ for all gains other than +1. Gain of +1 is a special case where R_F is shorted and R_G is left open.

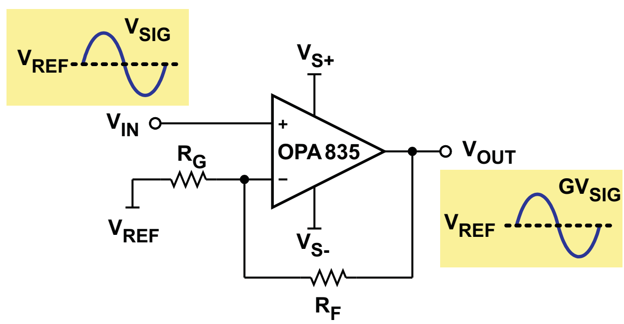

Figure 53. Non-Inverting Amplifier

Inverting Amplifier

The OPA835 and OPA2835 can be used as inverting amplifiers with signal input to the inverting input, V_{IN-}, through the gain setting resistor R_G. A basic block diagram of the circuit is shown in Figure 54.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

The signal gain of the circuit is set by: $G = \frac{-R_F}{R_G}$ and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F should be 2kΩ for inverting gains.

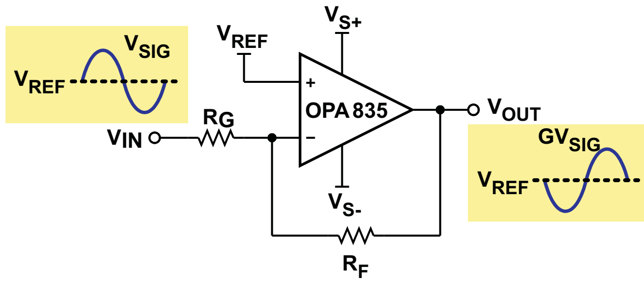

Figure 54. Inverting Amplifier

Attenuators

The non-inverting circuit of Figure 53 has minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for gain of 1 by shorting V_{OUT} to V_{IN-} and removing R_G. Since the op amp input is high impedance, the attenuation is set by the resistor divider.

The inverting circuit of Figure 54 can be used as an attenuator by making R_G larger than R_F. The attenuation is simply the resistor ratio. For example a 10:1 attenuator can be implemented with R_F = 2 kΩ and R_G = 20 kΩ.

Single Ended to Differential Amplifier

Figure 55 shows an amplifier circuit that is used to convert single-ended signals to differential, and provides gain and level shifting. This circuit can be used for converting signals to differential in applications like line drivers for CAT 5 cabling or driving differential input SAR and ΔΣ ADCs.

By setting $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and } V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \tag{3}$$

The differential signal gain of the circuit is 2x G, and V_{REF} provides a reference around which the output signal swings. The differential output signal is in-phase with the single ended input signal.

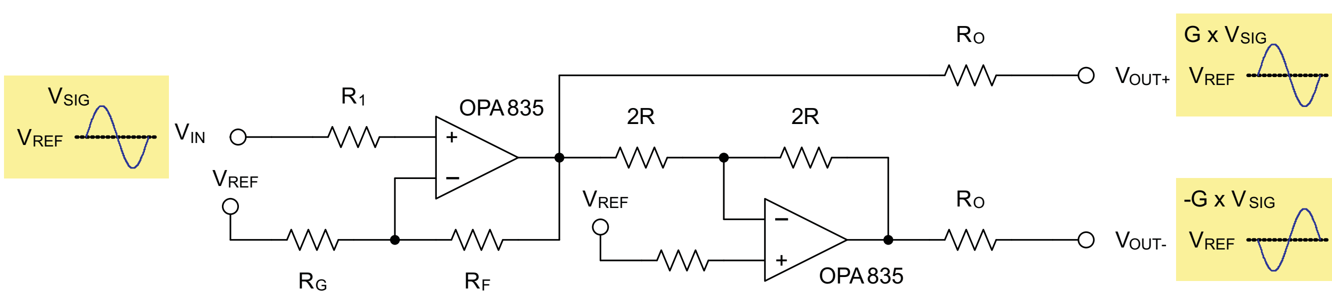

Figure 55. Single Ended to Differential Amplifier

Line termination on the output can be accomplished with resistors R_O. The impedance seen differential from the line will be 2x R_O. For example if 100 Ω CAT 5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with R_F = 0 Ω (short) R_G = ∞Ω (open), 2R = 2 kΩ, R1 = 0 Ω, R = 1 kΩ to balance the input bias currents, and R_O = 49.9 Ω for output line termination. This configuration is shown in Figure 56.

For driving a differential input ADC the situation is similar, but the output resistors, R_O, are typically chosen along with a capacitor across the ADC input for optimum filtering and settling time performance.

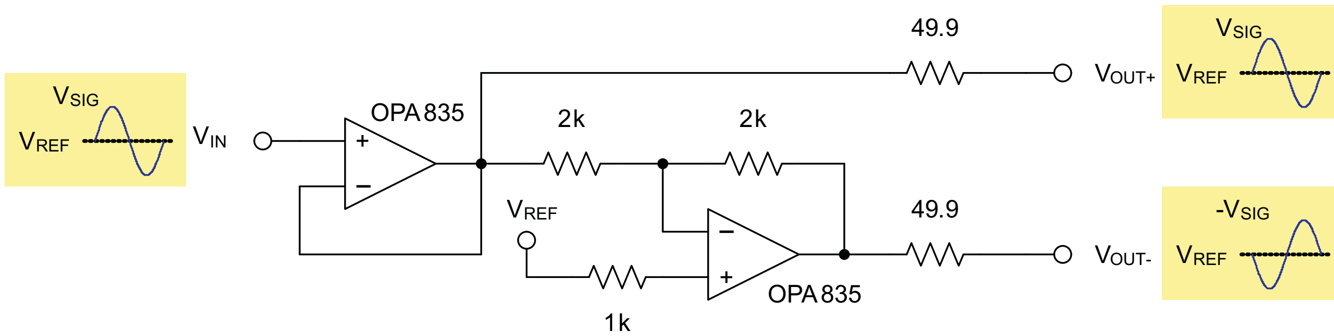

Figure 56. CAT 5 Line Driver with Gain = 2 V/V (6 dB)

Differential to Signal Ended Amplifier

Figure 57 shows a differential amplifier that is used to convert differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications like a line receiver for converting a differential signal from a CAT 5 cable to single-ended.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \tag{4}$$

The signal gain of the circuit is set by: $G = \frac{R_F}{R_G}$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

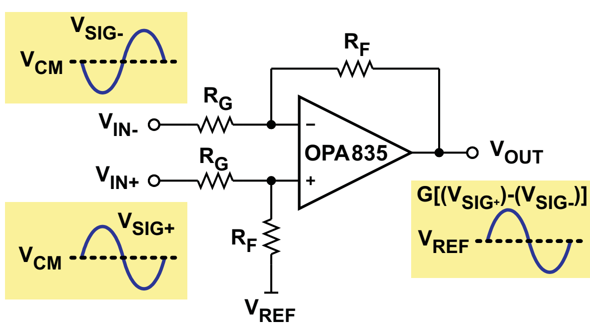

Figure 57. Differential to Single Ended Amplifier

Line termination can be accomplished with a resistor shunt across the input. The impedance seen differential from the line will be the resistor value in parallel with the amplifier circuit. For low gain and low line impedance the resistor value to add is approximately the impedance of the line. For example, if 100 Ω CAT5 cable is used with a gain of 1 amplifier and $R_F = R_G = 2$ kΩ, adding a 100 Ω shunt across the input will give a differential impedance of 99 Ω; this should be adequate for most applications.

For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

Differential to Differential Amplifier

Figure 58 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is often used in differential line driver applications where the signal source is a high impedance driver like a differential DAC that needs to drive a line.

If we set $V_{IN\pm} = V_{CM} + V_{SIG\pm}$ then

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \quad (5)$$

The signal gain of the circuit is set by: $G = 1 + \frac{2R_F}{R_G}$, and V_{CM} passes with unity gain. The amplifier in essence combines two non-inverting amplifiers into one differential amplifier with the R_G resistor shared, which makes R_G effectively ½ its value when calculating the gain. The output signals are in-phase with the input signals.

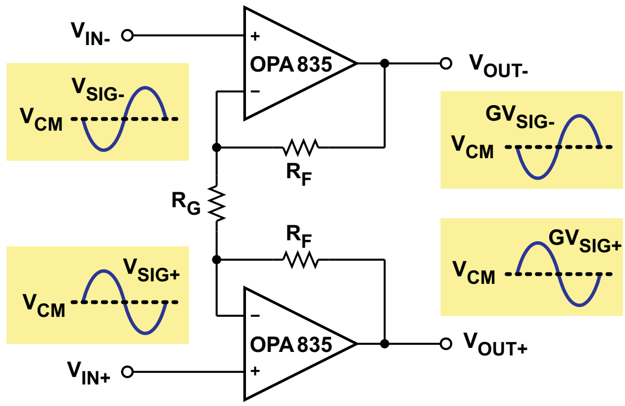

Figure 58. Differential to Differential Amplifier

Instrumentation Amplifier

Figure 59 is an instrumentation amplifier that combines the high input impedance of the differential to differential amplifier circuit and the common-mode rejection of the differential to single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required like taps from a differential line or in cases where the signal source is a high impedance.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (6)$$

The signal gain of the circuit is set by:

$G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

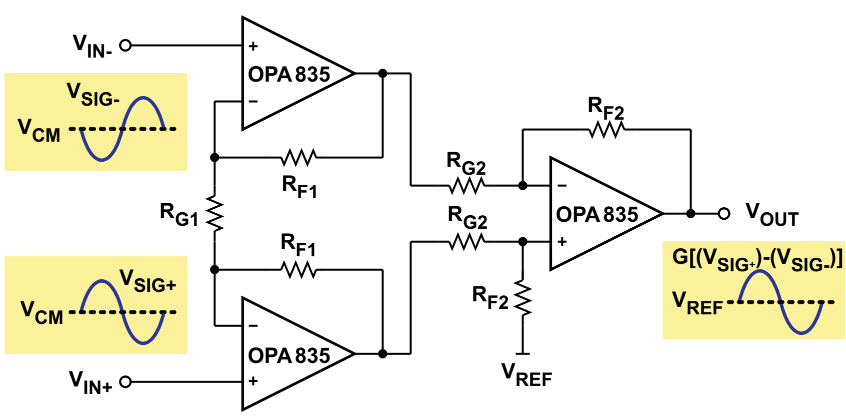

Figure 59. Instrumentation Amplifier

Integrated solutions are available, but the OPA835 provides a much lower power high frequency solution. For best CMRR performance, resistors must be matched. A rule of thumb is CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

Gain Setting with OPA835 RUN Integrated Resistors

The OPA835 RUN package option includes integrated gain setting resistors for smallest possible footprint on a printed circuit board (≈ 2mm x 2mm). By adding circuit traces on the PCB, gains of +1, -1, -1.33, +2, +2.33, -3, +4, -4, +5, -5.33, +6.33, -7, +8 and inverting attenuations of -0.1429, -0.1875, -0.25, -0.33, -0.75 can be achieved.

Figure 60 shows a simplified view of how the OPA835IRUN integrated gain setting network is implemented. Table 1 shows the required pin connections for various non-inverting and inverting gains (reference Figure 53 and Figure 54). Table 2 shows the required pin connections for various attenuations using the inverting amplifier architecture (reference Figure 54). Due to ESD protection devices being used on all pins, the absolute maximum and minimum input voltage range, V_{S-} - 0.7V to V_{S+} + 0.7V, applies to the gain setting resistors, and so attenuation of large input voltages will require external resistors to implement.

The gain setting resistors are laser trimmed to 1% tolerance with nominal values of 2.4 kΩ, 1.8 kΩ, and 600 Ω. They have excellent temperature coefficient and gain tracking is superior to using external gain setting resistors. The 800 Ω and 1.25 pF capacitor in parallel with the 2.4 kΩ gain setting resistor provide compensation for best stability and pulse response.

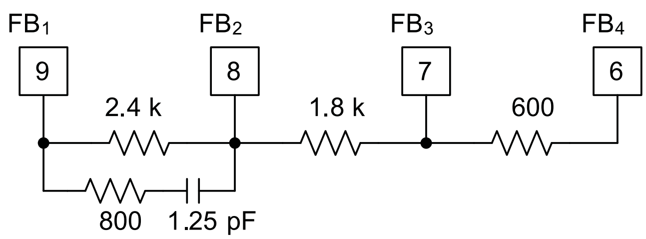

Figure 60. OPA835IRUN Gain Setting Network

Table 1. Gains Setting

Non-inverting Gain (Figure 53)	Inverting Gain (Figure 54)	Short Pins	Short Pins	Short Pins	Short Pins
1 V/V (0 dB)	-	1 to 9			-
2 V/V (6.02 dB)	-1 V/V (0 dB)	1 to 9	2 to 8	6 to GND	-
2.33 V/V (7.36 dB)	-1.33 V/V (2.5 dB)	1 to 9	2 to 8	7 to GND	-
4 V/V (12.04 dB)	-3 V/V (9.54 dB)	1 to 8	2 to 7	6 to GND	-
5 V/V (13.98 dB)	-4 V/V (12.04 dB)	1 to 9	2 to 7 or 8	7 to 8	6 to GND
6.33 V/V (16.03 dB)	-5.33 V/V (14.54 dB)	1 to 9	2 to 6 or 8	6 to 8	7 to GND
8 V/V (18.06 dB)	-7 V/V (16.90 dB)	1 to 9	2 to 7	6 to GND	-

Table 2. Attenuator Settings

Inverting Gain (Figure 54)	Short Pins	Short Pins	Short Pins	Short Pins
-0.75 V/V (-2.5 dB)	1 to 7	2 to 8	9 to GND	-
-0.333 V/V (-9.54 dB)	1 to 6	2 to 7	8 to GND	-
-0.25 V/V (-12.04 dB)	1 to 6	2 to 7 or 8	7 to 8	9 to GND
-0.1875 V/V (-14.54 dB)	1 to 7	2 to 6 or 8	6 to 8	9 to GND
-0.1429 V/V (-16.90 dB)	1 to 6	2 to 7	9 to GND	-

Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier, with high CMRR, it is important to not violate the input common-mode voltage range (V_{ICR}) of an op amp.

Common-mode input range low and high specifications in the table data use CMRR to set the limit. The limits are chosen to ensure CMRR will not degrade more than 3dB below its limit if the input voltage is kept within the specified range. The limits cover all process variations and most parts will be better than specified. The typical specifications are from 0.2V below the negative rail to 1.1V below the positive rail.

Assuming the op amp is in linear operation the voltage difference between the input pins is very small (ideally 0V) and input common-mode voltage can be analyzed at either input pin and the other input pin is assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In non-inverting configuration, Figure 53, the input signal, V_{IN}, must not violate the V_{ICR}. In inverting configuration, Figure 53, the reference voltage, V_{REF}, needs to be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For with single 5 V supply, the linear input voltage range is –0.2 V to 3.9 V and with 2.7 V supply it is –0.2 V to 1.6 V. The delta from each power supply rail is the same in either case; –0.2 V and 1.1 V.

Output Voltage Range

The OPA835 and OPA2835 are rail-to-rail output (RRO) op amps. Rail-to-rail output typically means the output voltage can swing to within a couple hundred milli-volts of the supply rails. There are different ways to specify this; one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Both saturation and linear operation limits are affected by the current in the output, where higher currents lead to more loss in the output transistors.

Data in the ELECTRICAL SPECIFICATIONS tables list both linear and saturated output voltage specifications with 2kΩ load. Figure 11 and Figure 37 show saturated voltage swing limits versus output load resistance and Figure 12 and Figure 38 show the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power supply voltages. For example with 2 kΩ load and single 5 V supply the linear output voltage range is 0.15 V to 4.8 V and with 2.7 V supply it is 0.15 V to 2.5 V. The delta from each power supply rail is the same in either case; 0.15 V and 0.2 V.

With devices like the OPA835 and OPA2835, where the input range is lower than the output range, it is typical that the input will limit the available signal swing only in non-inverting gain of 1. Signal swing in non-inverting configurations in gains > +1 and inverting configurations in any gain is generally limited by the output voltage limits of the op amp.

Split-Supply Operation (±1.25V to ±2.75V)

To facilitate testing with common lab equipment, the OPA835 EVM SLOU314 is built to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground.

Figure 61 shows a simple non-inverting configuration analogous to Figure 53 with ±2.5V supply and V_{REF} equal to ground. The input and output will swing symmetrically around ground. Due to its ease of use, split supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.

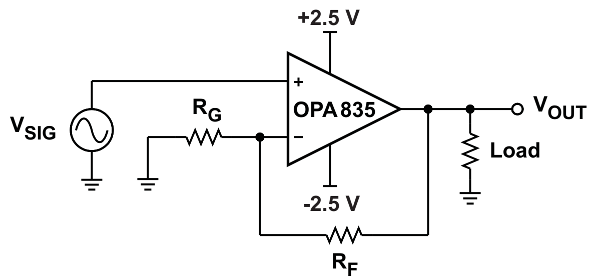

Figure 61. Split Supply Operation

Single-Supply Operation (2.5V to 5.5V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the power supply. OPA835 and OPA2835 are designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single supply, level shift of all voltages by ½ the difference between the power supply rails. For example, changing from ±2.5 V split supply to 5 V single supply is shown conceptually in Figure 62.

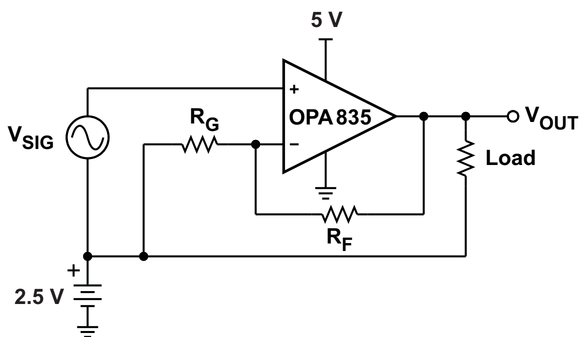

Figure 62. Single Supply Concept

A more practical circuit will have an amplifier or other circuit before to provide the bias voltage for the input and the output provides the bias for the next stage.

Figure 63 shows a typical non-inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the negative side via R_G. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example if gain of 2 is required and R_F = 2 kΩ, select R_G = 2 kΩ to set the gain and R_1 = 1 kΩ for bias current cancellation. The value for C is dependent on the reference, but at least 0.1μF is recommended to limit noise.

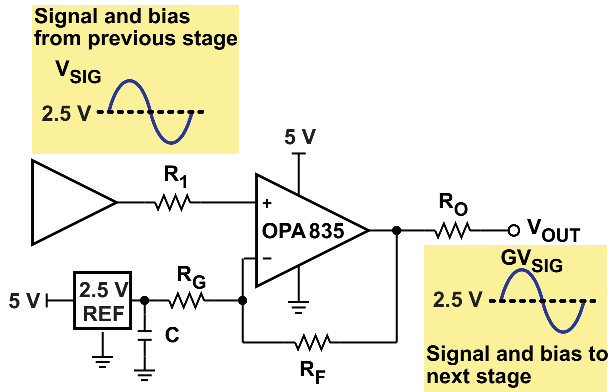

Figure 63. Non-Inverting Single Supply with Reference

Figure 64 shows a similar non-inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5V supply and are used to bias the negative side with their parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 in is chosen to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F||R_G'||R_G"). For example if gain of 2 is required and R_F = 2 kΩ, selecting R_G' = R_G" = 4 kΩ gives equivalent parallel sum of 2 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is then set to 1kΩ for bias current cancellation. This can be lower cost, but note the extra current draw required in the resistor divider.

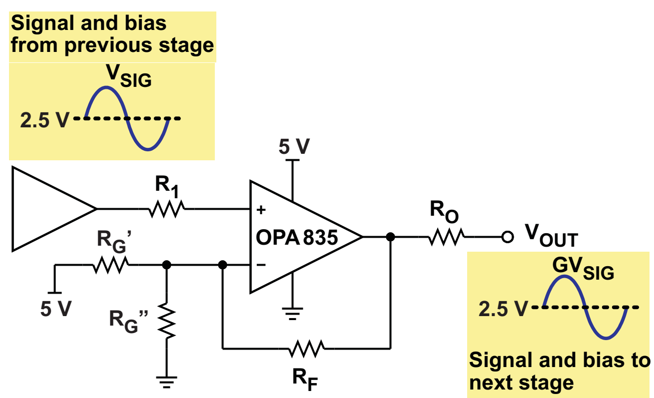

Figure 64. Non-Inverting Single Supply with Resistors

Figure 65 shows a typical inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the positive side via R_1. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is chosen to be equal to R_F in parallel with R_G. For example if gain of -2 is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 665 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1µF is recommended to limit noise into the op amp.

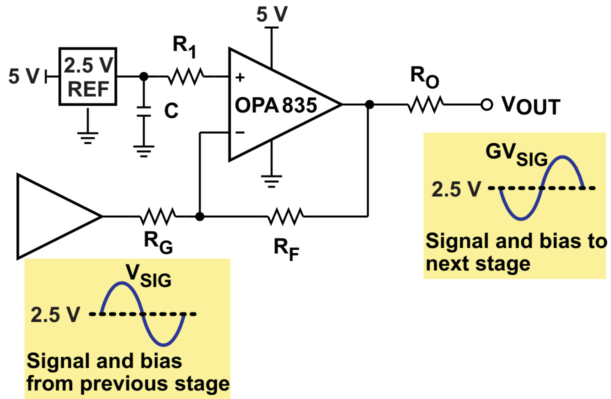

Figure 65. Inverting Single Supply with Reference

Figure 66 shows a similar inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5V supply and are used to bias the positive side. To cancel the voltage offset that would otherwise be caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C should be added to limit coupling of noise into the positive input. For example if gain of –2 is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain. R_1 = R_2 = 1.33 kΩ for mid supply voltage bias and for op amp input bias current cancellation. A good value for C is 0.1µF. This can be lower cost, but note the extra current draw required in the resistor divider.

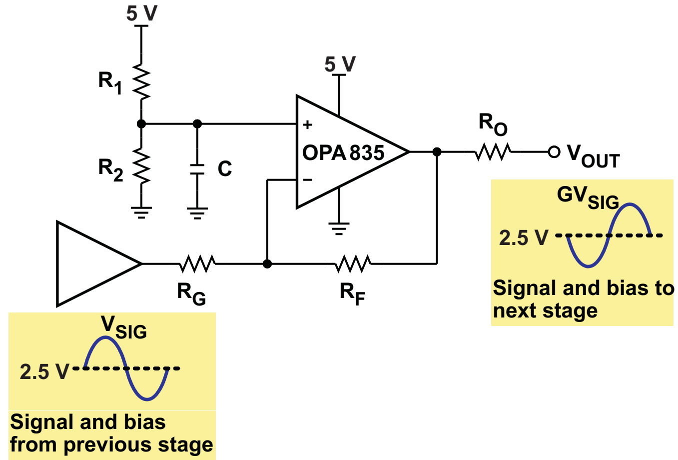

Figure 66. Inverting Single Supply with Resistors

Pulse Application with Single-Supply

For pulsed applications, where the signal is at ground and pulses to some positive or negative voltage, the circuit bias voltage considerations are different than with a signal that swings symmetrical about a reference point and the circuit configuration should be adjusted accordingly. Figure 67 shows a pulsed situation where the signal is at ground (0 V) and pulses to a positive value.

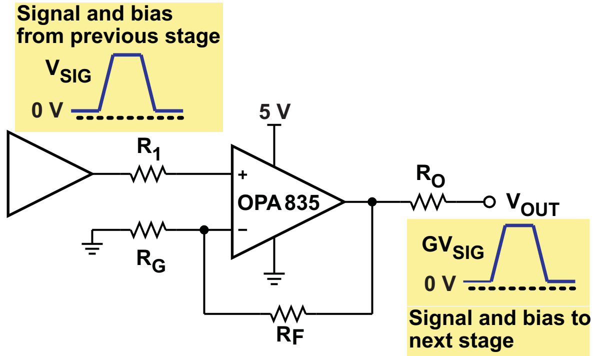

Figure 67. Non-Inverting Single Supply with Pulse

If the input signal pulses negative from ground, an inverting amplifier is more appropriate as shown in Figure 68. A key consideration in both non-inverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier, and since the V_{ICR} of the OPA835 includes the negative supply rail, the op amp lends itself to this application.

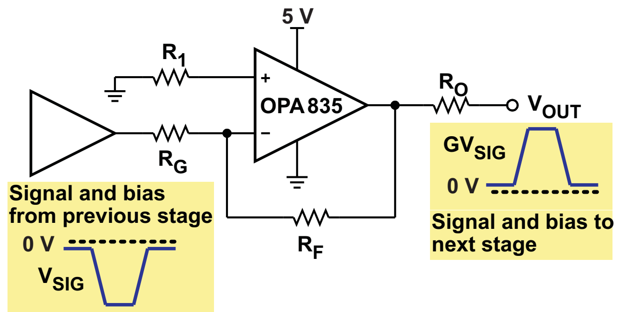

Figure 68. Inverting Single Supply with Pulse

Power-Down Operation

The OPA835 and OPA2835 include a power-down mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of <1.5 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting $\overline{PD}$ pin low disables the amplifier, and places the output in a high impedance state. Note: the op amp's output in gain of +1 is high impedance similar to a 3-state high impedance gate, but in other gains the feedback network is a parallel load.

The $\overline{PD}$ pin must be actively driven high or low and should not be left floating. If the power-down mode is not used, $\overline{PD}$ should be tied to the positive supply rail.

$\overline{PD}$ logic states are TTL with reference to the negative supply rail, V_{S-}. When the op amp is powered from single supply and ground, driving from logic devices with similar V_{DD} voltages to the op amp should not require any special consideration. When the op amp is powered from split supply, V_{S-} is below ground and an open collector type of interface with pull-up resistor is more appropriate. Pull-up resistor values should be lower than 100k and the drive logic should be negated due to the inverting action of an open collector gate.

Low Power Applications and the Effects of Resistor Values on Bandwidth

The OPA835 and OPA2835 are designed for the nominal value of R_F to be 2 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 2 with $R_F = R_G$ = 2 kΩ, R_G to ground, and V_{OUT} = 4 V, 1mA of current will flow through the feedback path to ground. In gain of +1, R_G is open and no current will flow to ground. In low power applications, it is desirable to reduce this current by increasing the gain setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with parasitic circuit capacitance.

1. Lowers the bandwidth.
2. Lowers the phase margin
   (a) This will cause peaking in the frequency response.
   (b) And will cause over shoot and ringing in the pulse response.

Figure 69 shows the small signal frequency response on OPA835EVM for non-inverting gain of 2 with R_F and R_G equal to 2 kΩ, 10 kΩ, and 100 kΩ. The test was done with R_L = 2 kΩ. Due to loading effects of R_L, lower values may reduce the peaking, but higher values will not have a significant effect.

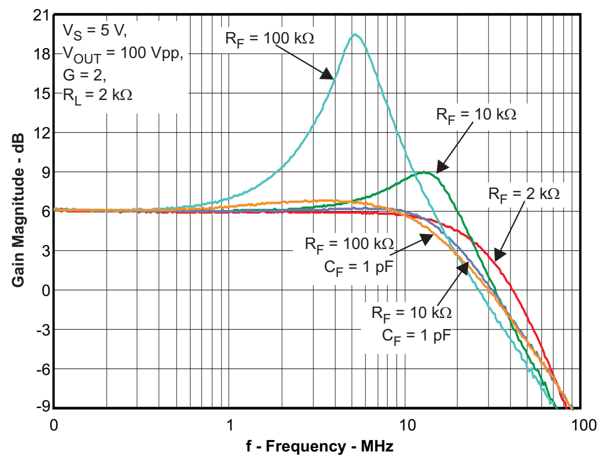

Figure 69. Frequency Response with Various Gain Setting Resistor Values

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). Adding 1 pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. Figure 70 shows the test circuit used.

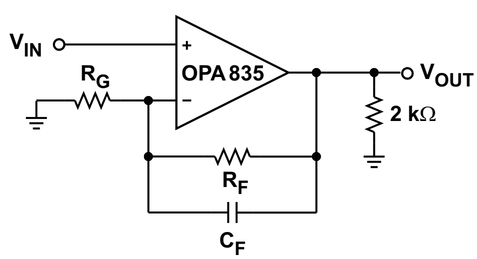

Figure 70. G=2 Test Circuit for Various Gain Setting Resistor Values

Driving Capacitive Loads

The OPA835 and OPA2835 can drive up to a nominal capacitive load of 10pF on the output with no special consideration. When driving capacitive loads greater than this, it is recommended to use a small resister (R_O) in series with the output as close to the device as possible. Without R_O, capacitance on the output will interact with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin. This will cause peaking in the frequency response and overshoot and ringing in the pulses response. Interaction with other parasitic elements may lead to instability or oscillation. Inserting R_O will isolate the phase shift from the loop gain path and restore the phase margin; however, it will also limit the bandwidth.

Figure 71 shows the test circuit and Figure 41 shows the recommended values of R_O versus capacitive loads, C_L. See Figure 40 for frequency response with various values.

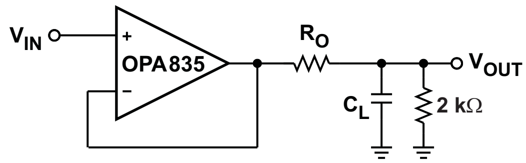

Figure 71. R_O versus C_L Test Circuit

Active Filters

The OPA835 and OPA2835 can be used to design active filters. Figure 73 and Figure 72 show MFB and Sallen-Key circuits designed using FilterPro™ http://focus.ti.com/docs/toolsw/folders/print/filterpro.html to implement 2^{nd} order low-pass butterworth filter circuits. Figure 74 shows the frequency response.

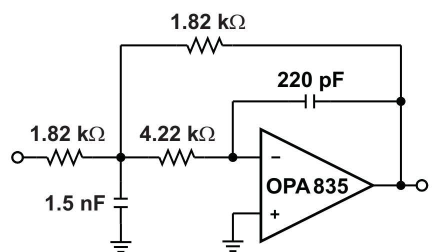

Figure 72. MFB 100kHz 2^{nd} Order Low-Pass Butterworth Filter Circuit

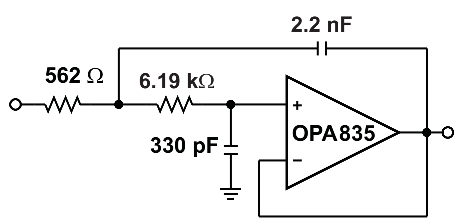

Figure 73. Sallen-Key 100kHz 2nd Order Low-Pass Butterworth Filter Circuit

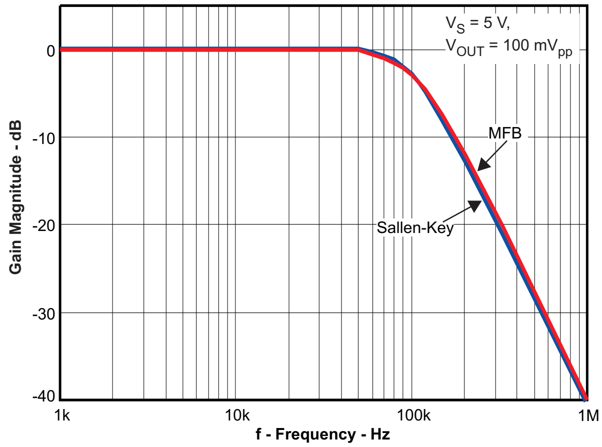

Figure 74. MFB and Sallen-Key 2_{nd} Order Low-Pass Butterworth Filter Response

MFB and Sallen-Key filter circuits offer similar performance. The main difference is the MFB is an inverting amplifier in the pass band and the Sallen-Key is non-inverting. The primary pro for each is the Sallen-Key in unity gain has no resistor gain error term, and thus no sensitivity to gain error, while the MFB has inherently better attenuation properties beyond the bandwidth of the op amp.

Audio Frequency Performance

The OPA835 and OPA2835 provide excellent audio performance with very low quiescent power. To show performance in the audio band, a 2700 series Audio Analyzer from Audio Precision was used to test THD+N and FFT at 1 V_{RMS} output voltage. Figure 75 is the test circuit used. Note the 100 pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

Figure 76 shows the THD+N performance with 100 kΩ and 300 Ω loads, and with no weighting and A-weighting. With no weighting the THD+N performance is dominated by the noise for both loads. A-weighting provides filtering that improves the noise so a larger difference can be seen between the loads due to more distortion with R_L = 300 Ω.

Figure 77 and Figure 78 show FFT output with a 1 kHz tone and 100kΩ and 300Ω loads. To show relative performance of the device versus the test set, one channel has the OPA835 in line between generator output and analyzer input and the other channel is in “Gen Mon” loopback mode, which internally connects the signal generator to the analyzer input. With 100 kΩ load, Figure 77, the curves are basically indistinguishable from each other except for noise, which means the OPA835 cannot be directly measured. With 300Ω load, Figure 78, the main difference between the curves is OPA835 shows higher even order harmonics, but odd order is masked by the test set performance.

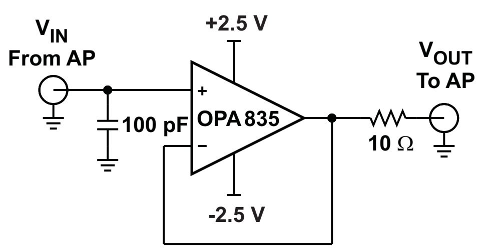

Figure 75. OPA835 AP Analyzer Test Circuit

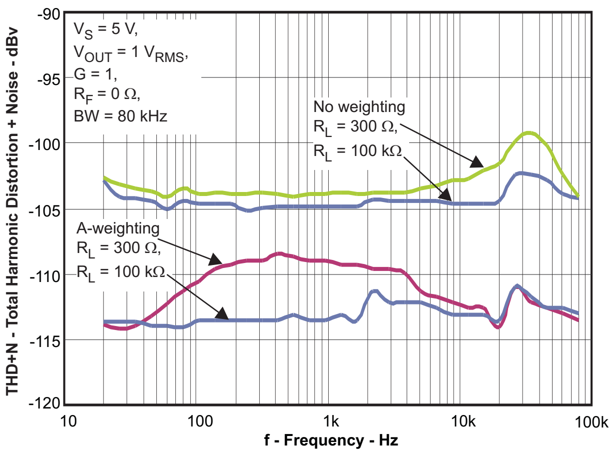

Figure 76. OPA835 1 Vrms 20 Hz to 80 kHz THD+N

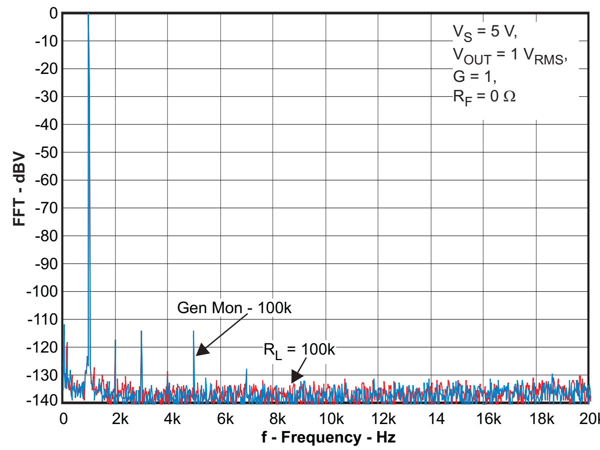

Figure 77. OPA835 and AP Gen Mon 1kHz FFT Plot; V_{OUT} = $1V_{RMS}$, R_L = 100kΩ

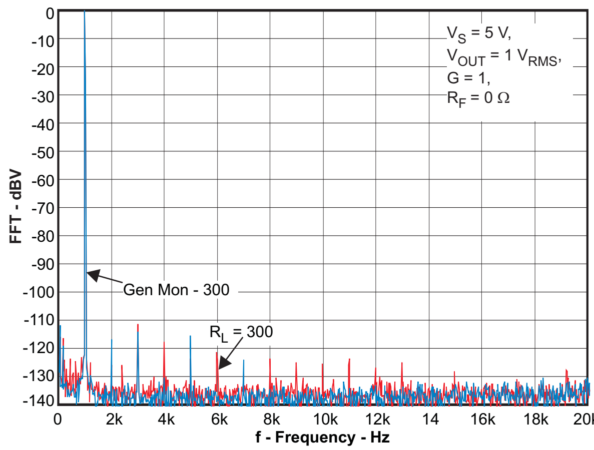

Figure 78. OPA835 and AP Gen Mon 1kHz FFT Plot; V_{OUT} = $1V_{RMS}$, R_L = 300Ω

ADC Driver Performance

The OPA835 provides excellent performance when driving high performance delta-sigma (ΔΣ) and successive approximation register (SAR) ADCs in low power audio and industrial applications.

OPA835 and ADS8326 Combined Performance

To show achievable performance, the OPA835 is tested as the drive amplifier for the ADS8326. The ADS8326 is a 16-bit, micro power, SAR ADC with pseudo-differential inputs and sample rates up to 250kSPS. It offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA835 an ideal solution for portable and battery-operated systems, for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

The circuit shown in Figure 79 is used to test the performance, Figure 80 is the FFT plot with 10kHz input frequency showing the spectral performance, and the tabulated AC analysis results are in Table 3.

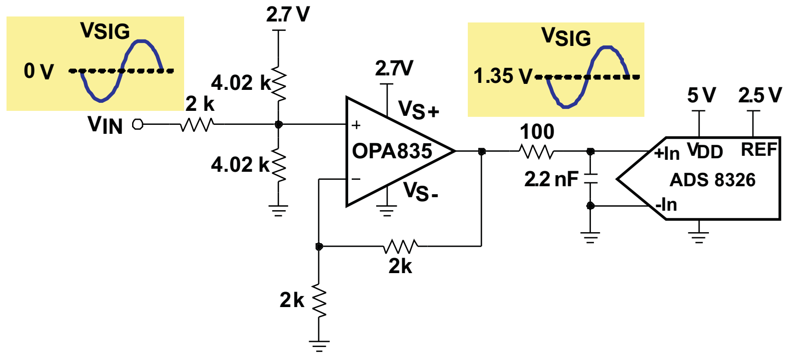

Figure 79. OPA835 and ADS8326 Test Circuit

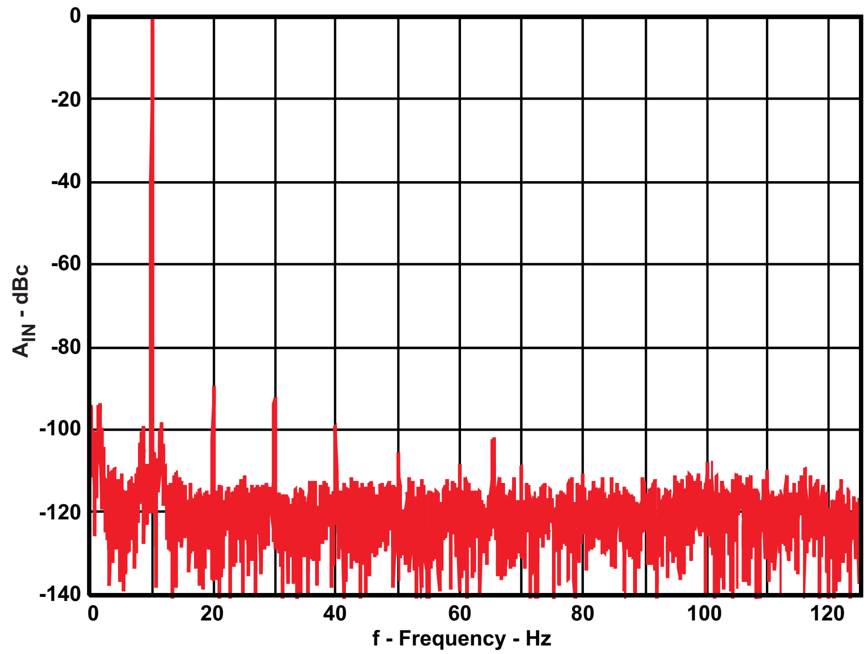

Figure 80. ADS8326 and OPA835 10kHz FFT

Table 3. AC Analysis

Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
10k	–0.85	81.9	–87.5	80.8	89.9

Layout Recommendations

OPA835 EVM (SLOU314) should be used as a reference when designing the circuit board. It is recommended to follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into an out of the op amp.
2. The feedback path should be short and direct avoiding vias if possible especially with G = +1.
3. Ground or power planes should be removed from directly under the amplifier's negative input and output pins.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See "Recommended Series Output Resistor vs. Capacitive Load" (Figure 41) for recommended values given expected capacitive load of design.
5. A 2.2 µF power supply decoupling capacitor should be placed within 2 inches of the device and can be shared with other op amps. For spit supply, a capacitor is required for both supplies.
6. A 0.1 µF power supply decoupling capacitor should be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels. If not used it should tied to the positive supply to enable the amplifier. If used, it must be actively driven. A bypass capacitor is not necessary, but can be used for robustness in noisy environments.

REVISION HISTORY

Changes from Revision A (March 2011) to Revision B — **Page**

- Changed OPA835 from product preview to production data 1

Changes from Revision B (May 2011) to Revision C — **Page**

- Added the "The OPA835 RUN package..." text to the DESCRIPTION 1
- Removed Product Preview from all devices except OPA835IRUNT and OPA835IRUNR 2
- Replaced the TBD values in the Thermal Information table 2
- Changed - Channel to channel crosstalk (OPA2835) Typ value From: TBD To: -120 dB 3
- Changed the Common-mode rejection ratio Min value From: 91 dB To: 88 dB 4
- Added GAIN SETTING RESISTORS (OPA835IRUN ONLY) 5
- Changed the Quiescent operating current (T_A = 25°C) Min value From: 190 µA To: 175 µA 5
- Changed the Power supply rejection (±PSRR) Min value From: 91 dB To: 88 dB 5
- Changed the Powerdown pin bias current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V 5
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V 5
- Changed - Channel to channel crosstalk (OPA2835) Typ value From: TBD To: -120 dB 6
- Changed the Common-mode rejection ratio Min value From: 94 dB To: 91 dB 7
- Added GAIN SETTING RESISTORS (OPA835IRUN ONLY) 8
- Changed the Quiescent operating current (T_A = 25°C) Min value From: 215 µA To: 200 µA 8
- Changed the Power supply rejection (±PSRR) Min value From: 93 dB To: 90 dB 8
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V 8
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V 8
- Changed the OPA835 WQFN-10 (RUN) pinout image 9
- Added Figure Crosstalk vs Frequency 14
- Added Figure Crosstalk vs Frequency 20
- Added section Single Ended to Differential Amplifier 24

Changes from Revision C (September 2011) to Revision D **Page**

- Removed Product Preview from OPA835IRUNT and OPA835IRUNR ... 2
- Changed Resistor Temperature Coefficient From: TBD To: <10 ... 5
- Changed Quiescent operating current To: Quiescent operating current per amplifer ... 5
- Changed Resistor Temperature Coefficient From: TBD To: <10 ... 8
- Changed Quiescent operating current To: Quiescent operating current per amplifer ... 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2835ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2835IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2835IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2835IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2835IRUNR	ACTIVE	QFN	RUN	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2835IRUNT	ACTIVE	QFN	RUN	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA835IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA835IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA835IRUNR	ACTIVE	QFN	RUN	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA835IRUNT	ACTIVE	QFN	RUN	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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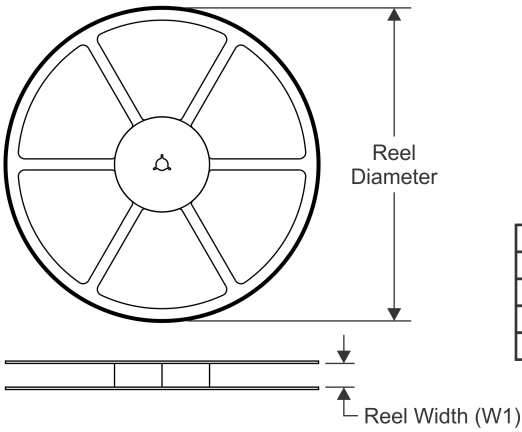
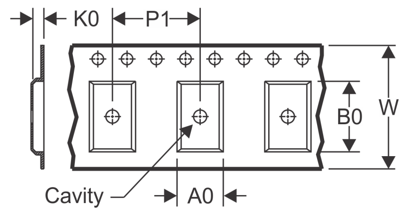
TAPE AND REEL INFORMATION

REEL DIMENSIONS

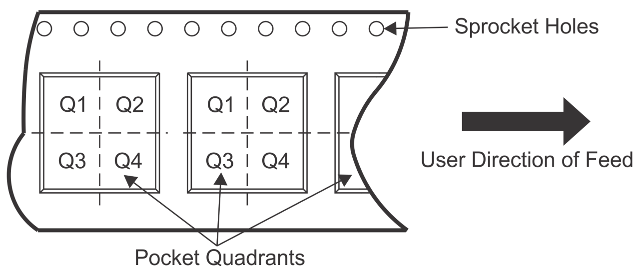


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

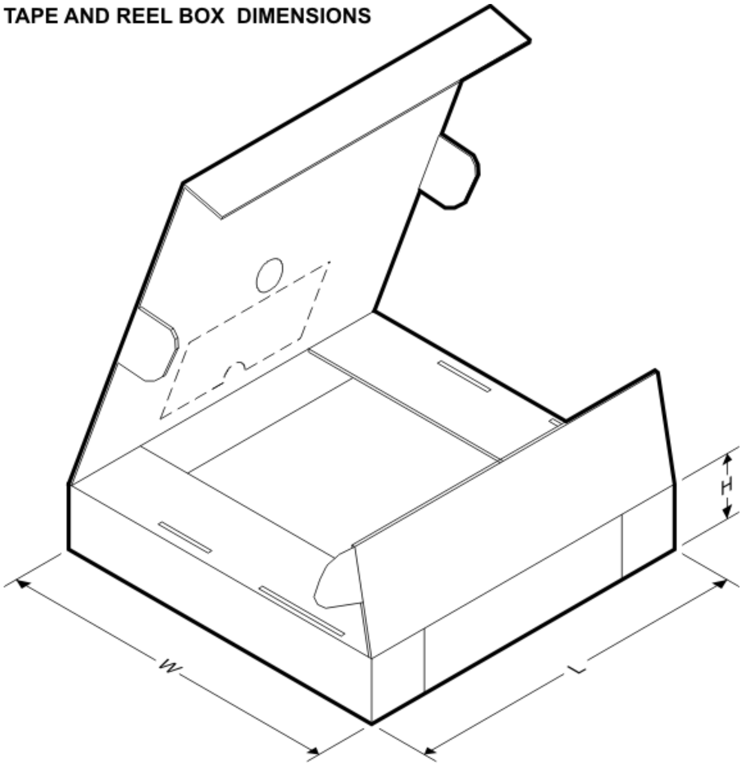
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2835IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2835IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2835IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2835IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA835IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA835IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA835IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA835IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

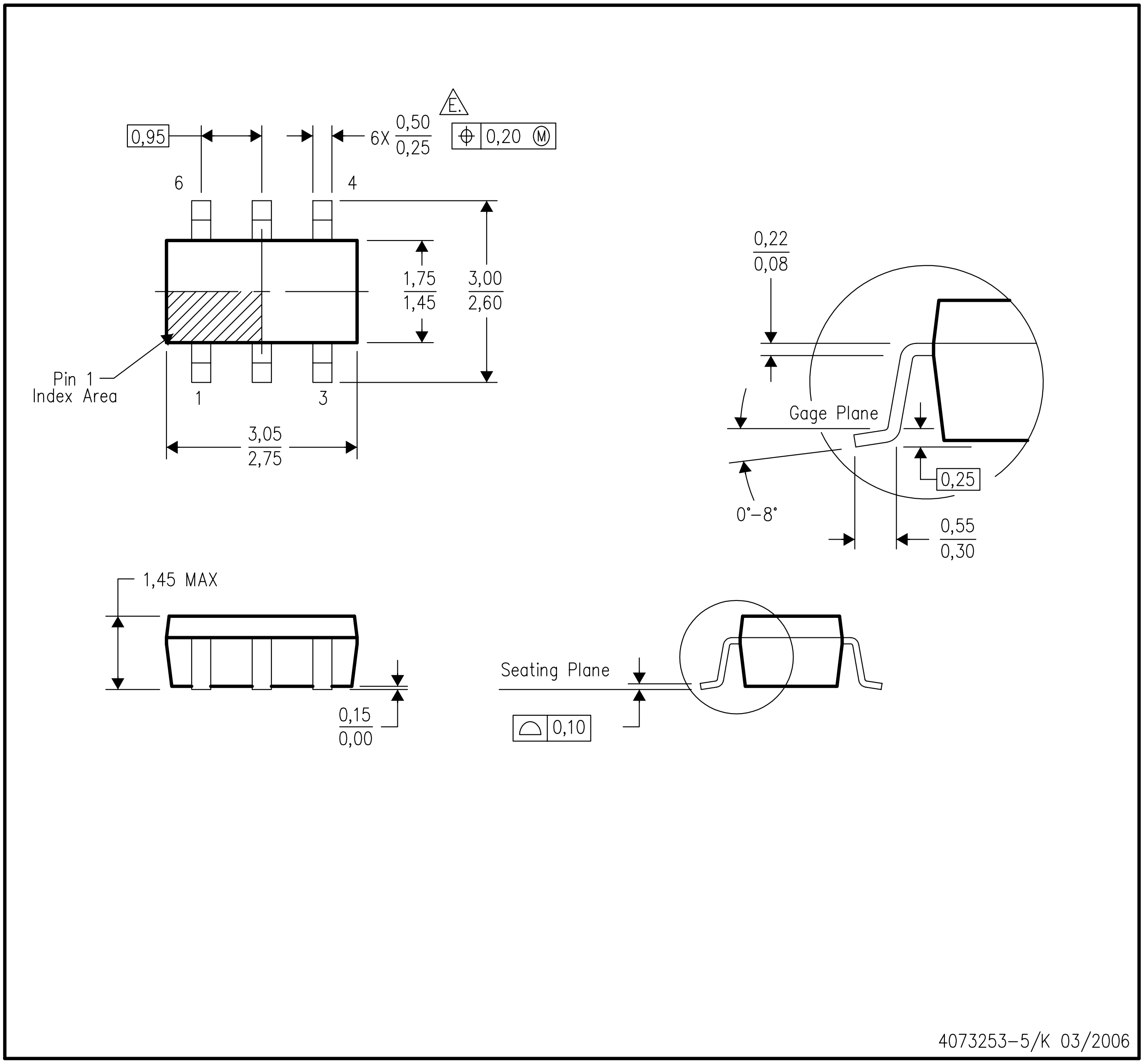
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

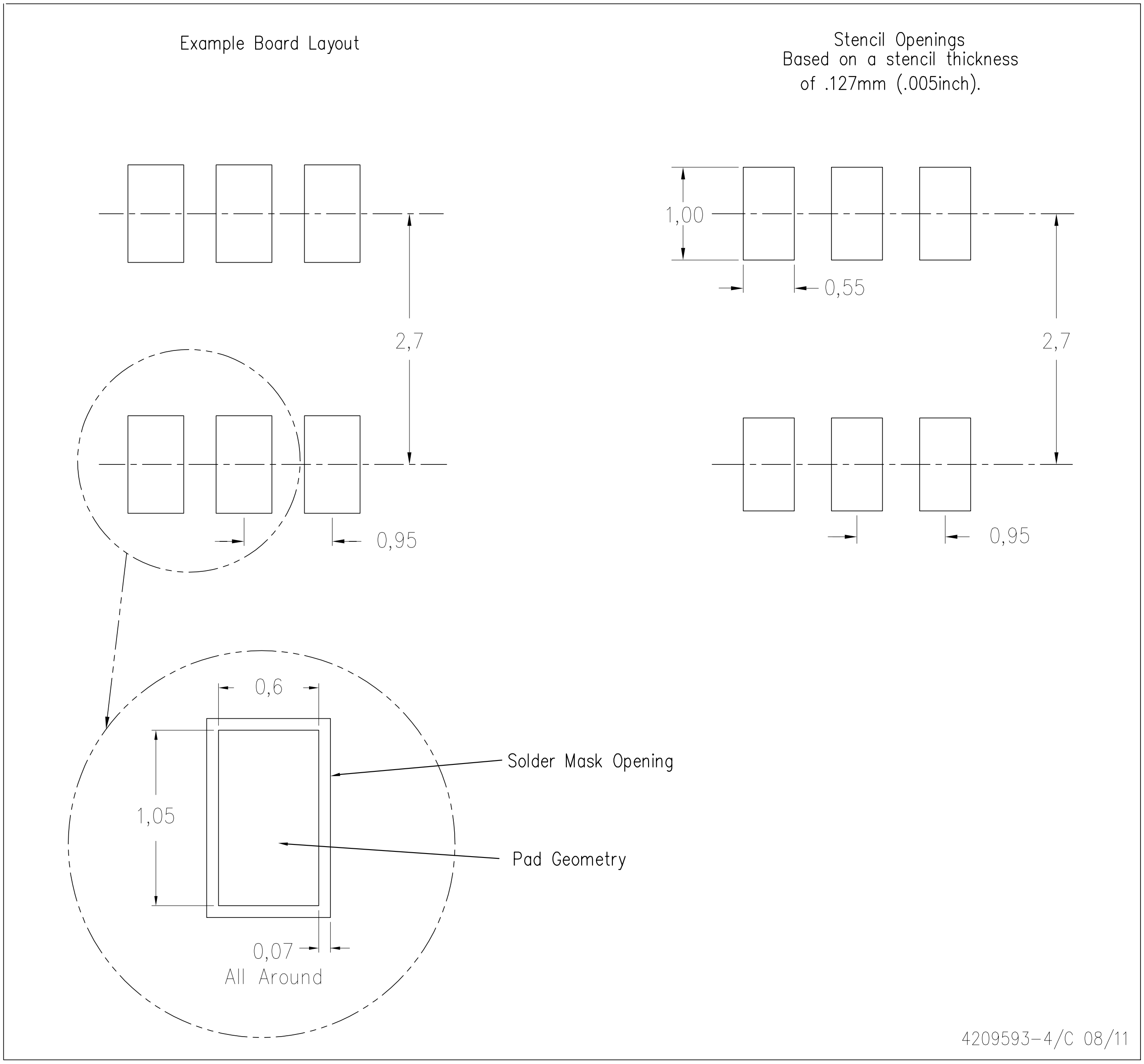
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2835IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
OPA2835IDR	SOIC	D	8	2500	340.5	338.1	20.6
OPA2835IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA2835IRUNT	QFN	RUN	10	250	210.0	185.0	35.0
OPA835IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA835IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA835IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA835IRUNT	QFN	RUN	10	250	210.0	185.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

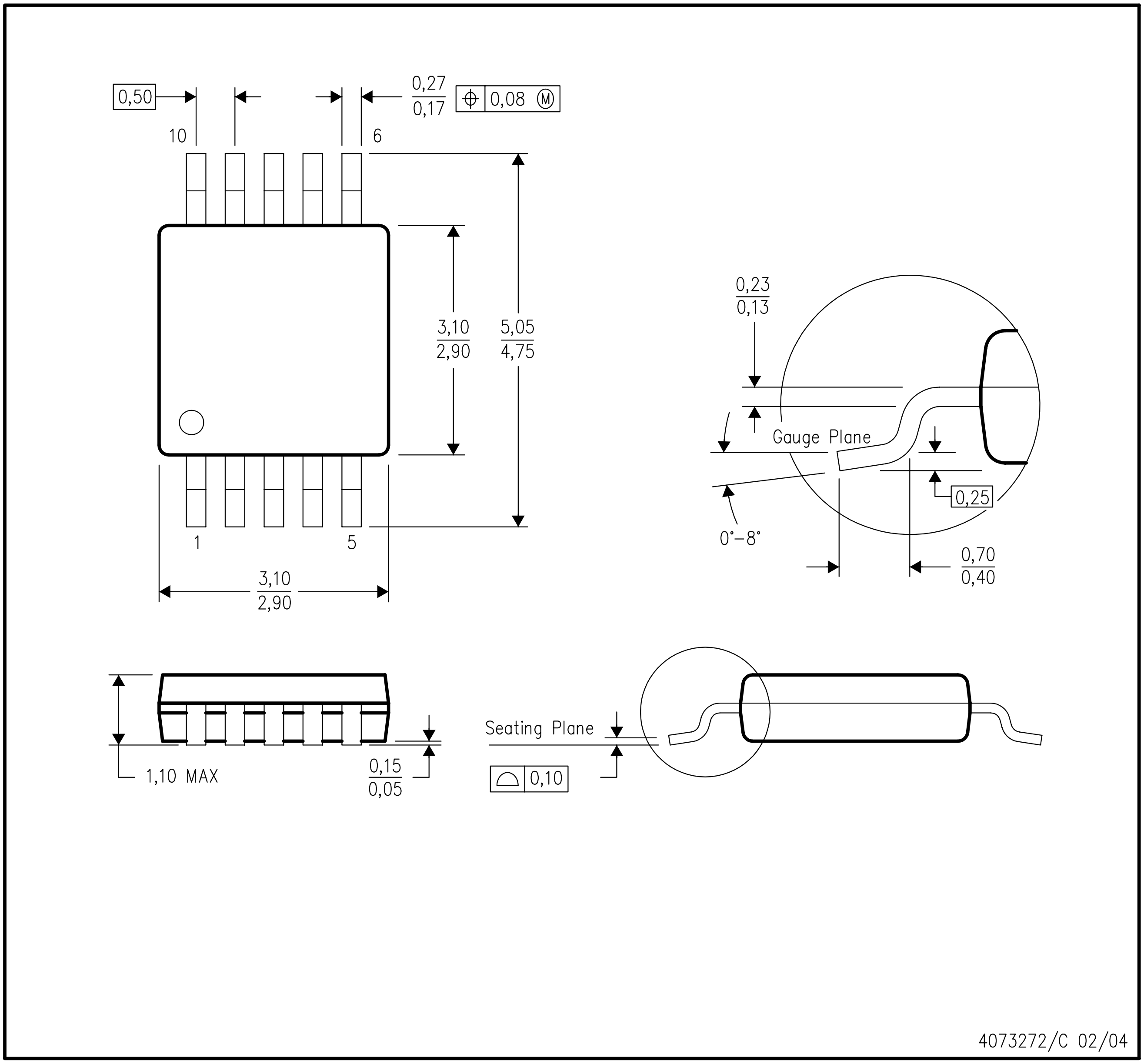
DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:

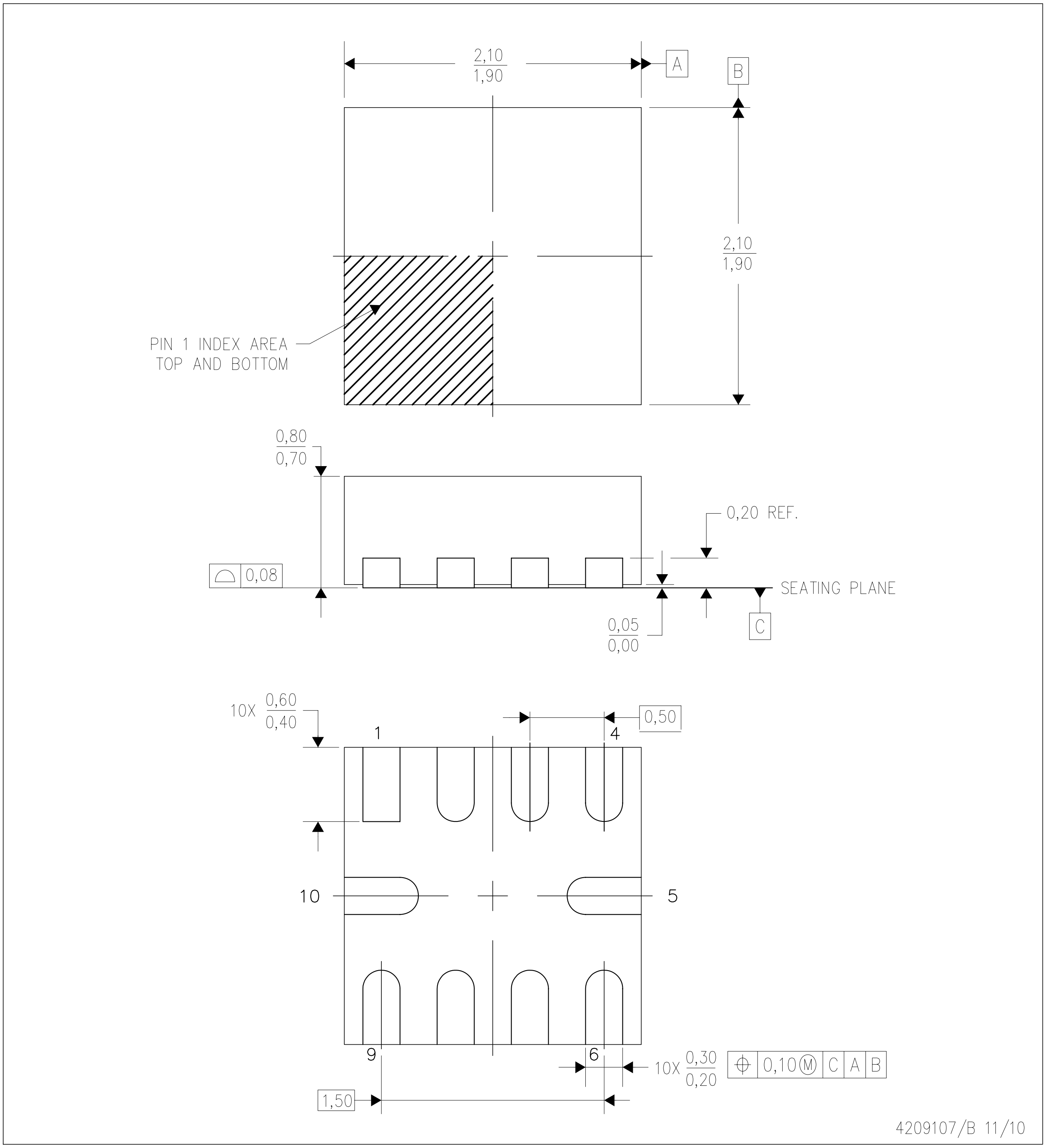
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



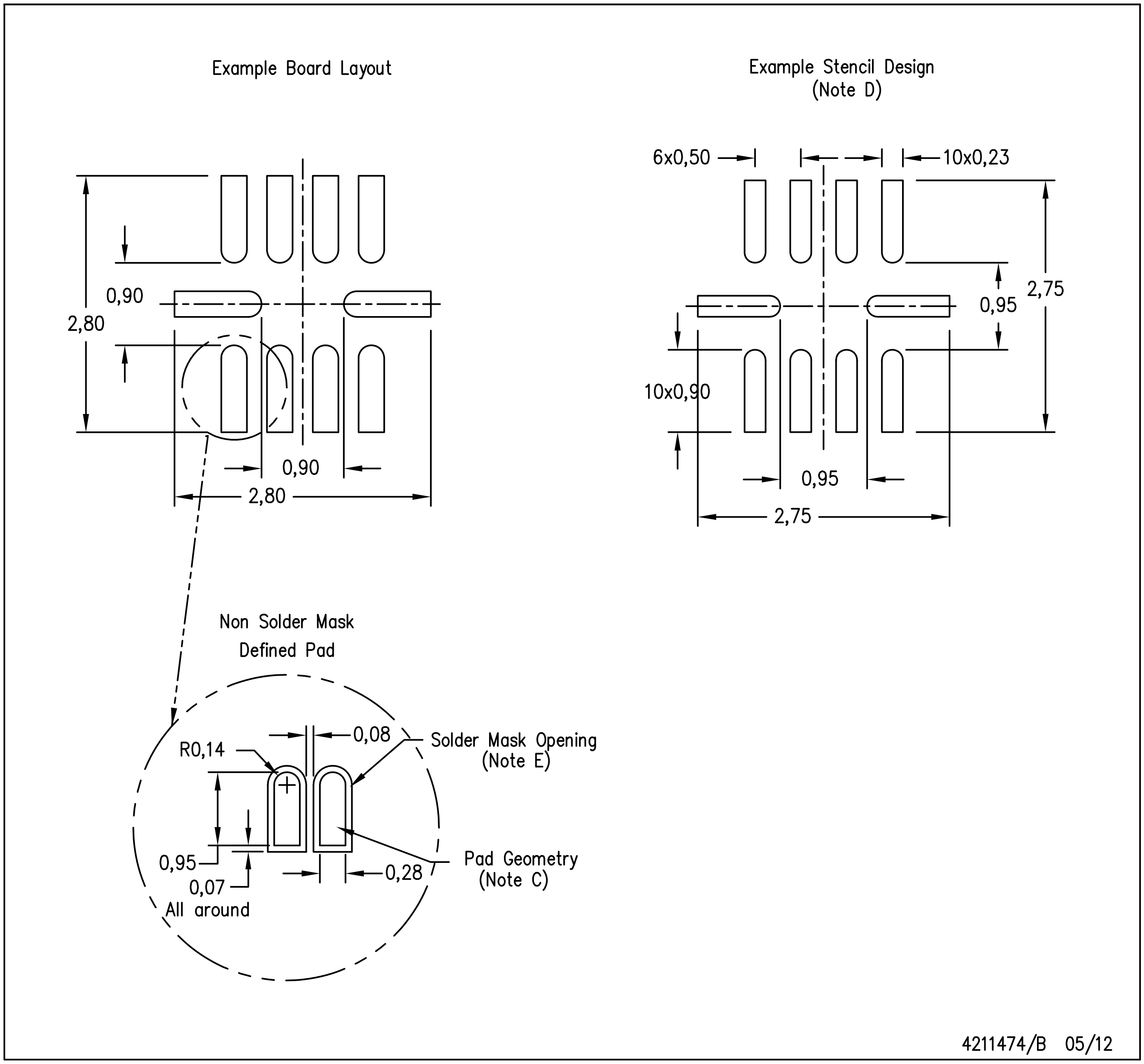
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

RUN (S-PWQFN-N10) PLASTIC QUAD FLATPACK NO-LEAD



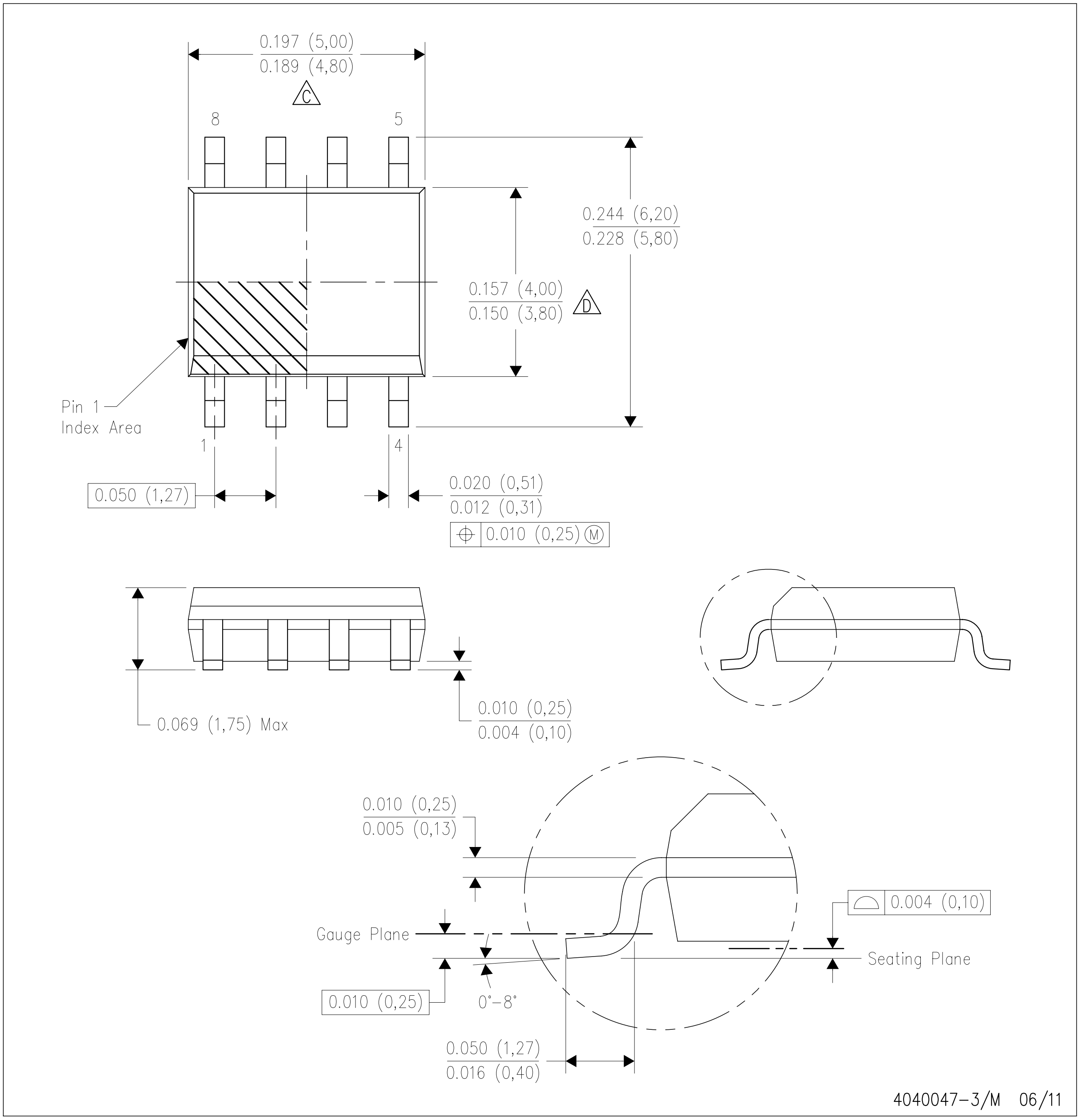
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.

RUN (S-PWQFN-N10) PLASTIC QUAD FLATPACK NO-LEAD



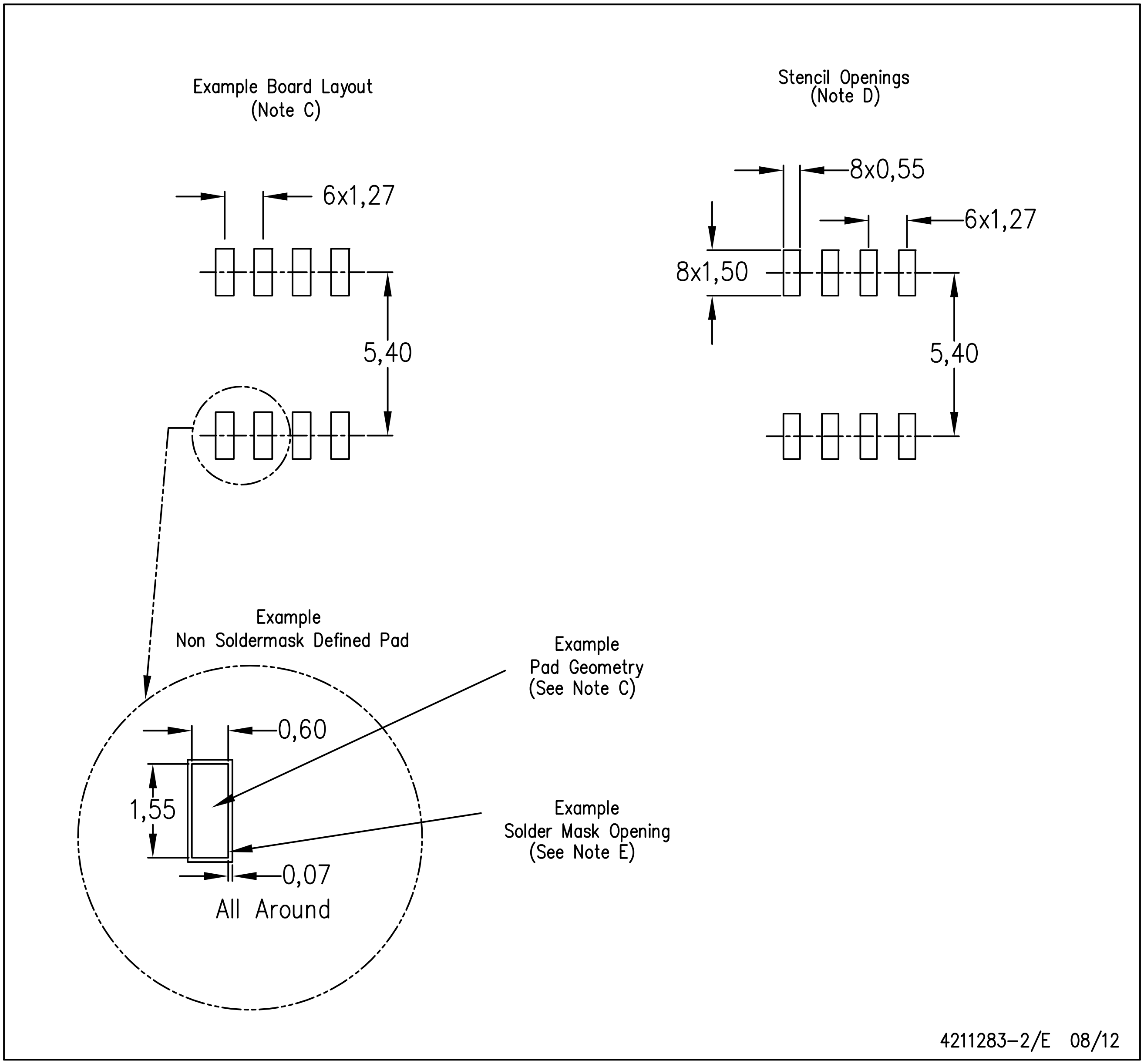
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265