General Purpose I²S Input Class D Amplifier

Check for Samples: TAS5760M

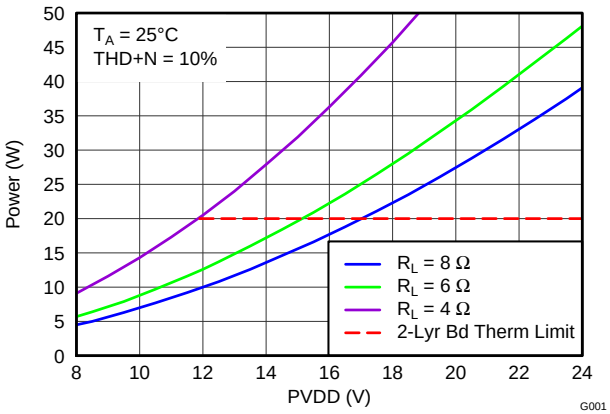
FEATURES

- **Audio I/O Configuration:**
  - **Single Stereo I²S Input**
  - **Stereo Bridge Tied Load (BTL) or Mono Parallel Bridge Tied Load (PBTL) Operation**
  - **32, 44.1, 48, 88.2, 96 kHz Sample Rates**
- **General Operational Features:**
  - **Selectable Hardware or Software Control**
  - **Integrated Digital Output Clipper**
  - **Programmable I²C Address (1101100[R/W] or 1101101[R/W])**
  - **Closed Loop Amplifier Architecture**
  - **Adjustable Switching Frequency for Speaker Amplifier**
- **Robustness Features:**
  - **Clock Error, and Short Circuit Protection**
  - **Programmable Overcurrent and Overtemperature Protection**
- **Audio Performance (PVDD = 19 V, R_{LOAD} = 8 Ω)**
  - **Idle Channel Noise = 100uVrms**
  - **THD+N at 1 W, 1 kHz, = 0.03 %**
  - **SNR = 105 (ref. to 0dBFS)**

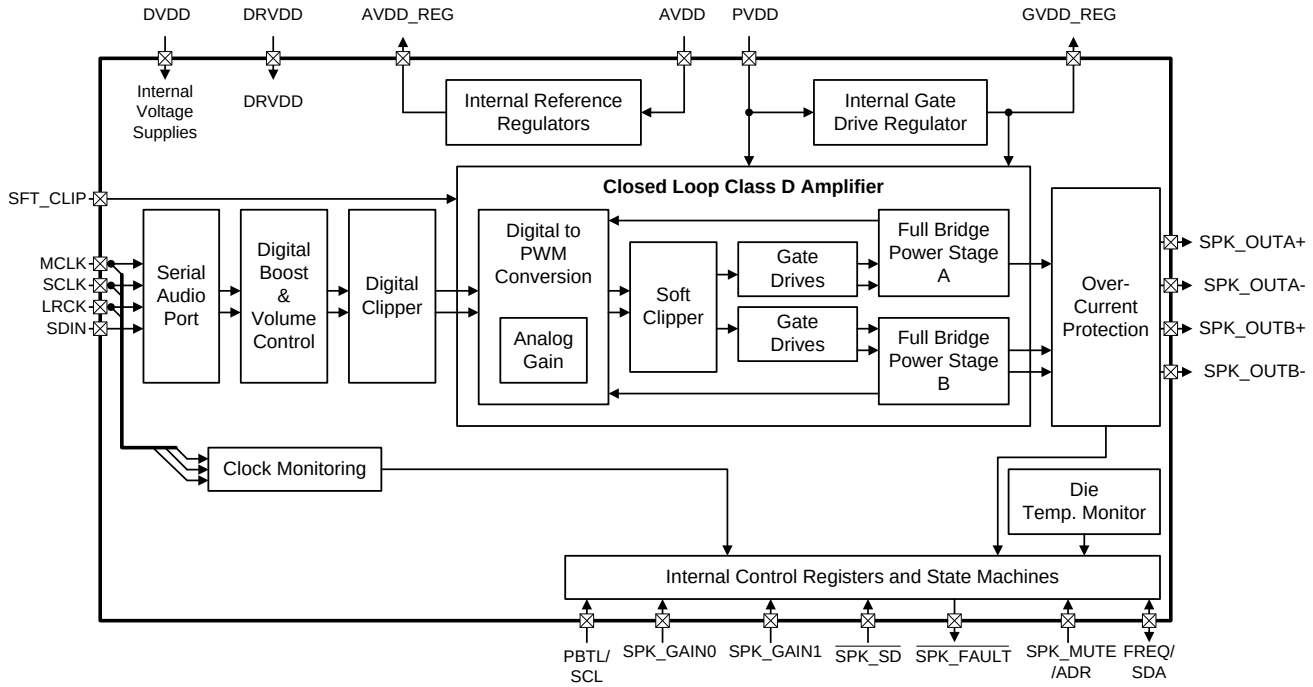
APPLICATIONS

- **LCD/LED TV and Multi-Purpose Monitors**
- **Sound Bars, Docking Stations, PC Audio**
- **General Purpose Audio Equipment**

Power at 10% THD+N vs PVDD



PRODUCT PREVIEW



DESCRIPTION

The TAS5760M is a stereo I^2S input device which includes hardware and software (I^2C) control modes, integrated power limiter, several gain options, and a wide power supply operating range to enable use in a multitude of applications. The TAS5760M operates with a nominal supply voltage from 4.5 to 24 VDC.

An optimal mix of thermal performance and device cost is provided in the 120 mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 48-Pin TSSOP provides excellent operation in the elevated ambient temperatures found in today's modern consumer electronic devices.

The entire TAS5760xx family is pin to pin compatible in the 48-Pin TSSOP package. For systems using the devices in the family that do not have a need for a headphone or line driver amplifier, and which do not require pin to pin compatibility with the devices in the family which do have a headphone or line driver amplifier, an alternate 32-Pin TSSOP is available minimize the total solution size. Additionally, the I^2C register map in all of the TAS5760xx family is identical, to ensure low development overhead to choose between devices based upon system level requirements.

PREVIEW ORDERING INFORMATION

Device	Description	Status	Package
TAS5760MDCA	Flexible, general purpose I²S input class D Amplifier with integrated power limiter, which supports PVDD levels ≤ 24 V	Preview	48 Pin, 0.5mm Lead-Pitch, Pad-down TSSOP (DCA)
TAS5760MDAP		Preview	32 Pin, 0.65mm Lead Pitch, Pad-down TSSOP (DAP)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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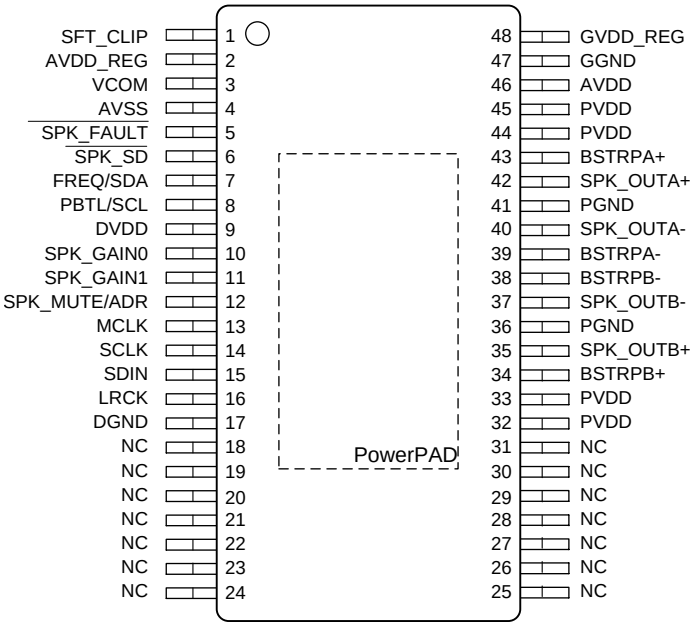
PINOUT AND PIN DESCRIPTIONS

TSSOP PACKAGE
DCA-48
(TOP VIEW)



Pin Descriptions

TAS5760M Name	No.	Type(1)	Internal Termination	Description
AVDD	46	P	-	Power supply for internal analog circuitry
AVDD_REG	2	P	-	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
AVSS	4	P	-	Connection point for internal reference used by AVDD_REG and VCOM filter capacitors
BSTRPA-	39	P	-	Connection point for the SPK_OUTA- bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTA-
BSTRPA+	43	P	-	Connection point for the SPK_OUTA+ bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB-	38	P	-	Connection point for the SPK_OUTB- bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTB-
BSTRPB+	34	P	-	Connection point for the SPK_OUTB+ bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTB+
DGND	17	G	-	Ground reference for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	9	P	-	Power supply for the internal digital circuitry
FREQ/SDA	7	DI	-	Dual function terminal that functions as an I²C data input terminal in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
GGND	47	G	-	Ground reference for gate drive circuitry (this terminal should be connected to the system ground)
GVDD_REG	48	P	-	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCK	16	DI	-	Word select clock for the digital signal that is active on the serial port's input data line

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)

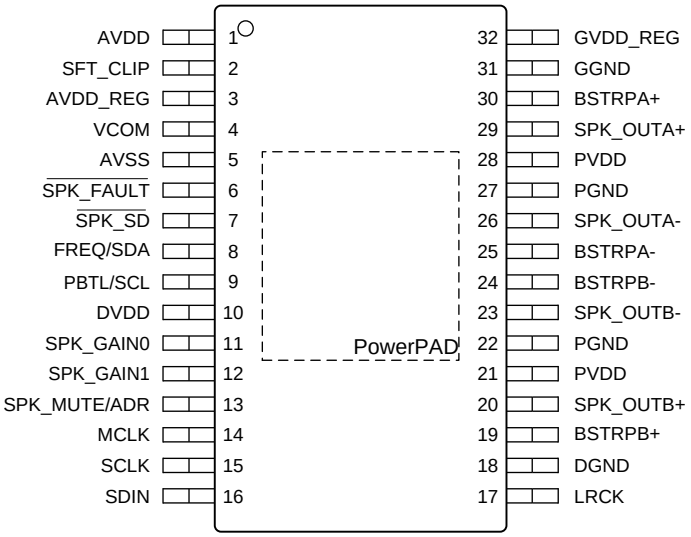
PRODUCT PREVIEW

Pin Descriptions (continued)

TAS5760M Name	No.	Type(1)	Internal Termination	Description
MCLK	13	DI	-	Master clock used for internal clock tree and sub-circuit/state machine clocking
NC	18-31	-	-	Not connected inside the device (all "no connect" terminals should be connected to ground for best thermal performance, however they can be used as routing channels if required.)
PBTL/SCL	8	DI	-	Dual function terminal that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode
PGND	36	G	-	Ground reference for power device circuitry (NOTE: This terminal should be connected to the system ground)
PGND	41	G	-	Ground reference for power device circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	32, 33, 44, 45	P	-	Power Suppy for interal power circuitry
SCLK	14	DI	-	Bit clock for the digital signal that is active on the serial data port's input data line
SDIN	15	DI	-	Data line to the serial data port
SFT_CLIP	1	AI	-	Sets the maximum power before clipping
$\overline{\text{SPK\_FAULT}}$	5	DO	-	Speaker amplifier fault terminal, which is pulled low when an internal fault occurs
SPK_GAIN0	10	DI	-	Adjusts the LSB of the multi-bit gain of the speaker amplifier
SPK_GAIN1	11	DI	-	Adjusts the 2nd LSB of the multi-bit gain of the speaker amplifier
SPK_MUTE/ADR	12	DI	-	Places the speaker amplifier in mute
SPK_OUTA-	40	AO	-	Negative terminal for differential speaker amplifier output "A"
SPK_OUTA+	42	AO	-	Positive terminal for differential speaker amplifier output "A"
SPK_OUTB-	37	AO	-	Negative terminal for differential speaker amplifier output "B"
SPK_OUTB+	35	AO	-	Positive terminal for differential speaker amplifier output "B"
$\overline{\text{SPK\_SD}}$	6	AO	-	Places the speaker amplifier in shutdown
VCOM	3	P	-	Bias voltage for internal PWM conversion block
PowerPAD	-	G	-	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder

PRODUCT PREVIEW

TSSOP PACKAGE
DAP-32
(TOP VIEW)



Pin Descriptions

TAS5760M Name	No.	Type(1)	Internal Termination	Description
AVDD	1	P	-	Power supply for internal analog circuitry
AVDD_REG	3	P	-	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
AVSS	5	P	-	Connection point for internal reference used by AVDD_REG and VCOM filter capacitors
BSTRPA-	25	P	-	Connection point for the SPK_OUTA- bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTA-
BSTRPA+	30	P	-	Connection point for the SPK_OUTA+ bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB-	24	P	-	Connection point for the SPK_OUTB- bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTB-
BSTRPB+	19	P	-	Connection point for the SPK_OUTB+ bootstrap capacitor , which is used to create a power supply for the high-side gate drive for SPK_OUTB+
DGND	18	G	-	Ground reference for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	10	P	-	Power supply for the internal digital circuitry
$\overline{\text{FAULT}}$	6	DO	-	Fault terminal, which is pulled low when an internal fault occurs
FREQ/SDA	8	DI	-	Dual function terminal that functions as an I²C data input terminal in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
GGND	31	G	-	Ground reference for gate drive circuitry (this terminal should be connected to the system ground)
GVDD_REG	32	P	-	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCK	17	DI	-	Word select clock for the digital signal that is active on the serial port's input data line
MCLK	14	DI	-	Master clock used for internal clock tree and sub-circuit/state machine clocking
PBTL/SCL	9	DI	-	Dual function terminal that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)

PRODUCT PREVIEW

Pin Descriptions (continued)

TAS5760M Name	No.	Type(1)	Internal Termination	Description
PGND	22, 27	G	-	Ground reference for power device circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	21, 28	P	-	Power Suppy for interal power circuitry
SCLK	15	DI	-	Bit clock for the digital signal that is active on the serial data port's input data line
$\overline{\text{SPK\_SD}}$	7	DI	-	Places the device in shutdown when pulled low
SDIN	16	DI	-	Data line to the serial data port
SFT_CLIP	2	AI	-	Sets the maximum power before clipping
SPK_GAIN0	11	DI	-	Adjusts the LSB of the multi-bit gain of the speaker amplifier
SPK_GAIN1	12	DI	-	Adjusts the 2nd LSB of the multi-bit gain of the speaker amplifier
SPK_MUTE/ADR	13	DI	-	Places the speaker amplifier in mute, as described in TBD
SPK_OUTA-	26	AO	-	Negative terminal for differential speaker amplifier output "A"
SPK_OUTA+	29	AO	-	Positive terminal for differential speaker amplifier output "A"
SPK_OUTB-	23	AO	-	Negative terminal for differential speaker amplifier output "B"
SPK_OUTB+	20	AO	-	Positive terminal for differential speaker amplifier output "B"
VCOM	4	P	-	Bias voltage for internal PWM conversion block
PowerPAD	-	G	-	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(2)

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
T_A	Ambient Operating Temperature	-25	85	°C
T_S	Ambient Storage Temperature	-40	125	°C
AVDD	AVDD Supply	-0.3	30	V
DVDD	DVDD Supply	-0.3	4.0	V
	DVDD Referenced Digital Inputs	-0.5	DVDD+0.5	V
PVDD	PVDD Supply	-0.3	30	V
SPK_OUTxx	Voltage at speaker output pins	-0.03	32	V

(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Specifications- 48 Pin DCA Package

THERMAL METRIC(1)		TAS5760M 48 Pin DCA JEDEC Standard 2 Layer Board	TAS5760M 48 Pin DCA JEDEC Standard 4 Layer Board	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	60.3	30.2	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	16.0	14.3	°C/W
θ_{JB}	Junction-to-board thermal resistance	12.0	12.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	12.7	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	0.8	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Thermal Specifications- 32 Pin DAP Package

THERMAL METRIC(1)		TAS5760M 32 Pin DAP JEDEC Standard 2 Layer Board	TAS5760M 32 Pin DAP JEDEC Standard 4 Layer Board	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	60.3	31.9	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	16.0	16.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	12.0	17.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	16.8	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	0.8	0.81	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
T_A	Ambient Operating Temperature		-15	-	65	°C
T_S	Ambient Storage Temperature		-	25	-	°C
AVDD	AVDD Supply		4.5	-	26.4	V
DVDD	DVDD Supply		2.8	-	3.63	V
$VIH_{(DR)}$	Input Logic "High" for DVDD Referenced Digital Inputs		-	DVDD	-	V
$VIL_{(DR)}$	Input Logic "Low" for DVDD Referenced Digital Inputs		-	0	-	V
$RLOAD_{(SPK)}$	Minimum Speaker Load in BTL Mode		4	-	-	Ω
$RLOAD_{(SPK)}$	Minimum Speaker Load in PBTL Mode		2	-	-	Ω
PVDD	PVDD Supply		4.5	-	26.4	V

PRODUCT PREVIEW

ELECTRICAL SPECIFICATIONS AND CHARACTERISTICS

DIGITAL I/O PINS

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$\|IIH\|_1$	Input Logic "High" Current Level	All digital pins	-	-	15	µA
VIH_1	Input Logic "High" threshold for DVDD Referenced Digital Inputs	All digital pins	70	-	-	%DVDD
$\|IIL\|_1$	Input Logic "Low" Current Level	All digital pins	-	-	-15	µA
VIL_1	Input Logic "Low" threshold for DVDD Referenced Digital Inputs	All digital pins	-	-	30	%DVDD
VOH	Output Logic "High" Voltage Level	IOH = 2 mA	75	-	-	%DVDD
VOL	Output Logic "Low" Voltage Level	IOH = -2mA	N/A	N/A	25	%DVDD

MASTER CLOCK

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
D_{MCLK}	Allowable MCLK Duty Cycle		45	50	55	%
f_{MCLK}	Supported MCLK Frequencies	Values include: 128, 192, 256, 384, 512.	128	-	512	x f_S

SERIAL AUDIO PORT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
D_{SCLK}	Allowable SCLK Duty Cycle		45	50	55	%
	Required LRCK to SCLK Rising Edge		15	-	-	nS
t_{HLD}	Required SDIN Hold Time after SCLK Rising Edge		15	-	-	nS
t_{su}	Required SDIN Setup Time before SCLK Rising Edge		15	-	-	nS
f_S	Supported Input Sample Rates		32	N/A	96	kHz
f_{SCLK}	Supported SCLK Frequencies		32	N/A	64	x f_S

SPEAKER AMPLIFIER IN ALL MODES

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
AV_{00}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 00	(Hardware Control Mode-additional gain settings available in Software Control Mode)	-	24	-	dBV
AV_{01}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 01	(Hardware Control Mode-additional gain settings available in Software Control Mode)	-	30	-	dBV
AV_{10}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 10	(Hardware Control Mode-additional gain settings available in Software Control Mode)	-	32	-	dBV
AV_{11}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 11	(This setting places the device in Software Control Mode)	-	(Set via I²C)	-	-
$f_{SPK\_AMP(0)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 0	(Hardware Control Mode-additional switching speeds available in Software Control Mode)	-	16	-	x fS
$f_{SPK\_AMP(1)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 1	(Hardware Control Mode-additional switching speeds available in Software Control Mode)	-	8	-	x fS

PRODUCT PREVIEW

SPEAKER AMPLIFIER IN ALL MODES (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
RDS_{ON}	On Resistance of Output Mosfet (both high-side and low-side)	PVDD = 15 V, TA = 25 °C, Die Only	-	120	-	mΩ
		PVDD= 15V, TA = 25 °C, Includes: Die, Bond Wires, Leadframe	-	150	-	mΩ

SPEAKER AMPLIFIER IN STEREO BRIDGE TIED LOAD (BTL) MODE

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$ICN_{(SPK)}$	Idle Channel Noise	PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted	-	92	-	µVrms
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, A-Weighted	-	66	-	µVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, RSPK = 8Ω, A-Weighted	-	186	-	µVrms
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted	-	106	-	µVrms
$Po_{(SPK)}$	Maximum Instantaneous Output Power Per. Ch.	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	14.2	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	55.2	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, THD+N = 0.1%	-	31.8	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, THD+N = 0.1%	-	8	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	33.5	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	20	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	21.9	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	12.5	-	W

PRODUCT PREVIEW

SPEAKER AMPLIFIER IN STEREO BRIDGE TIED LOAD (BTL) MODE (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$Po_{(SPK)}$	Maximum Continuous Output Power Per. Ch.	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	14.2	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	20	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, THD+N = 0.1%	-	20	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, THD+N = 0.1%	-	8	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	20	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	20	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	20	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	12.5	-	W
$SNR_{(SPK)}$	Signal to Noise Ratio (Referenced to 0dBFS Input Signal)	PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB

SPEAKER AMPLIFIER IN STEREO BRIDGE TIED LOAD (BTL) MODE (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, Po = 1 W	-	0.04	-	%
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, Po = 1 W	-	0.03	-	%
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Po = 1 W	-	0.04	-	%
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, Po = 1 W	-	0.03	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, Po = 1 W	-	0.03	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, Po = 1 W	-	0.02	-	%
$X\text{-}Talk_{(SPK)}$	Cross-talk (worst case between LtoR and RtoL coupling)	PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-93	-	dB
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-92	-	dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-93	-	dB
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-94	-	dB

PRODUCT PREVIEW

SPEAKER AMPLIFIER IN MONO PARALLEL BRIDGE TIED LOAD (PBTL) MODE

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
ICN	Idle Channel Noise	PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted	-	100	-	µVrms
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, A-Weighted	-	69	-	µVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, RSPK = 8Ω, A-Weighted	-	189	-	µVrms
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted	-	111	-	µVrms
$Po_{(SPK)}$	Maximum Instantaneous Output Power	PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	65.3	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	16	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	63.5	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, THD+N = 0.1%	-	34.1	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	68.3	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, THD+N = 0.1%	-	8.5	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	39.8	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	21.3	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	44.3	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	24.9	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	13.2	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	28.6	-	W

PRODUCT PREVIEW

SPEAKER AMPLIFIER IN MONO PARALLEL BRIDGE TIED LOAD (PBTL) MODE (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$Po_{(SPK)}$	Maximum Continuous Output Power	PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	16	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, THD+N = 0.1%	-	40	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, THD+N = 0.1%	-	8.5	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	40	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, THD+N = 0.1%	-	13.2	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 2Ω, THD+N = 0.1%, Unless otherwise noted	-	40	-	W
SNR	Signal to Noise Ratio (Referenced to 0dBFS Input Signal)	PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, A-Weighted, -60dBFS Input	-	105	-	dB

PRODUCT PREVIEW

SPEAKER AMPLIFIER IN MONO PARALLEL BRIDGE TIED LOAD (PBTL) MODE (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, RSPK = 8Ω, Po = 1 W	-	0.02	-	%
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, RSPK = 8Ω, Po = 1 W	-	0.03	-	%
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 19 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, RSPK = 8Ω, Po = 1 W	-	0.02	-	%

PRODUCT PREVIEW

I²C CONTROL PORT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
$C_{L(I^2C)}$	Allowable Load Capacitance for Each I²C Line		-	-	400	pF
f_{SCL}	Support SCL frequency	No Wait States	100	-	400	kHz
t_{buf}	Bus Free time between stop and start conditions		1.3	-	-	µS
$t_{f(I^2C)}$	Rise Time, SCL and SDA		-	-	300	nS
$t_{h1(I^2C)}$	Hold Time, SCL to SDA		0	-	-	nS
$t_{h2(I^2C)}$	Hold Time, start condition to SCL		0.6	-	-	uS
$t_{I^2C(start)}$	I²C Startup Time		-	-	12	mS
$t_{r(I^2C)}$	Rise Time, SCL and SDA		-	-	300	nS
$t_{su1(I^2C)}$	Setup Time, SDA to SCL		100	-	-	nS
$t_{su2(I^2C)}$	Setup Time, SCL to start condition		0.6	-	-	µS
$t_{su3(I^2C)}$	Setup Time, SCL to stop condition		0.6	-	-	µS
$T_{w(H)}$	Required Pulse Duration, SCL High		0.6	-	-	µS

I²C CONTROL PORT (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
$T_{w(L)}$	Required Pulse Duration, SCL Low		1.3	-	-	µS

TYPICAL PERFORMANCE CHARACTERISTICS (BTL Mode)

At T_A = 25°C, unless otherwise noted.

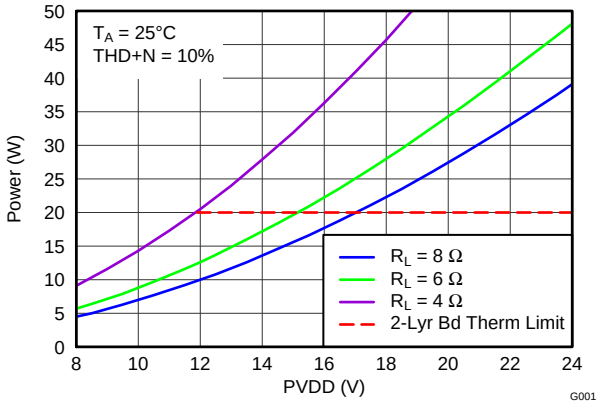


Figure 1. Output Power vs PVDD (2 Bridge Tied Loads (BTL))

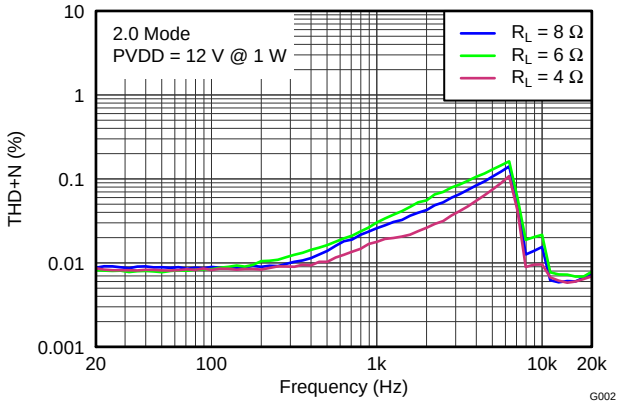


Figure 2. THD+N vs Frequency in 2.0 Mode with PVDD = 12 V @ 1 W

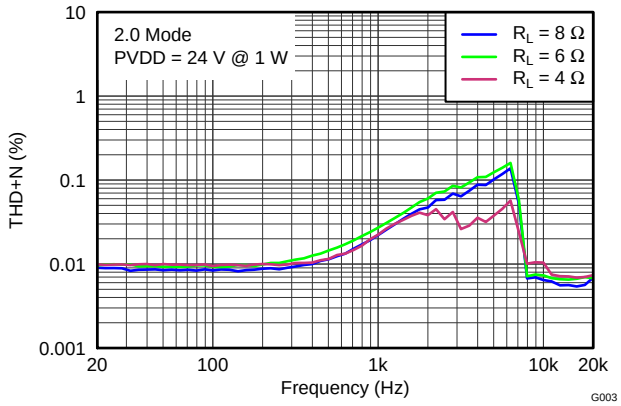


Figure 3. THD+N vs Frequency in 2.0 Mode with PVDD = 24 V @ 1 W

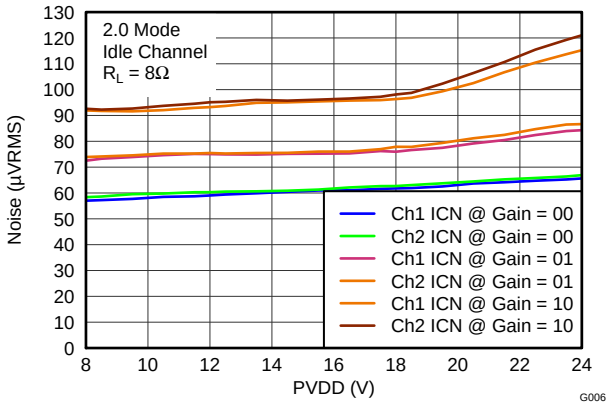


Figure 4. 2.0 Idle Channel Noise vs PVDD

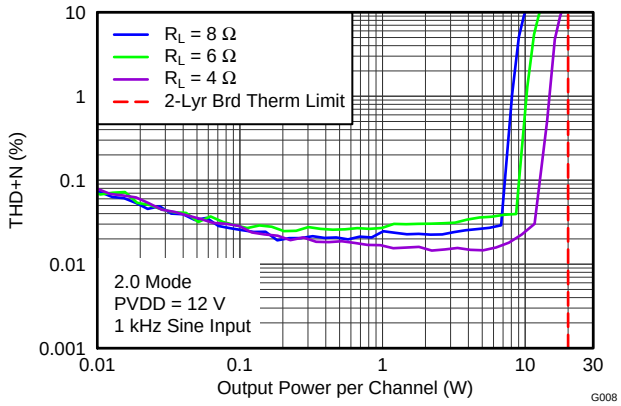


Figure 5. THD+N vs Output Power in 2.0 Mode with PVDD = 12 V with 1 kHz Sine Input, Both Channels Driven

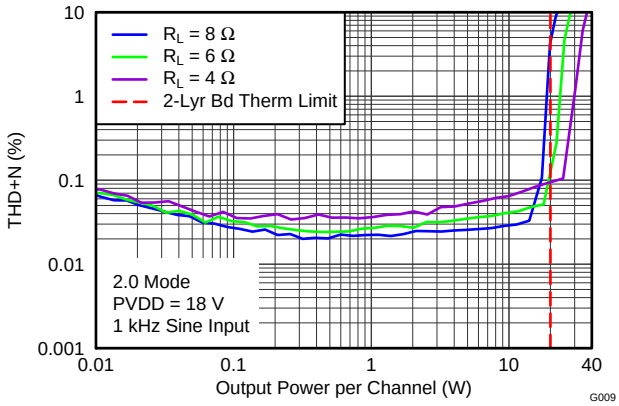


Figure 6. THD+N vs Output Power in 2.0 Mode with PVDD = 18 V with 1 kHz Sine Input, Both Channels Driven

PRODUCT PREVIEW

TYPICAL PERFORMANCE CHARACTERISTICS (BTL Mode) (continued)

At T_A = 25°C, unless otherwise noted.

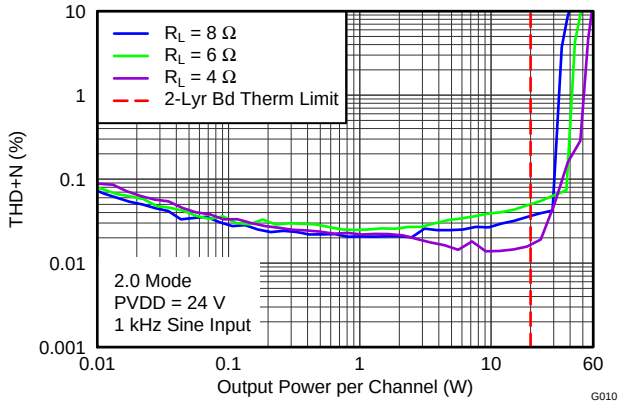


Figure 7. THD+N vs Output Power in 2.0 Mode with PVDD = 24 V with 1 kHz Sine Input, Both Channels Driven

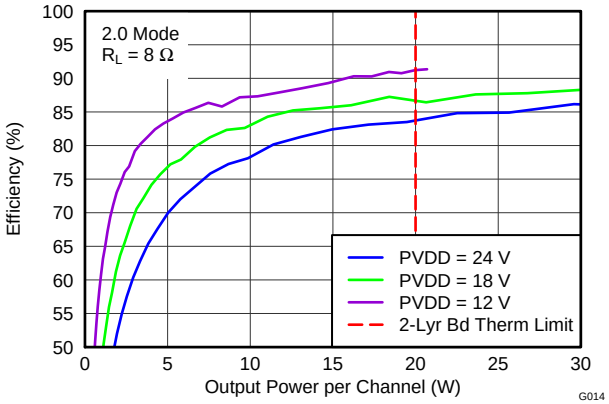


Figure 8. 2.0 Efficiency vs Output Power

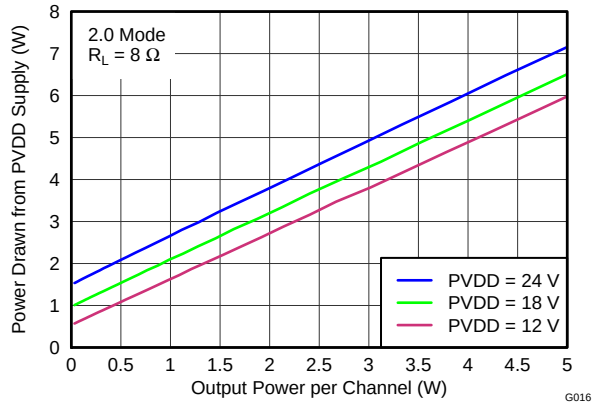


Figure 9. 2.0 Power In vs Output Power

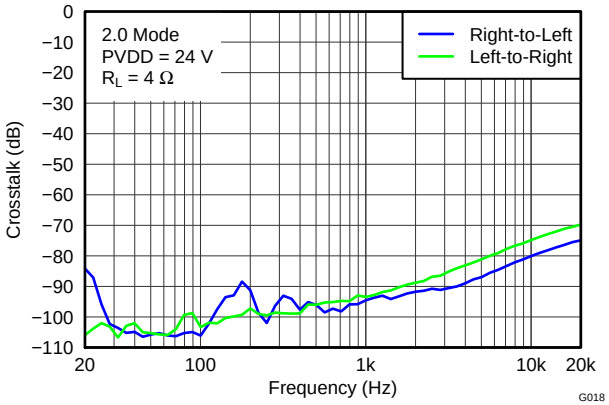


Figure 10. 2.0 X-Talk vs Frequency

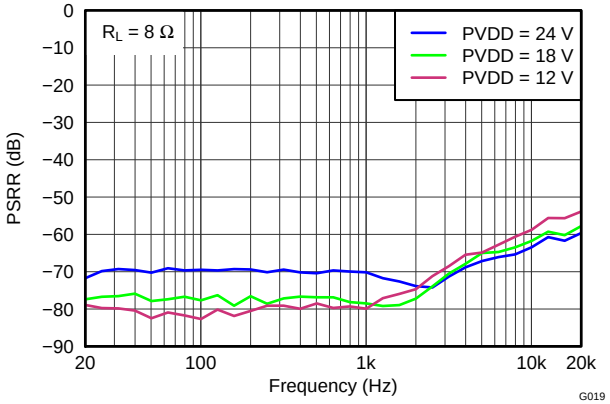


Figure 11. PVDD PSRR vs Frequency

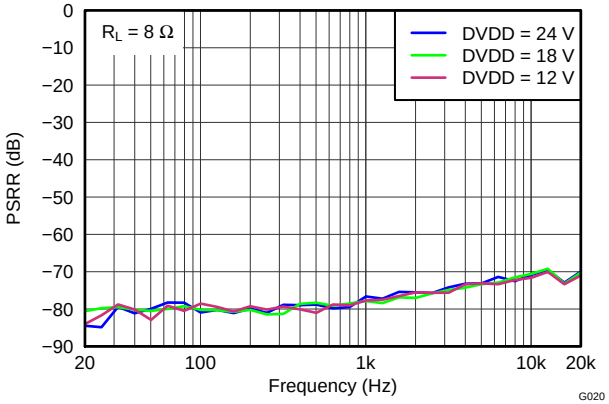


Figure 12. DVDD PSRR vs Frequency

PRODUCT PREVIEW

TYPICAL PERFORMANCE CHARACTERISTICS (BTL Mode) (continued)

At T_A = 25°C, unless otherwise noted.

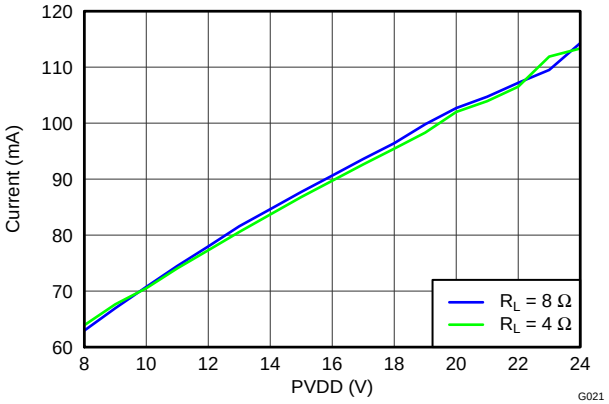


Figure 13. Filterless Idle Current Draw vs PVDD

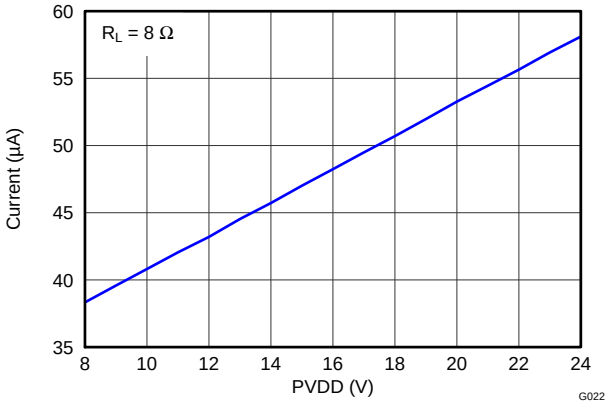


Figure 14. Filterless Shutdown Current Draw vs PVDD

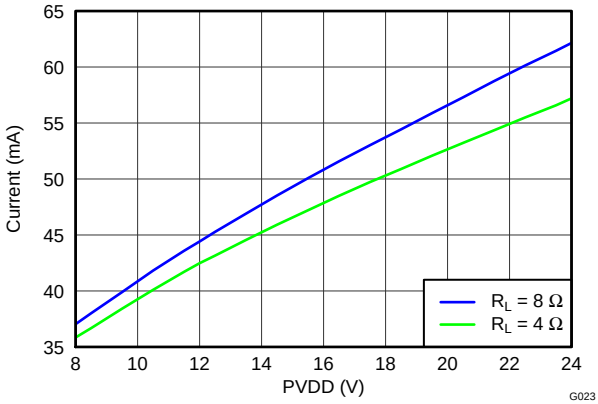


Figure 15. Idle Current Draw (with Filter) vs PVDD

PRODUCT PREVIEW

TYPICAL PERFORMANCE CHARACTERISTICS (PBTL Mode)

At T_A = 25°C, unless otherwise noted.

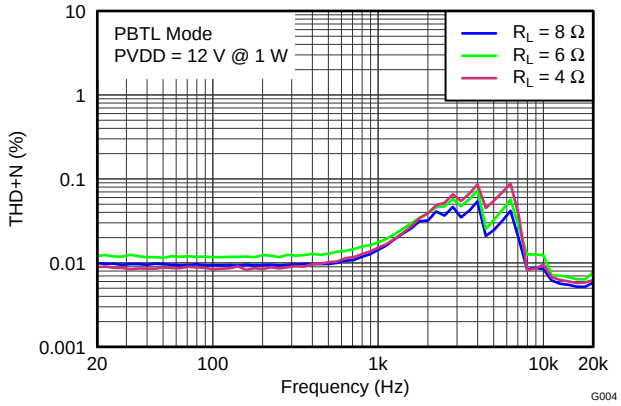


Figure 16. THD+N vs Frequency in PBTL Mode with PVDD = 12 V @ 1 W

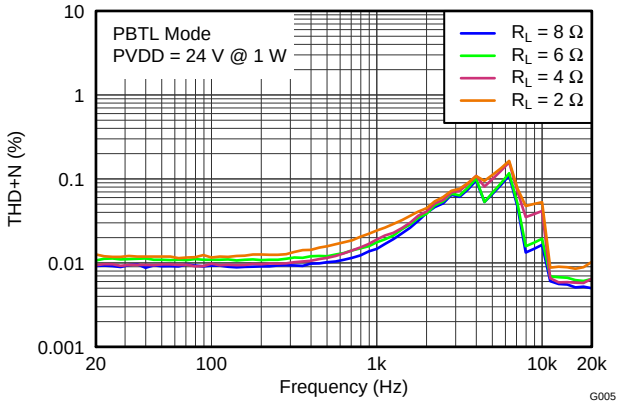


Figure 17. THD+N vs Frequency in PBTL Mode with PVDD = 24 V @ 1 W

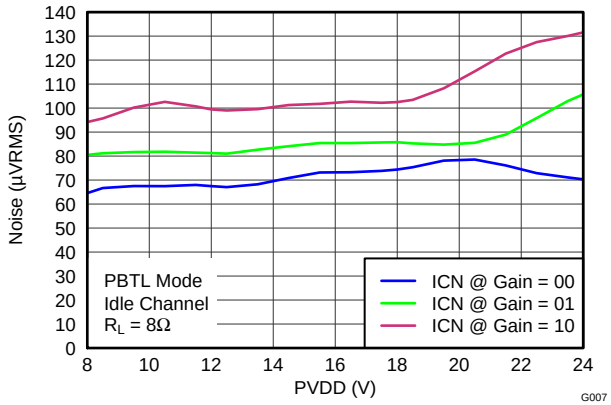


Figure 18. PBTL Idle Channel Noise vs PVDD

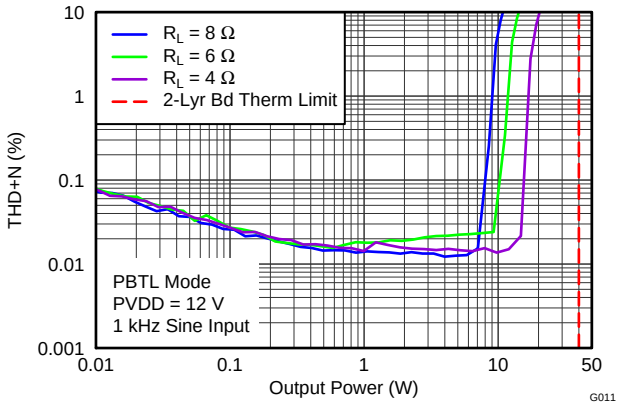


Figure 19. THD+N vs Output Power in PBTL with PVDD = 12 V with 1 kHz Sine Input

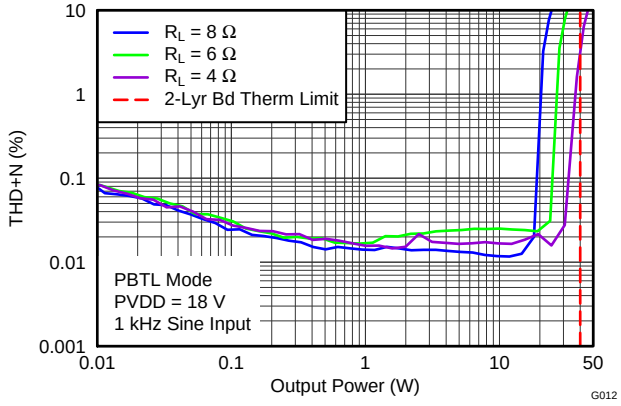


Figure 20. THD+N vs Output Power in PBTL with PVDD = 18 V with 1 kHz Sine Input

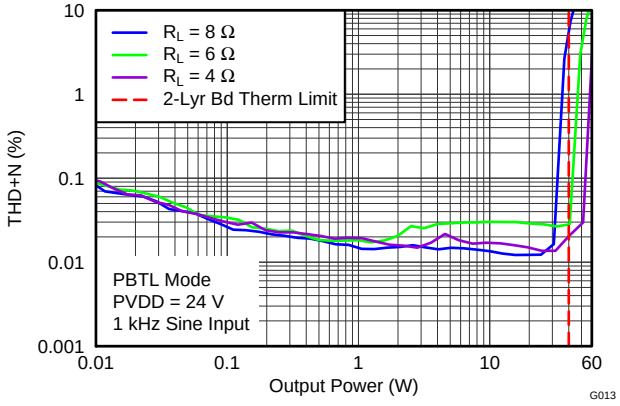


Figure 21. THD+N vs Output Power in PBTL with PVDD = 24 V with 1 kHz Sine Input

PRODUCT PREVIEW

TYPICAL PERFORMANCE CHARACTERISTICS (PBTL Mode) (continued)

At T_A = 25°C, unless otherwise noted.

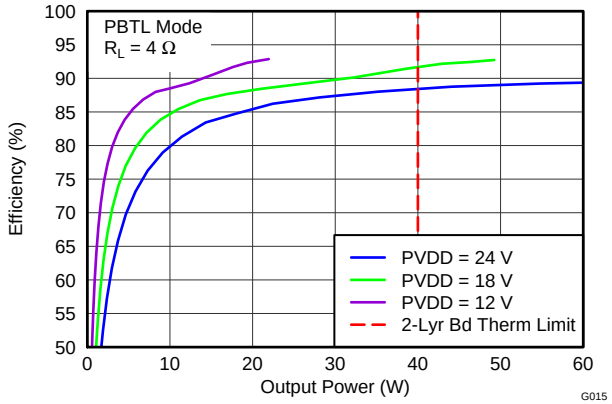


Figure 22. PBTL Efficiency vs Output Power

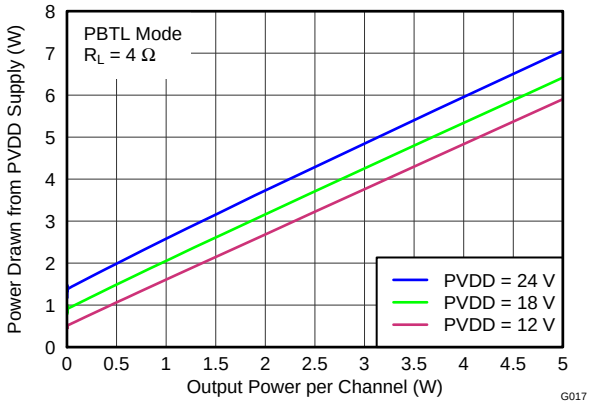


Figure 23. PBTL Power In vs Output Power

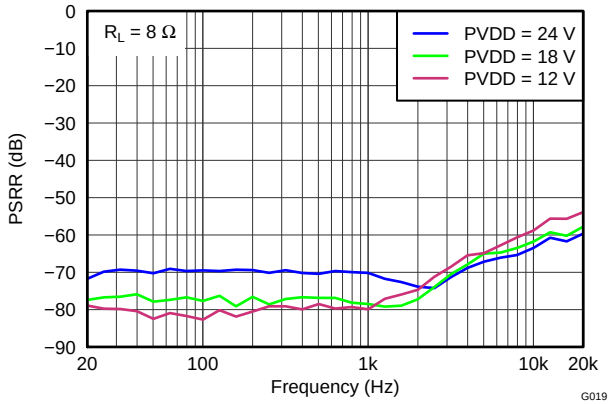


Figure 24. PVDD PSRR vs Frequency

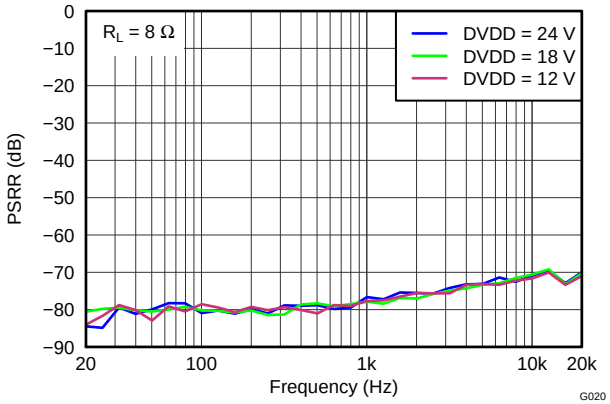


Figure 25. DVDD PSRR vs Frequency

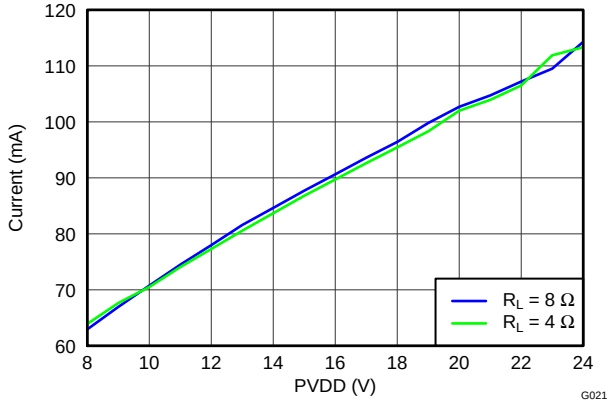


Figure 26. Filterless Idle Current Draw vs PVDD

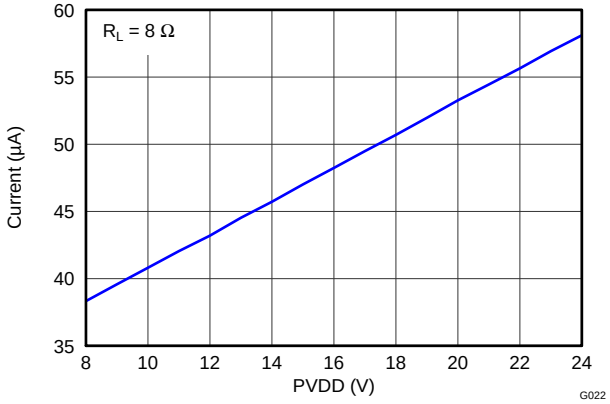


Figure 27. Filterless Shutdown Current Draw vs PVDD

PRODUCT PREVIEW

TYPICAL PERFORMANCE CHARACTERISTICS (PBTL Mode) (continued)

At T_A = 25°C, unless otherwise noted.

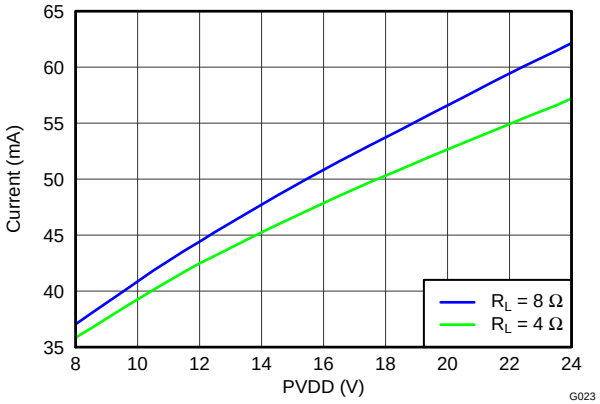


Figure 28. Idle Current Draw (with Filter) vs PVDD

PRODUCT PREVIEW

Theory of Operation and Detailed Description

Device Overview and Summary

The TAS5760Mis an flexible and easy to use stereo Class D speaker amplifier with an I²S input serial audio port. The TAS5760M supports a variety of audio clock configurations via two speed modes. In hardware control mode, the device only operates in single-speed mode. When used in software control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2kHz and 96kHz. The outputs of the TAS5760Mcan be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

Only two power supplies are required for the TAS5760M- a 3.3V power supply for the low-voltage analog and digital and a higher voltage power supply, called PVDD, for the output stage of the speaker amplifier. To enable use in a variety of applications, PVDD can operated over a large range of voltages, as specified in the Recommended Operating Conditions table.

To configure and control the TAS5760M, two methods of control are available. In Hardware Control Mode, the configuration and real-time control of the device is accomplished through hardware control pins. In software control mode, the I²C control port is used both to configure the device and for real-time control. In software mode control, several of the hardware control pins remain functional, such as the SPK_SD, SPK_FAULT, and SFT_CLIP pins.

Hardware Control Mode

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the TAS5760M can be used in hardware mode control.. In this mode of operation, the device operates in its default configuration and any changes to the device are accomplished via the hardware control pins, described below. The audio performance between hardware and software control mode is identical, how every more features and more functionality are available when the device is operated in software control mode. The behavior of these hardware mode control pins is described in the sections below.

Power Supplies

The power supply requirements for the TAS5760M consists of one low-voltage supply to power the low voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-board regulators are included on the TAS5760M to generate the voltages necessary for the internal circuitry of the audio path. The power supply distribution scheme is shown in the diagram below. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. External circuitry must not be connected to these regulator outputs, or reduced performance of and even damage to the device may occur.

Serial Audio Port in Hardware Control Mode

When used in Hardware Control Mode, the Serial Audio Port (SAP) accepts only I²S formatted data. Additionally, the device operates in SSM, which means that supported sample rates, MCLK rates, and SCLK rates are limited to those shown in the table below. More clocking options, including higher sample rates, are available when operating the device in Software Control Mode.

The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 1. Supported SCLK Rates in Single Speed Mode

	MCLK Rate [x f_S]				
	128	192	256	384	512

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Table 1. Supported SCLK Rates in Single Speed Mode (continued)

Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 64	32, 48, 64	32, 64
	44.1	32, 48, 64	32, 48, 64	32, 64	32, 48, 64	32, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 64

Soft Clipper Control (SFT_CLIP Pin)

The TAS5760M has a soft clipper that can be used to clip the output voltage level below the supply rail. When this circuit is active, the amplifier operates as if it was powered by a lower supply voltage, and thereby enters into clipping sooner than if the circuit wasn't active. The point at which clipping begins is controlled by a resistor divider from GVDD_REG to ground, which sets the voltage at the SFT_CLIP pin. The precision of the threshold at which clipping occurs is dependent upon the voltage level at the SFT_CLIP pin. Because of this, increasing the precision of the resistors used to create the voltage divider, or using an external reference will increase the precision of the point at which the device enters into clipping. To ensure stability, and soften the edges of the clipping event, a capacitor should be connected from pin SFT_CLIP to ground.

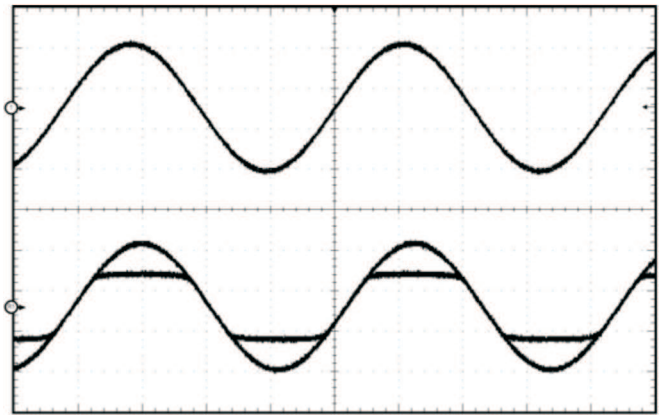

Figure 29. Soft Clipper Example Wave Form

To move the output stage into clipping, the soft clipper circuit limits the duty cycle of the output PWM pulses to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is approximately 4 times the voltage at the SFT_CLIP pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

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$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \text{ for unclipped power} \quad (1)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ SFT_CLIP voltage if SFT_CLIP $< 4 \times V_P$
P_{OUT} (10%THD) $\approx 1.25 \times P_{OUT}$ (unclipped)

Table 2. Soft Clipper Example

PVDD [V]	SFT_CLIP Pin Voltage [V](1)	Resistor to GND [kΩ]	Resistor to GVDD [kΩ]	Output Voltage [V_{rms}]
24	GVDD	0	(Open)	17.90
24	3.3	45	51	12.67
24	2.25	24	51	9.00
12	GVDD	0	(Open)	10.33
12	2.25	24	51	9.00
12	1.5	18	68	6.30

(1) Output voltage measurements taken with EVM gain set to TBD dB and input signal set to 0 dBFS.

Speaker Amplifier Fault Notification ($\overline{\text{SPK\_FAULT}}$ Pin)

In hardware control mode, the $\overline{\text{SPK\_FAULT}}$ pin of the TAS5760M serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier. This pin is an open drain output pin and has an external pull-up resistor to the DVDD rail, ensuring no external resistor is needed to pull the pin high when it is not being driven by a fault condition. In hardware mode, the behavior of this pin varies based upon the type of error which has occurred. In the case of a latching error, such as an Over-Temperature Error (OTE) event, the fault line will remain low until such time that the TAS5760M has resumed normal operation (i.e. the device has cooled down sufficiently to resume normal operation). Conversely, a non-latching error such an Over-Current Error (OCE) event, will result in the pin only being pulled low while the fault is active.

Speaker Amplifier Shut Down ($\overline{\text{SPK\_SD}}$ Pin)

In hardware control mode, the $\overline{\text{SPK\_SD}}$ pin is provided to place the speaker amplifier into shutdown. Pulling this pin low will place the device into shutdown, while pulling it high (DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into mute, by pulling the SPK_MUTE/ADR pin high before pulling the $\overline{\text{SPK\_SD}}$ low.

Speaker Amplifier Switching Frequency Select (FREQ/SDA Pin)

In hardware control mode, the output frequency of the TAS5760M is configurable via the FREQ/SDA pin. This pin sets the output switching frequency of the PWM output signal of the speaker amplifier. When connected to the system ground, the pin sets the output switching frequency to 16 * f_S. When connected to DVDD, the pin sets the output switching frequency to 8 * f_S. More switching frequencies are available when the TAS5760M is used in software mode control.

Parallel Bridge Tied Load Mode Select (PBTL/SCL Pin)

The TAS5760M can be configured to combine both the left and the right channels into a single channel which can be used to drive a single speaker. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode, after the load configuration. In order to place the TAS5760M into PBTL Mode, the PBTL/SCL pin should be pulled high (i.e. connected to the DVDD supply). If the device is to operate in BTL mode instead, the PBTL/SCL pin should be pulled low, i.e. connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

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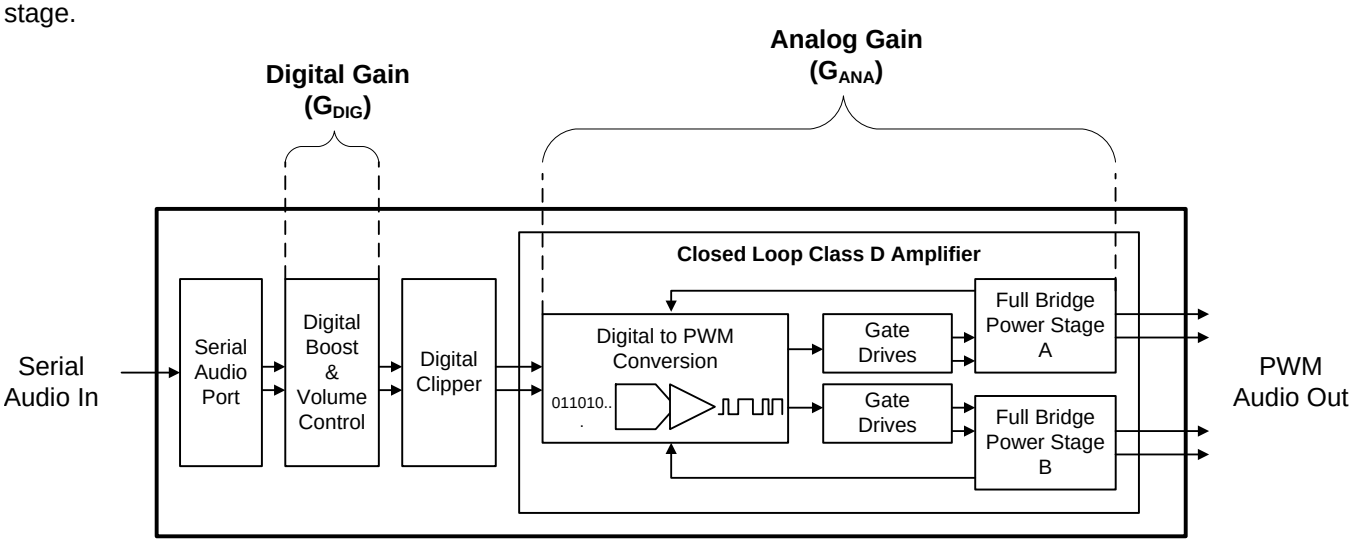
Speaker Amplifier Mute Enable (SPK_MUTE/ADR Pin)

In hardware control mode, pulling the the SPK_MUTE/ADR pin high transitions the switching of the output devices to a high-z (i.e. non-switching) state. It is recommended to mute the device before stopping the audio signal coming in on the SDIN line or before bringing down the power supplies connected to the TAS5760M. When placed in software control mode, the SPK_MUTE/ADR pin serves as an address pin for the I²C control port. This is described in TBD.

Speaker Amplifier Gain Select (SPK_GAIN [1:0] Pins)

In hardware mode control, a combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. The decode of of the two pins "SPK_GAIN1" and "SPK_GAIN0" sets the gain of the speaker amplifier. Additionally, pulling both of the SPK_GAIN[1:0] pins high places the device into software control mode.

As seen in the figure below, the audio path of the consists of a digital audio input port, a digital audio path, a digital to PWM converter, a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the analog modulator to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.



As shown above, the the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default and, in hardware control mode, it does not change. Manipulation of the GAIN[1:0] pins does, however, change the setting of the digtial boost block, in addition to the analog gain.

The three gain configurations provided in hardware control mode were chosen to align with 3 popular power supply levels found in many consumer electronics and to balance the trade-off between power output and noise performance. These gain settings ensure that the output signal can be driven into clipping at those three PVDD levels. If the power level required is lower than that which is possible with the PVDD level, a lower gain setting can be used. Additionally, if clipping at a level lower than the PVDD supply is desired, the digital clipper or soft clipper can be used.

The values of G_{DIG} and G_{ANA} for each of the GAIN[1:0] settings are shown in the table below. Additionally, the recommended PVDD level for each gain setting, along with the typical unclipped peak to peak output voltage swing for a 0dBFS input signal is provided.

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Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760M. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason it may be necessary to limit the voltage swing of the amplifier via a lower gain setting in order to reduce the voltage presented, and therefore the power delivered, to the speaker.

Recommendations for Setting the Speaker Amplifier Gain Structure in Hardware Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest gain setting via the GAIN[1:0] pins thatwill produce an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the gain setting.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the gain.
5. Repeat Step 4 above until the optimum balance of power, noise, and clipping behavior is achieved.

Error Handling in Hardware Control Mode

The TAS5760M includes a robust error handling suite to protect against clock errors, under and over-voltage errors, over-temperature errors, output DC errors, and over-current errors. In hardware control mode, all of these errors are “OR-ed” into a single fault which is used to drive the SPK_FAULT pin when an error occurs. Some of the errors are “latching” errors, which means that the SPK_SD pin must be toggled in order to clear the error and resume normal operation of the device. The other errors are “non-latching” errors, which means that once the error which has occurred stops, the fault will be cleared and the device will automatically resume normal operation. The table below outlines the latching or non-latching behavior of each of the errors. One technique to ensure that operation of the device continues even after a latching type error occurs is to connect the SPK_FAULT pin to the SPK_SD pin. In this way, any fault which occurs will reset the device and the device will attempt to resume operation after the SPK_SD pin is toggled. It should be noted that, if the error is still present after the device resets itself, the device will begin to toggle on and off as it attempts to clear the error. This will produce audible artifacts on the speaker outputs.

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Software Control Mode

Power Supplies

The power supply requirements for the TAS5760M consists of one low-voltage supply to power the low voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-board regulators are included in the device to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. External circuitry must not be connected to these regulator outputs, or reduced performance and even damage to the device may occur.

Serial Audio Port

In software control mode, additional digital audio data formats are made available via the I²C control port. With these controls, the audio format can be set to left justified, right justified, or I²S formatted data.

Serial Audio Port (SAP) Clocking

When used in software control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2kHz and 96kHz. The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 3. Supported SCLK Rates in Single Speed Mode

		MCLK Rate [x f_S]				
		128	**192**	**256**	**384**	**512**
Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 64	32, 48, 64	32, 64
	44.1	32, 48, 64	32, 48, 64	32, 64	32, 48, 64	32, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 64

Table 4. Supported SCLK Rates in Double Speed Mode

		MCLK Rate [x f_S]		
		128	**192**	**256**
Sample Rate [kHz]	**88.2**	32, 48, 64	32, 48, 64	32, 64
	96	32, 48, 64	32, 48, 64	32, 64

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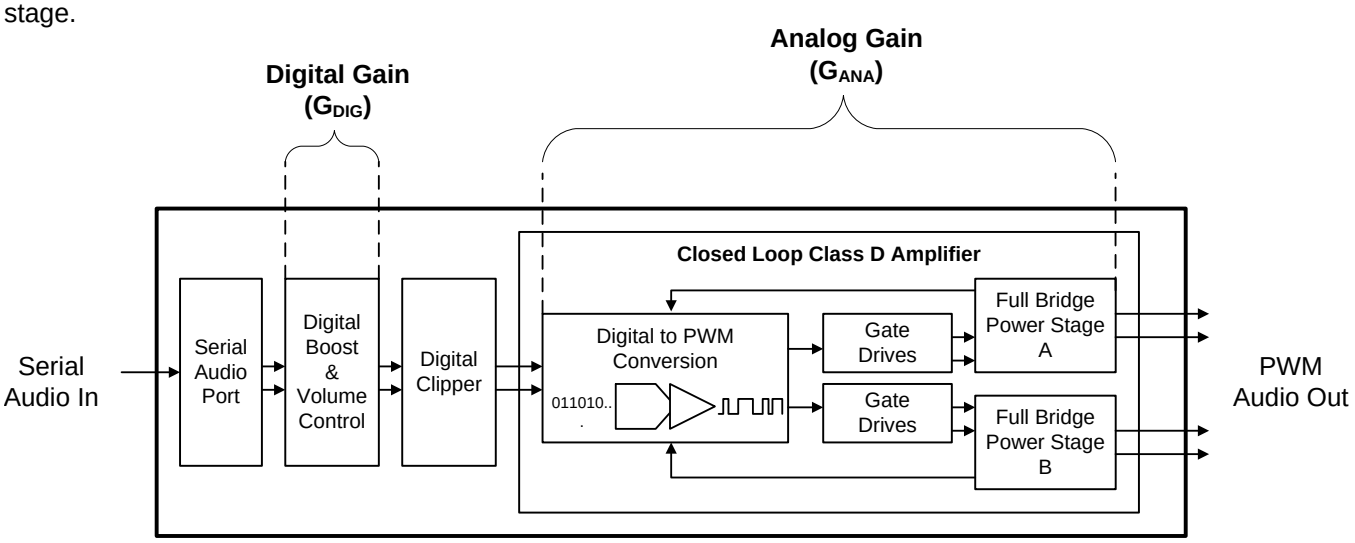
Speaker Amplifier Gain Structure

As seen below, the audio path of the consists of a digital audio input port, a digital audio path, a digital to analog converter, an analog modulator, a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the analog modulator to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.



The values of G_{DIG} and G_{ANA} for each of the GAIN[1:0] settings are shown in the table below. Additionally, the recommended PVDD level for each gain setting, along with the typical unclipped peak to peak output voltage swing for a 0dBFS input signal is provided.

Speaker Amplifier Gain in Software Control Mode

The analog and digital gain are configured directly when operating in software control mode. It is important to note that the digital boost block is separate from the volume control. The digital boost block should be set before the speaker amplifier is brought out of mute and not changed during normal operation. In most cases, the digital gain block can be left in it's default configuration, and no further adjustment is necessary. As mentioned previously, the analog gain is directly set via the I²C control port in software control mode.

Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760M. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason it may be necessary to limit the voltage swing of the amplifier via a lower gain setting in order to reduce the voltage presented, and therefore the power delivered, to the speaker.

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Recommendations for Setting the Speaker Amplifier Gain Structure in Software Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest analog gain setting via the A_GAIN[3:2] bits in the control port which will produce an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the analog gain.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper or the digital clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the analog gain.
5. Repeat Step 4 above until the optimum balance of power, noise, and clipping behavior is achieved.

I^2C Software Control Port

The TAS5760M includes an I^2C control port for increased flexibility and extended feature set.

Setting the I^2C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the MSB. The TAS5760M has a configurable I²C address. The SPK_MUTE/ADR can be used to set the device address of the TAS5760M. In software control mode, the seven bit I²C device address is configured as “110110x[$^R/_W$]”, where “x” corresponds to the state of the SPK_MUTE/ADR pin. If the SPK_MUTE/ADR pin is tied low (i.e. connected to the system ground), the address will be set to 1101100[$^R/_W$]. If it is pulled high (i.e. connected to the DVDD supply), the address will be set to 1101101[$^R/_W$].

General Operation of the I^2C Control Port

The TAS5760M device has a bidirectional I^2C interface that is compatible with the Inter IC (I^2C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 30. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5760M holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

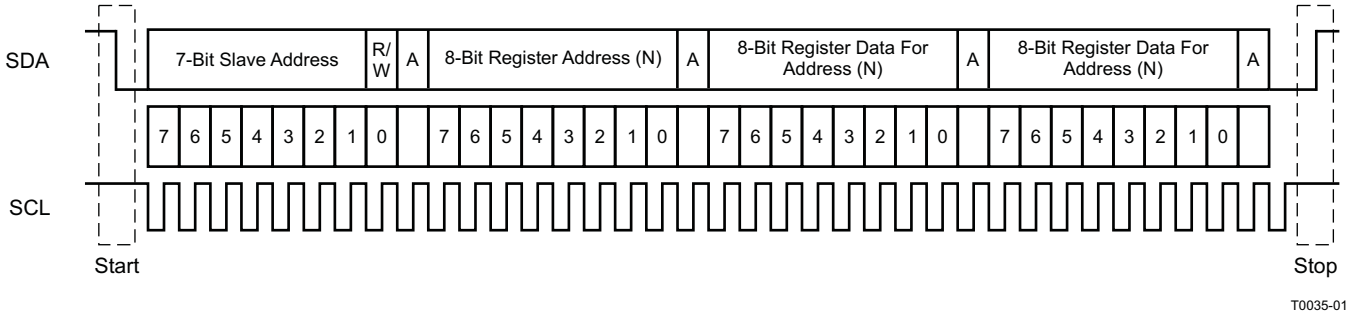

Figure 30. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 30.

Writing to the I²C Control Port

As shown in Figure 31, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the TAS5760M responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the TAS5760M register being accessed. After receiving the address byte, the TAS5760M again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5760M again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

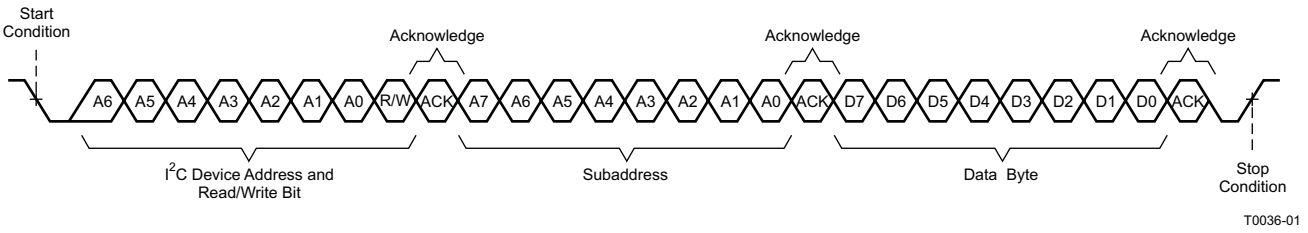

Figure 31. Write Transfer

Reading from the I²C Control Port

As shown in Figure 32, a data-read transfer begins with the master device transmitting a start condition, followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal register to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5760M address and the read/write bit, TAS5760M responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5760M address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5760M again responds with an acknowledge bit. Next, the TAS5760M transmits the data byte from the register being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the data-read transfer.

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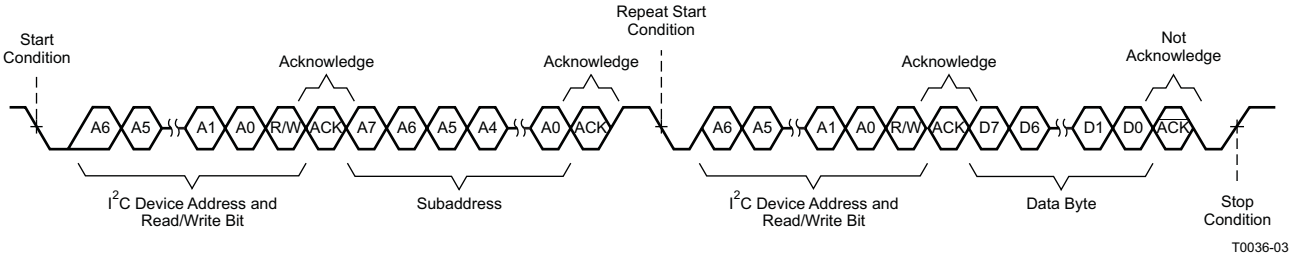

Figure 32. Read Transfer

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Table 5. Control Port Quick Reference Table

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
0	0	Device Identification	Device Identification								0x00
			0	0	0	0	0	0	0	0	
1	1	Power Control	Digital Clip Level 3						SLEEP	$\overline{\text{SPK\_SD}}$	0xFD
			1	1	1	1	1	1	0	1	
2	2	Digital Control	HPF Bypass	Reserved	Digital Boost		$\overline{\text{SS}}$/DS	Serial Audio Input Format			0x14
			0	0	0	1	0	1	0	0	
3	3	Volume Control Configuration	Fade	Reserved	Attack Speed	Zero Cross	Reserved	Reserved	Mute R	Mute L	0x80
			1	0	0	0	0	0	0	0	
4	4	Left Channel Volume Control	Volume Left								0xCF
			1	1	0	0	1	1	1	1	
5	5	Right Channel Volume Control	Volume Right								0xCF
			1	1	0	0	1	1	1	1	
6	6	Analog Control	PBTL Enable	PWM Rate Select			A_GAIN		PBTL Ch Sel	Analog Error Resp.	0x51
			0	1	0	1	0	0	0	1	
7	7	Clock Detection Control	M/L Ratio Error Bypass	DAC Clock Resync	MCLK Halt Thres		MCLK Rate Error Bypass	S/L Ratio Error Bypass	SCLK Halt Error Bypass	LRCK Rate Error Bypass	0x00
			0	0	0	0	0	0	0	0	
8	8	Fault Configuration and Error Status	Reserved		OCE Thres		CLKE	OCE	DCE	OTE	0x00
			0	0	0	0	0	0	0	0	
9	9	Reserved	-	-	-	-	-	-	-	-	-
...		Reserved	-	-	-	-	-	-	-	-	-
15	F	Reserved	-	-	-	-	-	-	-	-	-
16	10	Digital Clipper 2	Digital Clip Level 2								0xFF
			1	1	1	1	1	1	1	1	
17	11	Digital Clipper 1	Digital Clip Level 1								0xFF
			1	1	1	1	1	1	1	1	

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Control Port Detailed Register Description

Device Identification (1 / 0x01)

Device Identification [7:0] (Read Only)	0000000
TAS5760Mx	00000000

Power Control (2 / 0x02)

Digital Clip Level 3 [7:2] (R/W)	111111**01**
The digital clipper is decoded from 3 registers- Digital Clip Level 1, 2 and 3. Digital Clip Level 3, shown here, represents the upper 6 bits of the total of 22 bits that are used to set the Digital Clipping Threshold.	(decoded)

Sleep Mode [1] (R/W)	11111101
Device is placed in sleep mode	- - - - - - 0 -
Device is not in sleep mode	- - - - - - 1 -

Speaker Shutdown [0] (R/W)	11111101
Speaker amplifier is shut down	- - - - - - - 0
Speaker amplifier is not shut down	- - - - - - - 1

Digital Control (3 / 0x03)

High-Pass Filter Bypass [7] (R/W)	00010100
The internal high-pass filter in the digital path is not bypassed.	0 - - - - - - -
The internal high-pass filter in the digital path is bypassed.	1 - - - - - - -

Reserved [6] (Read Only)	00010100
This control is reserved and must not be changed from its default setting.	- 0 - - - - - -

Digital Boost [5:4] (R/W)	00010100
+0 dB is added to the signal in the digital path	- - 0 0 - - - -
+6 dB is added to the signal in the digital path	- - 0 1 - - - -
+12 dB is added to the signal in the digital path	- - 1 0 - - - -
+18 dB is added to the signal in the digital path	- - 1 1 - - - -

Single Speed / Double Speed Mode Select	00010100
Serial Audio Port will accept single speed sample rates (i.e. 32kHz, 44.1kHz, 48kHz)	- - - - 0 - - -
Serial Audio Port will accept double speed sample rates (i.e. 64kHz, 88.2kHz, 96kHz)	- - - - 1 - - -

Serial Audio Input Format	00010100
Serial Audio Input Format is 24 Bits, Right Justified	- - - - - 0 0 0
Serial Audio Input Format is 20 Bits, Right Justified	- - - - - 0 0 1
Serial Audio Input Format is 18 Bits, Right Justified	- - - - - 0 1 0
Serial Audio Input Format is 16 Bits, Right Justified	- - - - - 0 1 1
Serial Audio Input Format is I²S	- - - - - 1 0 0
Serial Audio Input Format is 16-24 Bits, Left Justified	- - - - - 1 0 1
Settings above 101 are reserved and must not be used	> - - - - - 1 0 1

Volume Control Configuration (4 / 0x04)

Volume Fade Enable [7] (R/W)	10000000
Volume fading is disabled	0 - - - - - - -
Volume fading is enabled	1 - - - - - - -

Reserved [6] (Read Only)	10000000
This control is reserved and must not be changed from its default setting.	- 0 - - - - - -

Attack Speed [5] (R/W)	10000000
When transitioning from one volume setting to another, the steps between adjacent settings occur on every 8th LRCK rising edge	- - 0 - - - - -
When transitioning from one volume setting to another, the steps between adjacent settings occur on every LRCK rising edge	- - 1 - - - - -

Zero Cross [4] (R/W)	10000000
When transitioning from one volume setting to another, the steps between adjacent settings occur on the first sample after a zero cross	- - 0 - - - - -
When transitioning from one volume setting to another, the steps between adjacent settings occur on the first sample after a zero cross	- - 1 - - - - -

Reserved [3] (R)	10000000
This control is reserved and must not be changed from its default setting.	- - - - 0 - - -

Reserved [2] (R)	10000000
This control is reserved and must not be changed from its default setting.	- - - - - - - -

Mute Right Channel [1] (R/W)	10000100
The right channel is not muted	- - - - - - 0 -
The right channel is muted	- - - - - - 1 -

Mute Left Channel [0] (R/W)	10000000
The left channel is not muted	- - - - - - - 0
The left channel is muted	- - - - - - - 1

Left Channel Volume Control (5 / 0x05)

Left/Right Channel Volume Control [7:0] (R/W)	11001111
Channel Volume is +24 dB	11111111
Channel Volume is +23.5 dB	11111110
Channel Volume is +23.0 dB	11111101
...	...
Channel Volume is 0 dB	11001111
...	...
Channel Volume is -100 dB	00000111
Any setting less than 00000111 places the channel in Mute	< 00000111

Right Channel Volume Control (6 / 0x06)

Left/Right Channel Volume Control [7:0] (R/W)	11001111
Channel Volume is +24 dB	11111111
Channel Volume is +23.5 dB	11111110
Channel Volume is +23.0 dB	11111101
...	...
Channel Volume is 0 dB	11001111
...	...
Channel Volume is -100 dB	00000111
Any setting less than 00000111 places the channel in Mute	< 00000111

Analog Control (7 / 0x07)

PBTL Enable [7] (R/W)	01010001
Device is placed in BTL mode	0 - - - - - - -
Device is placed in PBTL mode	1 - - - - - - -

PWM Rate Select [6:4] (R/W)	01010001
Output switching rate of the Speaker Amplifier is 6 * LRCK	- 0 0 0 - - - -
Output switching rate of the Speaker Amplifier is 8* LRCK	- 0 0 1 - - - -
Output switching rate of the Speaker Amplifier is 10 * LRCK	- 0 1 0 - - - -
Output switching rate of the Speaker Amplifier is 12 * LRCK	- 0 1 1 - - - -
Output switching rate of the Speaker Amplifier is 14 * LRCK	- 1 0 0 - - - -
Output switching rate of the Speaker Amplifier is 16 * LRCK	- 1 0 1 - - - -
Output switching rate of the Speaker Amplifier is 20 * LRCK	- 1 1 0 - - - -
Output switching rate of the Speaker Amplifier is 24 * LRCK	- 1 1 1 - - - -
Please note that all rates listed above are valid for single speed mode. For double speed mode, switching frequency is half of that represented above.	

A_GAIN[3:2] (R/W)	01010001
Analog Gain Setting is 8 V/V (or 18.062 dBV)	- - - - 0 0 - -
Analog Gain Setting is 12 V/V (or 21.583 dBV)	- - - - 0 1 - -
Analog Gain Setting is 16 V/V (or 24.082 dBV)	- - - - 1 0 - -
This setting is reserved and must not be used	- - - - 1 1 - -

Channel Selection for PBTL Mode [1] (R/W)	01010001
When placed in PBTL mode, the audio information from the Left channel of the serial audio input stream is used by the speaker amplifier	- - - - - - 0 -
When placed in PBTL mode, the audio information from the Right channel of the serial audio input stream is used by the speaker amplifier	- - - - - - 1 -

Clock Error Response [3] (R/W)	01010001
Upon a clock error, the speaker amplifier will be placed in mute as governed by the digital audio path settings, such as zero-cross, volume attack speed, and volume fading	- - - - - - - 0
Upon a clock error, the speaker amplifier will be placed in mute immediately	- - - - - - - 1

Clock Detection Control (8 / 0x08)

MCLK to LRCK Ratio Error Bypass [7] (R/W)	00000000
MCLK to LRCK ratio is monitored. If the ratio between the two is greater than 16, a clock error occurs	0 - - - - - - -
The MCLK to LRCK ratio monitoring circuit is bypassed	1 - - - - - - -

Reserved [6] (R/W)	00000000
This control is reserved and must not be changed from its default setting.	- - - - - - - -

MCLK Halt Threshold [5:4] (R/W)	00000000
In order for a clock error to occur, the MCLK must not have switched for 50 nS	- - 0 0 - - - -
In order for a clock error to occur, the MCLK must not have switched for 112nS	- - 0 1 - - - -
In order for a clock error to occur, the MCLK must not have switched for 176 nS	- - 1 0 - - - -
In order for a clock error to occur, the MCLK must not have switched for 240 nS	- - 1 1 - - - -
Please note that all rates listed above are valid for single speed mode. For double speed mode, switching frequency is half of that represented above.	

MCLK Rate Error Bypass [3] (R/W)	10000000
A clock error will occur if MCLK is stopped for the amount of time set by the MCLK Halt Threshold control	- - - - 0 - - -
The MCLK halt monitoring circuit is bypassed	

SCLK to LRCK Ratio Error Bypass [2] (R/W)	10000000
SCLK to LRCK ratio is monitored. If the ratio between the two is greater than TBD, a clock error occurs	- - - - - - - -
The SCLK to LRCK ratio monitoring circuit is bypassed	

SCLK Halt Error Bypass [1] (R/W)	10000100
A clock error will occur if SCLK is stopped	- - - - - - 0 -
The SCLK monitoring circuit is bypassed	- - - - - - 1 -

LRCK Halt Error Bypass [0] (R/W)	10000000
A clock error will occur if LRCK is stopped	- - - - - - - 0
The LRCK halt monitoring circuit is bypassed	- - - - - - - 1

Reserved Controls (9 / 0x09) - (15 / 0x0F)

The controls in this section of the control port are reserved and must not be used.

Digital Clipper Control 2 (16 / 0x10)

Digital Clip Level 2 [7:0] (R/W)	11111111
The digital clipper is decoded from 3 registers- Digital Clip Level 1, 2 and 3. Digital Clip Level 2, shown here, represents the [16:8] bits of the total of 22 bits that are used to set the Digital Clipping Threshold.	(decoded)

Digital Clip Level 1 [7:0] (R/W)	11111111
The digital clipper is decoded from 3 registers- Digital Clip Level 1, 2 and 3. Digital Clip Level 2, shown here, represents the [7:0] bits of the total of 22 bits that are used to set the Digital Clipping Threshold.	(decoded)

APPLICATION INFORMATION

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in all available modes of operation. Additioanlly, some of the application circuits are available as reference designs and can be found on the TI website. See the TBA for ordering information of the EVMs. Note that not all configurations are available as reference designs; however, any design variation can be supported by TI through schematic and layout reviews. Visit support.ti.com for additional design assistance. Also, join the audio amplifier discussion forum at http://e2e.ti.com.

TAS5760x Typical Application Circuits

These application circuits detail the recommended component selection and board configurations for the TAS5760M or TAS5760L device. Note that in software control mode, the clipping point of the amplifier and thus the "rated power" of the end equipment can be set using the digital clipper if desired. Additionally, if the sonic signature of the soft clipper is preferred, it can be used in addition to or in lieu of the digital clipper. The software control application circuit detailed in this section shows the soft clipper in its bypassed state, which results in a lower BOM count than when using the soft clipper. The trade-off between the sonic characteristics of the clipping events in the amplifier and BOM minimization can be chosen based upon the design goals related to the end product.

For further information regarding component selection, please refer tothe user guide provided with the device's EVM.

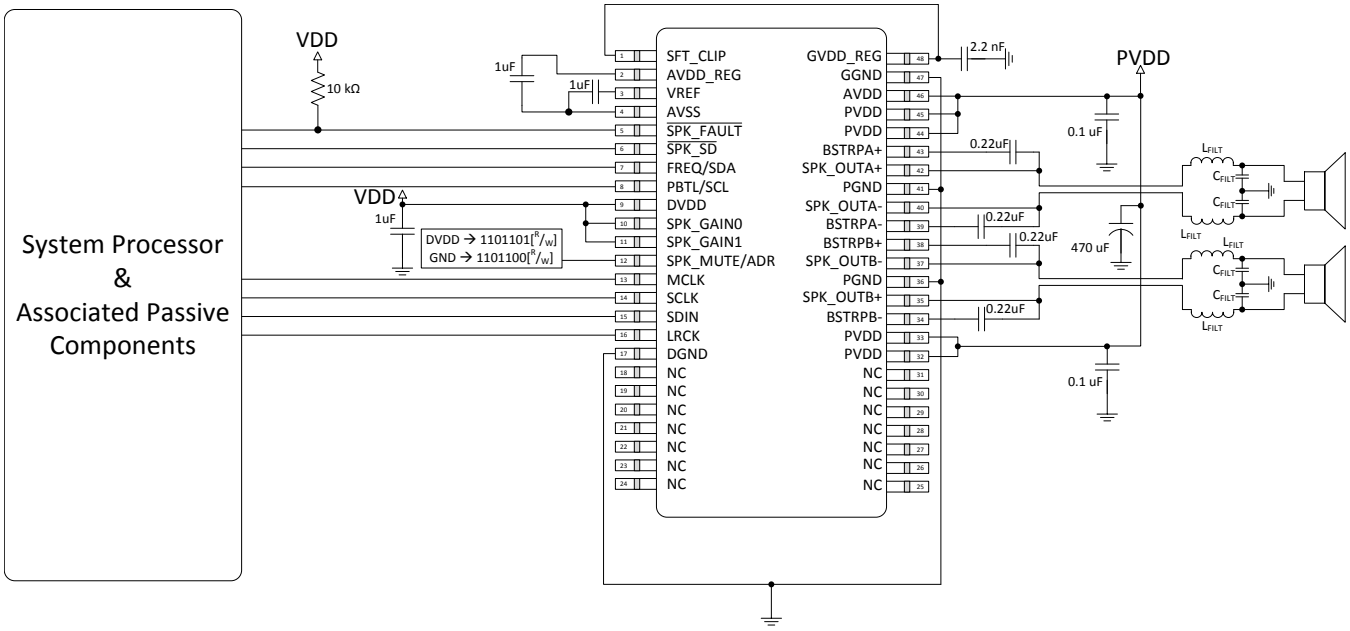

Figure 33. Stereo BTL using Software Control, 48 Pin DCA Package Option

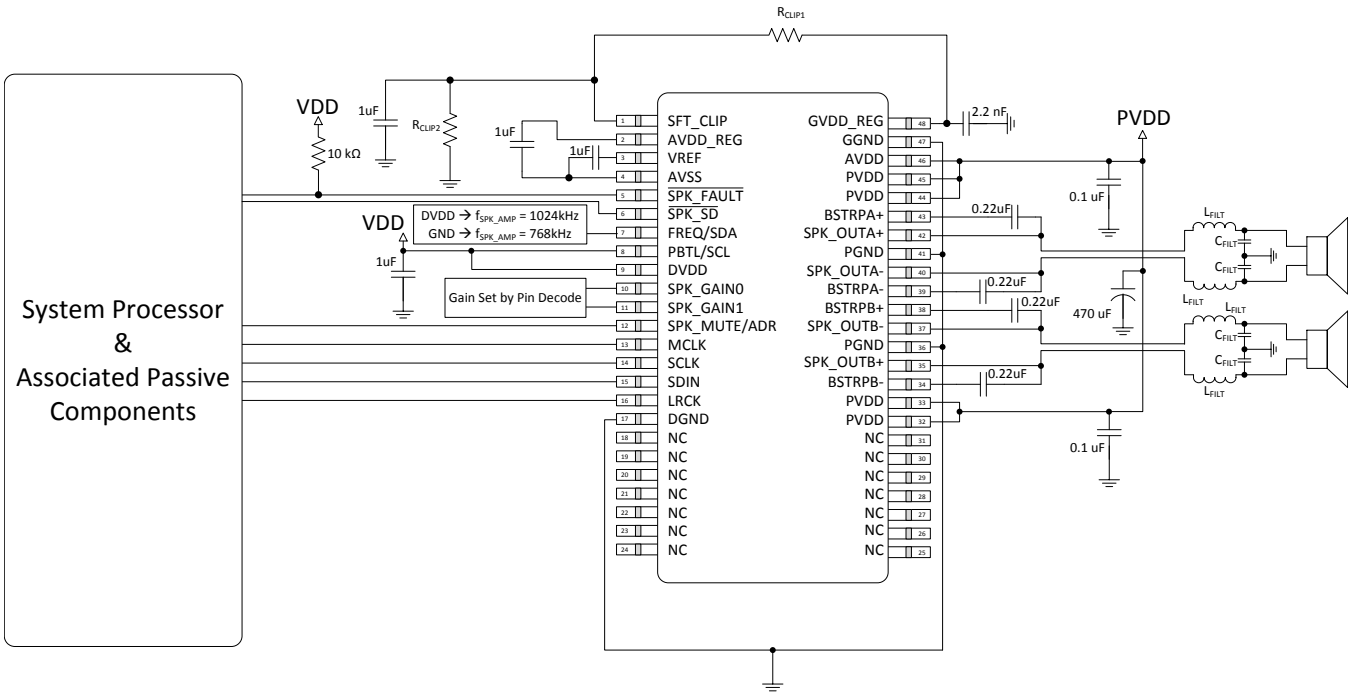

Figure 34. Stereo BTL using Hardware Control, 48 Pin DCA Package Option

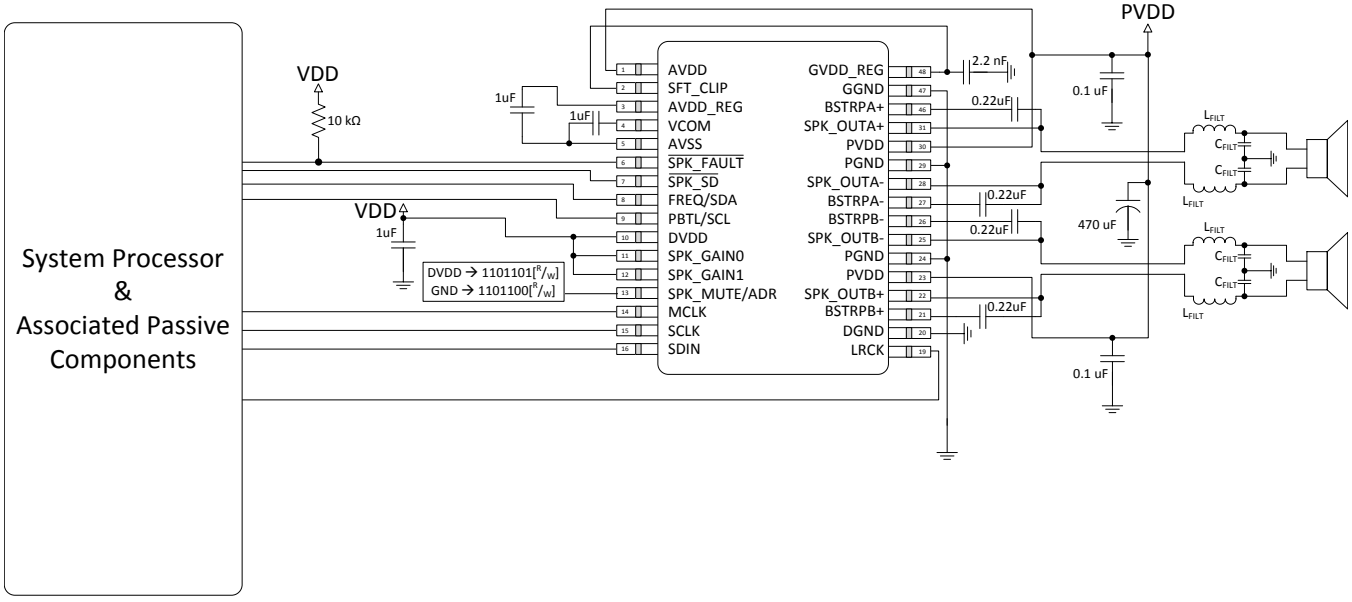

Figure 35. Stereo BTL using Software Control, 32 Pin DAP Package Option

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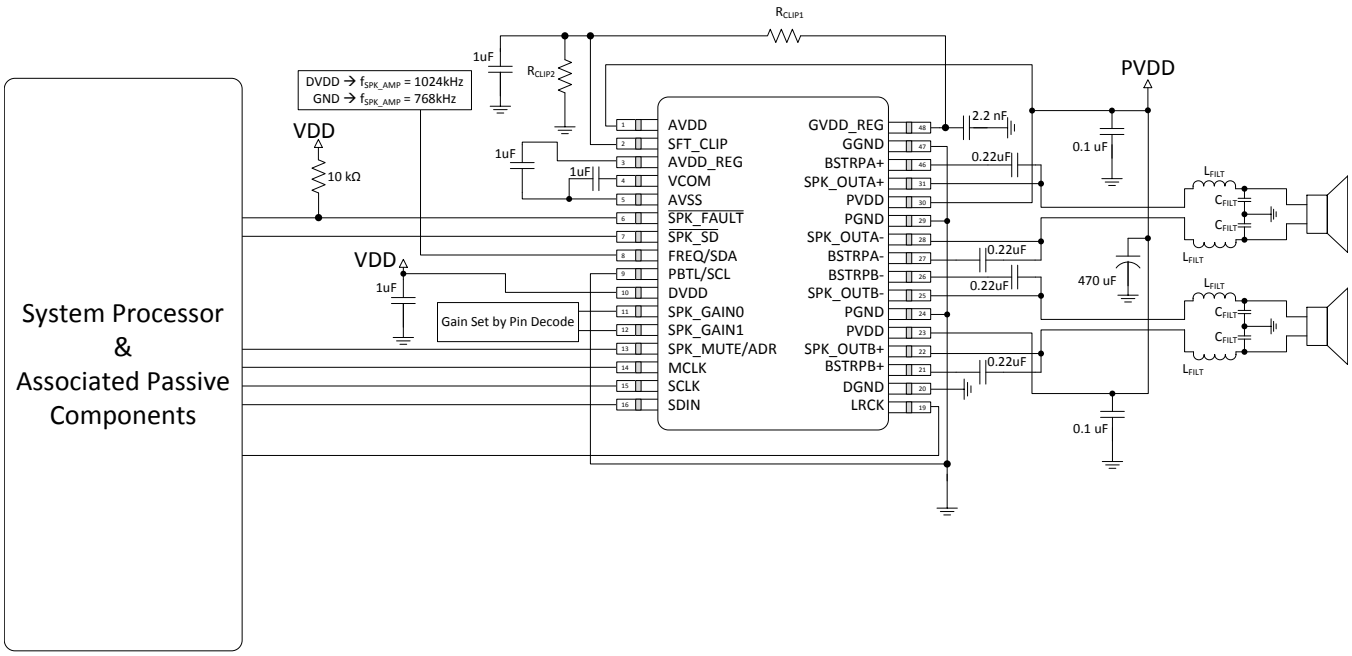


Figure 36. Stereo BTL using Software Control, 32 Pin DAP Package Option

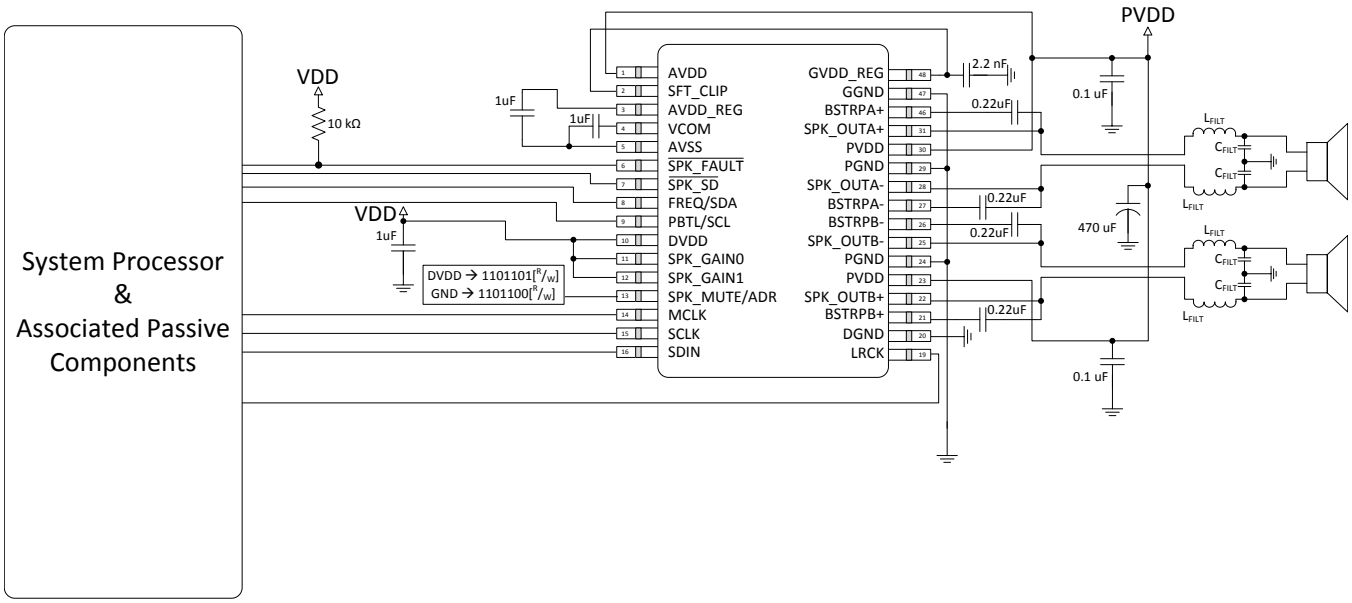


Figure 37. Mono PBTL using Software Control, 32 Pin DAP Package Option

PRODUCT PREVIEW

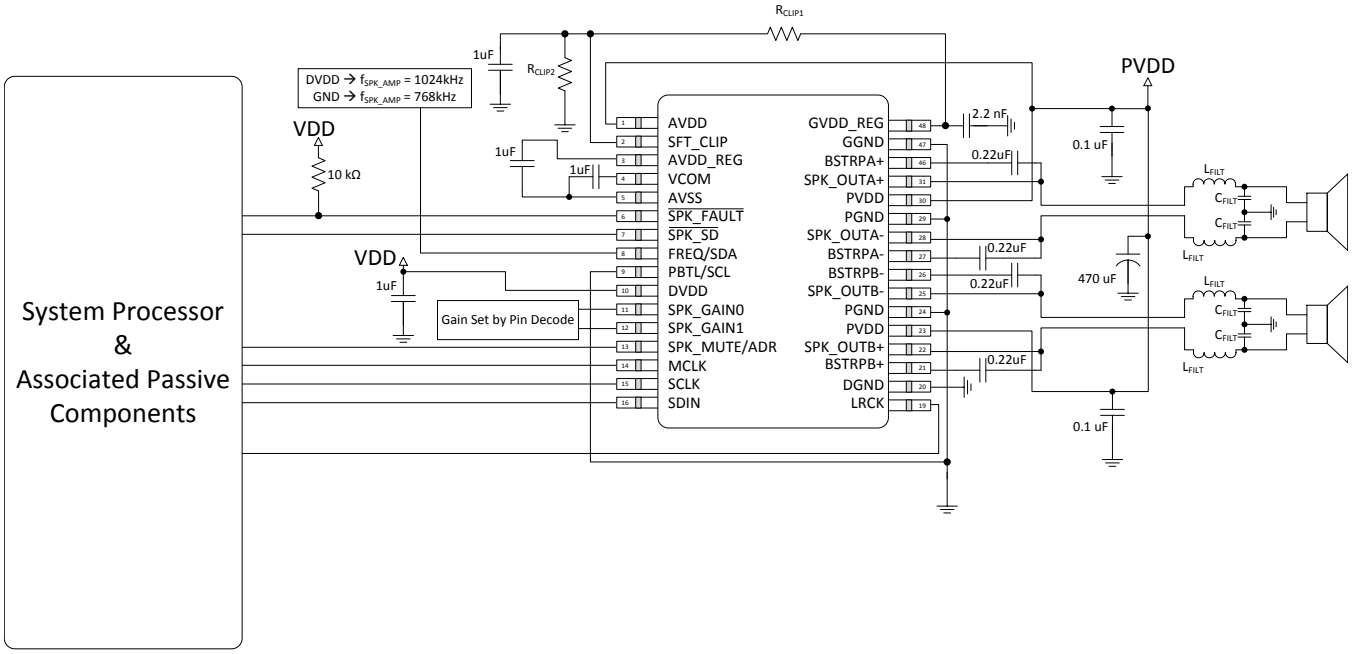


Figure 38. Mono BTL using Hardware Control, 32 Pin DAP Package Option

Recommended Startup and Shutdown Procedures

The start up and shutdown procedures for both hardware mode control and software mode control are shown below.

Startup Procedures- Hardware Mode Control

1. Configure all hardware pins as required by the application using PCB connections (i.e. PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled low and SPK_MUTE/ADR pin pulled high
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ high
6. Once the device is out of shutdown mode, bring $\overline{\text{SPK\_SD}}$ high
7. The device is now in normal operation

PRODUCT PREVIEW

Shutdown Procedures- Hardware Mode Control

1. The device is in normal operation
2. Pull SPK_MUTE/ADR high
3. Pull $\overline{\text{SPK\_SD}}$ low
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

Startup Procedures- Software Mode Control

1. Configure all hardware control pins as required by the application using PCB connections (i.e. GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = LOW
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ HIGH
7. Unmute the device via the control port
8. The device is now in normal operation

It is important to note that control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin low or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

Shutdown Procedures- Software Mode Control

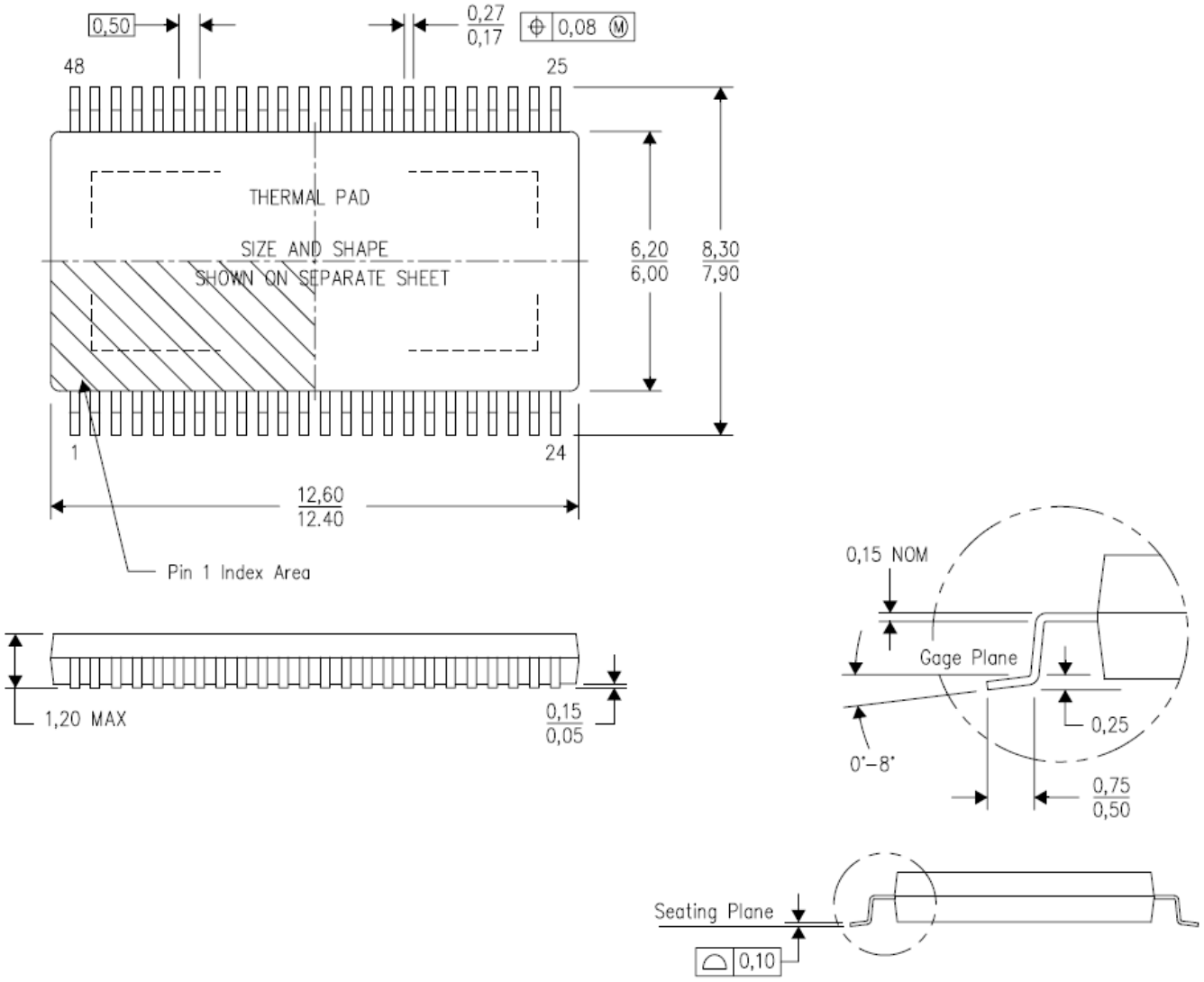
1. The device is in normal operation
2. Mute via the control port
3. Pull $\overline{\text{SPK\_SD}}$ low
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

It is important to note that control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin low or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

PRODUCT PREVIEW

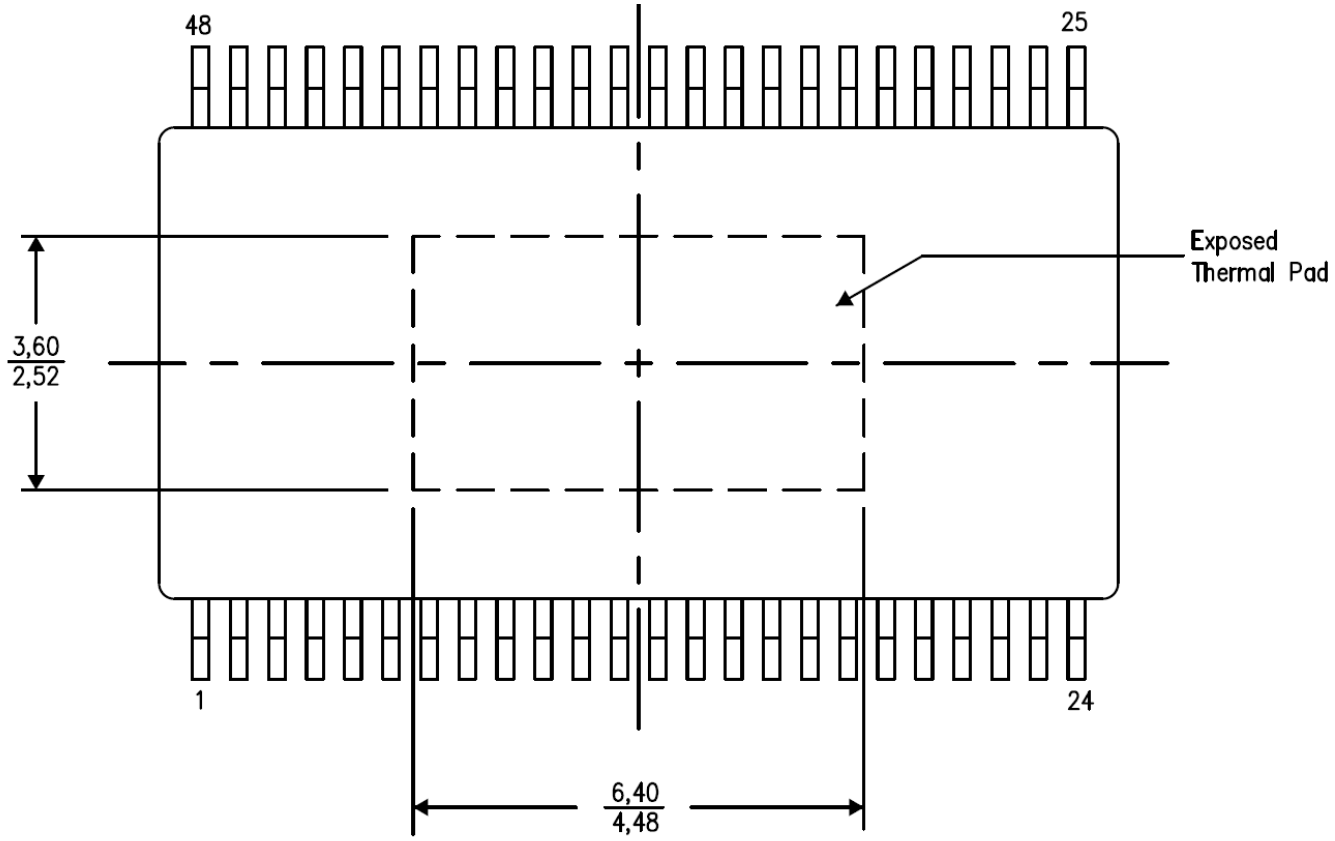
MECHANICALS

Package Dimensions- 48 Pin DCA



PRODUCT PREVIEW

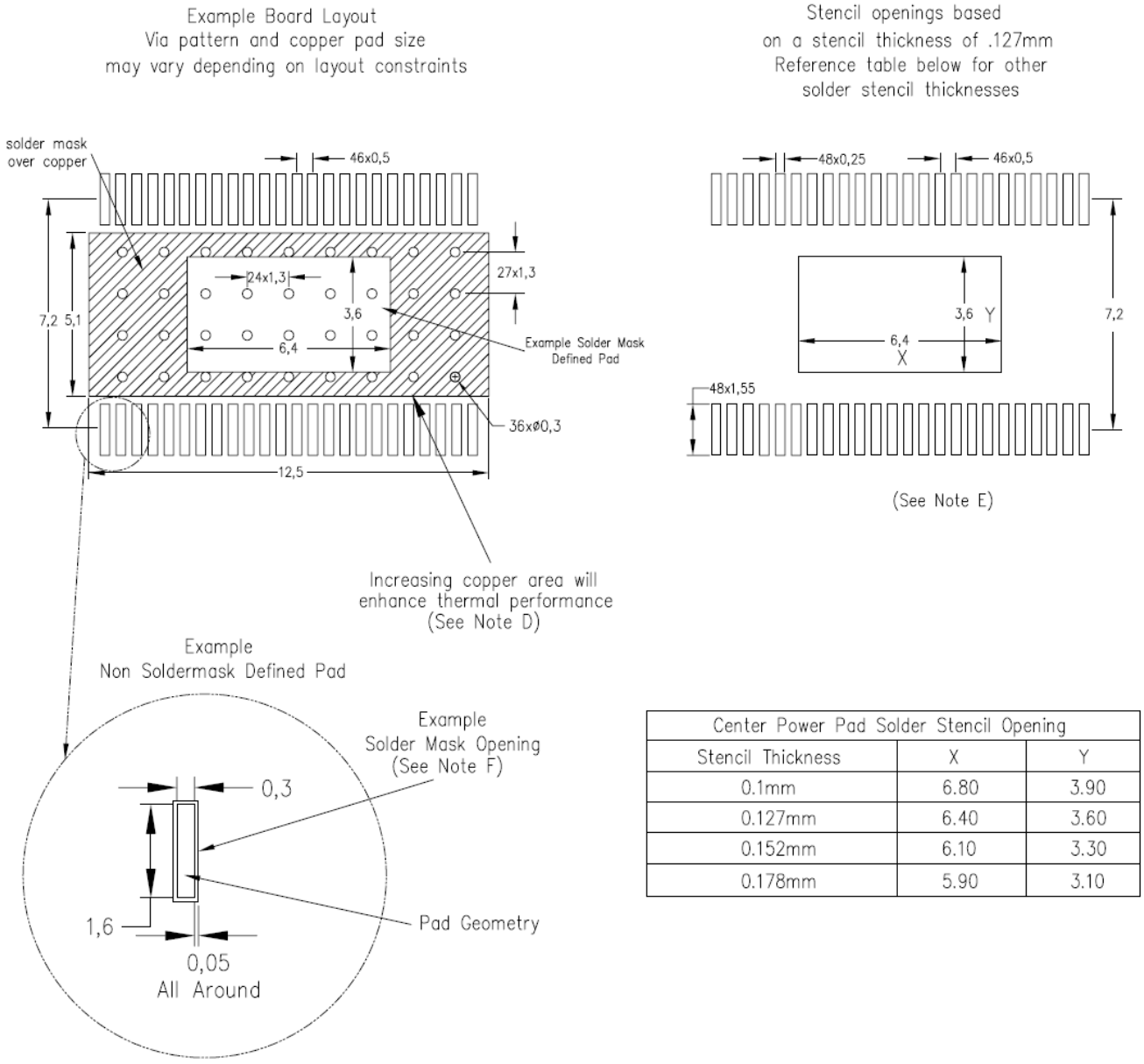
PowerPAD™ Dimensions- 48 Pin DCA



Top View

PRODUCT PREVIEW

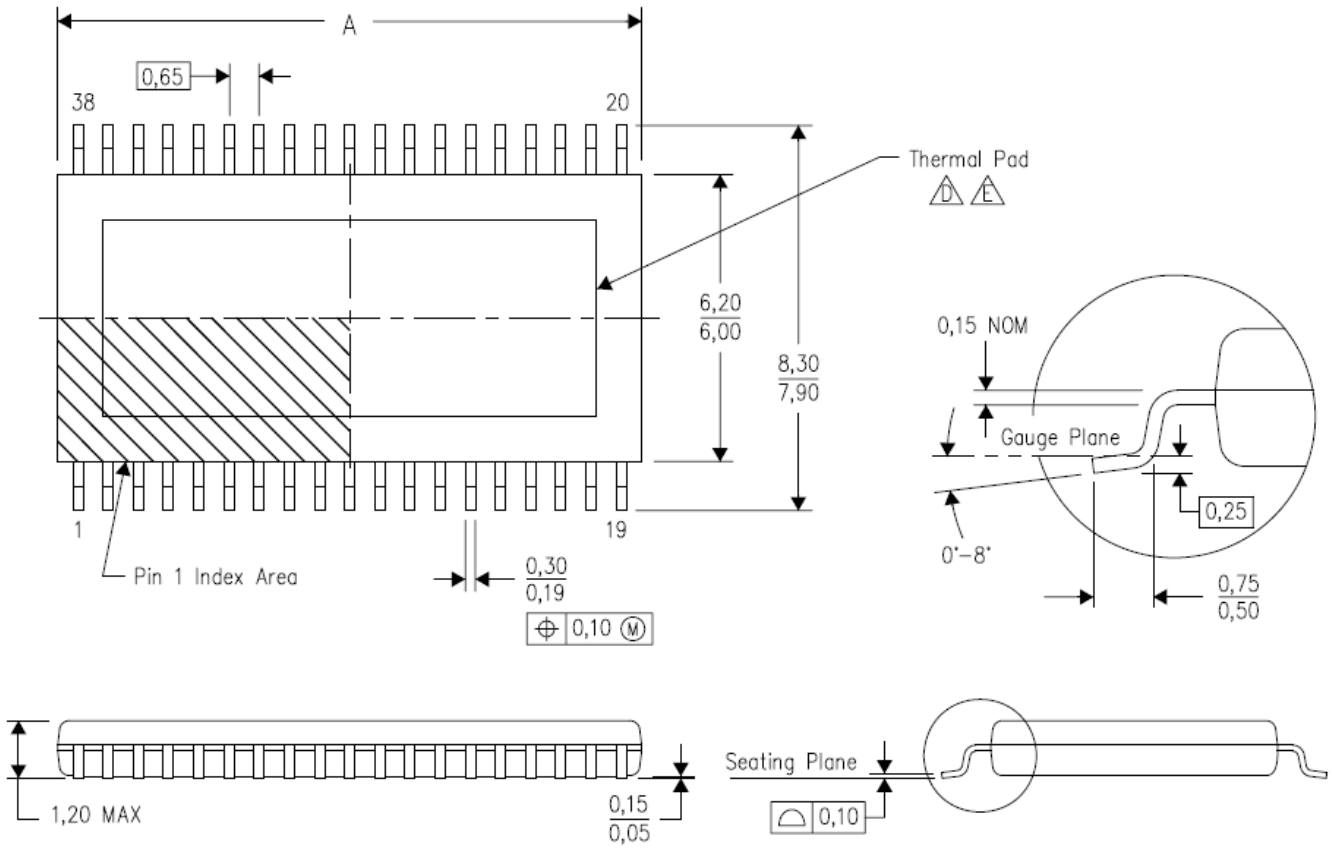
Land Pattern and Stencil Dimensions- 48 Pin DCA



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.80	3.90
0.127mm	6.40	3.60
0.152mm	6.10	3.30
0.178mm	5.90	3.10

PRODUCT PREVIEW

Package Dimensions- 32 Pin DAP

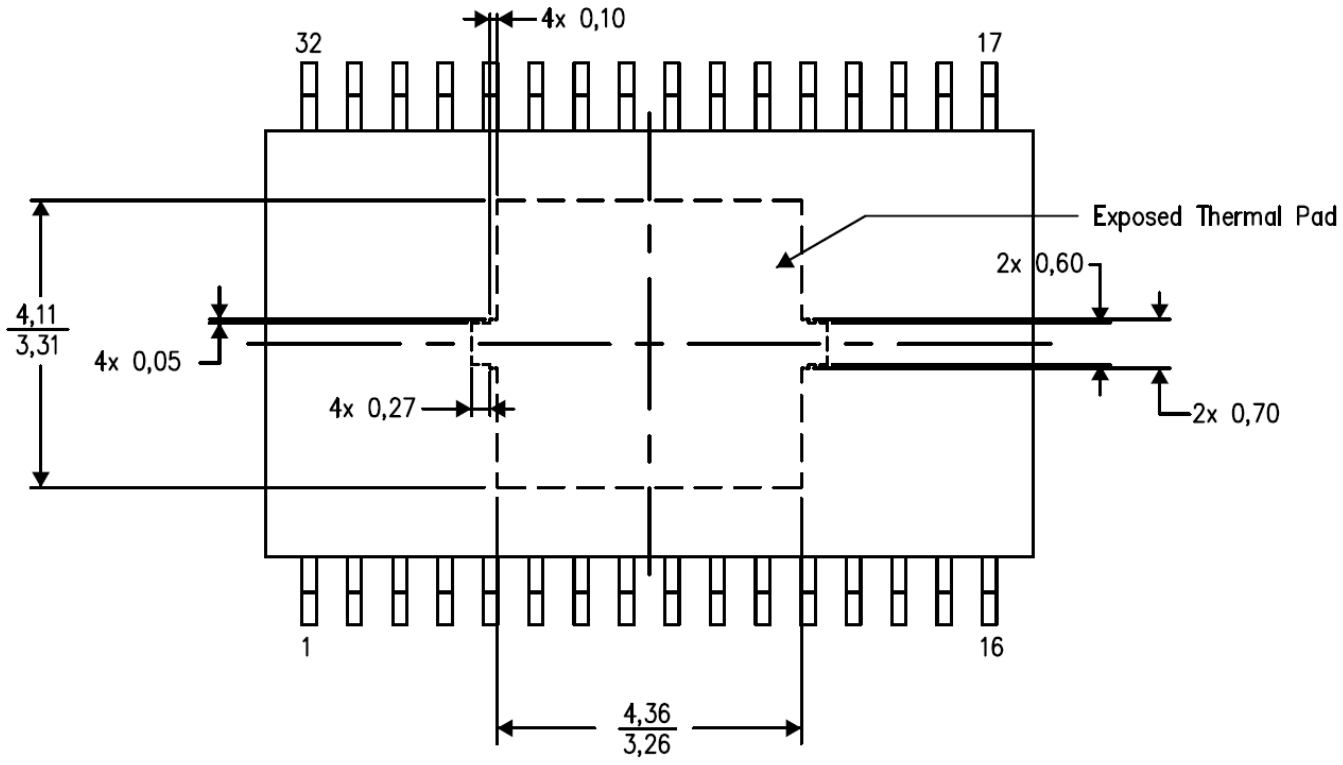


E

DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

PRODUCT PREVIEW

PowerPAD™ Dimensions- 32 Pin DAP

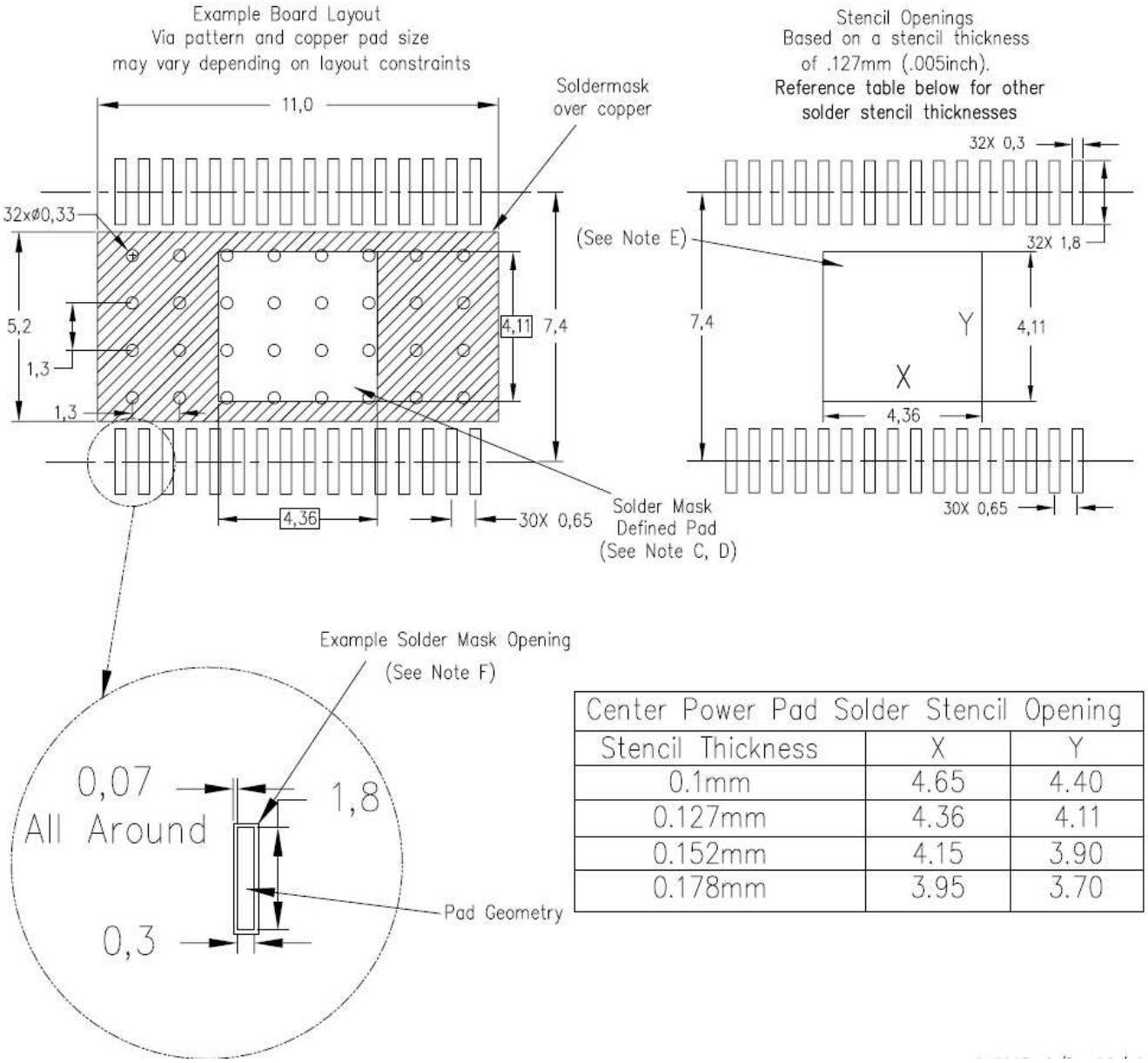


Top View

Exposed Thermal Pad Dimensions

PRODUCT PREVIEW

Land Pattern and Stencil Dimensions- 32 Pin DAP



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.65	4.40
0.127mm	4.36	4.11
0.152mm	4.15	3.90
0.178mm	3.95	3.70

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5760MDAP	PREVIEW	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85		
TAS5760MDAPR	PREVIEW	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85		
TAS5760MDCA	PREVIEW	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85		
TAS5760MDCAR	PREVIEW	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85		
TAS5760MDDCA	PREVIEW	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760MD	
TAS5760MDDCAR	PREVIEW	HTSSOP	DCA	48		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760MD	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

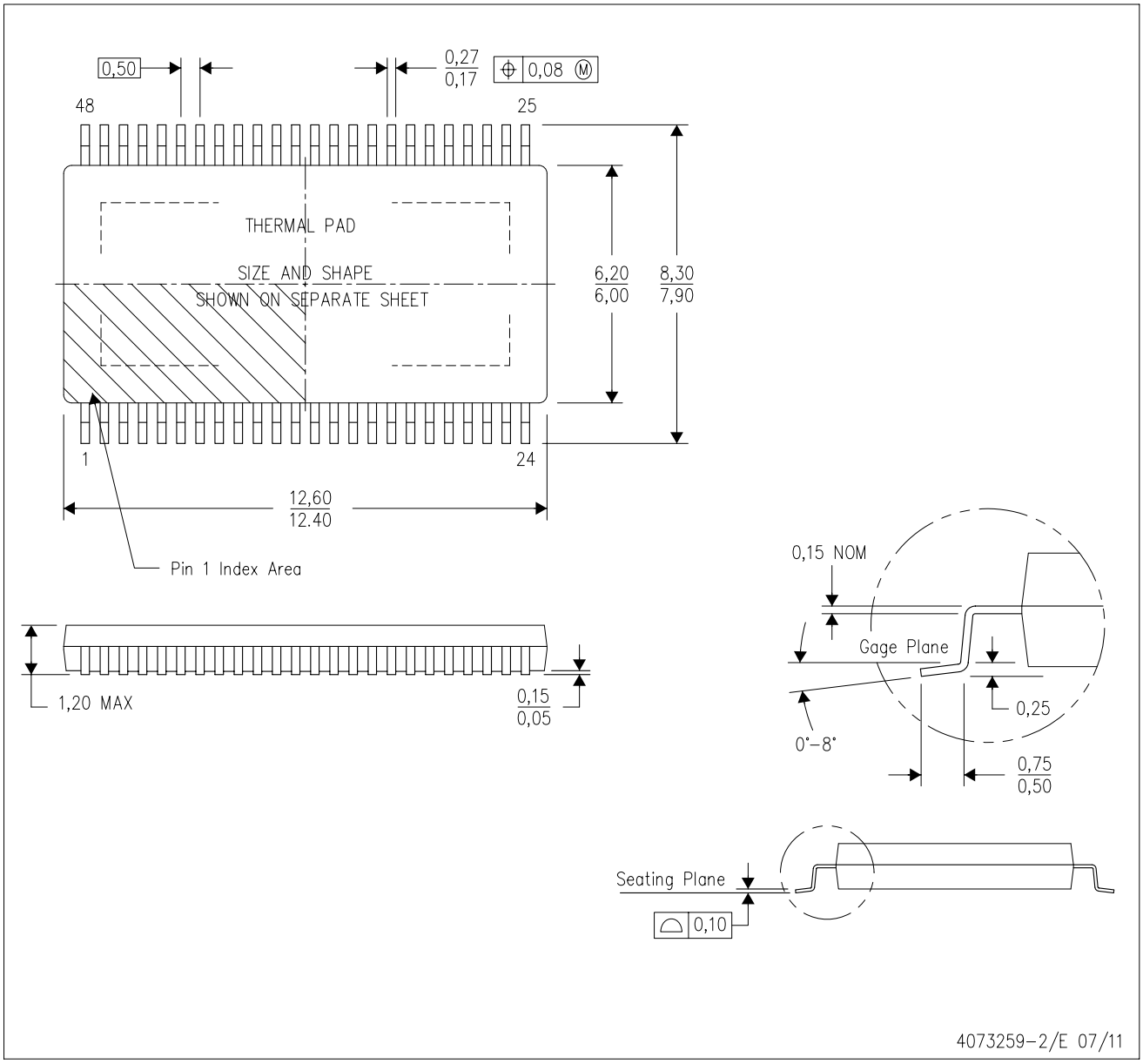
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

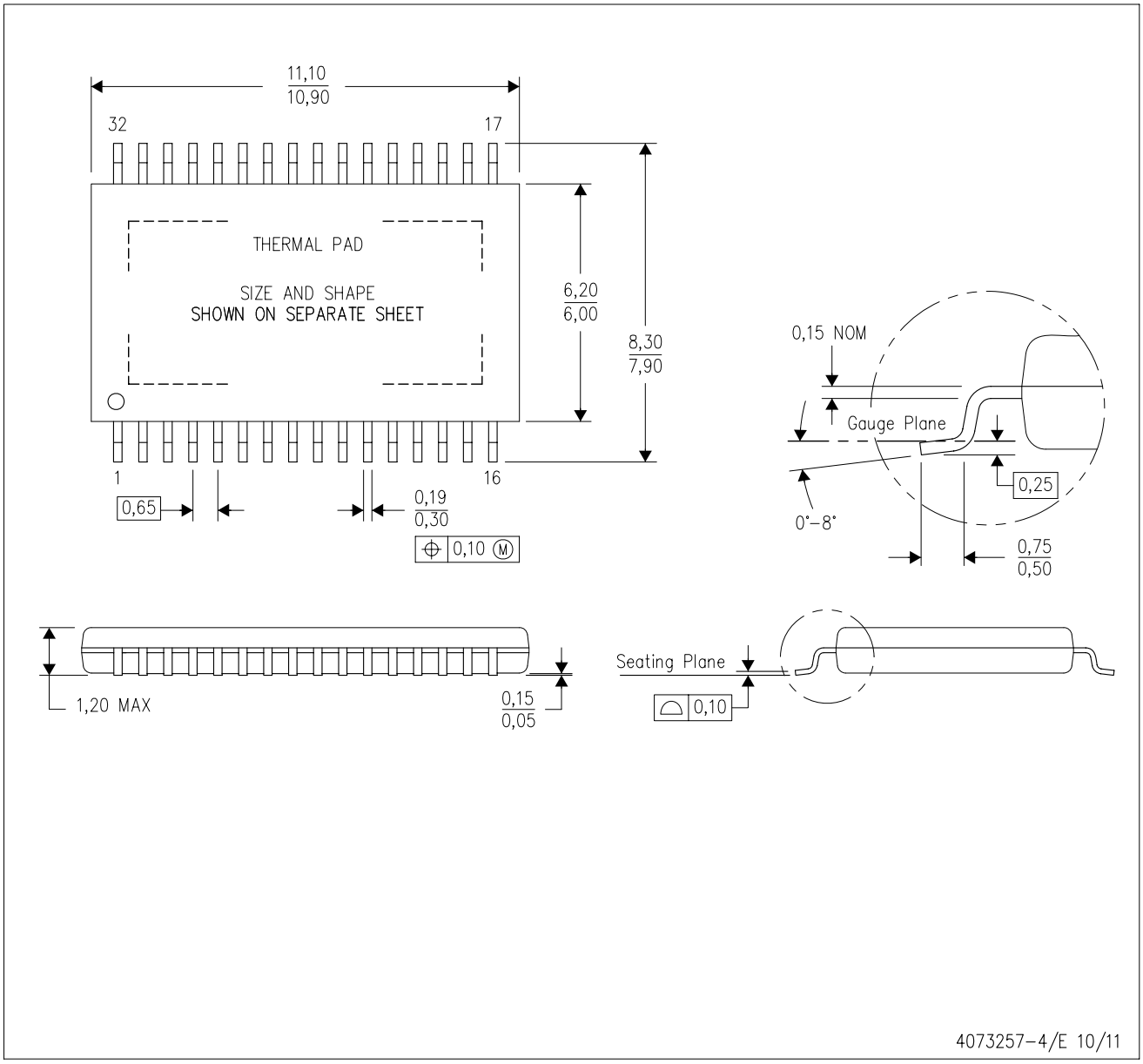
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

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