20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier With Shutdown

Check for Samples: OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H3A**
  - **Device CDM ESD Classification Level C5**
- **Gain Bandwidth: 20 MHz**
- **Low Noise: 8.5 nV/√Hz at 1 kHz**
- **Slew Rate: 10 V/µs**
- **Low THD+N: 0.0005%**
- **Rail-to-Rail I/O**
- **Offset Voltage: 2 mV (max)**
- **Supply Voltage: 1.8 V to 5.5 V**
- **Supply Current: 1.5 mA/ch**
  - **Shutdown: 0.1 µA/ch**
- **Unity-Gain Stable**
- **Small Packages:**
  - **SOT23, DFN, MSOP, TSSOP**

APPLICATIONS

- **Automotive**
- **Sensor Signal Conditioning**
- **Consumer Audio**
- **Multi-Pole Active Filters**
- **Control-Loop Amplifiers**
- **Communications**
- **Security**
- **Scanners**

DESCRIPTION

The OPA322-Q1 family consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs/outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, and with a low quiescent current of only 1.5 mA per channel, these devices are well-suited for power-sensitive applications.

The combination of very low noise (8.5 nV/√Hz at 1 kHz), high gain-bandwidth (20 MHz), and fast slew rate (10 V/µs) make the OPA322-Q1 family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPA322-Q1 family is also excellent for consumer audio applications, particularly for single-supply systems.

The OPAx322S-Q1 models include a shutdown mode allowing the amplifiers to switch from normal operation to a standby current that is typically less than 0.1 µA.

The OPA322-Q1 (single version) is available in SOT23-5 and SOT23-6, whereas the OPA2322 (dual version) comes in MSOP-8, MSOP-10, SO-8, and DFN-8 packages. The quad versions OPA4322 come in TSSOP-14 and TSSOP-16 packages. The specification on all versions is for operation from –40°C to 125°C.

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA322-Q1	SOT23-5	DBV	Preview
OPA322S-Q1	SOT23-6	DBV	Preview
OPA2322AQDGKRQ1	MSOP-8	DGK	OVDQ
OPA2322S-Q1	MSOP-10	DGS	Preview
OPA4322-Q1	TSSOP-14	PW	Preview
OPA4322S-Q1	TSSOP-16	PW	Preview

(1) For the most-current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1	UNIT
Supply voltage, V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit current(3)		Continuous	mA
Operating temperature, T_A		–40 to 125	°C
Storage temperature, T_{stg}		–65 to 150	°C
Junction temperature, T_J		150	°C
ESD ratings	Human-body model (HBM) AEC-Q100 Classification Level H3A	4	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C5	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute-maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

PRODUCT PREVIEW

THERMAL INFORMATION: OPA322-Q1

THERMAL METRIC(1)		OPA322-Q1	OPA322S-Q1	UNIT
		DBV	DBV	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	°C/W
θ_{JB}	Junction-to-board thermal resistance	57.5	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA2322-Q1

THERMAL METRIC(1)		OPA2322-Q1			OPA2322S-Q1	UNIT
		D	DRG	DGK	DGS	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	50.6	174.8	171.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	43.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	64.0	25.2	95.0	91.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2.0	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	89.9	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	5.7	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA4322-Q1

THERMAL METRIC(1)		OPA4322-Q1	OPA4322S-Q1	UNIT
		PW	PW	
		14 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	109.8	105.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.9	28.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	52.5	51.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.8	50.4	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V

Boldface limits apply over the specified temperature range, **T_A = –40°C to 125°C.**
At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and $\overline{SHDN\_x}$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.5	2	mV
versus Temperature	**dV_{OS}/dT**	**V_S = 5.5 V**		**1.8**	**6**	**µV/°C**
versus Power supply	PSR	V_S = 1.8 V to 5.5 V		10	50	µV/V
Over temperature		**V_S = 1.8 V to 5.5 V**		**20**	**65**	**µV/V**
Channel separation		At 1 kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	90	100		dB
Over temperature			**90**			**dB**
INPUT BIAS CURRENT						
Input bias current	I_B			±0.2	±10	pA
Over temperature		**T_A = –40°C to 85°C**			**±50**	**pA**
		OPA322-Q1, OPA322S-Q1, T_A = –40°C to 125°C			**±800**	**pA**
		OPA2322, OPA2322S, T_A = –40°C to 125°C			**±400**	**pA**
		OPA4322, OPA4322S, T_A = –40°C to 125°C			**±400**	**pA**
Input offset current	I_{OS}			±0.2	±10	pA
Over temperature		**T_A = –40°C to 85°C**			**±50**	**pA**
		T_A = –40°C to 125°C			**±400**	**pA**
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		2.8		μV_{PP}
Input voltage noise density	e_n	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
Input current noise density	i_n	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	100	130		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	**94**			**dB**
Phase margin	PM	V_S = 5 V, C_L = 50 pF		47		Degrees
FREQUENCY RESPONSE		**V_S = 5.0 V, C_L = 50 pF**				
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = 1		10		V/µs
Settling time	t_S	To 0.1%, 2-V step, G = 1		0.25		µs
		To 0.01%, 2-V step, G = 1		0.32		µs
Overload recovery time		V_{IN} × G > V_S		100		ns
Total harmonic distortion + noise(1)	THD+N	V_O = 4 V_{PP}, G = 1, f = 10 kHz, R_L = 10 kΩ		0.0005		%
		V_O = 2 V_{PP}, G = 1, f = 10 kHz, R_L = 600 Ω		0.0011		%

(1) Third-order filter; bandwidth = 80 kHz at –3 dB

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to 125°C.**
At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and $\overline{SHDN}\_x$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322-Q1, OPA322S-Q1, OPA2322-Q1, OPA2322S-Q1, OPA4322-Q1, OPA4322S-Q1			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage output swing from both rails	V_O	R_L = 10 kΩ		10	20	mV
Over temperature		**R_L = 10 kΩ**			**30**	**mV**
Short-circuit current	I_{SC}	V_S = 5.5 V		±65		mA
Capacitive load drive	C_L		See Typical Characteristics			
Open-loop output resistance	R_O	I_O = 0 mA, f = 1 MHz		90		Ω
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0 mA, V_S = 5.5 V				
OPA322-Q1, OPA322S-Q1		I_O = 0 mA, V_S = 5.5 V		1.6	1.9	mA
Over temperature		**I_O = 0 mA, V_S = 5.5 V**			**2**	**mA**
OPA2322-Q1, OPA2322S-Q1		I_O = 0 mA, V_S = 5.5 V		1.5	1.75	mA
Over temperature		**I_O = 0 mA, V_S = 5.5 V**			**1.85**	**mA**
OPA4322-Q1, OPA4322S-Q1		I_O = 0 mA, V_S = 5.5 V		1.4	1.65	mA
Over temperature		**I_O = 0 mA, V_S = 5.5 V**			**1.75**	**mA**
Power-on time		V_{S+} = 0 V to 5 V, to 90% I_Q level		28		µs
SHUTDOWN(2)		V_S = 1.8 V to 5.5 V				
Quiescent current, per amplifier	I_{QSD}	All amplifiers disabled, $\overline{SHDN}$ = $V_{S–}$		0.1	0.5	µA
High voltage (enabled)	V_{IH}	Amplifier enabled	(V+) - 0.1			V
Low voltage (disabled)	V_{IL}	Amplifier disabled			(V–) + 0.1	V
Amplifier enable time (full shutdown)(3)	t_{ON}	Full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2 (4)		10		µs
Amplifier enable time (partial shutdown) (3)	t_{ON}	Partial shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2 (4)		6		µs
Amplifier disable time(3)	t_{OFF}	G = 1, V_{OUT} = 0.1 × V_S / 2		3		µs
$\overline{SHDN}$ pin input bias current (per pin)		V_{IH} = 5 V		0.13		µA
		V_{IL} = 0 V		0.04		µA
TEMPERATURE						
Specified range			–40		125	°C
Operating range			–40		150	°C

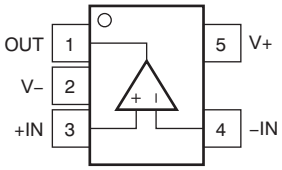
(2) Ensured by design and characterization; not production tested.
(3) The definition of isable time (t_{OFF}) and enable time (t_{ON}) is the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual OPA2322S-Q1 having both channels A and B disabled ($\overline{SHDN\_A}$ = $\overline{SHDN\_B}$ = $V_{S–}$) and the quad OPA4322S-Q1 having all channels A to D disabled ($\overline{SHDN\_A/B}$ = $\overline{SHDN\_C/D}$ = $V_{S–}$). Partial shutdown exercises only one $\overline{SHDN}$ pin; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

PRODUCT PREVIEW

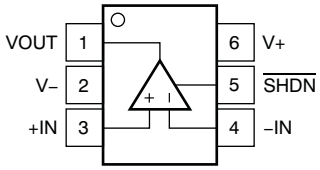
PRODUCT PREVIEW

PIN CONFIGURATIONS

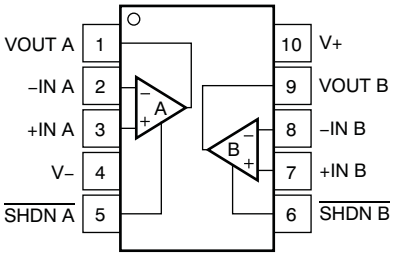
DBV PACKAGE
SOT23-5
(TOP VIEW)



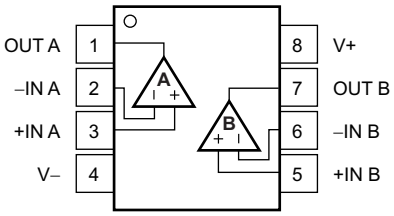
DBV PACKAGE
SOT23-6
(TOP VIEW)



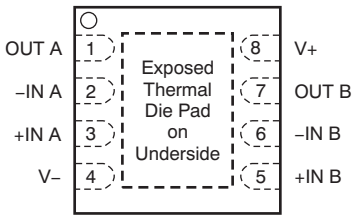
DGS PACKAGE
MSOP-10
(TOP VIEW)



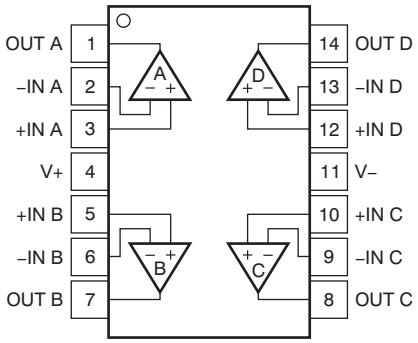
D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



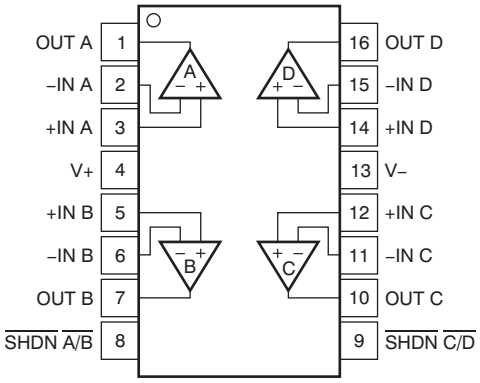
DRG PACKAGE(1)(2)
DFN-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



PW PACKAGE
TSSOP-16
(TOP VIEW)



(1) Connect thermal pad to V–.
(2) Pad size: 2 mm × 1.2 mm.

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OPEN-LOOP GAIN/PHASE versus FREQUENCY

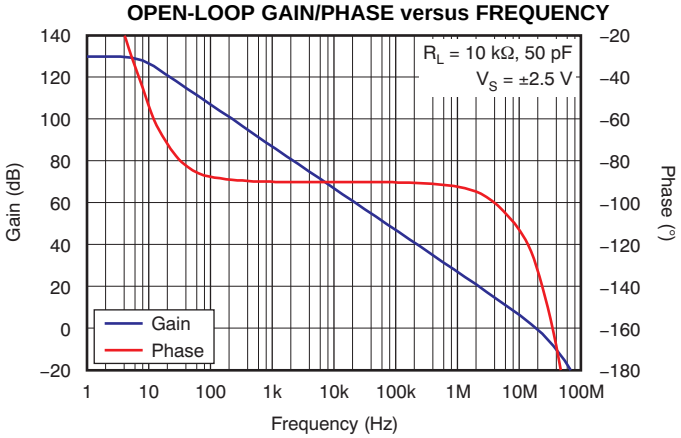


Figure 1.

OPEN-LOOP GAIN versus TEMPERATURE

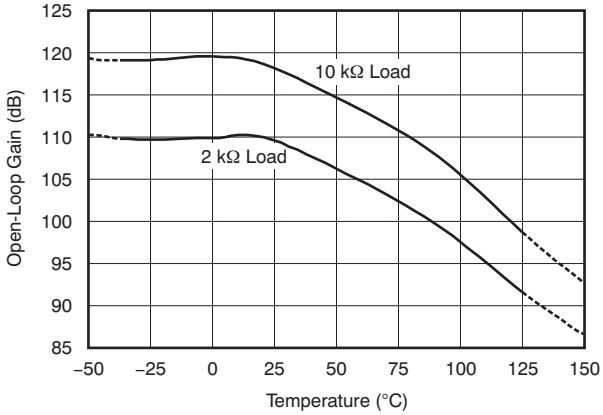


Figure 2.

INPUT BIAS CURRENT versus SUPPLY VOLTAGE

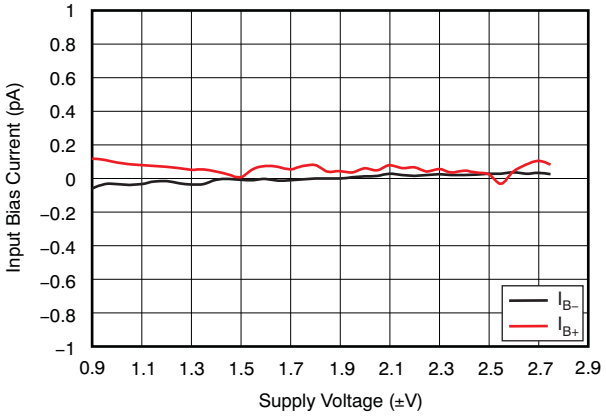


Figure 3.

INPUT BIAS CURRENT versus COMMON-MODE VOLTAGE

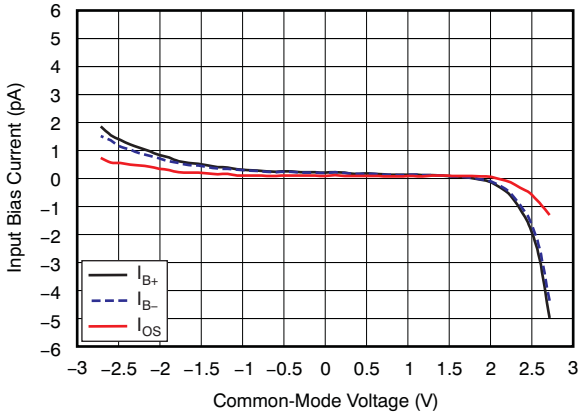


Figure 4.

INPUT BIAS CURRENT versus TEMPERATURE

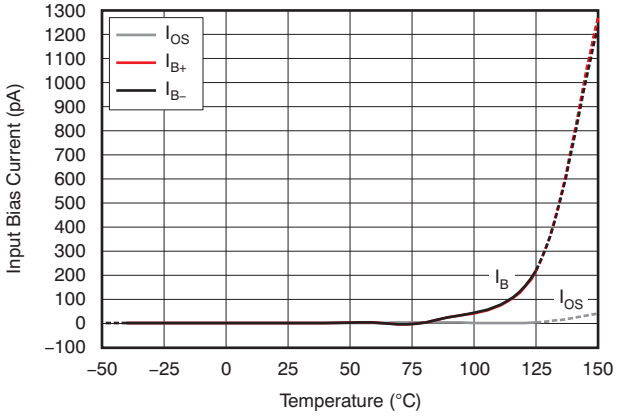


Figure 5.

QUIESCENT CURRENT versus SUPPLY VOLTAGE

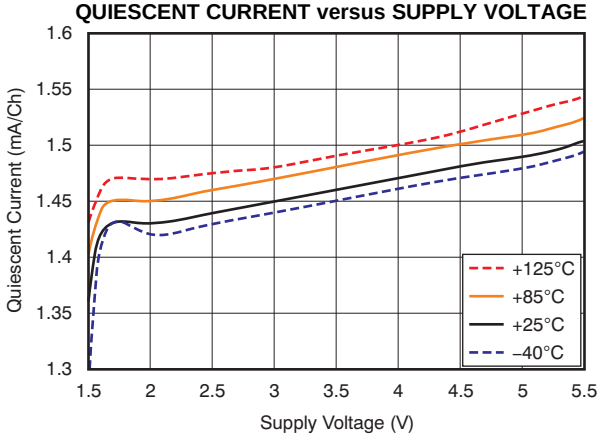


Figure 6.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION HISTOGRAM

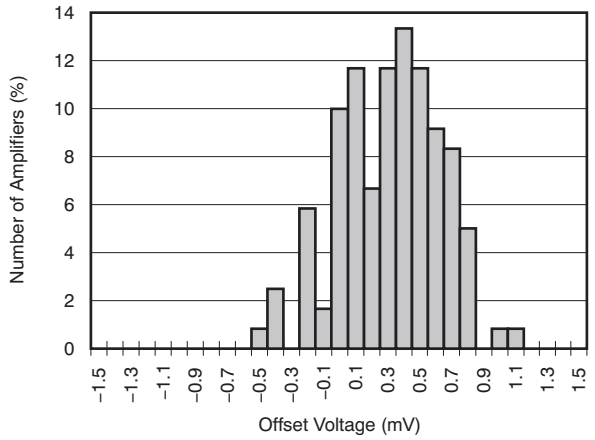


Figure 7.

OFFSET VOLTAGE versus COMMON-MODE VOLTAGE

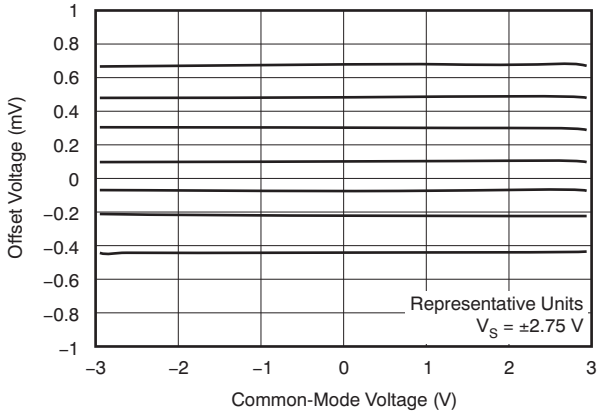


Figure 8.

INPUT VOLTAGE NOISE SPECTRAL DENSITY versus FREQUENCY

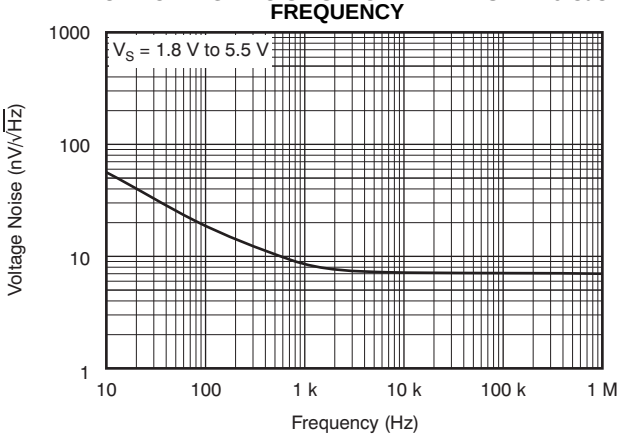


Figure 9.

0.1 Hz TO 10 Hz INPUT VOLTAGE NOISE

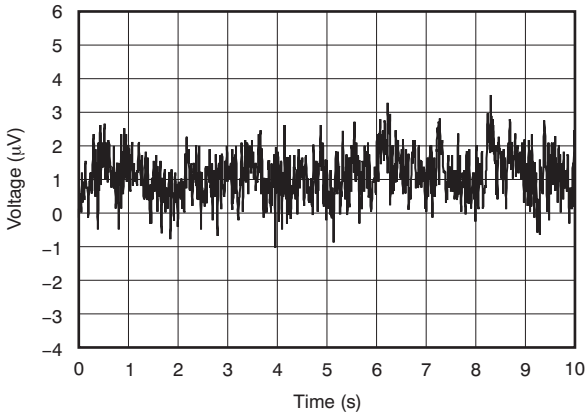


Figure 10.

CLOSED-LOOP GAIN versus FREQUENCY

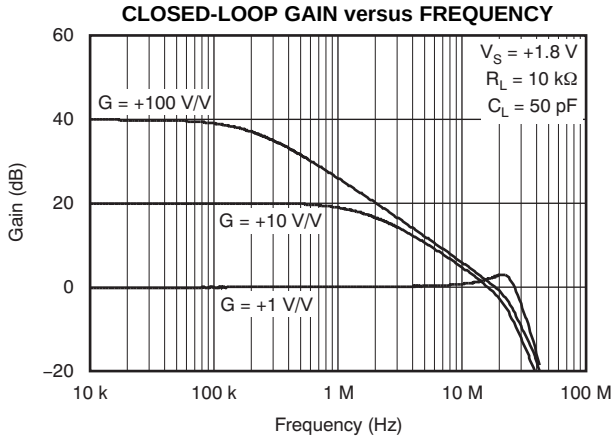


Figure 11.

CLOSED-LOOP GAIN versus FREQUENCY

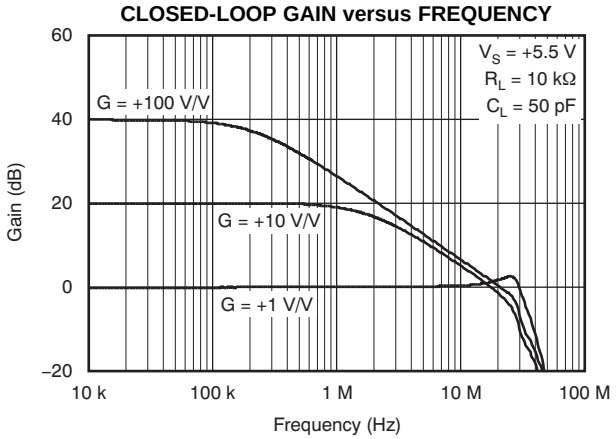


Figure 12.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

MAXIMUM OUTPUT VOLTAGE versus FREQUENCY

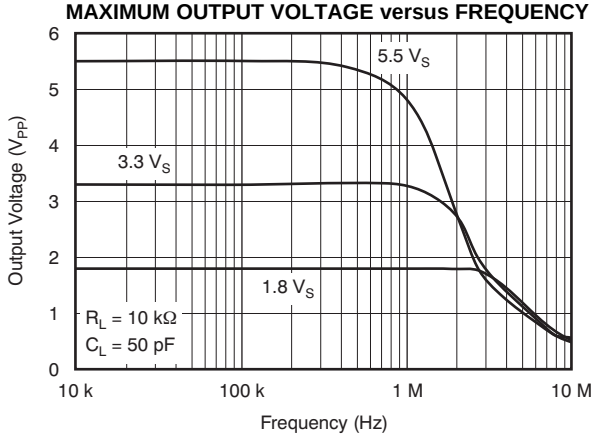


Figure 13.

OUTPUT VOLTAGE SWING versus OUTPUT CURRENT

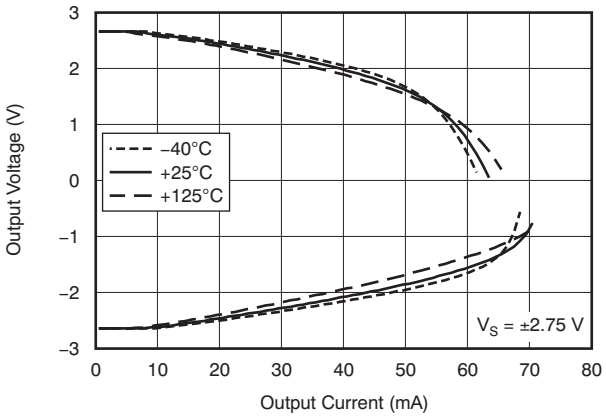


Figure 14.

OPEN-LOOP OUTPUT IMPEDANCE versus FREQUENCY

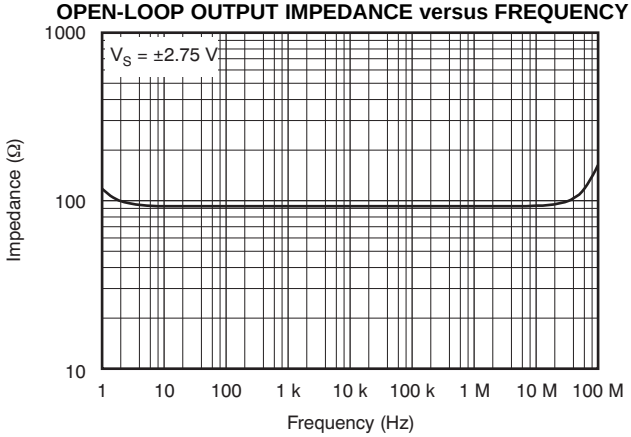


Figure 15.

SMALL-SIGNAL OVERSHOOT versus LOAD CAPACITANCE

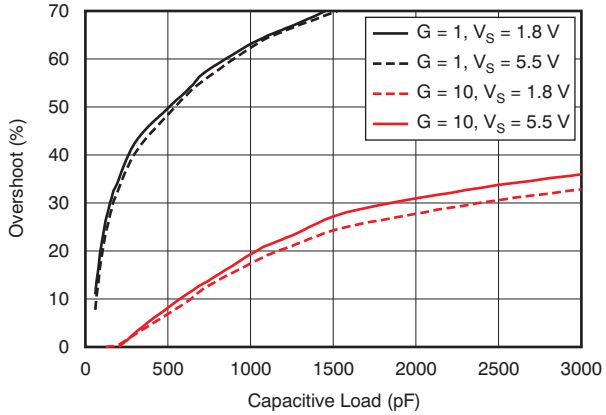


Figure 16.

THD+N versus AMPLITUDE

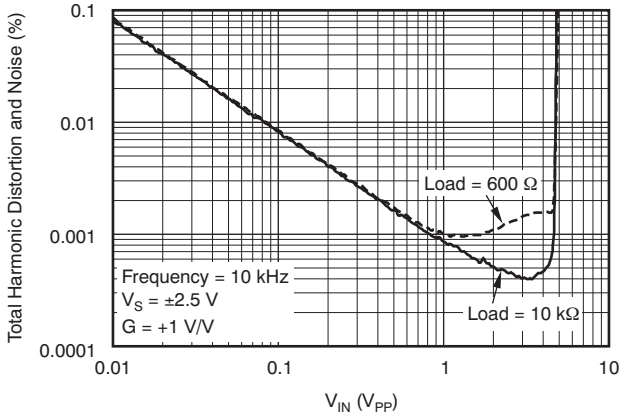


Figure 17.

THD+N versus FREQUENCY

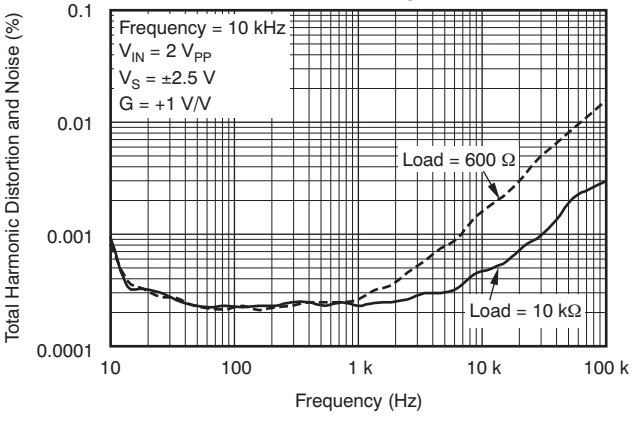


Figure 18.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

THD+N versus FREQUENCY

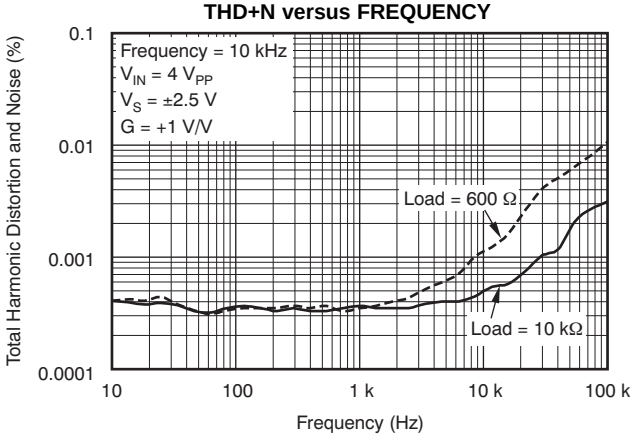


Figure 19.

CHANNEL SEPARATION versus FREQUENCY (for Dual)

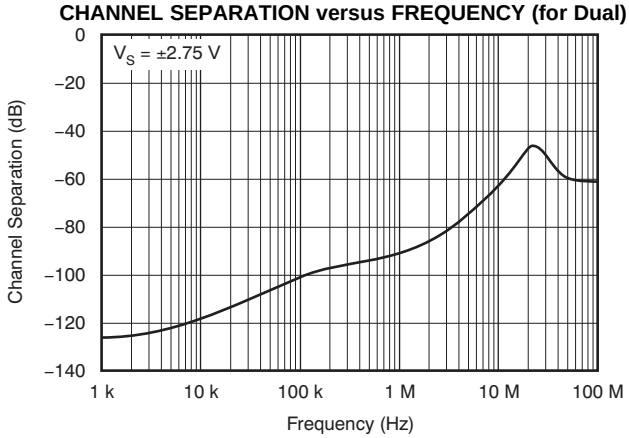


Figure 20.

SLEW RATE versus SUPPLY VOLTAGE

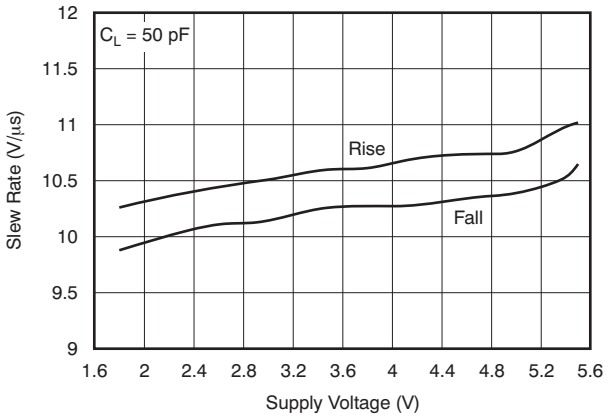


Figure 21.

SMALL-SIGNAL STEP RESPONSE

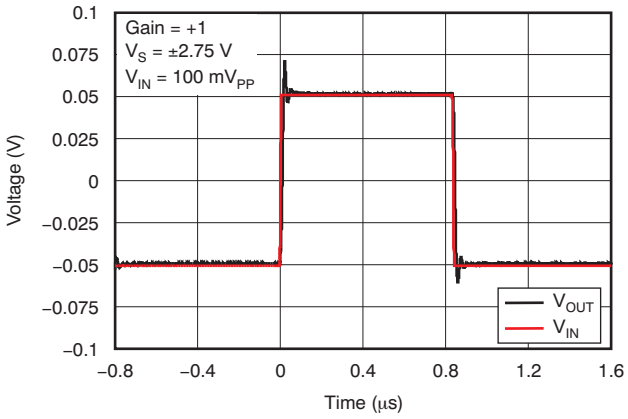


Figure 22.

SMALL-SIGNAL STEP RESPONSE

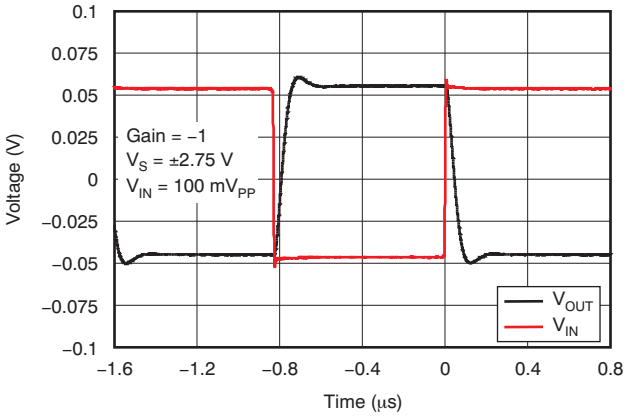


Figure 23.

LARGE-SIGNAL STEP RESPONSE versus TIME

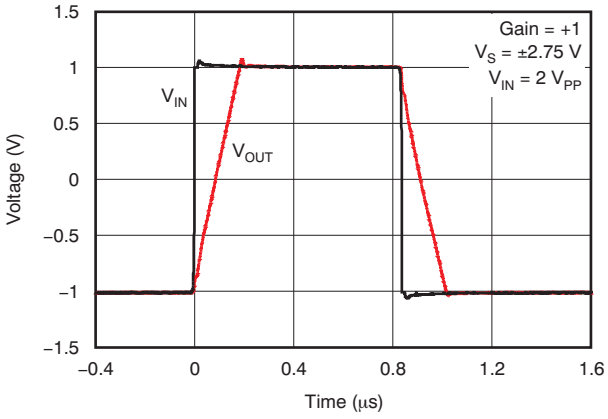


Figure 24.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

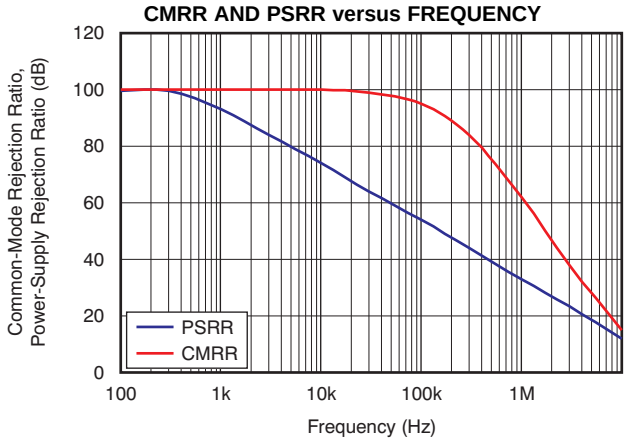


Figure 25.

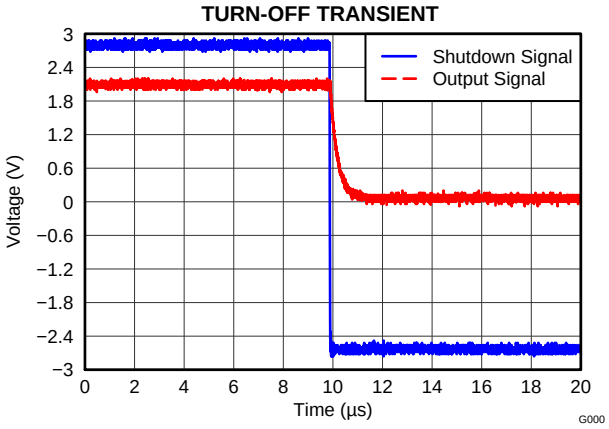


Figure 26.

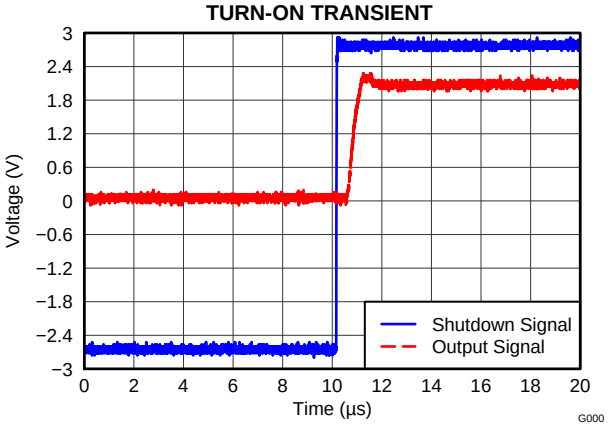


Figure 27.

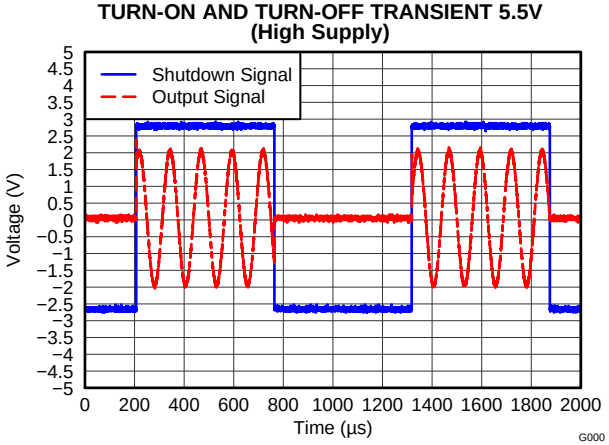


Figure 28.

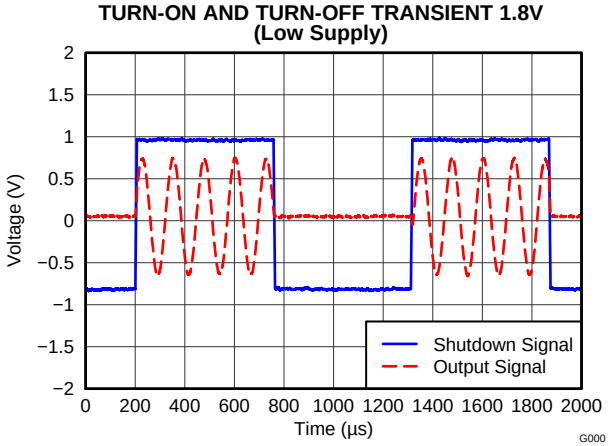


Figure 29.

PRODUCT PREVIEW

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA322-Q1 family of operational amplifiers are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 µF to 0.1 µF). The specifications of these amplifiers fully apply from 1.8 V to 5.5 V and over the extended temperature range of –40°C to 125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

INPUT AND ESD PROTECTION

The OPA322-Q1 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, there is no need for a limiting resistor. Figure 30 shows how one may add a series input resistor (R_S) to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; keep the value minimal in noise-sensitive applications.

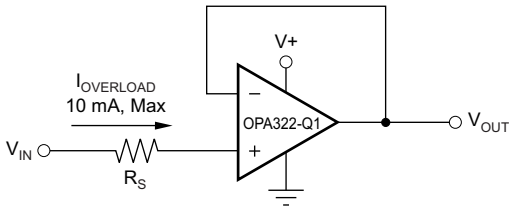


Figure 30. Input Current Protection

PHASE REVERSAL

The design of the OPA322-Q1 operational amplifiers is for immunity to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 31 shows the input voltage exceeding the supply voltage without any phase reversal.

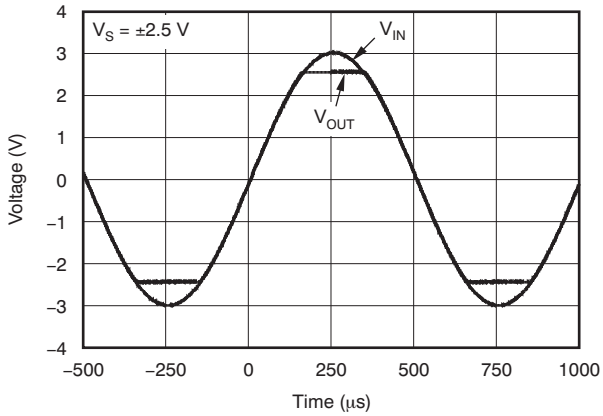
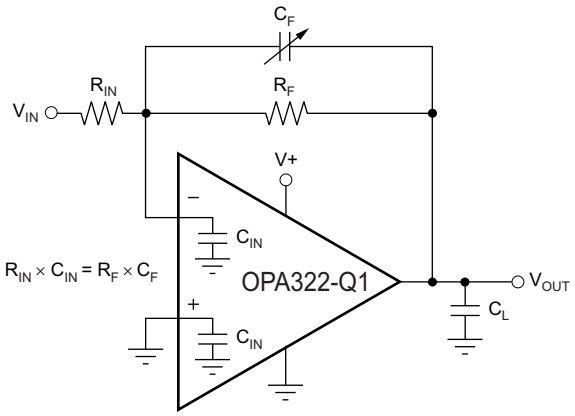


Figure 31. No Phase Reversal

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the OPA322-Q1 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher-impedance networks.



NOTE: Where C_{IN} is equal to the OPA322-Q1 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 32. Feedback Capacitor Improves Dynamic Performance

TI suggests the use of a variable capacitor for the feedback capacitor, because input capacitance may vary between operational amplifiers and layout capacitance is difficult to determine. For the circuit shown in Figure 32, choose the value of the variable feedback capacitor so that the input resistance times the input capacitance of the OPA322-Q1 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$R_{IN} \times C_{IN} = R_F \times C_F$

where:

C_{IN} is equal to the OPA322-Q1 input capacitance (sum of differential and common-mode) plus the layout capacitance.

Adjust the capacitor value until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the input pins are likely to be the most susceptible. The OPA322-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. The input filter proviede both common-mode and differential-mode filtering. The filter design is for a cutoff frequency of approximately 580 MHz (–3 dB), with a rolloff of 20 dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA322-Q1 common-source output stage is approximately 90 Ω. Connecting the operational amplifier with feedback significantly reduces this value by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA322-Q1 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the operational amplifier drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322-Q1 has excellent capacitive load-drive capability for an operational amplifier with its bandwidth.

PRODUCT PREVIEW

CAPACITIVE LOAD AND STABILITY

The OPA322-Q1 design is for use in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPA322-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322-Q1 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 33. One technique for increasing the capacitive load-drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 34.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is the creation of a voltage divider with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, R_L = 10 kΩ and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA322-Q1 is able to drive, the error increases to 7.5%.

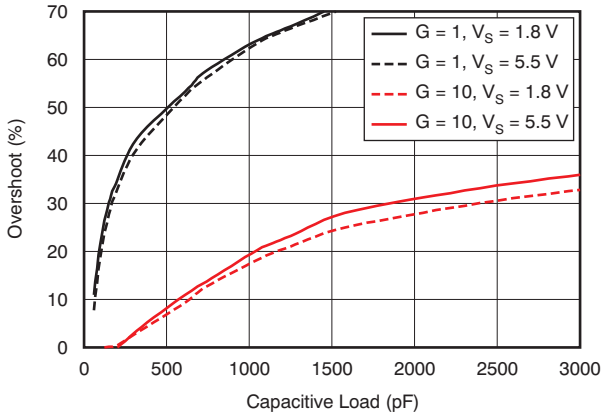


Figure 33. Small-Signal Overshoot versus Capacitive Load (100-mV$_{PP}$ Output Step)

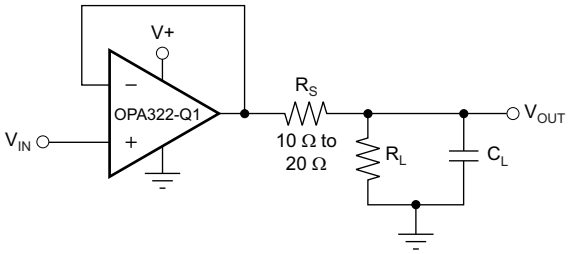


Figure 34. Improving Capacitive Load Drive

PRODUCT PREVIEW

OVERLOAD RECOVERY TIME

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications with a requirement for small-signals amplification in the presence of large transients. Figure 35 and Figure 36 show the positive and negative overload recovery times of the OPA322-Q1, respectively. In both cases, the time elapsed before the OPA322-Q1 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

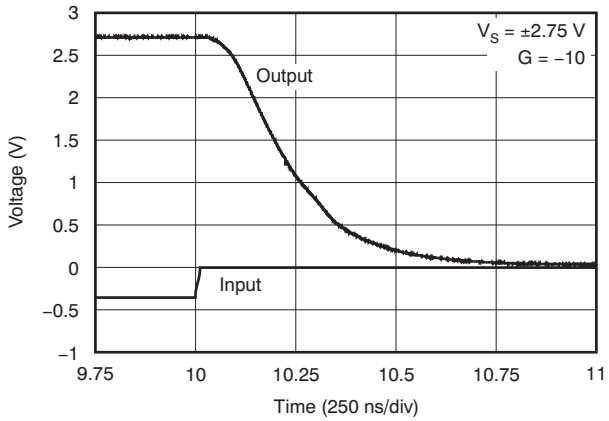


Figure 35. Positive Recovery Time

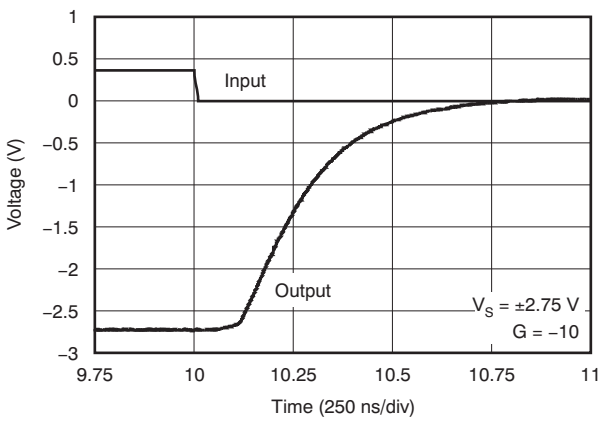


Figure 36. Negative Recovery Time

SHUTDOWN FUNCTION

The reference for the SHDN (enable) pin function of the OPAx322S-Q1 is to the negative supply voltage of the operational amplifier. A logic-level high enables the operational amplifier. The definition of a valid logic high is voltage [(V+) – 0.1 V], up to (V+), applied to the SHDN pin. The definition of a valid logic low is [(V–) + 0.1 V], down to (V–), applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. Drive this pin or connect it either to a valid high or low voltage; do not leave it as an open circuit.

The logic input is a high-impedance CMOS input. Control of dual operational amplifier versions is independent, and that of quad operational amplifier versions is in pairs with logic inputs. For battery-operated applications, use of this feature may greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx322S-Q1 to operate as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases with increased load resistance. Ensuring shutdown (disable) within a specific shutdown time requires the specified 10-kΩ load to mid-supply (V_S / 2). Using the OPAx322S-Q1 without a load significantly increases the resulting turn-off time.

GENERAL LAYOUT GUIDELINES

The OPA322-Q1 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed circuit board (PCB) layout practices. Connect the bypass capacitors between each supply pin and ground as close to the device as possible. Design the bypass capacitor traces for minimum inductance.

LEADLESS DFN PACKAGE

The OPA2322-Q1 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0,8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). The absence of external leads also eliminates bent-lead issues.

PRODUCT PREVIEW

Standard PCB-assembly techniques allow for easy mounting of the DFN package. See the application reports, *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com. **Connect the exposed leadframe die pad on the bottom of the DFN package to the most-negative potential (V–).** The dimension of the exposed thermal die pad is 2 mm × 1,2 mm and is centered.

APPLICATION EXAMPLES

ACTIVE FILTER

The OPA322-Q1 is well-suited for active filter applications that require a wide-bandwidth, fast-slew-rate, low-noise, single-supply operational amplifier. Figure 37 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The component selection provides a maximally-flat Butterworth response. Beyond the cutoff frequency, rolloff is –40 dB/decade. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is its inverted output, relative to the input. If this inversion is not required, or not desired, a one can achieve a noninverting output through one of these options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (shown in Figure 38).

One can quickly accomplish MFB and Sallen-Key, low-pass and high-pass filter synthesis using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

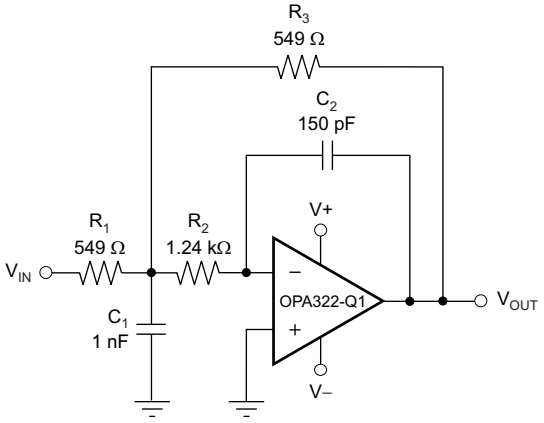


Figure 37. Second-Order Butterworth 500-kHz Low-Pass Filter

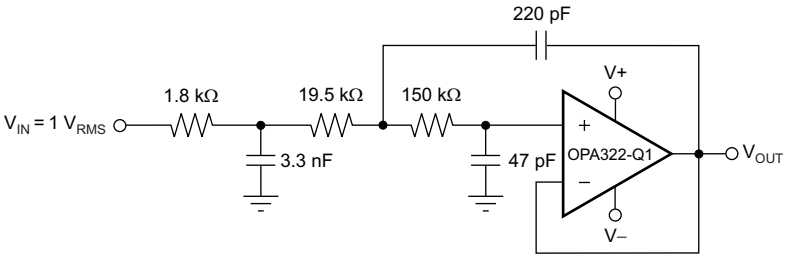


Figure 38. OPA322-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2322AQDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

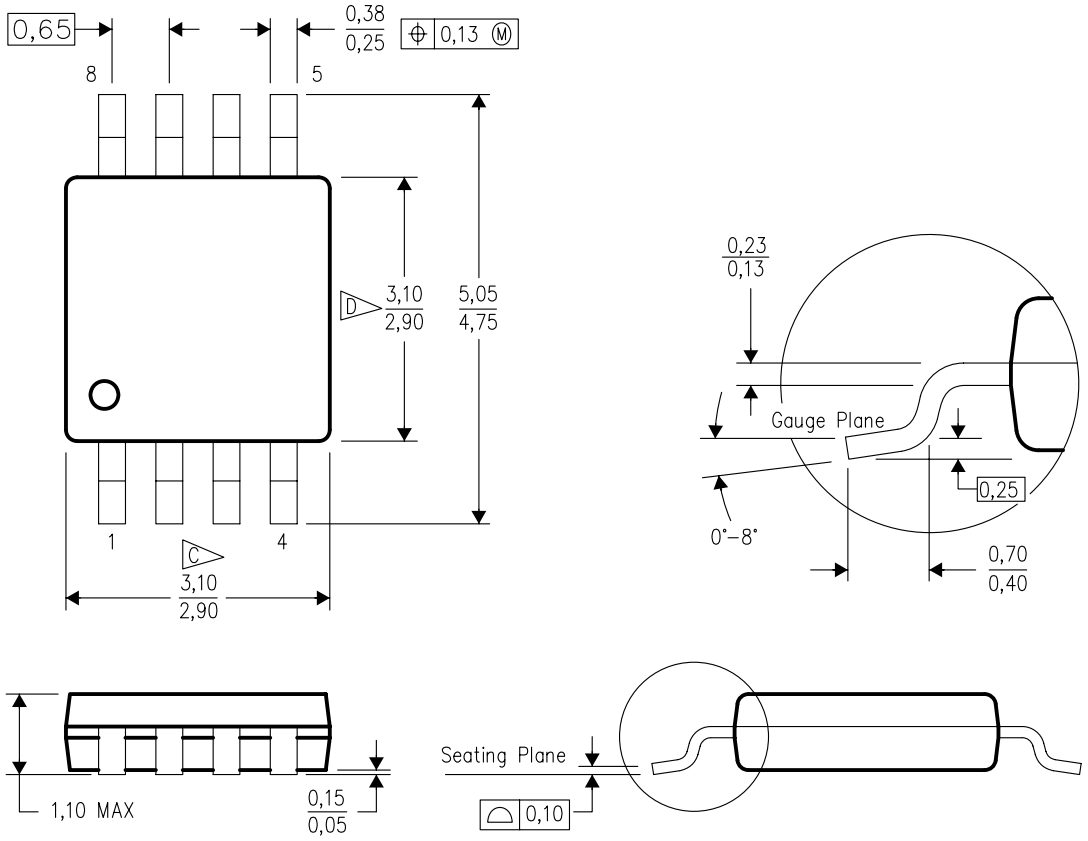
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265