



# N-Channel NexFET™ Power MOSFET

### **FEATURES**

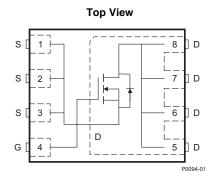
- Ultralow Q<sub>q</sub> and Q<sub>qd</sub>
- Low Thermal Resistance
- Avalanche Rated
- SON 5-mm × 6-mm Plastic Package

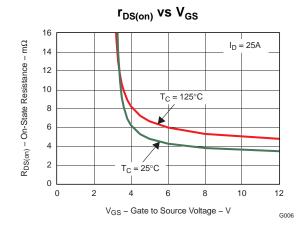
#### **APPLICATIONS**

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

### **DESCRIPTION**

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.





#### **PRODUCT SUMMARY**

$V_{DS}$	Drain-to-source voltage	25	V	
$Q_g$	Gate charge, total (4.5 V)	6.7	nC	
$Q_{gd}$	Gate charge, gate-to-drain 1.9		nC	
-	Drain-to-source on-resistance	V <sub>GS</sub> = 4.5 V	5.4	mΩ
r <sub>DS(on)</sub>	Diam-to-source on-resistance	V <sub>GS</sub> = 10 V	3.6	mΩ
V <sub>GS(th)</sub>	Threshold voltage	1.8	V	

#### **ORDERING INFORMATION**

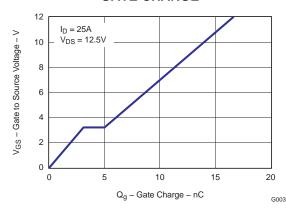
Device	Package	Media	Qty	Ship
CSD16408Q5	SON 5-mm × 6-mm plastic package	13-inch (33-cm) reel	2500	Tape and reel

#### **ABSOLUTE MAXIMUM RATINGS**

T <sub>A</sub> = 2	5°C unless otherwise stated	VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	25	V
$V_{GS}$	Gate-to-source voltage	-12 to 16	V
	Continuous drain current, T <sub>C</sub> = 25°C	113	Α
I <sub>D</sub>	Continuous drain current <sup>(1)</sup>	22	Α
$I_{DM}$	Pulsed drain current, T <sub>A</sub> = 25°C <sup>(2)</sup>	141	Α
$P_D$	Power dissipation <sup>(1)</sup>	3.1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating junction and storage temperature range	-55 to 150	°C
E <sub>AS</sub>	Avalanche energy, single-pulse $I_D$ = 23 A, L = 0.1 mH, $R_G$ = 25 $\Omega$	126	mJ

- (1) Typical  $R_{\theta JA}$  = 41°C/W on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration  $\leq$ 300  $\mu$ s, duty cycle  $\leq$ 2%

### **GATE CHARGE**



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#### **ELECTRICAL CHARACTERISTICS**

 $T_{A} = 25^{\circ}C$  unless otherwise stated

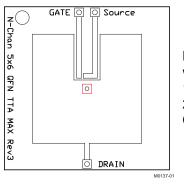
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static C	haracteristics				·	
BV <sub>DSS</sub>	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25			V
I <sub>DSS</sub>	Drain-to-source leakage	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V			1	μА
I <sub>GSS</sub>	Gate-to-source leakage	$V_{DS} = 0 \text{ V}, V_{GS} = -12 \text{ V to } 16 \text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.4	1.8	2.1	V
_	Drain-to-source on-resistance	$V_{GS} = 4.5 \text{ V}, I_D = 25 \text{ A}$		5.4	6.8	mΩ
r <sub>DS(on)</sub>	Drain-to-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$		3.6	4.5	mΩ
9 <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		60		S
Dynamic	c Characteristics		•		·	
C <sub>ISS</sub>	Input capacitance			990	1300	pF
Coss	Output capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 12.5 V , f = 1 MHz		760	1000	pF
C <sub>RSS</sub>	Reverse transfer capacitance			75	100	pF
R <sub>g</sub>	Series gate resistance			0.8	1.6	Ω
Qg	Gate charge total (4.5 V)			6.7	8.9	nC
Q <sub>gd</sub>	Gate charge, gate-to-drain	V 40.5 V 1 05.A		1.9		nC
Q <sub>gs</sub>	Gate charge, gate-to-source	$V_{DS} = 12.5 \text{ V}, I_{D} = 25 \text{ A}$		3.1		nC
Q <sub>g(th)</sub>	Gate charge at Vth			1.8		nC
Q <sub>OSS</sub>	Output charge	V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V		15.7		nC
t <sub>d(on)</sub>	Turnon delay time			11.3		ns
t <sub>r</sub>	Rise time	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 4.5 V,		25		ns
t <sub>d(off)</sub>	Turnoff delay time	$I_D = 20 \text{ A}, R_G = 2 \Omega$		11		ns
t <sub>f</sub>	Fall time		10.8			ns
Diode C	haracteristics		•			
V <sub>SD</sub>	Diode forward voltage	I <sub>S</sub> = 25 A, V <sub>GS</sub> = 0 V		0.8	1	V
Q <sub>rr</sub>	Reverse recovery charge	$V_{DD} = 13 \text{ V}, I_F = 2 \text{ 5A}, di/dt = 300 \text{ A/}\mu\text{s}$		17		nC
t <sub>rr</sub>	Reverse recovery time	$V_{DD} = 13 \text{ V}, I_F = 25 \text{ A}, di/dt = 300 \text{ A}/\mu\text{s}$		21		ns

### THERMAL CHARACTERISTICS

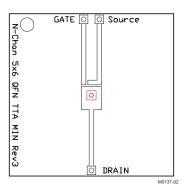
· A - 20 (	5 direct direct whole stated				
	PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)</sup> (2)			51	°C/W

 <sup>(1)</sup> R<sub>θJC</sub> is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.





Max  $R_{\theta JA} = 51^{o}C/W$  when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 125^{o} C/W$  when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

### TYPICAL MOSFET CHARACTERISTICS

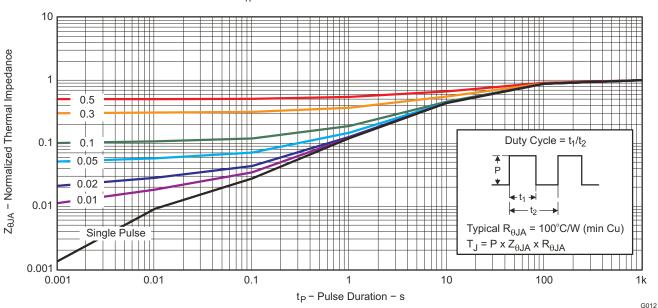


Figure 1. Transient Thermal Impedance



# TYPICAL MOSFET CHARACTERISTICS (continued)

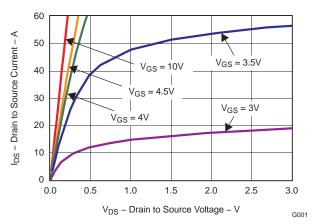


Figure 2. Saturation Characteristics

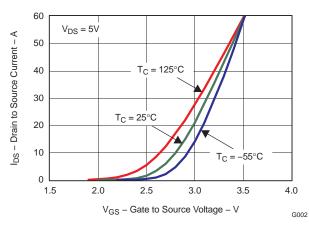


Figure 3. Transfer Characteristics

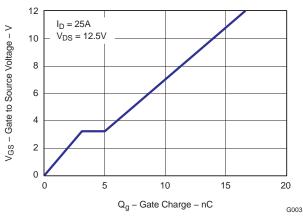


Figure 4. Gate Charge

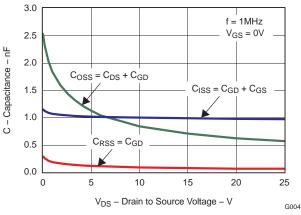


Figure 5. Capacitance

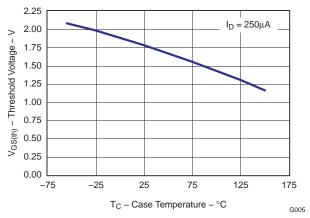


Figure 6. Threshold Voltage vs. Temperature

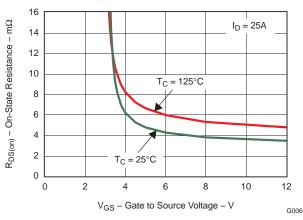


Figure 7. On-State Resistance vs. Gate-to-Source Voltage



## **TYPICAL MOSFET CHARACTERISTICS (continued)**

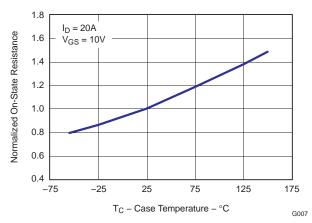


Figure 8. Normalized On-State Resistance vs. Temperature

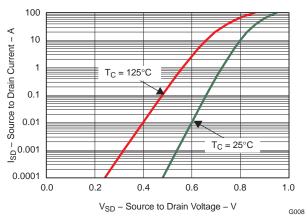


Figure 9. Typical Diode Forward Voltage

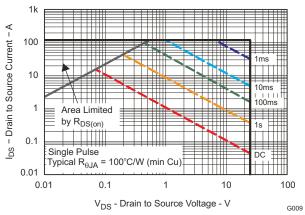


Figure 10. Maximum Safe Operating Area

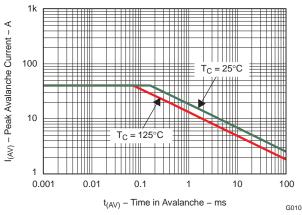


Figure 11. Single-Pulse Unclamped Inductive Switching

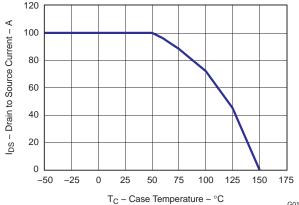
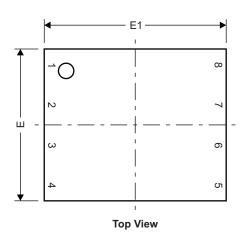


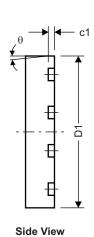
Figure 12. Maximum Drain Current vs. Temperature

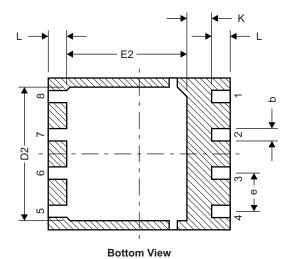


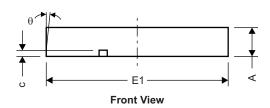
## **MECHANICAL DATA**

# **Q5 Package Dimensions**





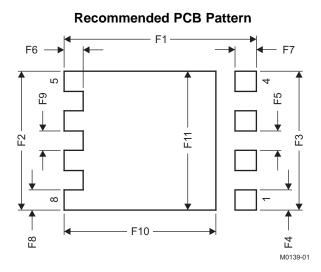




M0140-01

DIM	MILLIM	ETERS	INCHES		
DIW	MIN	MAX	MIN	MAX	
Α	0.950	1.050	0.037	0.039	
b	0.360	0.460	0.014	0.018	
С	0.150	0.250	0.006	0.010	
c1	0.150	0.250	0.006	0.010	
D1	4.900	5.100	0.193	0.201	
D2	4.320	4.520	0.170	0.178	
E	4.900	5.100	0.193	0.201	
E1	5.900	6.100	0.232	0.240	
E2	3.920	4.12	0.154	0.162	
е	1.27	typ	0.0	)50	
L	0.510	0.710	0.020	0.028	
θ	0.00	_	_	_	

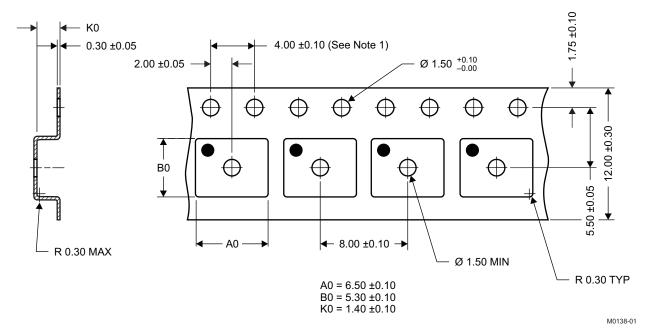




DIM	MILLIM	IETERS	INC	HES
DIN	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

### **Q5 Tape and Reel Information**



#### Notes:

- 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm, unless otherwise specified.
- 5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
- 6. MSL1 260°C (IR and convection) PbF reflow compatible



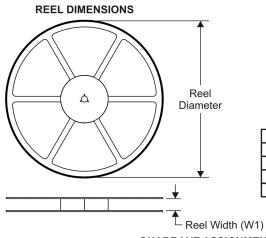
## **REVISION HISTORY**

C	Changes from Revision Original (October 2009) to Revision A						
•	Deleted environmental bullets from features list	1					
•	Deleted package marking section from end of data sheet	7					

# PACKAGE MATERIALS INFORMATION

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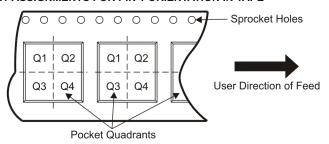
## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

	Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
I	CSD16408Q5	SON	DQH	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

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#### \*All dimensions are nominal

I	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
I	CSD16408Q5	SON	DQH	8	2500	335.0	335.0	32.0

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