

SLPS255A - FEBRUARY 2010-REVISED JULY 2010

30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD17310Q5A

FEATURES

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- · Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

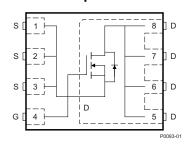
APPLICATIONS

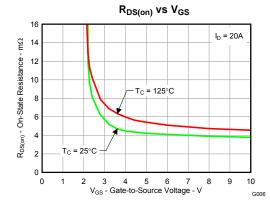
- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.







PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	30		
Q_g	Gate Charge Total (4.5V)	8.9		nC
Q_{gd}	Gate Charge Gate to Drain	2.1		nC
		$V_{GS} = 3V$	5.7	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V 4.5		mΩ
		V _{GS} = 8V	3.9	mΩ
V _{GS(th)}	Threshold Voltage	1.3		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship	
CSD17310Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel	

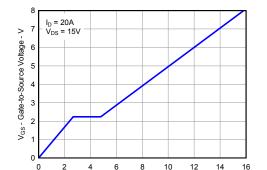
ABSOLUTE MAXIMUM RATINGS

T _A = 2	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	٧
V_{GS}	Gate to Source Voltage	+10 / -8	٧
	Continuous Drain Current, T _C = 25°C	100	Α
I _D	Continuous Drain Current ⁽¹⁾	21	Α
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	134	Α
P_D	Power Dissipation ⁽¹⁾	3.1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I_D = 58A, L = 0.1mH, R_G = 25 Ω	168	mJ

(1) $R_{\theta JA} = 40^{\circ} \text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

GATE CHARGE

(2) Pulse duration ≤300μs, duty cycle ≤2%



Q_g - Gate Charge - nC

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Cl	haracteristics				,	
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μА
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.9	1.3	1.8	V
		V _{GS} = 3V, I _D = 20A		5.7	7.8	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 20A		4.5	5.9	mΩ
		V _{GS} = 8V, I _D = 20A		3.9	5.1	mΩ
9 _{fs}	Transconductance	$V_{DS} = 15V, I_D = 20A$		85		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance			1200	1560	pF
C _{oss}	Output Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		630	820	pF
C _{rss}	Reverse Transfer Capacitance			59	77	pF
R _G	Series Gate Resistance			0.9	1.8	Ω
Qg	Gate Charge Total (4.5V)			8.9	11.6	nC
Q _{gd}	Gate Charge Gate to Drain	V 45V I 00A		2.1		nC
Q _{gs}	Gate Charge Gate to Source	$V_{DS} = 15V, I_{DS} = 20A$		2.7		nC
Q _{g(th)}	Gate Charge at Vth			1.4		nC
Q _{oss}	Output Charge	V _{DS} = 12.8V, V _{GS} = 0V		15.9		nC
t _{d(on)}	Turn On Delay Time			6.5		ns
t _r	Rise Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 20A,		11.6		ns
t _{d(off)}	Turn Off Delay Time	$R_G = 2\Omega$		15		ns
t _f	Fall Time		5			ns
Diode C	haracteristics					
V _{SD}	Diode Forward Voltage	$I_{SD} = 20A$, $V_{GS} = 0V$		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V 40.0V I 00A di/dt 000A / -		21		nC
t _{rr}	Reverse Recovery Time	V_{DD} = 12.8V, I_F = 20A, di/dt = 300A/ μ s		22		ns

THERMAL CHARACTERISTICS

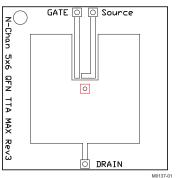
(T_A = 25°C unless otherwise stated)

	PARAMETER	MIN	TYP	MAX	UNIT
R_{\thetaJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1)(2)			51	°C/W

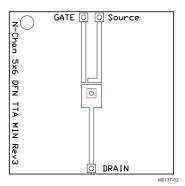
 $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch \times 1.5-inch (3.81-cm \times 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design. Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

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Max $R_{\theta JA} = 51^{\circ} C/W$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 123^{\circ} C/W$ when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

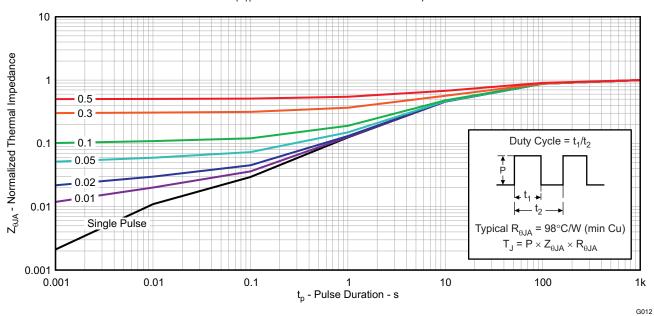


Figure 1. Transient Thermal Impedance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

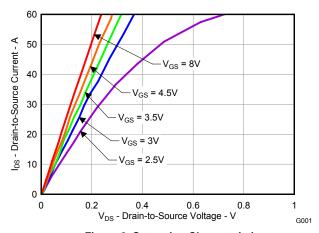


Figure 2. Saturation Characteristics

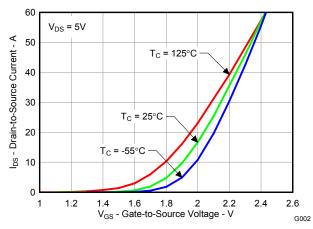


Figure 3. Transfer Characteristics

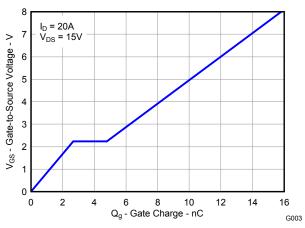


Figure 4. Gate Charge

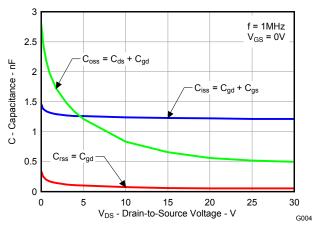


Figure 5. Capacitance

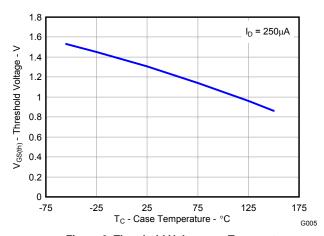


Figure 6. Threshold Voltage vs. Temperature

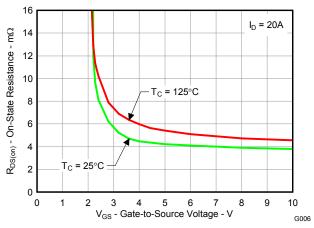


Figure 7. On-State Resistance vs. Gate-to-Source Voltage



TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

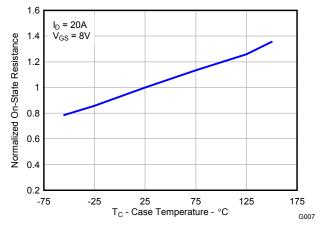


Figure 8. Normalized On-State Resistance vs. Temperature

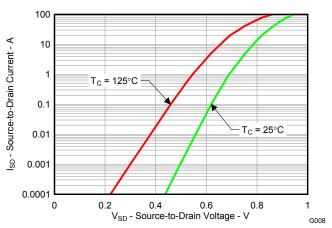


Figure 9. Typical Diode Forward Voltage

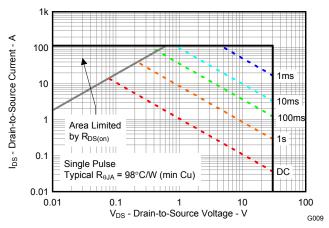


Figure 10. Maximum Safe Operating Area

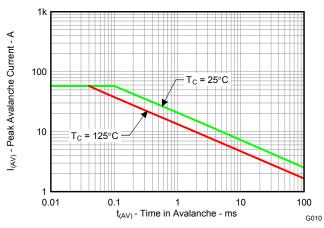


Figure 11. Single Pulse Unclamped Inductive Switching

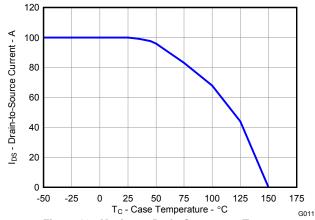
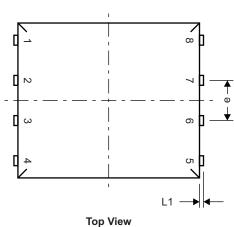


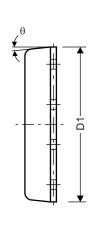
Figure 12. Maximum Drain Current vs. Temperature

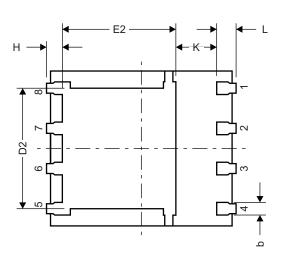


MECHANICAL DATA

Q5A Package Dimensions

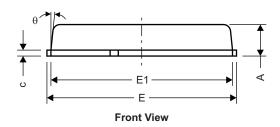






Side View

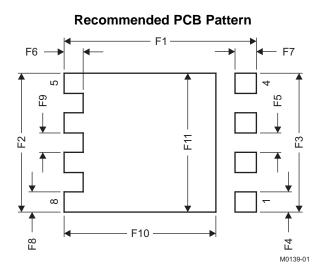
Bottom View



M0135-01

DIM	MILLIMETERS							
DIM	MIN	NOM	MAX					
А	0.90	1.00	1.10					
b	0.33	0.41	0.51					
С	0.20	0.25	0.34					
D1	4.80	4.90	5.00					
D2	3.61	3.81	4.02					
Е	5.90	6.00	6.10					
E1	5.70	5.75	5.80					
E2	3.38	3.58	3.78					
е	1.17	1.27	1.37					
Н	0.41	0.56	0.71					
K	1.10							
L	0.51	0.61	0.71					
L1	0.06	0.13	0.20					
θ	0°		12°					

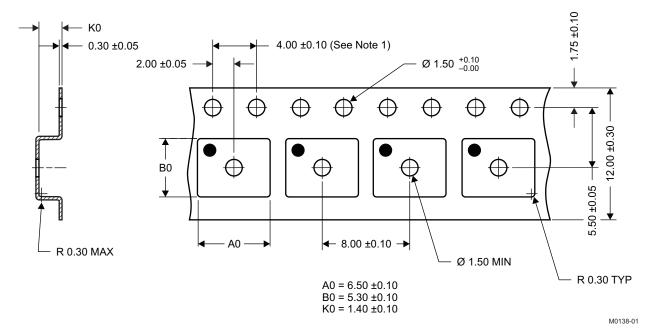




DIM	MILLIN	IETERS	INC	HES
DIIVI	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q5A Tape and Reel Information



Notes:

- 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

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REVISION HISTORY

CI	MAX was blank, DIM H NOM was 0.51 MAX was 0.61 Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible"	Page
•	Updated the Q5A Package Dimensions table. DIM c MAX was 0.30, DIM D2 MAX was 3.96, DIM e MIN was blank MAX was blank, DIM H NOM was 0.51 MAX was 0.61	6
•	Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible"	7
•	Deleted the Package Marking Information section	7

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17310Q5A	SON	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

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*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
CSD17310Q5A	SON	DQJ	8	2500	340.0	340.0	38.0	

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