

## Dual 30-V N-Channel NexFET™ Power MOSFETs

### FEATURES

- Common Source Connection
- Ultra Low Drain to Drain On-Resistance
- Space Saving SON 3.3 x 3.3mm Plastic Package
- Optimized for 5V Gate Drive
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free

### APPLICATIONS

- Adaptor/USB Input Protection for Notebook PCs and Tablets

### DESCRIPTION

The CSD87312Q3E is a 30V common-source, dual N-channel device designed for adaptor/USB input protection. This SON 3.3 x 3.3mm device has low drain to drain on-resistance that minimizes losses and offers low component count for space constrained multi-cell battery charging applications.

### PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$Q_g$	Gate Charge Total (4.5V)	6.3	nC
$Q_{gd}$	Gate Charge Gate to Drain	0.7	nC
$R_{DD(on)}$	Drain to Drain On Resistance (Q1+Q2)	$V_{GS} = 4.5\text{V}$	31 mΩ
		$V_{GS} = 8\text{V}$	27 mΩ
$V_{GS(th)}$	Threshold Voltage	1.0	V

### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD87312Q3E	SON 3.3 x 3.3mm Plastic Package	13-Inch Reel	2500	Tape and Reel

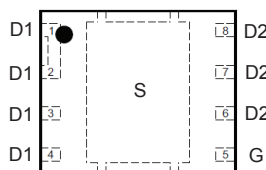
### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	+10/-8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}^{(1)}$	27	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	45	A
$P_D$	Power Dissipation	2.5	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 24\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	29	mJ

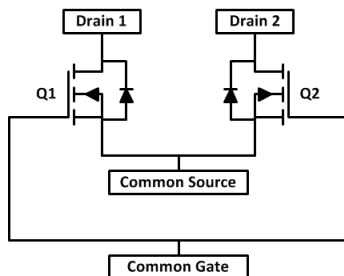
(1) Typical  $R_{\theta JC} = 63^\circ\text{C/W}$  on  $1\text{in}^2$  (2 oz.) on 0.060" thick FR4PCB

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

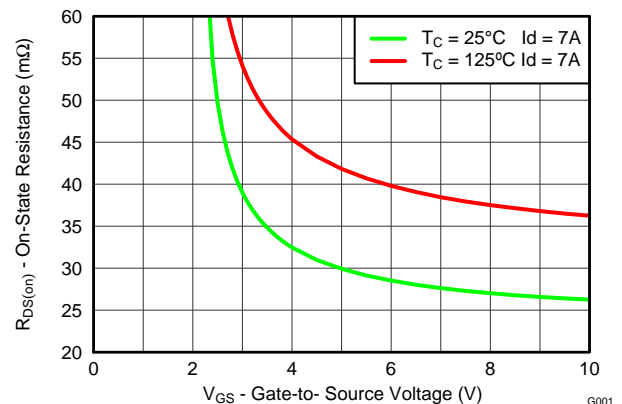
### Top View



### Circuit Image



### $V_{GS}$ vs. $R_{DDon}$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.8	1.0	1.3	V
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	$V_{GS} = 4.5V, I_D = 7A$		31	38	$m\Omega$
		$V_{GS} = 8V, I_D = 7A$		27	33	$m\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 7A$		39		S
<b>Dynamic Characteristics<sup>(1)</sup></b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		960	1250	pF
$C_{oss}$	Output Capacitance			190	247	pF
$C_{riss}$	Reverse Transfer Capacitance			12	16	pF
$R_G$	Series Gate Resistance			5	10	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_D = 7A$		6.3	8.2	nC
$Q_{gd}$	Gate Charge Gate to Drain			0.7		nC
$Q_{gs}$	Gate Charge Gate to Source			1.9		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.0		nC
$Q_{oss}$	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		4.0		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 7A, R_G = 2\Omega$		7.8		ns
$t_r$	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
$t_f$	Fall Time			2.9		ns
<b>Diode Characteristics<sup>(1)</sup></b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 7A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 15V, I_F = 7A, di/dt = 300A/\mu s$		5.3		nC
$t_{rr}$	Reverse Recovery Time			12.2		ns

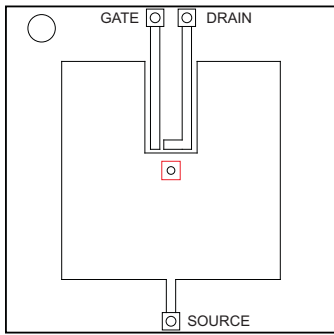
(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

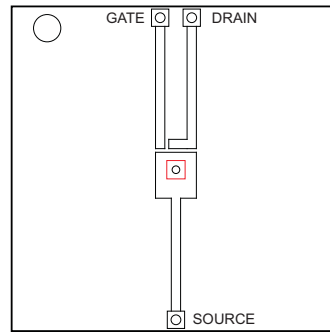
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			4.2	$^\circ\text{C}/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			63	$^\circ\text{C}/W$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 63^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-  
oz. (0.071-mm thick)  
Cu.

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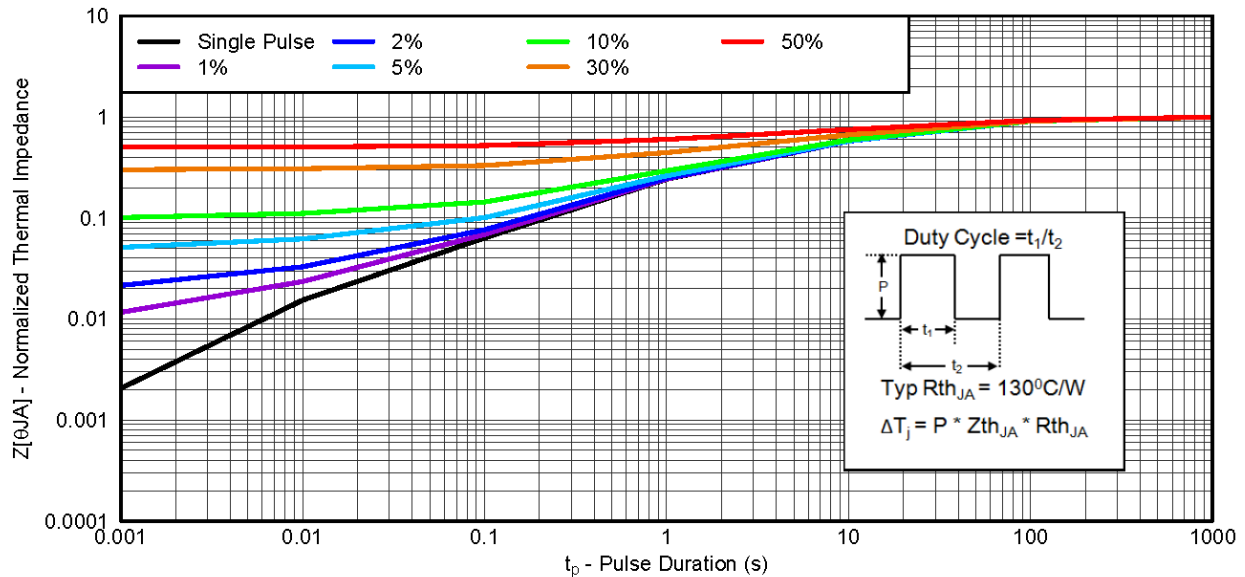


Max  $R_{\theta JA} = 165^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

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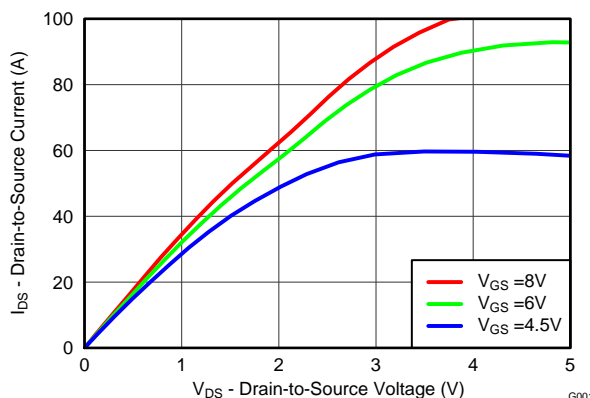
### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



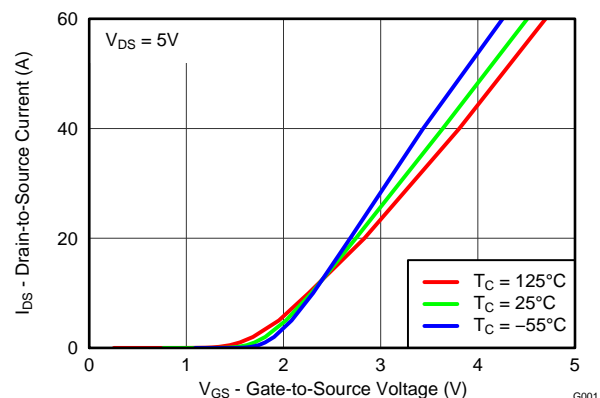
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Figure 1. Transient Thermal Impedance



G001

Figure 2. Saturation Characteristics

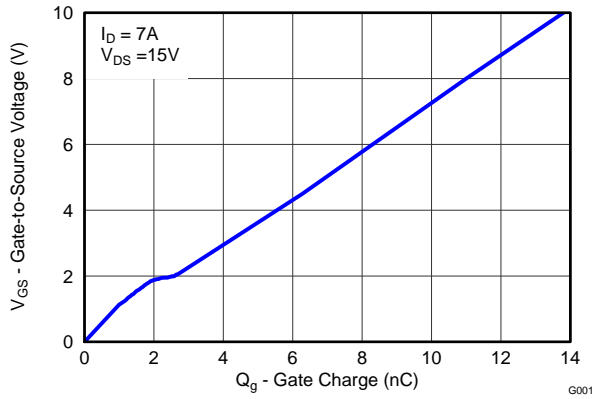


G001

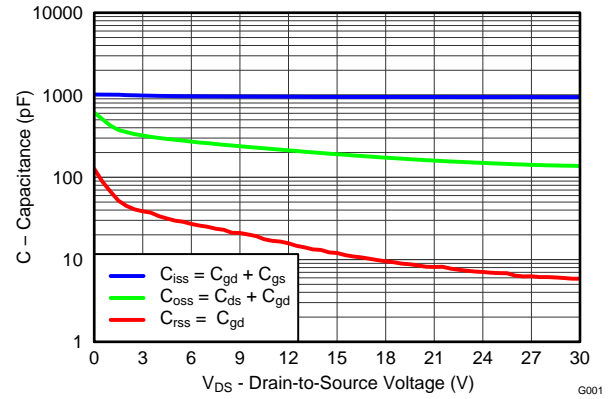
Figure 3. Transfer Characteristics

**TYPICAL MOSFET CHARACTERISTICS (continued)**

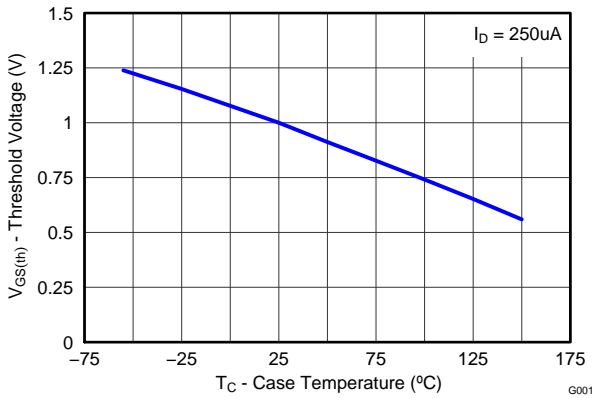
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



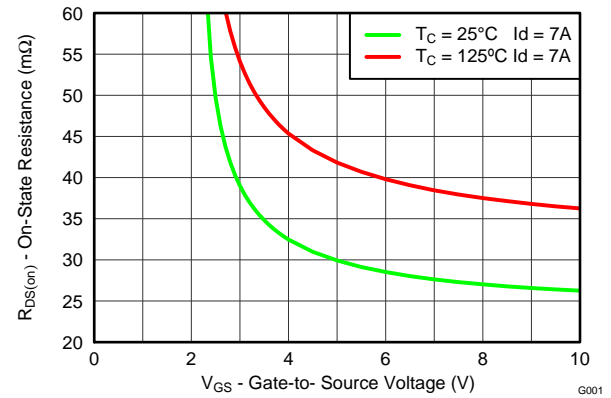
**Figure 4. Gate Charge**



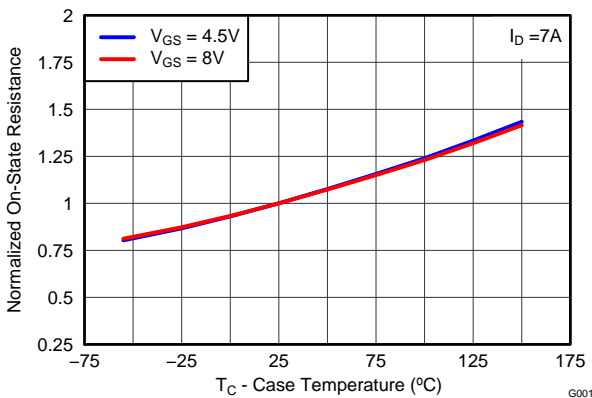
**Figure 5. Capacitance**



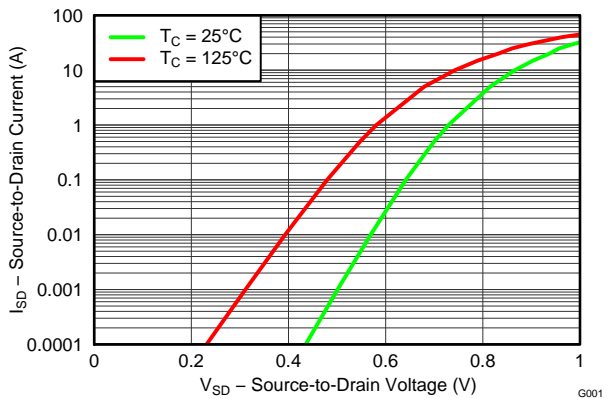
**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**



**Figure 8. Normalized On-State Resistance vs. Temperature**



**Figure 9. Typical Diode Forward Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

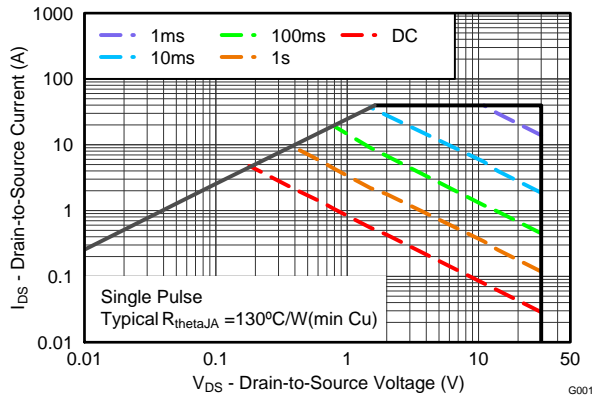


Figure 10. Maximum Safe Operating Area

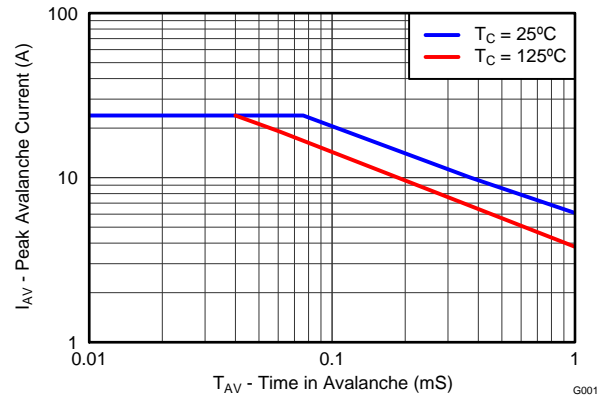


Figure 11. Single Pulse Unclamped Inductive Switching

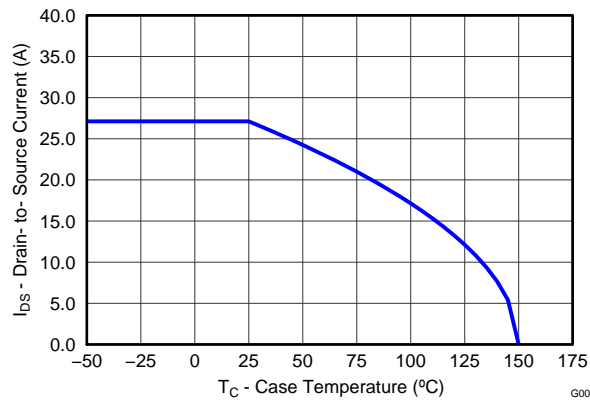
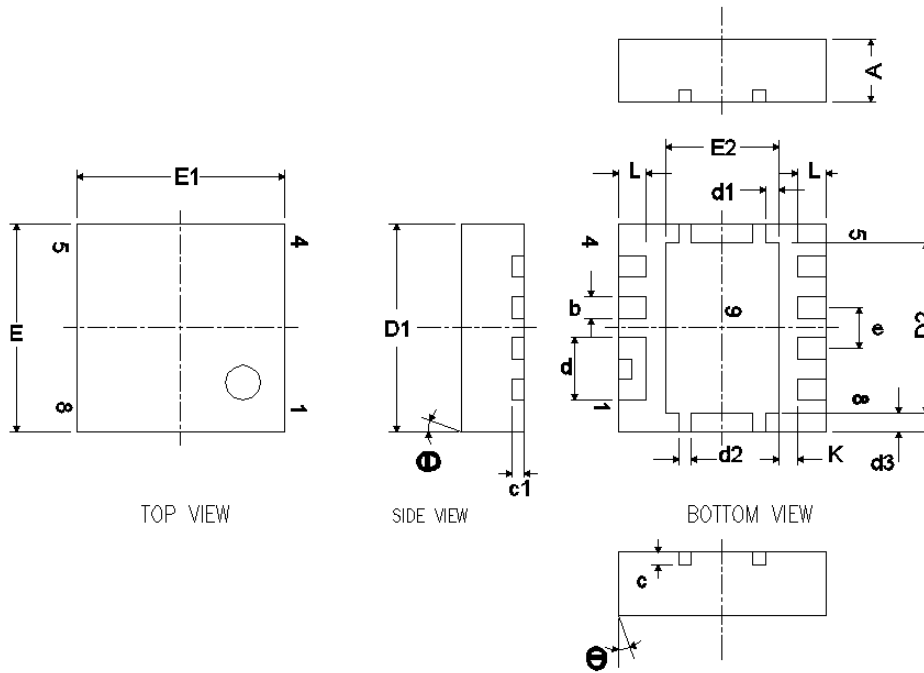


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3E Package Dimensions

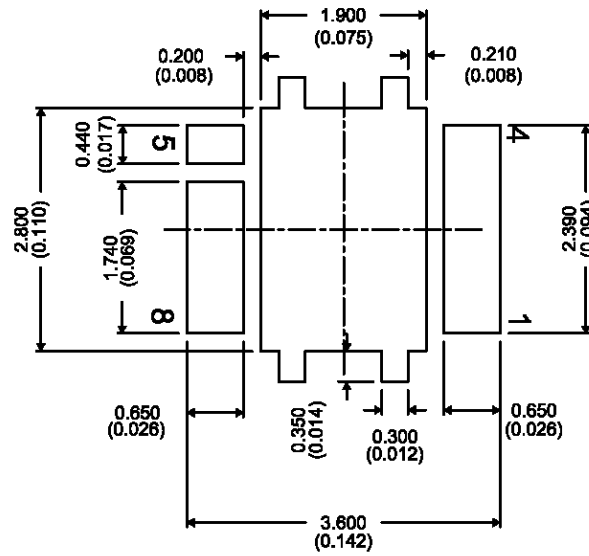


DIM	MILLIMETERS	
	MIN	MAX
A	0.850	1.050
b	0.280	0.400
c	0.150	0.250
c1	0.150	0.250
d	0.940	1.040
d1	0.160	0.260
d2	0.150	0.250
d3	0.250	0.350
D1	3.200	3.400
D2	2.650	2.750
E	3.200	3.400
E1	3.200	3.400
E2	1.750	1.850
e	0.650 TYP	
L	0.400	0.500
theta	0°	-
K	0.300 Typ	

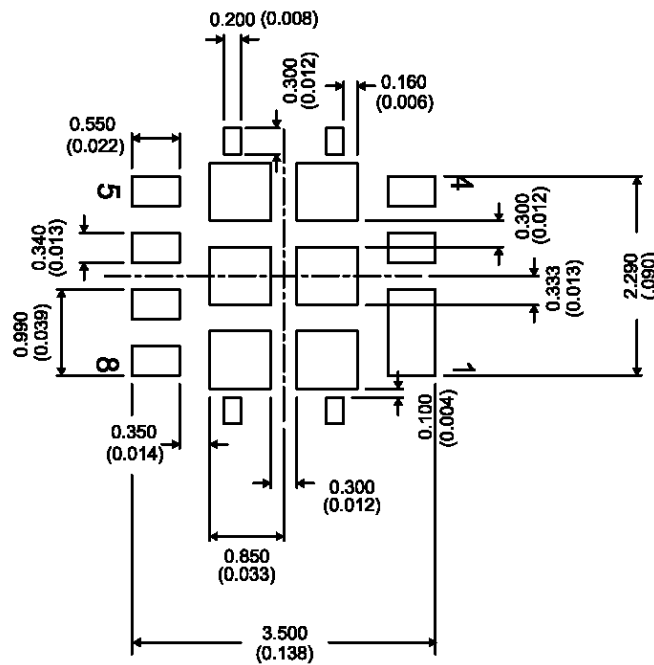
Notes:

1. Pin 1-4: Drain 1
2. Pin 5: Gate
3. Pin 6-8: Drain 2
4. Pin 9: Source

### Recommended PCB Pattern

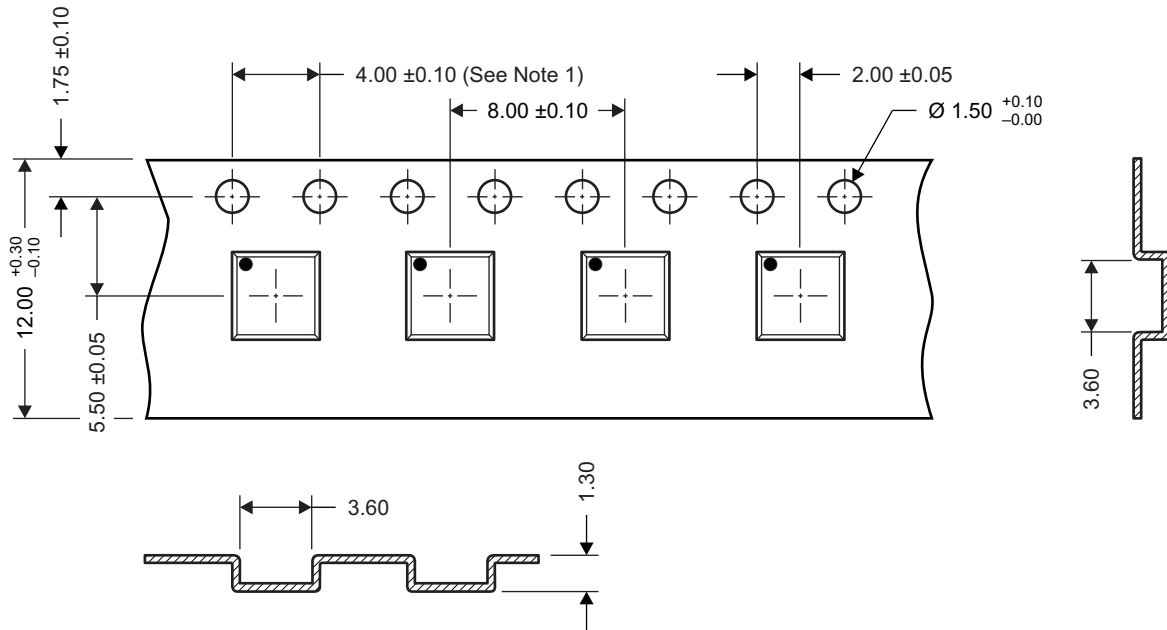


### Recommended Stencil Opening



For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q3E Tape and Reel Information



M0144-01

#### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness:  $0.30 \pm 0.05$ mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CSD87312Q3E	ACTIVE	VSON	DPB	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87312E	<b>Samples</b>
CSD87312Q3E-ASY	PREVIEW	VSON	DPB	8		TBD	Call TI	Call TI	-55 to 150		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87312Q3E	VSON	DPB	8	2500	330.0	16.4	3.6	3.6	1.2	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87312Q3E	VSON	DPB	8	2500	367.0	367.0	38.0

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### Applications

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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