NexFET™ Smart Synchronous Rectifier

FEATURES

- **Typical R_{on} of 0.55 mΩ at 4.5 V_{DD}**
- **Integrated FET Driver**
- **Max Rated Current 80A**
- **High Density – SON 5-mm × 6-mm Footprint**
- **Ultra Low Inductance Package**
- **System Optimized PCB Footprint**
- **TTL IN signal Compatible**
- **Halogen Free**
- **RoHS Compliant – Lead Free Terminal Plating Halogen Free**

APPLICATIONS

- **Secondary Synchronous Rectification for DC/DC Converters**

DESCRIPTION

The CSD43301Q5M NexFET™ Smart Synchronous Rectifier is a highly optimized design for secondary synchronous rectification in a high power high density DC/DC converter. This product integrates the driver IC and an ultra low R_{on} Power MOSFET to complete the synchronous rectification function. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD43301Q5M	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

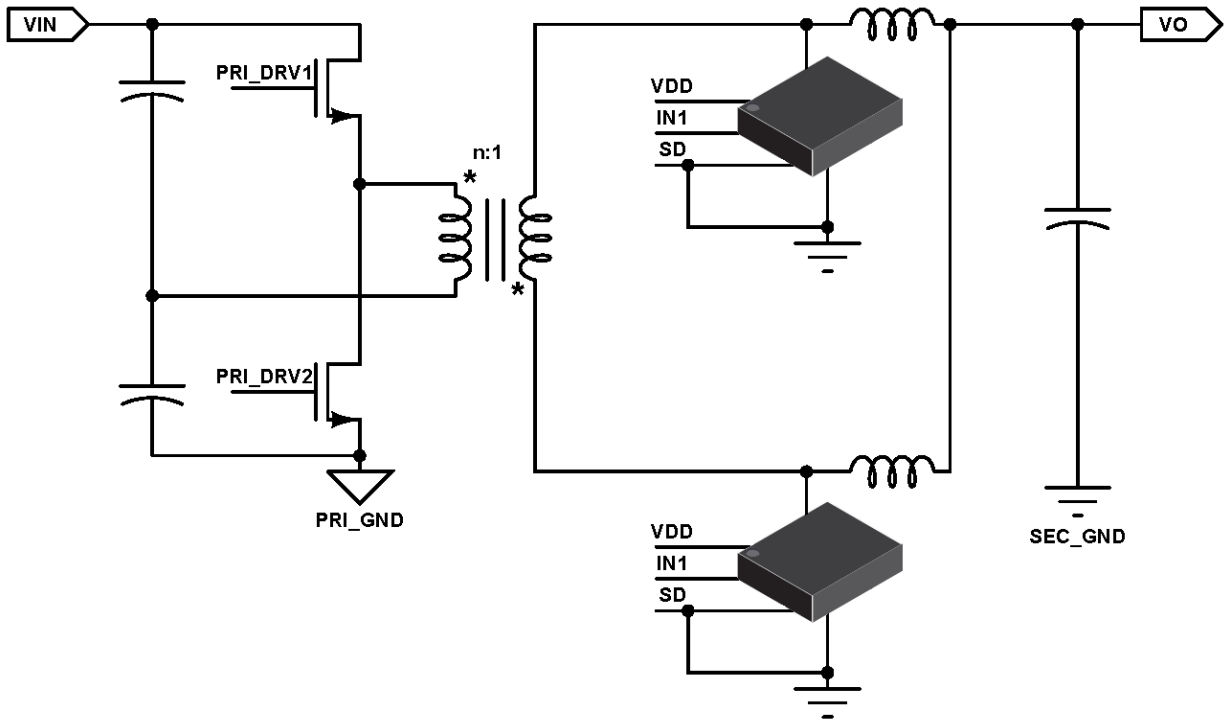


Figure 1. Application Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
DRAIN to P_{GND}		-0.3	12	V
DRAIN to P_{GND} (10ns)		-7	14	V
V_{DD} to P_{GND}		–0.3	8	V
IN, SD to P_{GND}(2)		–0.3	V_{DD} + 0.3	V
ESD Rating	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V
Power Dissipation (P_D)			12	W
Operating Temperature Range, (T_J)		-40	150	°C
Storage Temperature Range, (T_{STG})		–65	150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.
(2) Must not exceed 8V

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Bias Voltage (V_{DD})		4.5	6	V
Input Supply Voltage (V_{IN})			9.6	V
Continuous Output Current (I_{OUT})			80	A
Peak Output Current, (I_{OUT-PK})(1)			120	A
Switching Frequency, (f_{SW})			1500	kHz
Minimum IN Pulse Width		48		ns
Operating Temperature		–40	125	°C

(1) Peak Output Current is applied for t_p = 50µs.

THERMAL INFORMATION

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top of package)			20	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board(1)			2	°C/W

(1) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Device On Resistance					
R_{on}	I_D = 50A, , T_J = 25°C		0.55	0.70	mΩ
	I_D = 50A, T_J = 125°C		0.70	0.88	mΩ
V_{DD}					
Standby Supply Current (I_{DD})	SD = V_{DD} = 5V		153	300	µA
Operating Supply Current (I_{DD})	SD = 0V, IN = 50% Duty Cycle, f_{SW} = 300kHz		29.5		mA
POWER-ON RESET AND UNDER VOLTAGE LOCKOUT					
Power on Reset (V_{DD} Rising)	T_A = 25°C	3.9	4.2	4.5	V
	T_A = -40°C to 140°C	3.7	4.2	4.65	V
UVLO (V_{DD} Falling)		3.45	3.9	4.35	V
Hysteresis		200	300	500	mV
IN					
IN Logic Level High (V_{INH})		2.0			V
IN Logic Level Low (V_{INL})				0.8	V
IN Input Hysteresis			0.8		V
IN to DRAIN Propagation Delay (t_{PDLH})	V_{DD} = 5V, SD = 0, I_D = 25A (See Figure 4)		32		ns
IN to DRAIN Propagation Delay (t_{PDHL})			80		ns
Minimum Pulse Width Changes Output			36	48	ns
SD					
SD Logic Level High Threshold (V_{IH})		2.0			V
SD Logic Level Low Threshold (V_{IL})				0.8	V
Hysteresis			0.8		V
SD to DRAIN Propagation Delay (t_{PDLH})	V_{DD} = 5V, IN = V_{DD}, I_D = 25A (See Figure 5)		80		ns
SD to DRAIN Propagation Delay (t_{PDHL})			32		ns
Dynamic Characteristics					
Output Capacitance (C_O)	V_{DRAIN} = 6V		10	13	nF
Output Charge (Q_O)			54		nC
Body Diode					
Forward Voltage (V_F)	I_D = 40A		0.75	0.85	V
Reverse Recovery Charge (Q_{RR})	I_D = 40A, V_{DRAIN} = 6V, di/dt = 150A/µs		161		nC
Reverse Recovery Time Delay (t_{RR})			72		ns

PIN CONFIGURATION

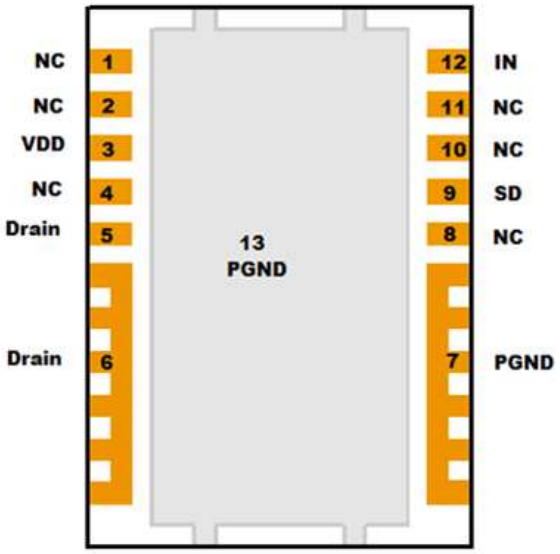


Figure 2. Pin Configuration

PIN DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1,2,4, 8, 10,11	NC	No connect. These should not be used for any electrical connection. These pins should not be connected to each other. Connect to dead copper only.
3	V_{DD}	Supply Voltage for IC
5,6	DRAIN	Drain terminal of internal MOSFET
7	P_{GND}	Power Ground and source terminal of the internal MOSFET. Needs to be connected to Pin 13 on PCB
9	SD	Shut Down Pin: Logic High disables the Device
12	IN	Input for Gate Driver
13	P_{GND}	Power Ground and source terminal of the internal MOSFET. Needs to be connected to Pin 7 on PCB

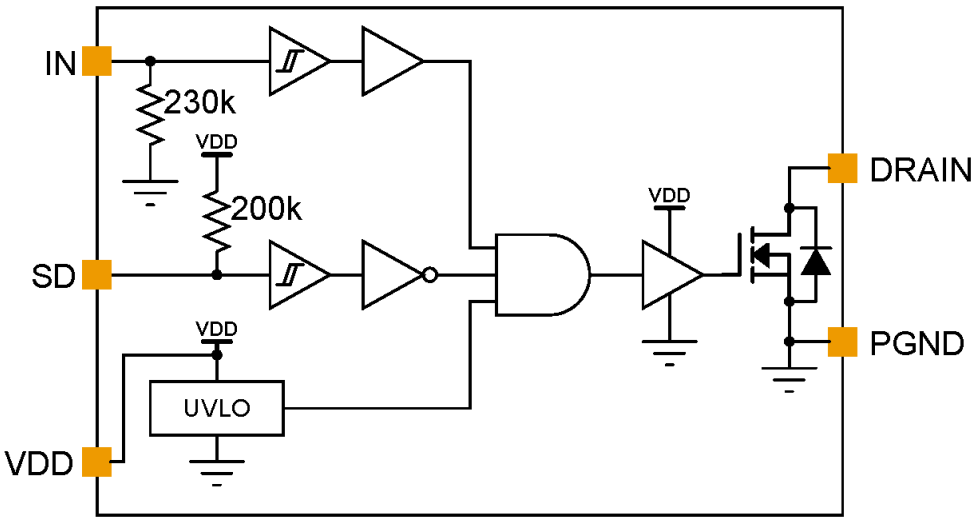


Figure 3. Functional Block Diagram

TYPICAL DEVICE CHARACTERISTICS

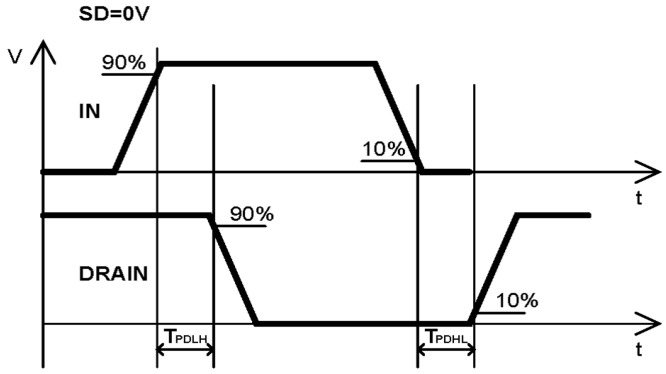


Figure 4. IN Switching Waveforms

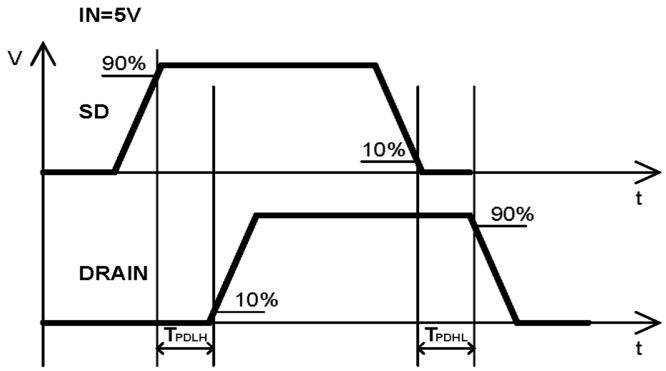


Figure 5. SD Switching Waveform

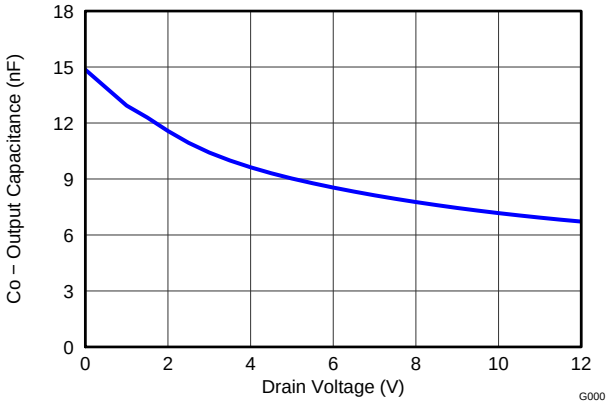


Figure 6. Output Capacitance

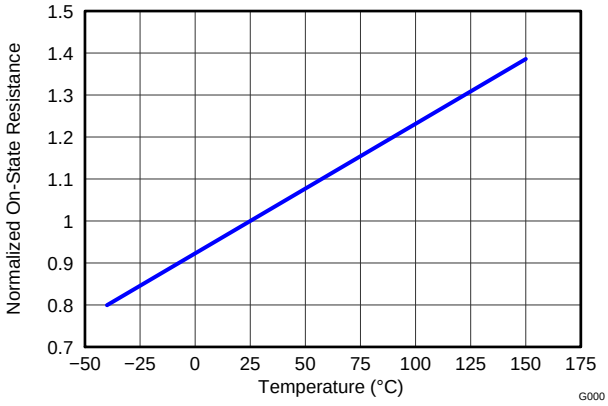


Figure 7. Normalized On Resistance R_{on}

TYPICAL DEVICE CHARACTERISTICS CONTINUED

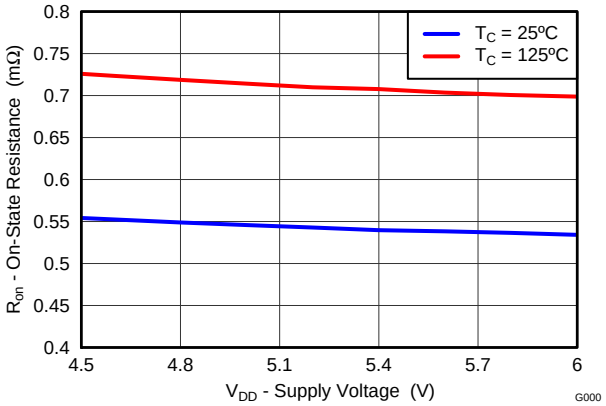


Figure 8. On Resistance vs. Supply Voltage

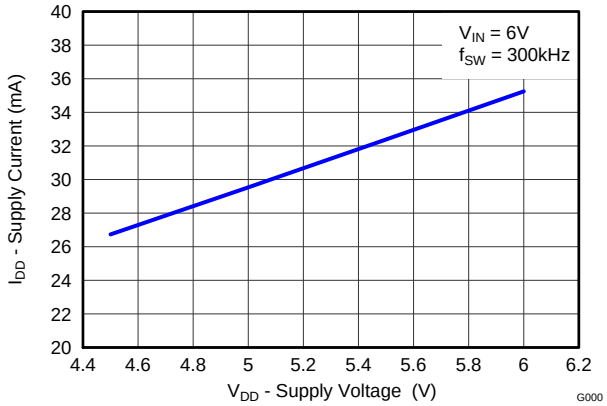


Figure 9. Supply Current vs. Supply Voltage

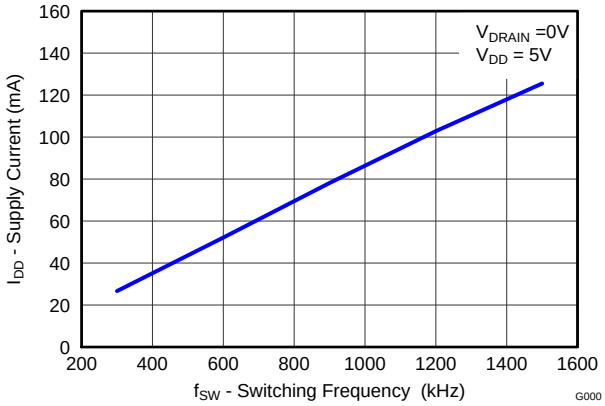


Figure 10. Supply Current vs. Switching Frequency

Application Information

V_{DD} and Under-Voltage Lockout (UVLO)

The driver IC in the CSD43301Q5M has an internal UVLO protection feature on the V_{DD} pin. Whenever the driver is in the UVLO condition (i.e. when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds the gate of the integrated MOSFET LOW, regardless of the status of IN and SD. The UVLO is typically 4.2V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the V_{DD} bias voltage when the system commences switching and there is a sudden increase in I_{DD}. This provides the capability to operate at low voltage levels (below 5V), along with best-in-class switching characteristics. For example, at power up, the MOSFET remains OFF until the V_{DD} voltages reaches the UVLO threshold. This prevents operating the MOSFET in the linear region and conducting a large load current at the same time, which often results in device overheating and can potentially damage the device.

Since the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, Multi-Layer Ceramic Capacitor (MLCC) bypass capacitors are recommended to prevent noise problems. A 1 µF MLCC type capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver.

Operating Supply Current

The driver IC in the CSD43301Q5M has a low quiescent current in normal operation. I_{DDQ} is less than 0.2 mA when the device is disabled (SD = 0). The operating current vs. supply voltage is shown in Figure 9, and the operating current vs. frequency is shown in Figure 10.

Input Stage

The input pins (IN and SD) of the CSD43301Q5M are based on a TTL/CMOS compatible input threshold logic that is independent of the V_{DD} supply voltage. With a typical high threshold of 2.2 V and a typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V digital power controllers. Wider hysteresis (typical of 0.8 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed. The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using a V_{DD} pull-up resistor on the SD input or a GND pull-down resistor on the IN input. This can be seen in the block diagram in Figure 3.

Power Dissipation

Power Dissipation of the CSD43301Q5M used in secondary rectification is given by the following:

$$P_{LOSS} = P_{DRV} + P_{COND} + P_{SW} \quad (1)$$

where driver loss is given by

$$P_{DRV} = V_{DD} \times I_{DD} \quad (2)$$

and conduction loss is given by

$$P_{COND} = I^2_{D\_RMS} \times R_{ON} \quad (3)$$

Switching losses consist of body diode conduction losses during dead time, body diode reverse recovery losses, and output charge losses, given by the following:

$$P_{SW} = I_D \times V_F \times (DT_R + DT_F) \times F_{SW} + Q_{RR} \times V_{DRAIN} \times F_{SW} + \tfrac{1}{2} Q_{OSS} \times V_{DRAIN} \times F_{SW} \quad (4)$$

Recommended PCB Design Overview

The CSD43301Q5M features extremely low nominal R_{ON}. In order to maximize the performance of this device, some simple layout guidelines should be followed.

- The DRAIN pins of the CSD43301Q5M should be placed as close as possible to the inductor and connected with a short wide trace. This reduces PCB conduction losses and reduce switching noise level. (1)
- The GND pin (pin 7) must be connected into the thermal pad (pin 13) on the bottom of the device via a copper pour (without thermal spokes) for maximum performance.
- The CSD43301Q5M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down via the barrel:
  - Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
  - Use the smallest drill size allowed in your design. The example in Figure 11 uses vias with a 10 mil drill hole and a 16 mil capture pad.
  - Tent the opposite side of the via with a solder mask.

  In the end, the number and size of the thermal vias should align with the end user's PCB design rules and manufacturing types.

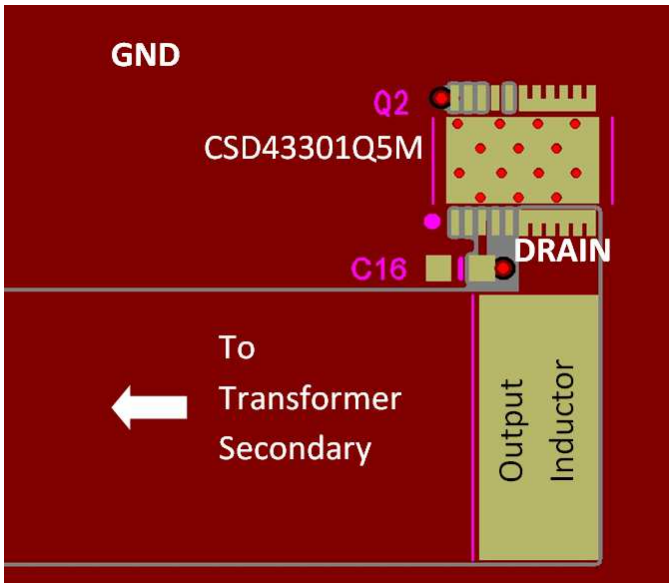
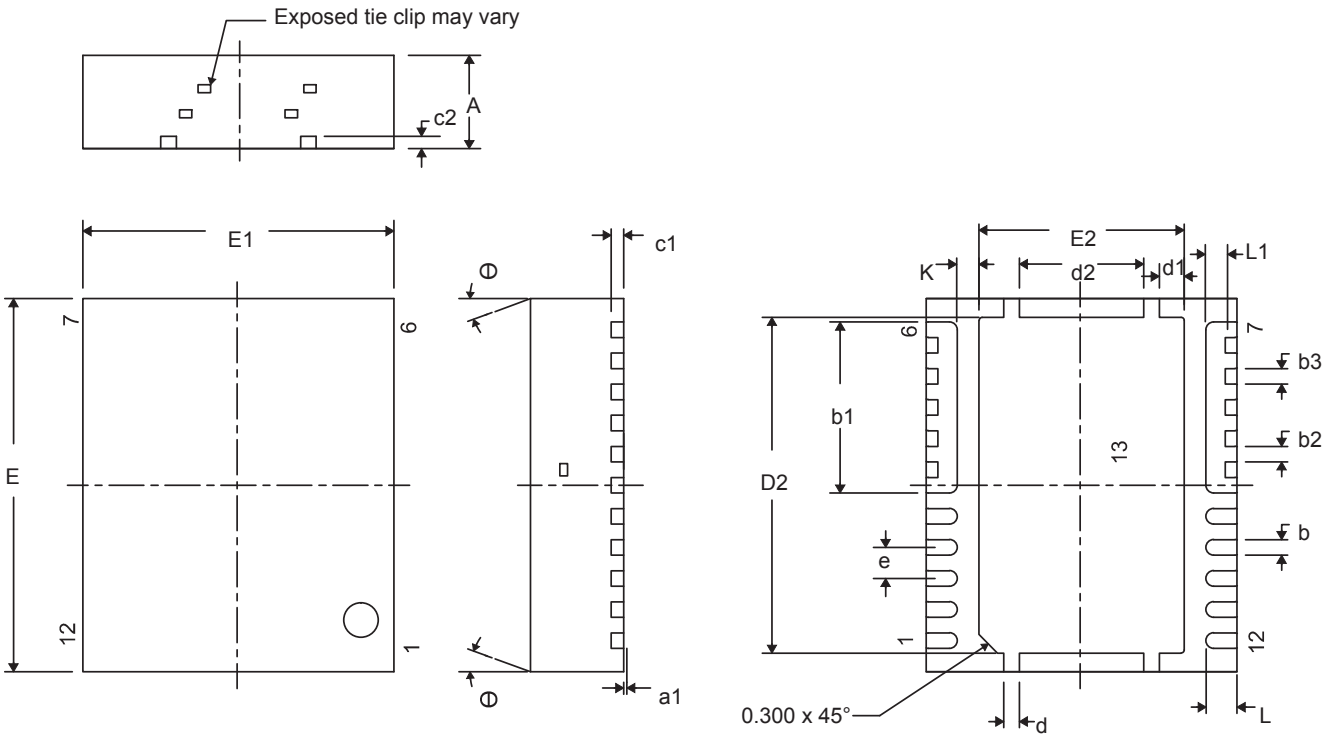


Figure 11. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, “EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis”, University of Missouri – Rolla

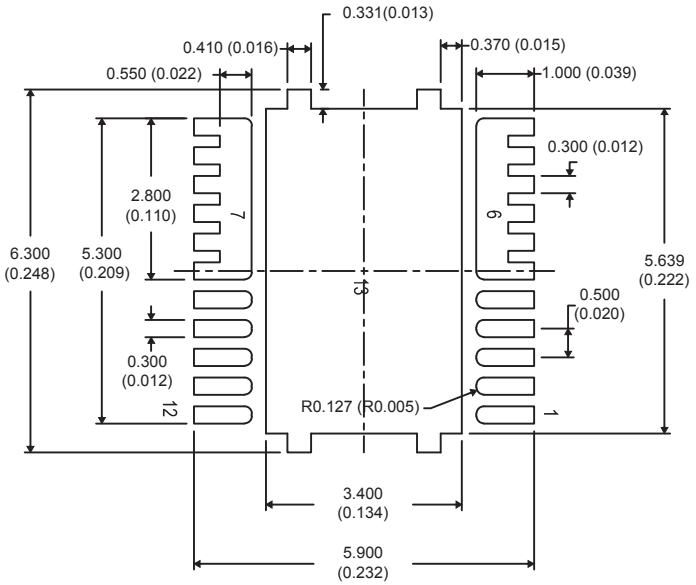
MECHANICAL DATA



TOP VIEW SIDE VIEW BOTTOM VIEW

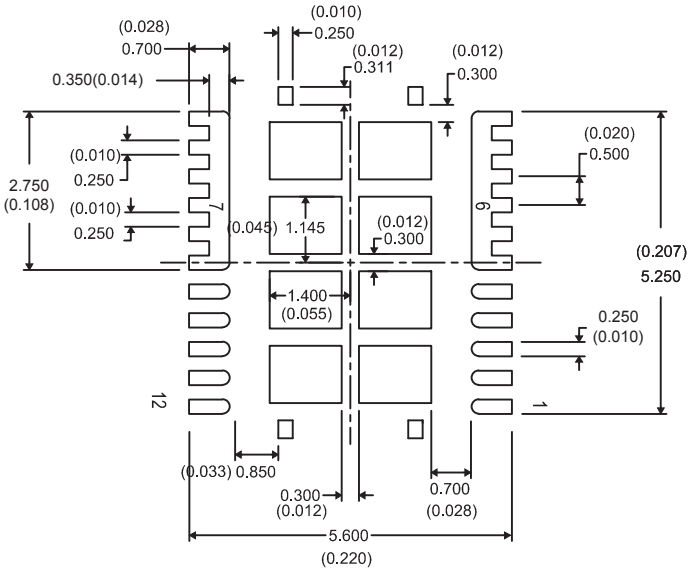
DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.400	1.450	1.500	0.055	0.057	0.059
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.350	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.150	0.200	0.250	0.006	0.008	0.010
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

Recommended PCB Pattern



NOTE: Dimensions are in mm (inches).

Recommended Stencil



NOTE: Dimensions are in mm (inches).

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed Figure 3	4

Changes from Revision A (December 2012) to Revision B	Page
• Changed the MECHANICAL DATA image and corresponding table	9
• Changed the Recommended PCB Pattern - lead width From: 0.300(0.012) To: 0.350(0.014)	10
• Changed the Recommended Stencil image	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CSD43301Q5M	ACTIVE	SON	DQP	12	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	43301M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

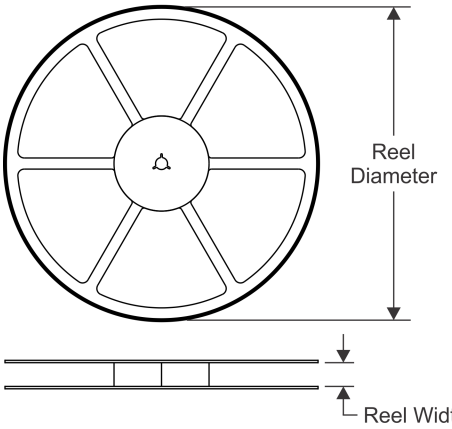
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

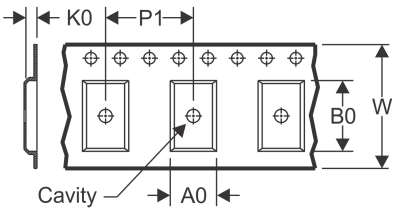
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

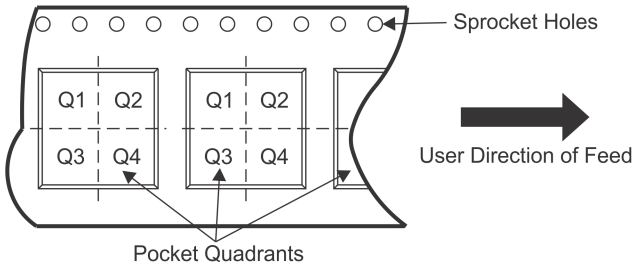


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

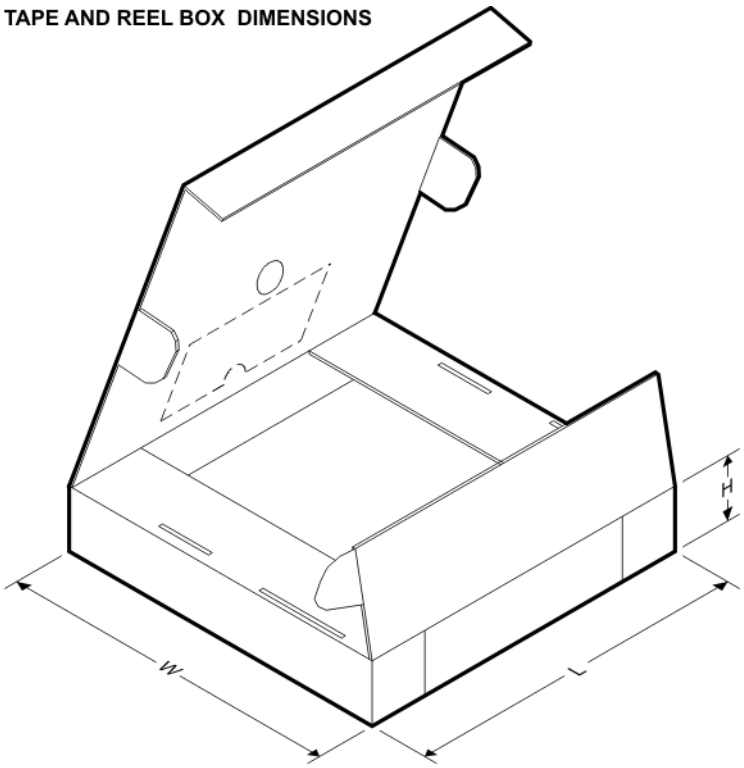
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD43301Q5M	SON	DQP	12	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD43301Q5M	SON	DQP	12	2500	367.0	367.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265