

## Synchronous Buck NexFET™ Power Stage

### FEATURES

- 90% System Efficiency at 15A
- Max Rated Continuous Current 20A, Peak 45A
- High Frequency Operation (up to 2 MHz)
- High Density - SON 3.5x4.5-mm Footprint
- Ultra Low Inductance Package
- System Optimized PCB Footprint
- Ultra Low Quiescent (ULQ) Current Mode
- 3.3V and 5V PWM Signal Compatible
- Diode Emulation Mode with FCCM
- Input Voltages up to 24V
- Three-State PWM Input
- Integrated Bootstrap Diode
- Shoot Through Protection
- RoHS Compliant – Lead Free Terminal Plating
- Halogen Free

### APPLICATIONS

- Ultrabook/Notebook DC/DC Converters
- Multiphase Vcore and DDR Solutions
- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems

### ORDERING INFORMATION

| Device      | Package                          | Media        | Qty  | Ship          |
|-------------|----------------------------------|--------------|------|---------------|
| CSD97376Q4M | SON 3.5 × 4.5-mm Plastic Package | 13-Inch Reel | 2500 | Tape and Reel |

### DESCRIPTION

The CSD97376Q4M NexFET™ Power Stage is a highly optimized design for use in a high power, high density Synchronous Buck converter. This product integrates the driver IC and NexFET technology to complete the power stage switching function. The driver IC has a built-in selectable diode emulation function that enables DCM operation to improve light load efficiency. In addition, the driver IC supports ULQ mode that enables Connected Standby for Windows™ 8. With the PWM input in tri-state, quiescent current is reduced to 130  $\mu$ A, with immediate response. When SKIP# is held at tri-state, the current is reduced to 8  $\mu$ A (typically 20  $\mu$ s is required to resume switching). This combination produces a high current, high efficiency, and high speed switching device in a small 3.5 × 4.5-mm outline package. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

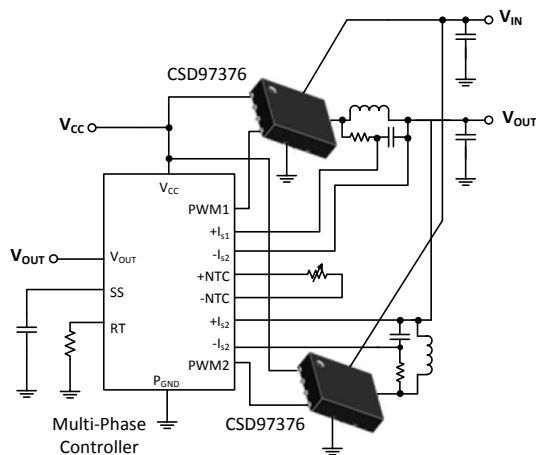


Figure 1. Application Diagram

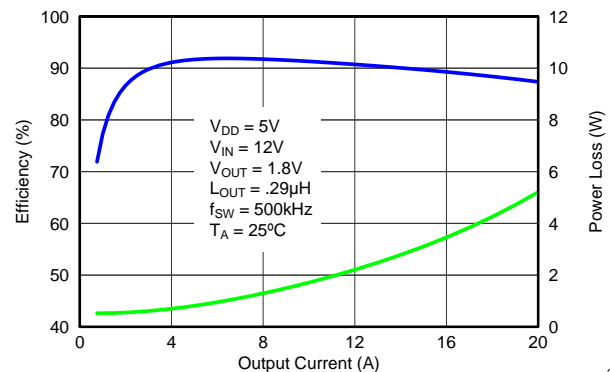


Figure 2. Efficiency and Power Loss



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

# CSD97376Q4M

SLPS422A – MARCH 2013 – REVISED JUNE 2013

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

T<sub>A</sub> = 25°C (unless otherwise noted)

|  |                            | VALUE |      | UNIT |
|--|----------------------------|-------|------|------|
|  |                            | MIN   | MAX  |      |
| V <sub>IN</sub> to P <sub>GND</sub>  |                            | -0.3  | 30   | V    |
| V <sub>SW</sub> to P <sub>GND</sub> , V <sub>IN</sub> to V <sub>SW</sub>         |                            | -0.3  | 30   | V    |
| V <sub>SW</sub> to P <sub>GND</sub> , V <sub>IN</sub> to V <sub>SW</sub> (<10ns) |                            | -7    | 33   | V    |
| V <sub>DD</sub> to P <sub>GND</sub>  |                            | -0.3  | 6    | V    |
| PWM, SKIP# to P <sub>GND</sub>   |                            | -0.3  | 6    | V    |
| BOOT to P <sub>GND</sub>   |                            | -0.3  | 35   | V    |
| BOOT to P <sub>GND</sub> (<10ns)   |                            | -2    | 38   | V    |
| BOOT to BOOT_R   |                            | -0.3  | 6    | V    |
| ESD Rating   | Human Body Model (HBM)     |       | 2000 | V    |
|  | Charged Device Model (CDM) |       | 500  | V    |
| Power Dissipation, P <sub>D</sub>  |                            |       | 8    | W    |
| Operating Temperature Range, T <sub>J</sub>                                      |                            | -40   | 150  | °C   |
| Storage Temperature Range, T <sub>STG</sub>                                      |                            | -55   | 150  | °C   |

- (1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

T<sub>A</sub> = 25° (unless otherwise noted)

| Parameter   | Conditions  | MIN | MAX  | UNIT |
|---|---|-----|------|------|
| Gate Drive Voltage, V <sub>DD</sub>                     |   | 4.5 | 5.5  | V    |
| Input Supply Voltage, V <sub>IN</sub>                   |   |     | 24   | V    |
| Continuous Output Current, I <sub>OUT</sub>             | V <sub>IN</sub> = 12V, V <sub>DD</sub> = 5V, V <sub>OUT</sub> = 1.8V,<br>f <sub>SW</sub> = 500kHz, L <sub>OUT</sub> = 0.29µH <sup>(1)</sup> |     | 20   | A    |
| Peak Output Current, I <sub>OUT-PK</sub> <sup>(2)</sup> |   |     | 45   | A    |
| Switching Frequency, f <sub>SW</sub>                    | C <sub>BST</sub> = 0.1µF (min)  |     | 2000 | kHz  |
| On Time Duty Cycle                                      |   |     | 85   | %    |
| Minimum PWM On Time                                     |   | 40  |      | ns   |
| Operating Temperature                                   |   | -40 | 125  | °C   |

- (1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V<sub>IN</sub> to P<sub>GND</sub> pins.  
 (2) System conditions as defined in Note 1. Peak Output Current is applied for t<sub>p</sub> = 10ms, duty cycle ≤ 1%

## THERMAL INFORMATION

T<sub>A</sub> = 25°C (unless otherwise noted)

| PARAMETER        |  | MIN | TYP | MAX  | UNIT |
|------------------|--|-----|-----|------|------|
| R <sub>θJC</sub> | Thermal Resistance, Junction-to-Case (Top of package) <sup>(1)</sup> |     |     | 22.8 | °C/W |
| R <sub>θJB</sub> | Thermal Resistance, Junction-to-Board <sup>(2)</sup>                 |     |     | 2.5  | °C/W |

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1-inch<sup>2</sup> (6.45 -cm<sup>2</sup>), 2-oz (.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch, 0.06-inch (1.52-mm) thick FR4 board.  
 (2) R<sub>θJB</sub> value based on hottest board temperature within 1mm of the package.

## ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = \text{POR to } 5.5\text{V}$  (unless otherwise noted)

| PARAMETER   | CONDITIONS  | MIN  | TYP  | MAX  | UNIT          |
|---|---|------|------|------|---------------|
| <b>P<sub>Loss</sub></b>                                       |   |      |      |      |               |
| Power Loss <sup>(1)</sup>                                     | $V_{IN} = 12\text{V}$ , $V_{DD} = 5\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 12\text{A}$ ,<br>$f_{SW} = 500\text{kHz}$ , $L_{OUT} = 0.29\mu\text{H}$ , $T_J = 25^\circ\text{C}$  |      | 2.2  |      | W             |
| Power Loss <sup>(2)</sup>                                     | $V_{IN} = 19\text{V}$ , $V_{DD} = 5\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 12\text{A}$ ,<br>$f_{SW} = 500\text{kHz}$ , $L_{OUT} = 0.29\mu\text{H}$ , $T_J = 25^\circ\text{C}$  |      | 2.4  |      | W             |
| Power Loss <sup>(2)</sup>                                     | $V_{IN} = 19\text{V}$ , $V_{DD} = 5\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 12\text{A}$ ,<br>$f_{SW} = 500\text{kHz}$ , $L_{OUT} = 0.29\mu\text{H}$ , $T_J = 125^\circ\text{C}$ |      | 3.0  |      | W             |
| <b>V<sub>IN</sub></b>   |   |      |      |      |               |
| $V_{IN}$ Quiescent Current, $I_Q$                             | PWM=Floating, $V_{DD} = 5\text{V}$ , $V_{IN} = 24\text{V}$  |      |      | 1    | $\mu\text{A}$ |
| <b>V<sub>DD</sub></b>   |   |      |      |      |               |
| Standby Supply Current, $I_{DD}$                              | PWM = Float, SKIP# = $V_{DD}$ or 0V   |      | 130  |      | $\mu\text{A}$ |
|   | SKIP# = Float   |      | 8    |      | $\mu\text{A}$ |
| Operating Supply Current, $I_{DD}$                            | PWM = 50% Duty cycle, $f_{SW} = 500\text{kHz}$  |      | 5.3  |      | mA            |
| <b>POWER-ON RESET AND UNDER VOLTAGE LOCKOUT</b>               |   |      |      |      |               |
| Power-On Reset, $V_{DD}$ Rising                               |   |      |      | 4.15 | V             |
| UVLO, $V_{DD}$ Falling  |   | 3.7  |      |      | V             |
| Hysteresis  |   |      | 0.2  |      | mV            |
| <b>PWM and SKIP# I/O Specifications</b>                       |   |      |      |      |               |
| Input Impedance, $R_I$  | Pull Up to $V_{DD}$   |      | 1700 |      | k $\Omega$    |
|   | Pull Down (to GND)  |      | 800  |      |               |
| Logic Level High, $V_{IH}$                                    |   | 2.65 |      |      | V             |
| Logic Level Low, $V_{IL}$                                     |   |      | 0.6  |      |               |
| Hysteresis, $V_{IH}$  |   |      | 0.2  |      |               |
| Tri-State Voltage, $V_{TS}$                                   |   | 1.3  |      | 2    |               |
| Tri-state Activation Time (falling) PWM,<br>$t_{THOLD(off1)}$ |   |      | 60   |      | ns            |
| Tri-state Activation Time (rising) PWM, $t_{THOLD(off2)}$     |   |      | 60   |      |               |
| Tri-state Activation Time (falling) SKIP#, $t_{TSKF}$         |   |      | 1    |      | $\mu\text{s}$ |
| Tri-state Activation Time (rising) SKIP#, $t_{TSKR}$          |   |      | 1    |      |               |
| Tri-state Exit Time PWM, $t_{3RD(PWM)}$ <sup>(2)</sup>        |   |      |      | 100  | ns            |
| Tri-state Exit Time SKIP#, $t_{3RD(SKIP\#)}$ <sup>(2)</sup>   |   |      |      | 50   | $\mu\text{s}$ |
| <b>BOOTSTRAP SWITCH</b>                                       |   |      |      |      |               |
| Forward Voltage, $V_{FBST}$                                   | $I_F = 10\text{mA}$   |      | 120  | 240  | mV            |
| Reverse Leakage, $I_{RLEAK}$ <sup>(2)</sup>                   | $V_{BST} - V_{DD} = 25\text{V}$   |      |      | 2    | $\mu\text{A}$ |

(1) Measurement made with six 10- $\mu\text{F}$  (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across  $V_{IN}$  to  $P_{GND}$  pins.

(2) Specified by design

TYPICAL CHARACTERISTICS

T<sub>J</sub> = 125°C, unless stated otherwise.

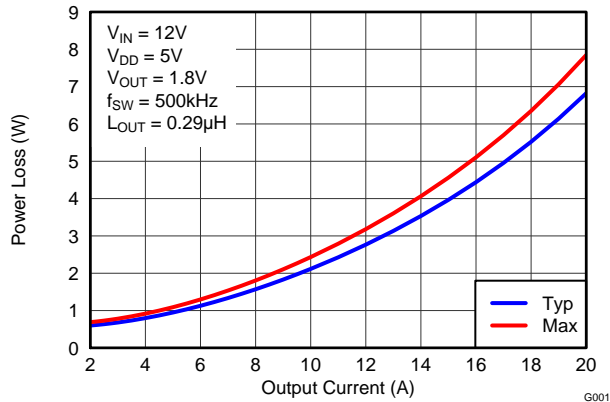


Figure 3. Power Loss vs Output Current

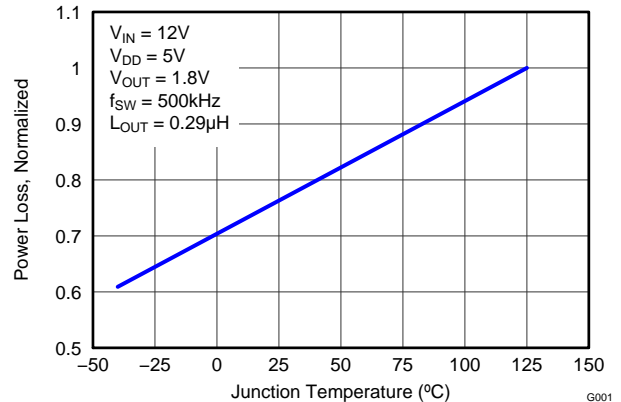


Figure 4. Power Loss vs Temperature

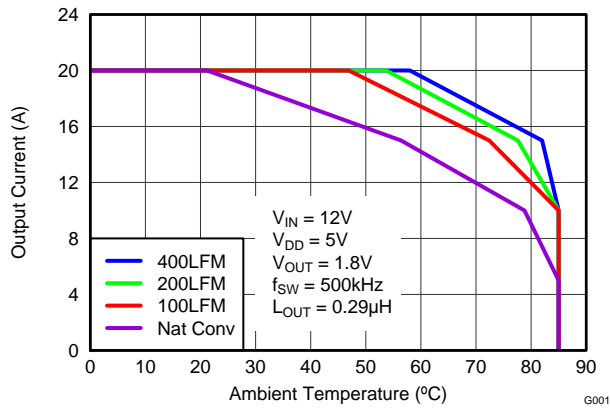


Figure 5. Safe Operating Area – PCB Horizontal Mount (1)

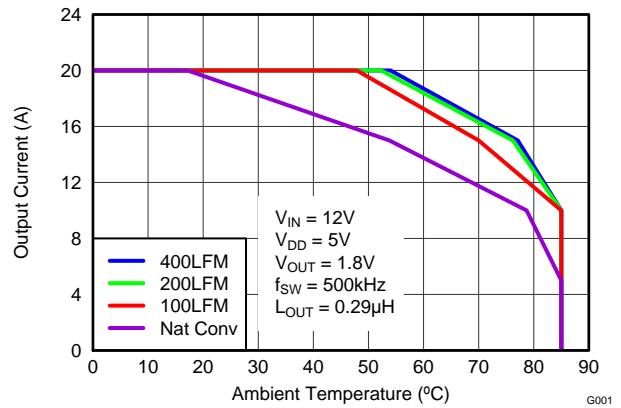


Figure 6. Safe Operating Area – PCB Vertical Mount (1)

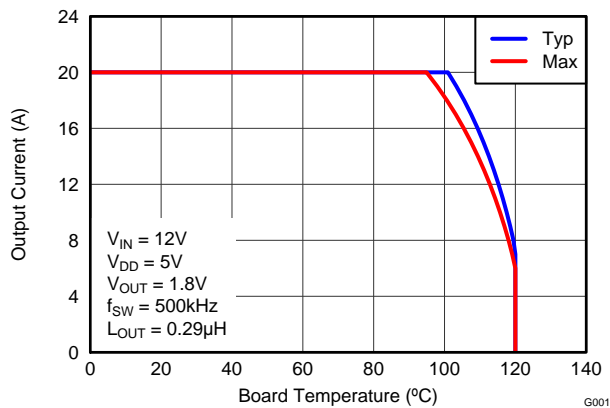


Figure 7. Typical Safe Operating Area (1)

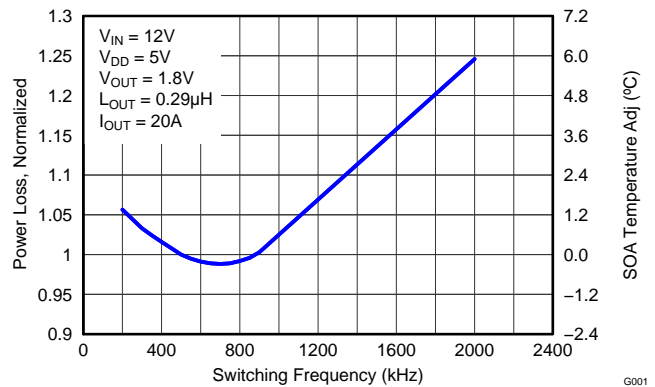


Figure 8. Normalized Power Loss vs Frequency

TYPICAL CHARACTERISTICS (continued)

T<sub>J</sub> = 125°C, unless stated otherwise.

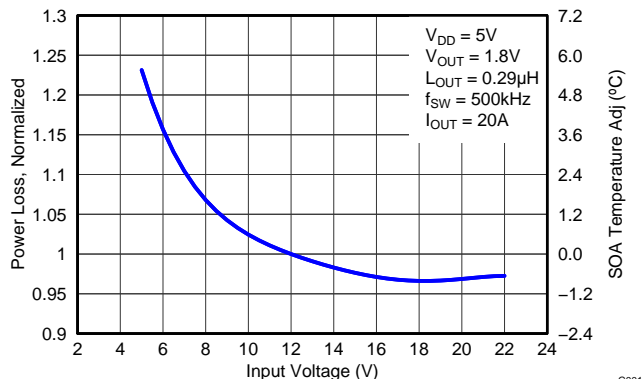


Figure 9. Normalized Power Loss vs Input Voltage

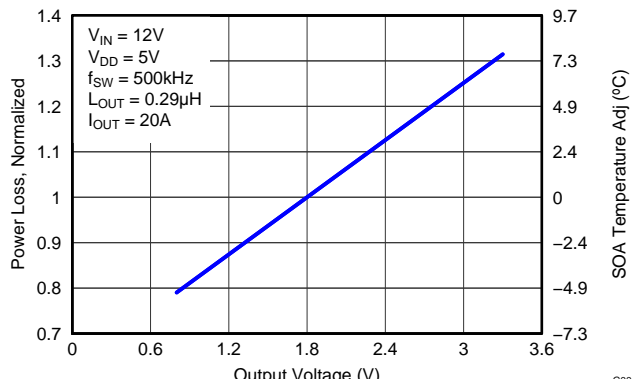


Figure 10. Normalized Power Loss vs Output Voltage

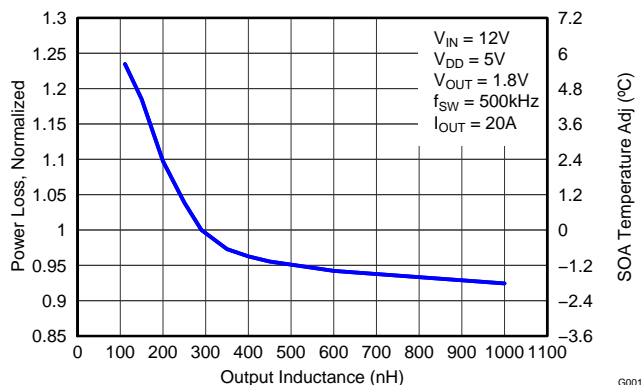


Figure 11. Normalized Power Loss vs Output Inductance

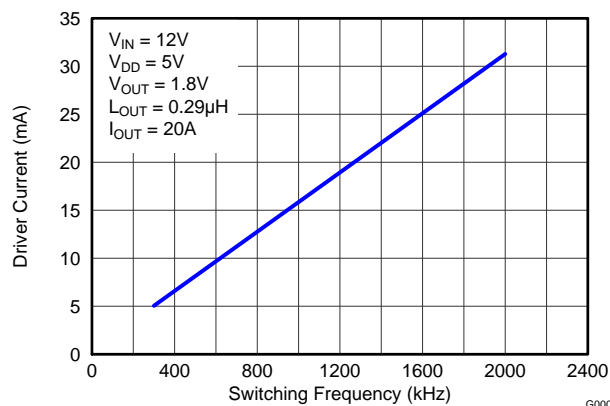


Figure 12. Driver Current vs Frequency

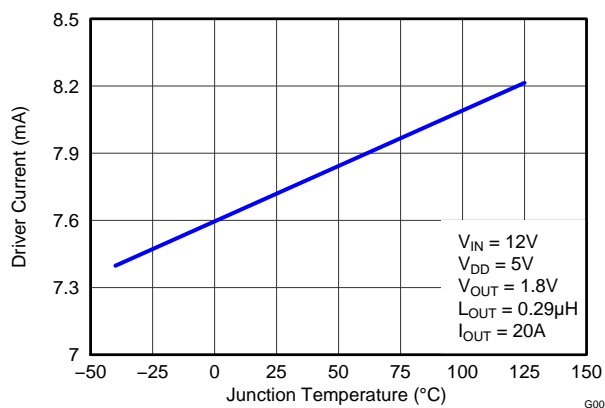
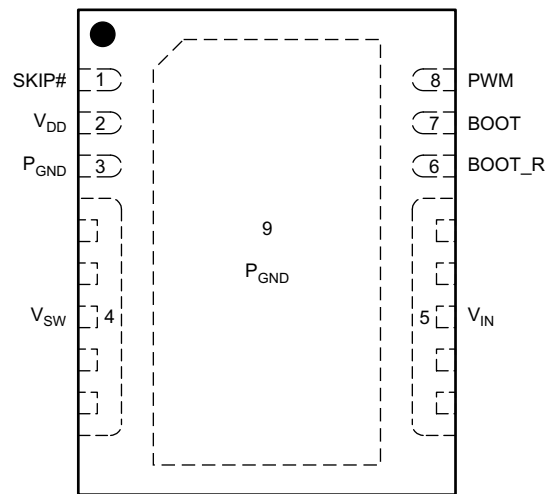


Figure 13. Driver Current vs Temperature

1. The Typical CSD97376Q4M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See the [Application Information](#) section for detailed explanation.

### PIN CONFIGURATION



**Figure 14. Top View**

### PIN DESCRIPTION

| PIN |                  | DESCRIPTION   |
|-----|------------------|---|
| NO. | NAME             |   |
| 1   | SKIP#            | This pin enables the Diode Emulation function. When this pin is held Low, Diode Emulation Mode is enabled for the Sync FET. When SKIP# is High, the CSD97376Q4M operates in Forced Continuous Conduction Mode. A tri-state voltage on SKIP# puts the driver into a very low power state.                |
| 2   | V <sub>DD</sub>  | Supply Voltage to Gate Drivers and internal circuitry.  |
| 3   | P <sub>GND</sub> | Power Ground, Needs to be connected to Pin 9 and PCB  |
| 4   | V <sub>SW</sub>  | Voltage Switching Node – pin connection to the output inductor.   |
| 5   | V <sub>IN</sub>  | Input Voltage Pin. Connect input capacitors close to this pin.  |
| 6   | BOOT_R           | Bootstrap capacitor connection. Connect a minimum 0.1µF 16V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated.   |
| 7   | BOOT             |   |
| 8   | PWM              | Pulse Width modulated 3-state input from external controller. Logic Low sets Control FET gate low and Sync FET gate high. Logic High sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the 3-State Shutdown Hold-off Time (t <sub>3HT</sub> ) |
| 9   | P <sub>GND</sub> | Power Ground  |

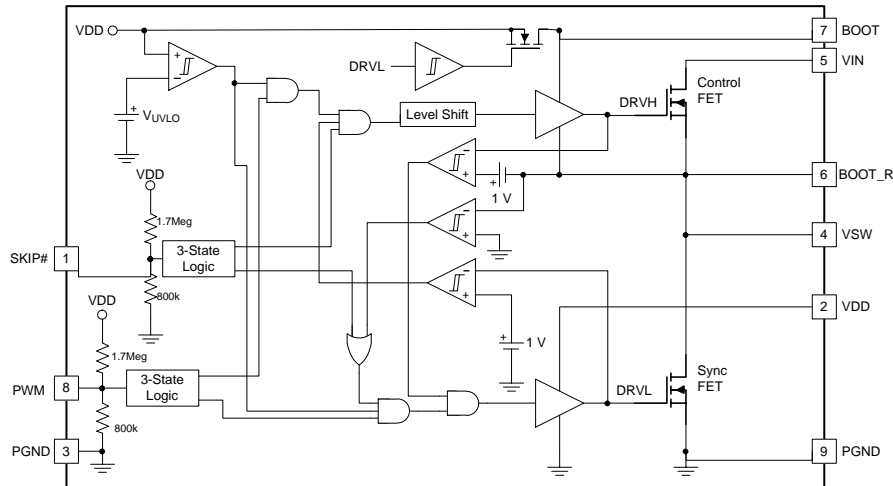


Figure 15. Functional Block Diagram

## FUNCTIONAL DESCRIPTION

### POWERING CSD97376Q4M AND GATE DRIVERS

An external  $V_{DD}$  voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. A  $1\mu\text{F}$  10V X5R or higher ceramic capacitor is recommended to bypass  $V_{DD}$  pin to  $P_{GND}$ . A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a  $100\text{nF}$  16V X5R ceramic capacitor between BOOT and BOOT\_R pins. An optional  $R_{BOOT}$  resistor can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the  $V_{SW}$  node. A typical  $1\Omega$  to  $4.7\Omega$  value is a compromise between switching loss and  $V_{SW}$  spike amplitude.

### Undervoltage Lockout Protection (UVLO)

The undervoltage lockout (UVLO) comparator evaluates the  $V_{DD}$  voltage level. As  $V_{VDD}$  rises, both the Control FET and Sync FET gates hold actively low at all times until  $V_{VDD}$  reaches the higher UVLO threshold ( $V_{UVLO\_H}$ ). Then the driver becomes operational and responds to PWM and SKIP# commands. If  $V_{DD}$  falls below the lower UVLO threshold ( $V_{UVLO\_L} = V_{UVLO\_H} - \text{Hysteresis}$ ), the device disables the driver and drives the outputs of the Control FET and Sync FET gates actively low. Figure 16 shows this function.

#### CAUTION

Do not start the driver in the very low power mode (SKIP# = Tri-state).

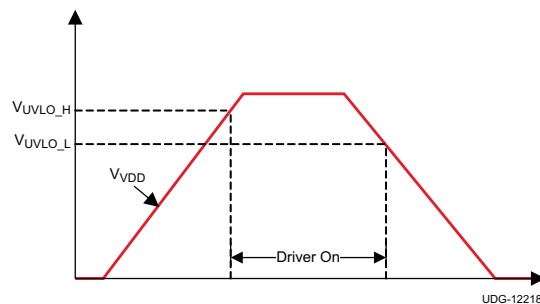


Figure 16. UVLO Operation

### PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pull-up to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 17.

When VDD reaches the UVLO\_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined the PWM voltage range between PWM logic high ( $V_{IH}$ ) and logic low ( $V_{IL}$ ) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3 V (typical) and 5 V (typical) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4  $\mu$ s, regardless of the state of the SKIP# pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

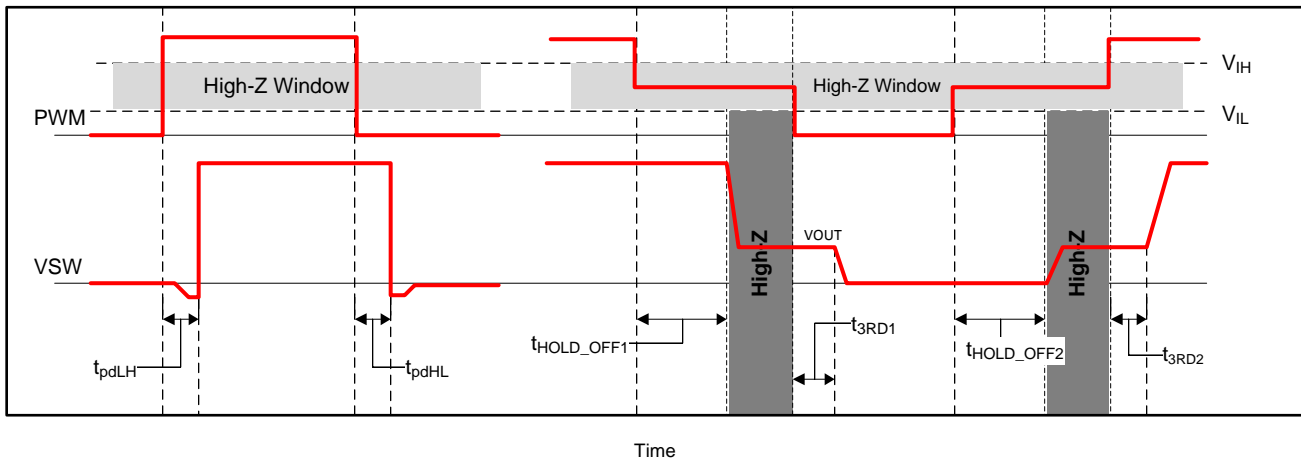


Figure 17. PWM Tri-State Timing Diagram

### SKIP# Pin

The SKIP# pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When SKIP# is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When SKIP# is high, the ZX comparator disables, and the converter enters FCCM mode. When both SKIP# and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When SKIP# is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50  $\mu$ s.

Table 1 shows the logic functions of UVLO, PWM, SKIP#, the Control FET Gate and the Sync FET Gate.

Table 1. Logic Functions of the Driver IC

| UVLO     | PWM       | SKIP#     | Sync FET Gate       | Control FET Gate | MODE               |
|----------|-----------|-----------|---------------------|------------------|--------------------|
| Active   | —         | —         | Low                 | Low              | Disabled           |
| Inactive | Low       | Low       | High <sup>(1)</sup> | Low              | DCM <sup>(1)</sup> |
| Inactive | Low       | High      | High                | Low              | FCCM               |
| Inactive | High      | H or L    | Low                 | High             |                    |
| Inactive | Tri-state | H or L    | Low                 | Low              | LQ                 |
| Inactive | —         | Tri-state | Low                 | Low              | ULQ                |

(1) Until zero crossing protection occurs.



### Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

### Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BST pin is replaced by a FET which is gated by the DRV1 signal.

## APPLICATION INFORMATION

The Power Stage CSD97376Q4M is a highly optimized design for synchronous buck applications using NexFET devices with a 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area and normalized graphs allow engineers to predict the product performance in the actual application.

### Power Loss Curves

MOSFET centric parameters such as  $R_{DS(ON)}$  and  $Q_{gd}$  are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 3 plots the power loss of the CSD97376Q4M as a function of load current. This curve is measured by configuring and running the CSD97376Q4M as it would be in the final application (see Figure 18). The measured power loss is the CSD97376Q4M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \tag{1}$$

The power loss curve in Figure 3 is measured at the maximum recommended junction temperature of  $T_J = 125^\circ\text{C}$  under isothermal test conditions.

### Safe Operating Curves (SOA)

The SOA curves in the CSD97376Q4M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 5 and Figure 7 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

### Normalized Curves

The normalized curves in the CSD97376Q4M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

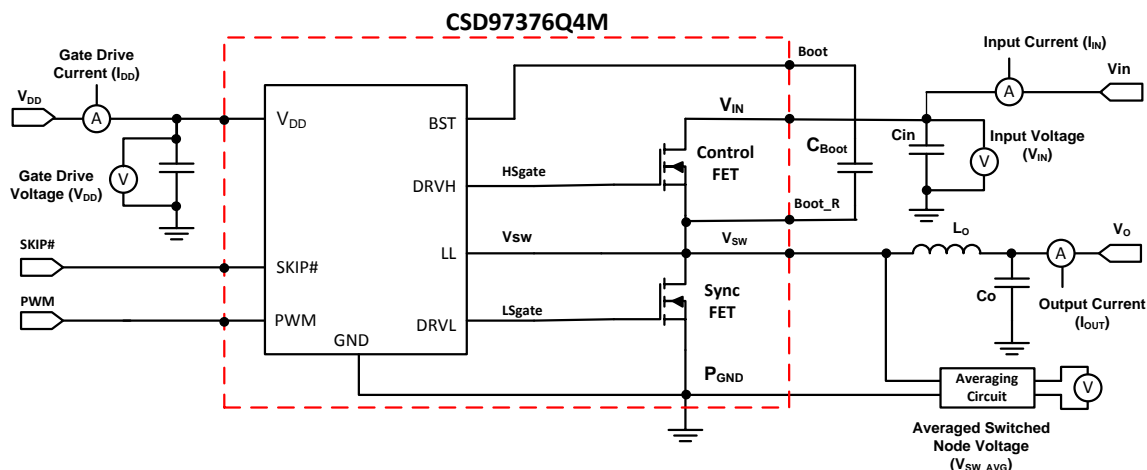


Figure 18. Power Loss Test Circuit

## Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

### Design Example

Operating Conditions: Output Current ( $I_{OUT}$ ) = 10A, Input Voltage ( $V_{IN}$ ) = 7V, Output Voltage ( $V_{OUT}$ ) = 1.5V, Switching Frequency ( $f_{SW}$ ) = 800kHz, Output Inductor ( $L_{OUT}$ ) = 0.2μH

### Calculating Power Loss

- Typical Power Loss at 10A = 2.1W (Figure 3)
- Normalized Power Loss for switching frequency  $\approx$  0.99 (Figure 8)
- Normalized Power Loss for input voltage  $\approx$  1.10 (Figure 9)
- Normalized Power Loss for output voltage  $\approx$  0.93(Figure 10)
- Normalized Power Loss for output inductor  $\approx$  1.10 (Figure 11)
- **Final calculated Power Loss = 2.1W  $\times$  0.99  $\times$  1.10  $\times$  0.93  $\times$  1.10  $\approx$  2.3W**

### Calculating SOA Adjustments

- SOA adjustment for switching frequency  $\approx$  -0.2°C (Figure 8)
- SOA adjustment for input voltage  $\approx$  2.5°C (Figure 9)
- SOA adjustment for output voltage  $\approx$  1.0°C (Figure 10)
- SOA adjustment for output inductor  $\approx$  2.3°C (Figure 11)
- **Final calculated SOA adjustment = -0.2 + 2.5 + (-1.5) + 2.3  $\approx$  3.1°C**

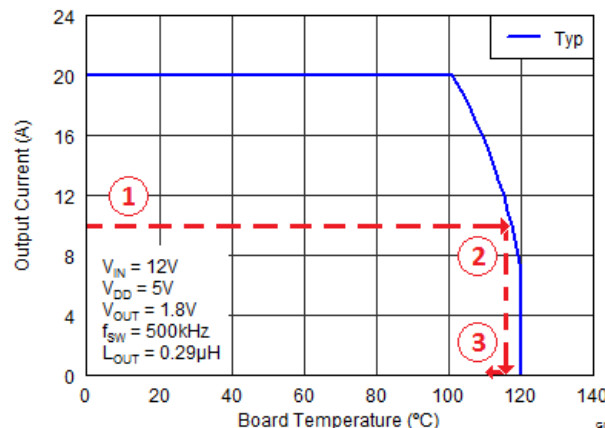


Figure 19. Power Stage CSD97376Q4M SOA

In the design example above, the estimated power loss of the CSD97376Q4M would increase to 2.3W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.1°C. Figure 19 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

## RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

### Electrical Performance

The CSD97376Q4M has the ability to switch at voltage rates greater than 10kV/μs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

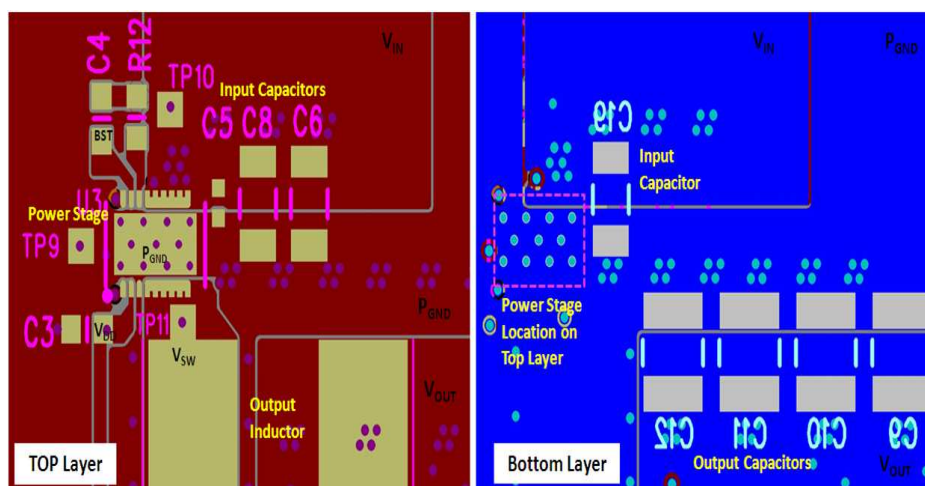
- The placement of the input capacitors relative to  $V_{IN}$  and  $P_{GND}$  pins of CSD97376Q4M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the  $V_{IN}$  and  $P_{GND}$  pins (see Figure 20). The example in Figure 20 uses 1 x 1nF 0402 25V and 3 x 10μF 1206 25V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C6, C19 should follow in order.
- The bootstrap cap  $C_{BOOT}$  0.1μF 0603 16V ceramic capacitor should be closely connected between BOOT and BOOT\_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD97376Q4M  $V_{SW}$  pins. Minimizing the  $V_{SW}$  node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. <sup>(2)</sup>

### Thermal Performance

The CSD97376Q4M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 20 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

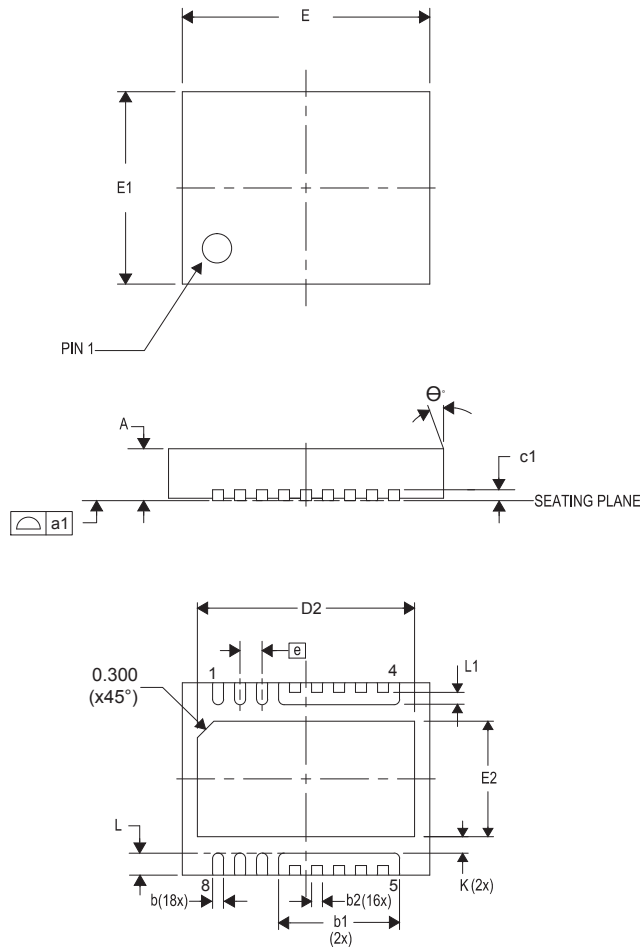
In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.



**Figure 20. Recommended PCB Layout (Top Down View)**

(2) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

**MECHANICAL DATA**



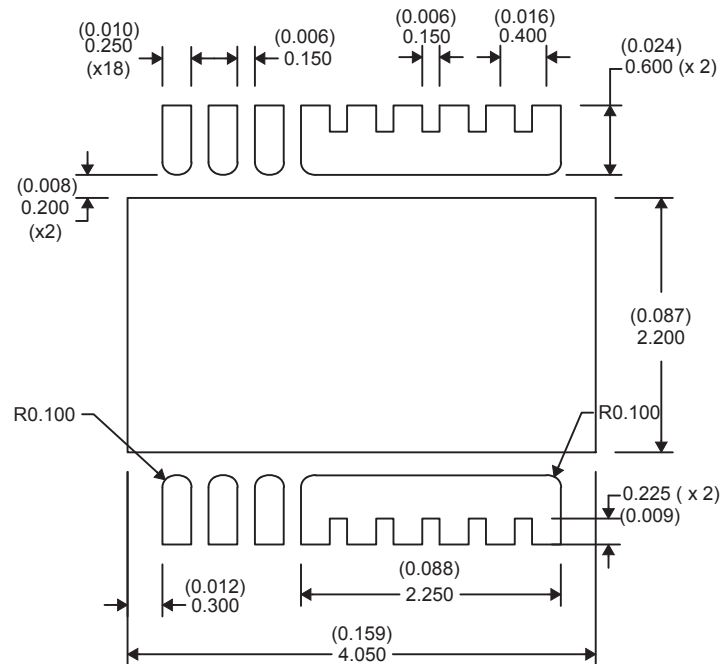
| DIM   | MILLIMETERS |       |       | INCHES    |       |       |
|-------|-------------|-------|-------|-----------|-------|-------|
|       | Min         | Nom   | Max   | Min       | Nom   | Max   |
| A     | 0.800       | 0.900 | 1.000 | 0.031     | 0.035 | 0.039 |
| a1    | 0.000       | 0.000 | 0.080 | 0.000     | 0.000 | 0.003 |
| b     | 0.150       | 0.200 | 0.250 | 0.006     | 0.008 | 0.010 |
| b1    | 2.000       | 2.200 | 2.400 | 0.079     | 0.087 | 0.095 |
| b2    | 0.150       | 0.200 | 0.250 | 0.006     | 0.008 | 0.010 |
| c1    | 0.150       | 0.200 | 0.250 | 0.006     | 0.008 | 0.010 |
| D2    | 3.850       | 3.950 | 4.050 | 0.152     | 0.156 | 0.160 |
| E     | 4.400       | 4.500 | 4.600 | 0.173     | 0.177 | 0.181 |
| E1    | 3.400       | 3.500 | 3.600 | 0.134     | 0.138 | 0.142 |
| E2    | 2.000       | 2.100 | 2.200 | 0.079     | 0.083 | 0.087 |
| e     | 0.400 TYP   |       |       | 0.016 TYP |       |       |
| K     | 0.300 TYP   |       |       | 0.012 TYP |       |       |
| L     | 0.300       | 0.400 | 0.500 | 0.012     | 0.016 | 0.020 |
| L1    | 0.180       | 0.230 | 0.280 | 0.007     | 0.009 | 0.011 |
| theta | 0.00        | —     | —     | 0.00      | —     | —     |

# CSD97376Q4M

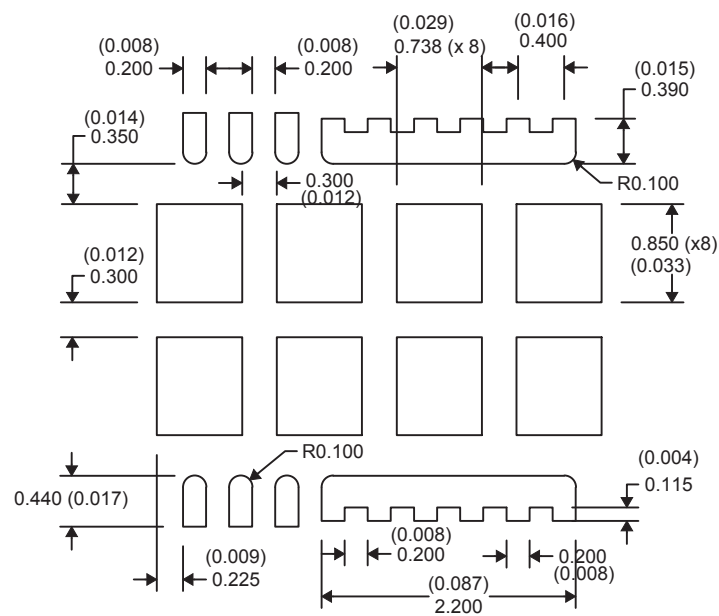
SLPS422A – MARCH 2013 – REVISED JUNE 2013

www.ti.com

## Recommended PCB Land Pattern



## Recommended Stencil Opening



NOTE: Dimensions are in mm (inches).

## REVISION HISTORY

| <b>Changes from Original (March 2013) to Revision A</b>  | <b>Page</b> |
|--|-------------|
| • Changed Feature From: Over 90% System Efficiency at 15A To: 90% System Efficiency at 15A ..... | 1           |
| • Changed the Mechanical Drawing image .....   | 13          |
| • Added dimension row b2 to the MECHANICAL DATA table .....                                      | 13          |
| • Changed the Recommended PCB Land Pattern image .....   | 14          |
| • Changed the Recommended Stencil Opening image .....  | 14          |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)          | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|--------------------------|------------------|----------------------|--------------|--------------------------|---------|
| CSD97376Q4M      | PREVIEW       | VSON         | DPC                | 8    | 2500           | Pb-Free (RoHS<br>Exempt) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 150   | 97376M                   |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)