

25-V N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16556Q5B](#)

FEATURES

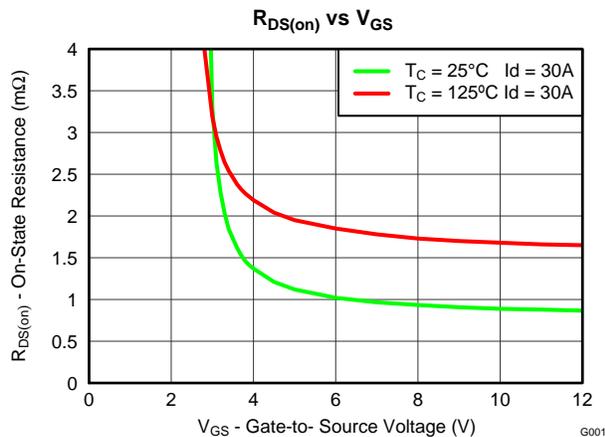
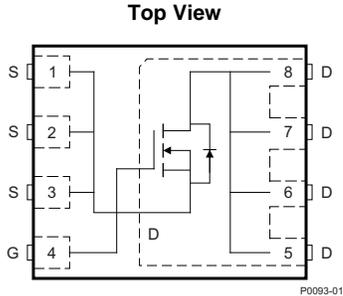
- Extremely Low Resistance
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in synchronous rectification and other power conversion applications.



PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$ unless otherwise stated		TYPICAL VALUE		UNIT
V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	36		nC
Q_{gd}	Gate Charge Gate to Drain	12		nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}$	1.2	m Ω
		$V_{GS} = 10\text{V}$	0.9	m Ω
$V_{GS(th)}$	Threshold Voltage	1.4		V

ORDERING INFORMATION

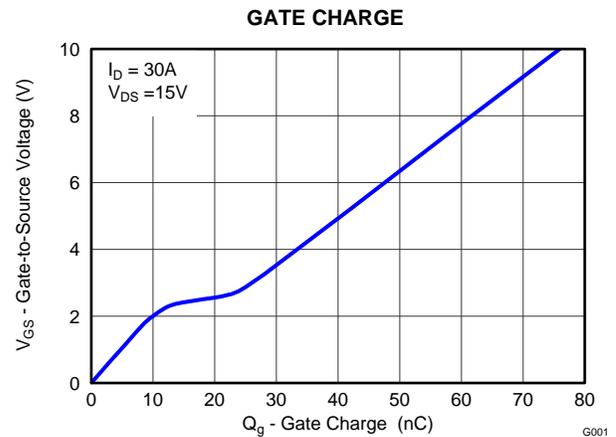
Device	Package	Media	Qty	Ship
CSD16556Q5B	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited), $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	263	
	Continuous Drain Current ⁽¹⁾	40	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽¹⁾⁽²⁾	249	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 103\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	530	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C}/\text{W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$



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NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

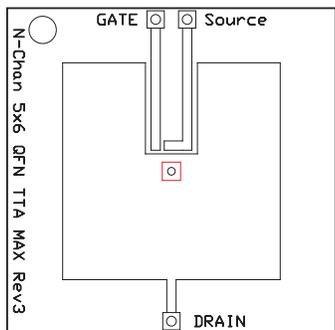
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250\mu A$	25			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1.2	1.4	1.7	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 30A$		1.2	1.5	$m\Omega$
		$V_{GS} = 10V, I_{DS} = 30A$		0.9	1.07	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 15V, I_{DS} = 30A$		191		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1MHz$		4750	6180	pF
C_{oss}	Output Capacitance			2270	2950	pF
C_{riss}	Reverse Transfer Capacitance			220	280	pF
R_G	Series Gate Resistance			0.7	1.4	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_{DS} = 30A$		36	47	nC
Q_{gd}	Gate Charge Gate to Drain			12		nC
Q_{gs}	Gate Charge Gate to Source			11		nC
$Q_{g(th)}$	Gate Charge at V_{th}			7.0		nC
Q_{oss}	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		45		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 30A, R_G = 2\Omega$		17		ns
t_r	Rise Time			34		ns
$t_{d(off)}$	Turn Off Delay Time			25		ns
t_f	Fall Time			13		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 30A, V_{GS} = 0V$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 15V, I_F = 30A, di/dt = 300A/\mu s$		84		nC
t_{rr}	Reverse Recovery Time			41		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

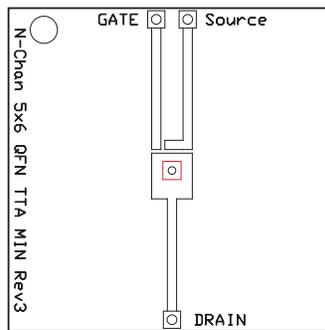
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.

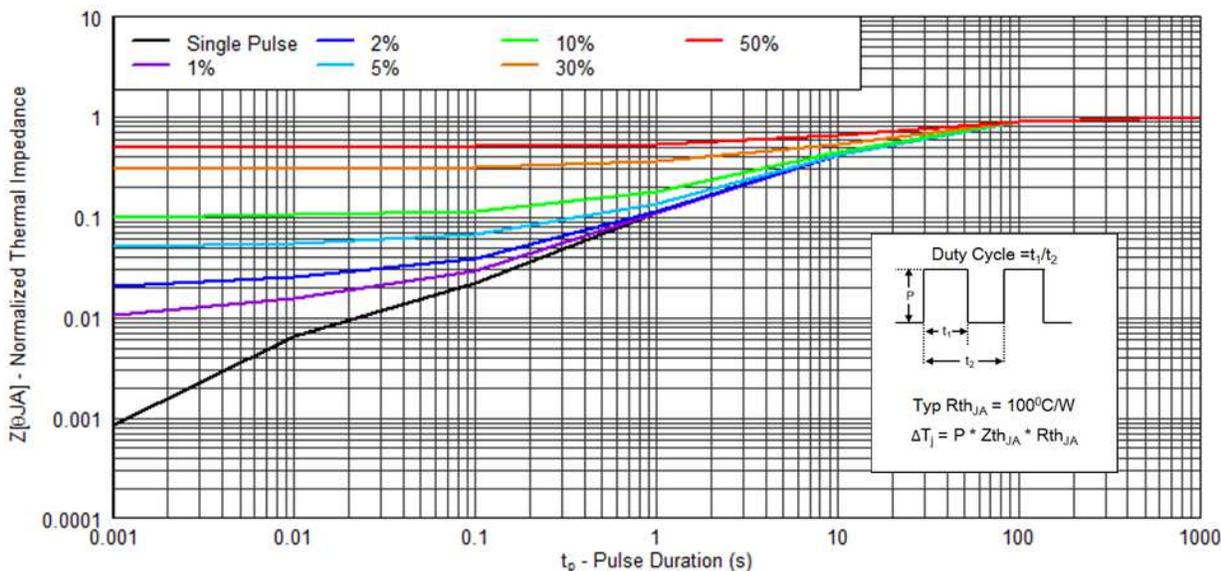


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



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Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

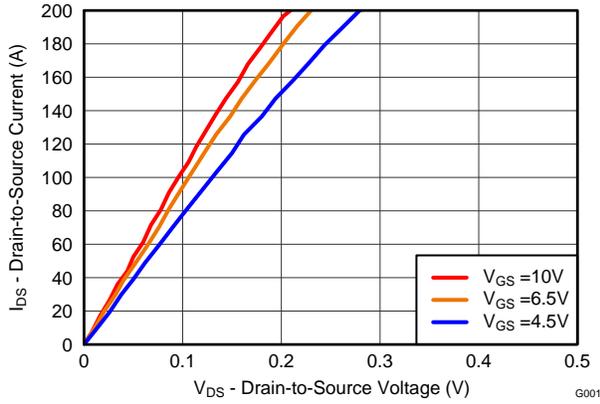


Figure 2. Saturation Characteristics

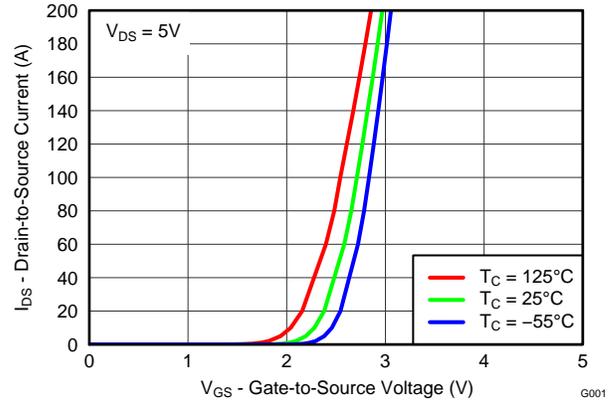


Figure 3. Transfer Characteristics

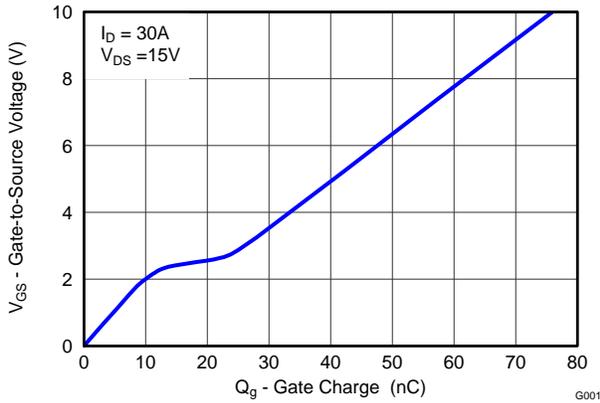


Figure 4. Gate Charge

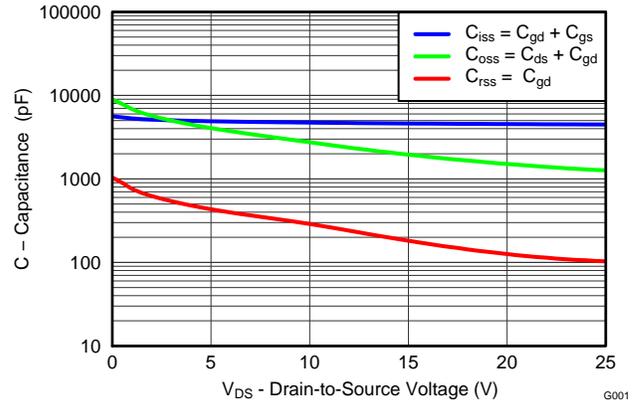


Figure 5. Capacitance

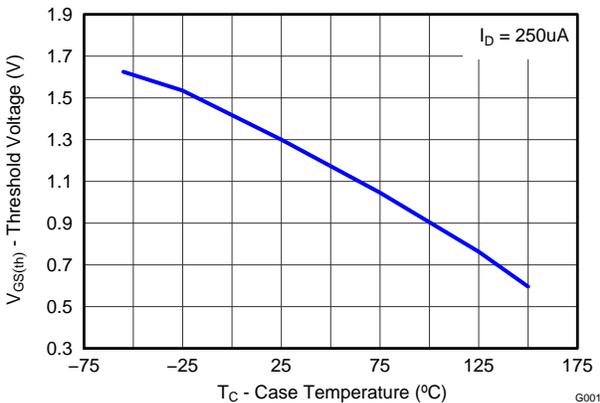


Figure 6. Threshold Voltage vs. Temperature

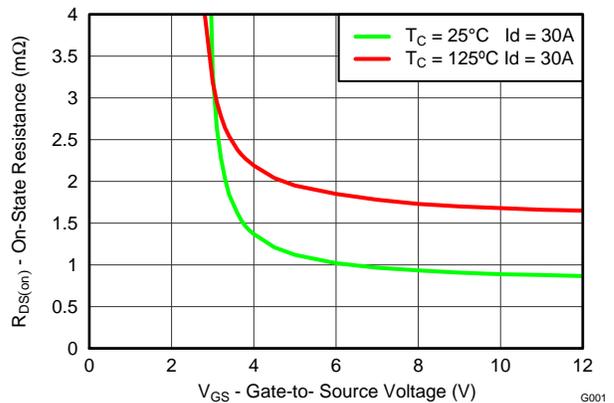


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

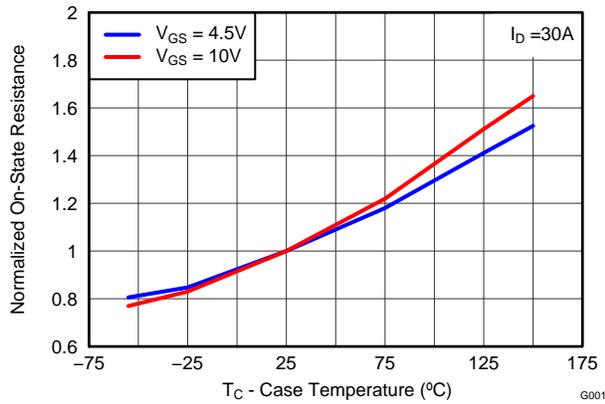


Figure 8. Normalized On-State Resistance vs. Temperature

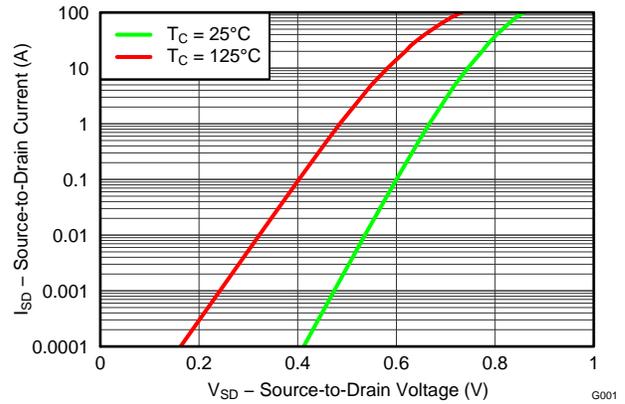


Figure 9. Typical Diode Forward Voltage

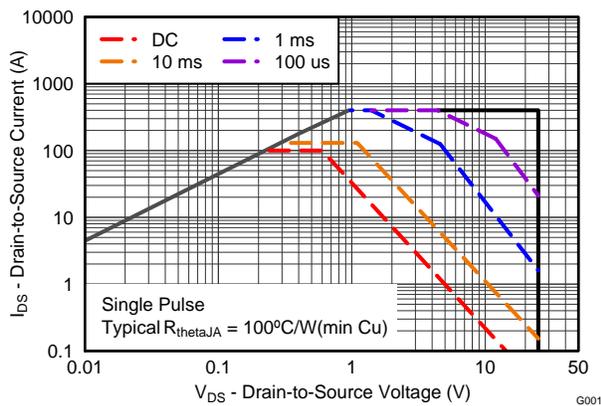


Figure 10. Safety Operating Area $T_C = 25^\circ\text{C}$

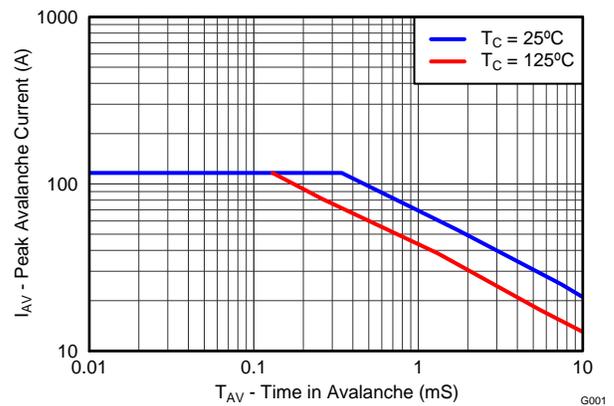


Figure 11. Single Pulse Unclamped Inductive Switching

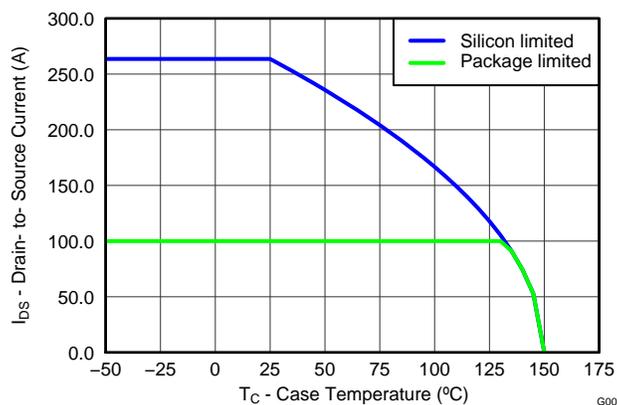
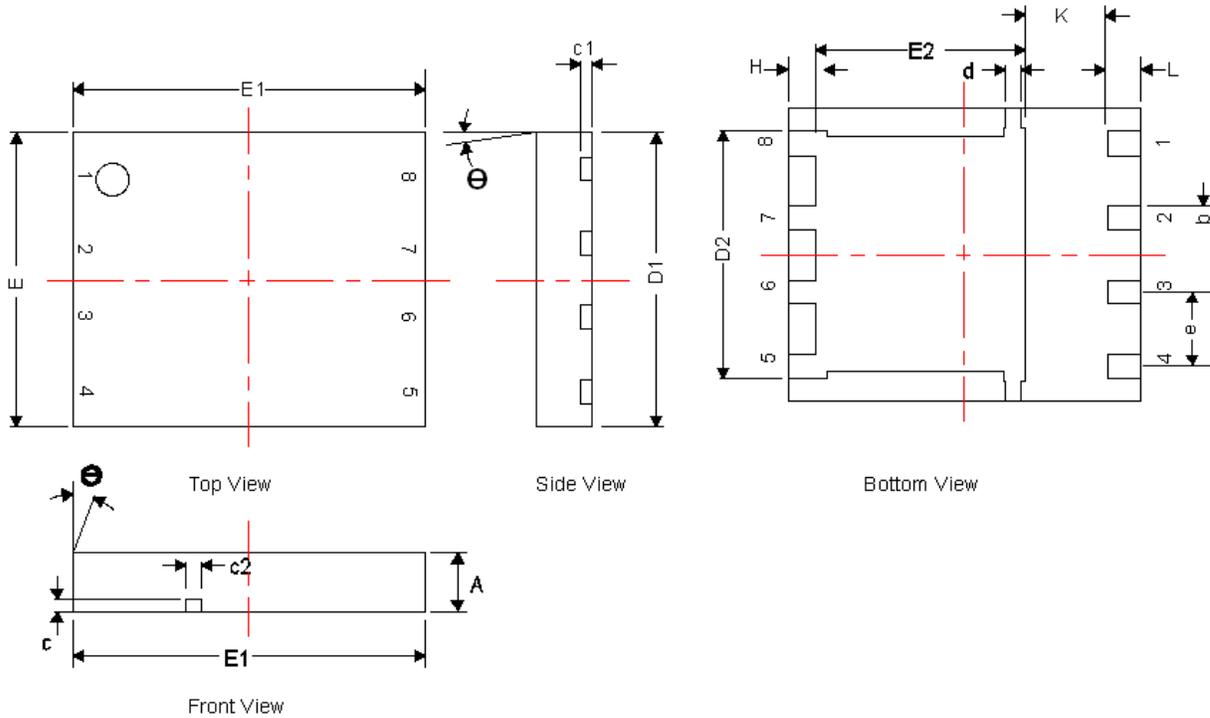


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.95	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
L	0.46	0.56	0.66
theta	0°	-	-
K	1.40 TYP		

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CSD16556Q5B	ACTIVE	VSON	DNK	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16556	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

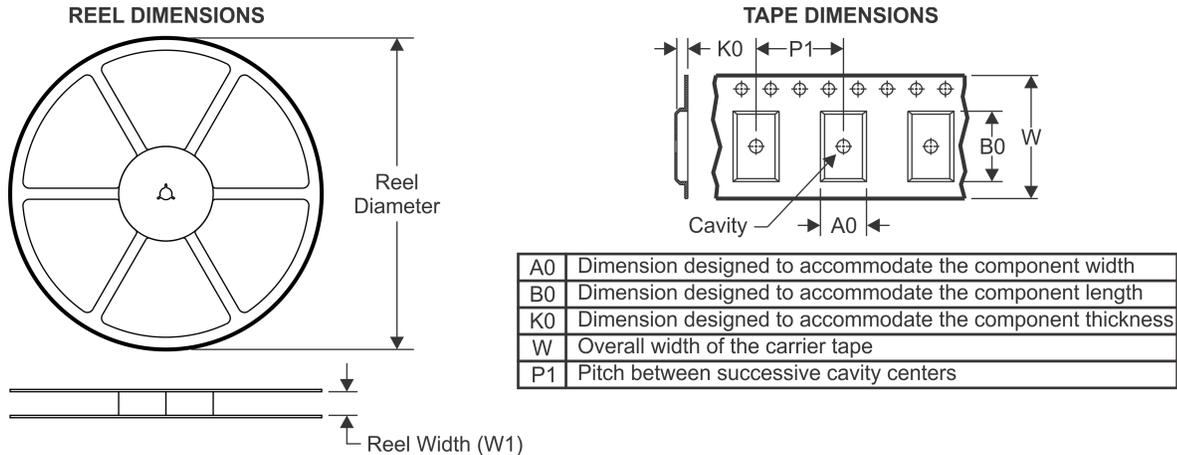
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION



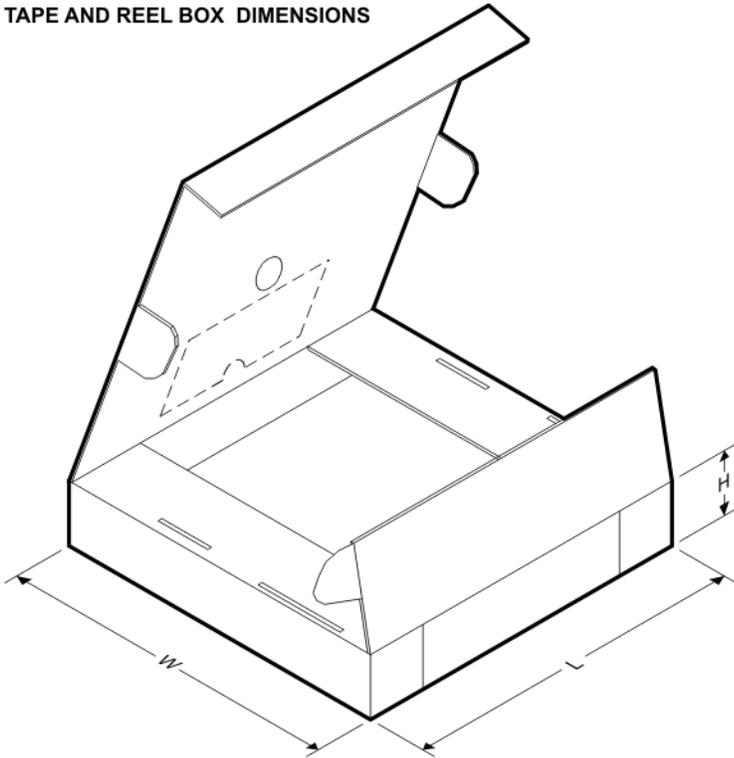
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16556Q5B	VSON	DNK	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16556Q5B	VSON	DNK	8	2500	335.0	335.0	32.0

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