PTB48600 —48-V Input

85 W Dual Complementary-Output DC/DC Converter for DSL

Features

- Dual Complementary Outputs (±5 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Temperature Shutdown
- Under-Voltage Lockout

- Temp Range: –40 to +85°C
- Fixed Frequency Operation
- Synchronizes with PTB4850x
- Powers line driver ICs for AC-7 and other xDSL chipsets
- Safety Approvals: (Pending)
  EN60950
  UL/cUL60950

Description

The PTB48600A is one of a series of isolated DC/DC converter modules that provide a pair of complementary supply voltages for powering line-driver ICs in xDSL telecom applications. These modules operate from a standard telecom (-48 V) central office supply and can provide up to a 85 W of power in a balanced load configuration.

The A-suffix module (±5 V) is designed to power the line driver ICs for the AC-7 ADSL chipset. It will also power any other applications that require a complementary supply with relatively balanced loads. The two complimentary outputs can also be configured as a single output of twice the voltage magnitude. As an example, the outputs of a PTB48600A can be adjusted up to ±6 V, and configured as a single 12-V output.

The PTB48600 includes an output "on/off" enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO).

The control inputs, "Enable" and "Sync In," are compatible with the "EN Out" and "Sync Out" signals of the PTB4850x DC/DC converter. This allows the power-up and switching frequency of a PTB48600 module to be directly controlled from a PTB48500. Together the PTB48500 and PTB48600 converters meet all the system power and sequencing requirements of the AC-7 ADSL chipset.

The PTB48600 employs double-sided surface mount construction. The package options include both through-hole and surface mount pin configurations.
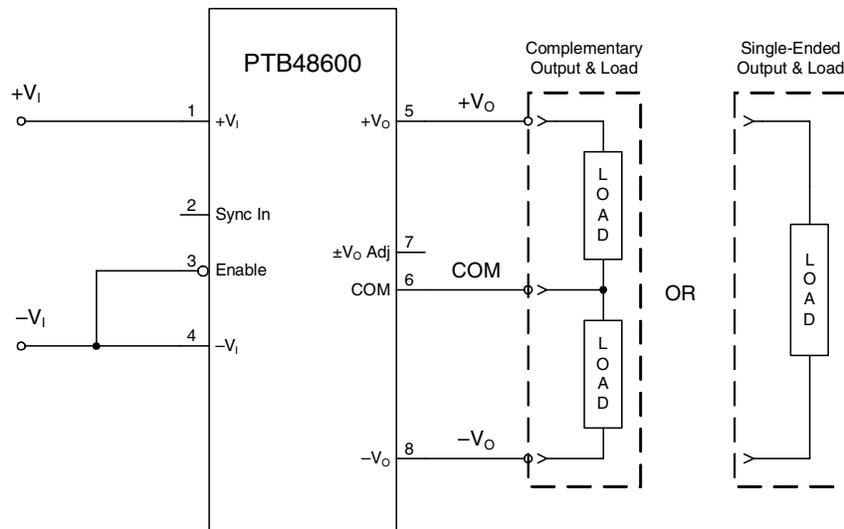
Pin Configuration

Pin	Function
1	+V_I
2	Sync In
3	Enable *
4	–V_I
5	+V_O
6	COM
7	V_O Adjust
8	–V_O

Shaded functions indicate signals that are referenced to –Vin.

* *Denotes negative logic:*
Open = Outputs Off
–Vin = Normal operation

Stand-Alone Application

TEXAS INSTRUMENTS

PTB48600 —48-V Input

**85 W Dual Complementary-Output
DC/DC Converter for DSL**

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Ordering Information

Base Pt. No. (PTB4860☐xxx)		Output Voltage (PTB48600☐xx)		Package Options (PT48600A☐☐)		
Order Prefix	**Description**	**Code**	**Voltage**	**Code**	**Description**	**Pkg Ref.** (1)
PTB48600xxx	Basic Model	A	±5 V	AH	Horiz. T/H	(ERT)
				AS	SMD, Standard (2)	(ERU)

Notes: (1) *Reference the applicable package reference drawing for the dimensions and PC board layout*
(2) *"Standard" option specifies 63/37, Sn/Pb pin solder material.*

Pin Descriptions

+V_I: The positive input supply for the module with respect to –V_I. When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.

–V_I: The negative input supply for the module, and the 0 VDC reference for the '*Enable**', and '*Sync In*' signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

+V_O: The positive output supply voltage, which is referenced to the '*COM*' node. The voltage at '+V_O' has the same magnitude, but is the complement to that at '-V_O'.

–V_O: The negative output supply voltage, which is referenced to the '*COM*' node. The voltage at '-V_O' has the same magnitude, but is the complement to that at '+V_O'.

COM: The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.

±V_O Adjust: Using a single resistor, this pin allows the magnitude of both '+V_O' and '–V_O' to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

Enable*: This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to -V_I. A logic '0' at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to –V_I. *Note: Connecting this input directly to the "EN Out" pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB48600) to power up in sequence.*

Sync In: This pin is used when the PTB48600 and PTB4850x DC/DC converter modules are used together. Connecting this pin to the '*Sync Out*' of the PTB4850x module allows the PTB48600 to be synchronized to the same switch conversion frequency as the PTB4850x.

Environmental and General Specifications (Unless otherwise stated, all voltages are with respect to –V_I)

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Input Voltage Range	V_I	Over output load range		36	48	75	VDC
Isolation Voltage		Input–output/input–case		1500	—	—	V
Capacitance		Input to output		—	1500	—	pF
Resistance		Input to output		10	—	—	MΩ
Operating Temperature Range	T_A	Over V_{in} Range		–40	—	+85	°C
Over-Temperature Protection	OTP	Shutdown threshold		—	115 (i)	—	°C
		Hysterisis		—	10	—	
Solder Reflow Temperature	T_{REFLOW}	Surface temperature of module body or pins				235 (ii)	°C
Storage Temperature	T_S	—		–40	—	125	°C
Mechanical Vibration		Mil-STD-883D, Method 2007.2	T/H	—	20	—	G's
		20-2000 Hz	SMD	—	2.5	—	
Mechanical Shock		Per Mil-STD-883D, Method 2002.3	T/H	—	500	—	G's
		1 msec, ½ Sine, mounted	SMD	—	250	—	
Weight	—			—	35	—	grams
Flammability	—	Meets UL 94V-O					

Notes: (i) *This parameter is defined by design*
(ii) *During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.*

PTB48600 —48-V Input

**85 W Dual Complementary-Output
DC/DC Converter for DSL**

SLTS239 JANUARY 2005

Specifications (Unless otherwise stated, $T_A = 25°C$, $V_I = 48$ V, $C_I = 0$ µF, $\pm C_O = 0$ µF, $|+I_O| = |-I_O|$, and $|\pm I_O| = 0.5\ |\pm I_O|_{max}$)

Characteristic	Symbol	Conditions		PTB48600A Min	Typ	Max	Units
Output Power	P_O	Total output power from $\pm V_O$		0	—	85 [1]	W
Output Current	$|\pm I_O|$	Over V_I range, $|+I_O|-|-I_O| \le 0.1$ A		0	—	8.5 [2]	A
Output Load Imbalance	$|+I_O|-|-I_O|$	$|+I_O| \ge 0.1$ A, $|-I_O| \ge 0.1$ A		0	—	1 [3]	A
Output Voltage	$|\pm V_O|$	Inlcudes set-point, line, $|+I_O|-|-I_O| \le 0.1$ A $-40 \le T_A \le +85°C$		4.75 [2]	5	5.25 [2]	V
Temperature Variation	ΔReg_{TEMP}	$-40 \le T_A \le +85°C$, $|\pm I_O| = 0.1$ A	$+V_O$ $-V_O$	— —	±1 ±1	— —	%V_o
Line Regulation	ΔReg_{LINE}	Over V_I range, balanced load	$\pm V_O$	—	±0.1	±0.4	%V_o
Load Regulation	ΔReg_{LOAD}	Over $\pm I_O$ range, balanced load	$\pm V_O$	—	±0.2	±0.4	%V_o
Efficiency	η			—	85	—	%
V_o Ripple (pk-pk)	$\pm V_R$	20 MHz bandwidth, $C_O = 10$ µF tantalum capacitor		—	20	30 [4]	mV$_{pp}$
Transient Response	t_{TR}	0.1 A/µs load step, 50% to 75% $\pm I_O$max		—	30	—	µs
	ΔV_{TR}	$|\pm V_O|$ over/undershoot		—	±1	—	%V_o
Over Current Threshold	$|\pm I_O|$ trip	$V_I = 36$ V, $|+I_O| = |-I_O|$, reset followed by auto-recovery		9	10	12	A
Short Circuit Current		Continuous over-current trip,	$|\pm I_O|_{PK}$	—	16	—	A
		$|+I_O| = |-I_O|$	Duty	—	10	—	%
Output Voltage Adjust Range	$|\pm V_O|$ adj	$|+V_O|$ and $|-V_O|$ adjust simultaneously		3.31	—	6	V
Switching Frequency	f_S	Over V_I and I_O ranges		440	470 [5]	500	kHz
Under-Voltage Lockout	V_I on V_I off	V_I increasing V_I decreasing		— —	33 32	— —	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	V_{IH} V_{IL}	Referenced to $-V_I$ (pin 4)		+3.6 −0.2	— —	+75 [6] +0.8	V
Input Low Current	I_{IL}			—	—	−1	mA
Standby Input Current	I_I standby	pin 3 open circuit		—	2	—	mA
Start-up Time	t_{ON}	$|\pm I_O| = 1$ A, $|\pm V_O|$ rising 0 to 0.95 $|\pm V_O|$ typ		6	10	22	ms
Internal Input Capacitance	C_I			—	3	—	µF
External Output Capacitance	$\pm C_O$	Capacitance from either output to COM		0	—	5,000 [7]	µF
Reliability	MTBF	Per Telcordia SR-332 50% stress, $T_A = 40°C$, gnd benign		2.8	—	—	10^6 Hrs

Notes:
(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within ±0.1 A of that flowing into $-V_O$.
(3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10 µF tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
(5) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(6) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_I$. The open-circuit voltage is 5 V max. If it is left open circuit the converter will operate when input power is applied.
(7) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.
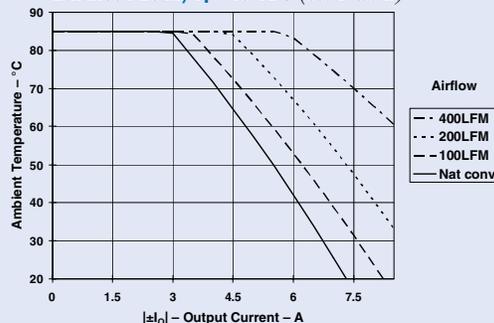
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Not Recommended for New Designs

Balanced

PTB48600 —48-V Input

Typical Characteristics

**85 W Dual Complementary-Output
DC/DC Converter for DSL**

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PTB48600A Characteristic Data @V$_{IN}$ =48 V *(See Notes A)*

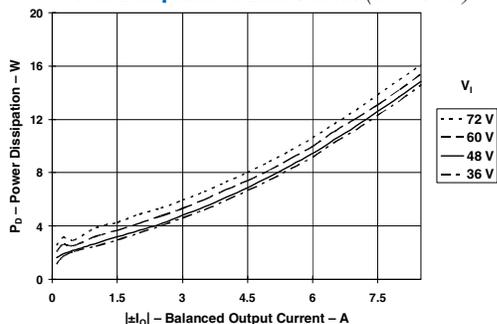**Safe Operating Area PTB48600A** *(See Note C)*
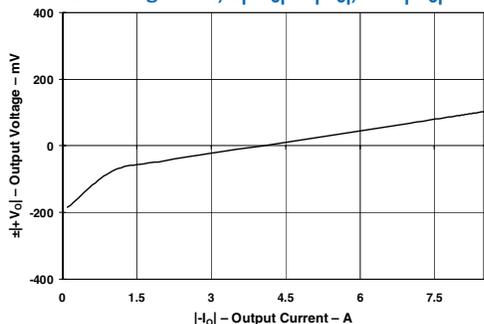
Efficiency vs Load Current *(See Note B)*
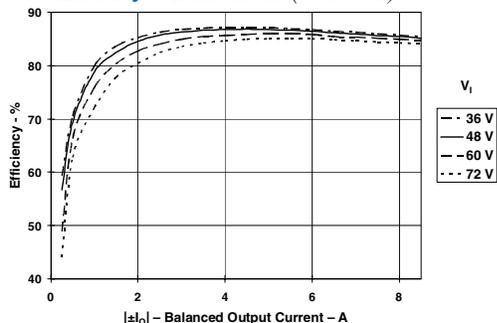
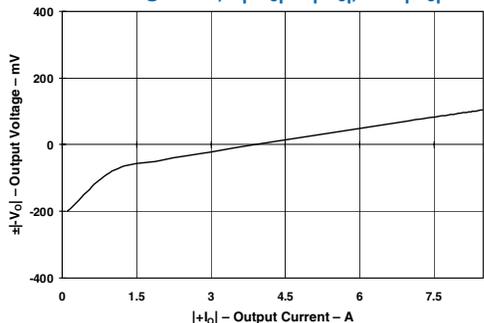**Balanced Load, V$_I$ =48 VDC** *(See Note B)*

Power Dissipation vs Load Current *(See Note B)*

Cross Regulation, Δ|+V$_0$| vs |−I$_0$|, with |+I$_0$| = 1 A

Cross Regulation, Δ|−V$_0$| vs |+I$_0$|, with |−I$_0$| = 1 A

Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *Under a balanced load, current flowing out of +V$_o$ is equal to that flowing into −V$_o$.*
Note C: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

TEXAS INSTRUMENTS

For technical support and further information visit http://power.ti.com

PTB48600

Adjusting the Output Voltages of the PTB48600 Series of DC/DC Converters

The PTB48600 DC/DC converter produces a balanced pair of complementary output voltages. They are identified $+V_O$ and $-V_O$, respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower. The adjustment method uses a single external resistor. [1] The value of the resistor determines the adjustment magnitude, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1-1. The placement of each resistor is as follows.

Adjust Up: To increase the magnitude of both output voltages, place a resistor R_1 between $\pm V_O$ *Adj* (pin 7) and the $-V_O$ (pin 8) voltage rail; see Figure 1-1(a).

Figure 1-1a
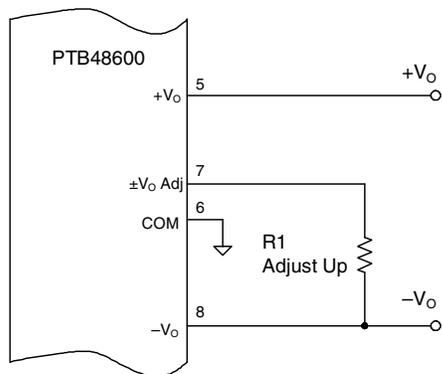
Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R2), between $\pm V_O$ *Adj* (pin 7) and the $+V_O$ (pin 5) voltage rail; see Figure 1-1(b).

Figure 1-1b
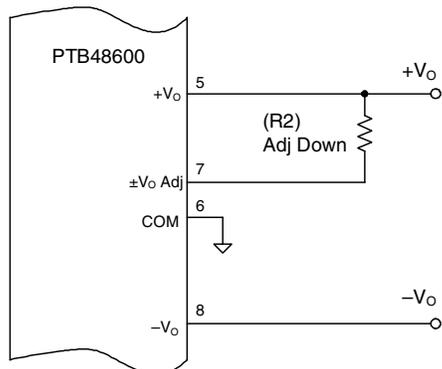
Calculation of Resistor Adjust Values

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R1 to adjust up, or (R2) to adjust down.

$$R1\ [\text{Adjust Up}] \quad = \quad \frac{V_R\,R_O}{2\,(V_A - V_O)} \quad - R_S \quad \text{k}\Omega$$

$$(R2)\ [\text{Adjust Down}] \quad = \quad \frac{R_o\,(2\,V_A - V_R)}{2\,(V_O - V_A)} \quad - R_S \quad \text{k}\Omega$$

Where: V_O = Magitude of the original $\pm V_O$
V_A = Magnitude of the adjusted voltage
V_R = The reference voltage from Table 1-1
R_O = The resistance value in Table 1-1
R_S = The series resistance from Table 1-1

Table 1-1

ADJUSTMENT RANGE AND FORMULA PARAMETERS	
Series Pt. No.	PTB48600A
V_O (nom)	5 V
V_A (min)	3.31 V
V_A (max)	6 V
V_R	2.495 V
R_O (kΩ)	7.5
R_S (kΩ)	9.09

Notes:

1. A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R1 or (R2) location, as close to the converter as possible.

2. Never connect capacitors to the $\pm V_O$ *Adj* pin. Capacitance added to this pin can affect the stability of the regulated output.

TEXAS INSTRUMENTS

Configuring the PTB48600 & PTB4850x DC/DC Converters for DSL Applications

When operated as a pair, the PTB48600 and PTB4850x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB48600 produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB48600 may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 2-1 shows the required cross-connects between the two converters to enable these two features.

Switching Frequency Synchronization
Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

Power-Up Sequencing
The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB48600 are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the "EN Out" pin of the PTB4850x is directly connected to the active-low "Enable" input of the PTB48600 (see Figure 2-1). This allows the PTB4850x to momentarily hold off the outputs from the PTB48600 until the logic-level voltages have risen first. Figure 2-2 shows the power-up waveforms of all four supply voltages from the schematic of Figure 2-1.
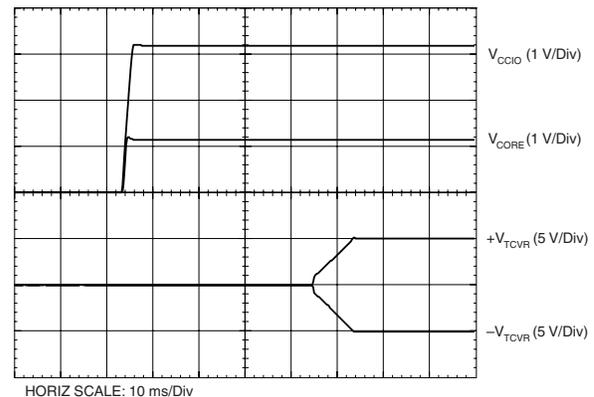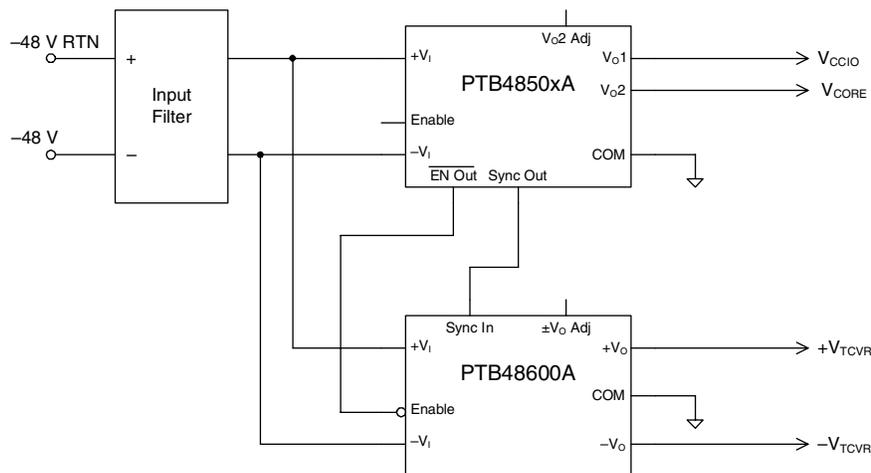
Figure 2-2; Power-Up Sequencing Waveforms

HORIZ SCALE: 10 ms/Div

Figure 2-1; Example of PTB4850x & PTB48600 Modules Configured for DSL Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PTB48600AAH	NRND	Through-Hole Module	ERT	8	9	Pb-Free (RoHS)	SN	N / A for Pkg Type	
PTB48600AAS	OBSOLETE	Surface Mount Module	ERU	8		TBD	Call TI	Call TI	
PTB48600AAZ	NRND	Surface Mount Module	ERU	8	9	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ERT (R–PDSS–T8)   **DOUBLE SIDED MODULE**

TOP VIEW

SIDE VIEW

PCB Layout

Note E

∅0.055 (1,40) Min. 8 Places
Plated through hole.
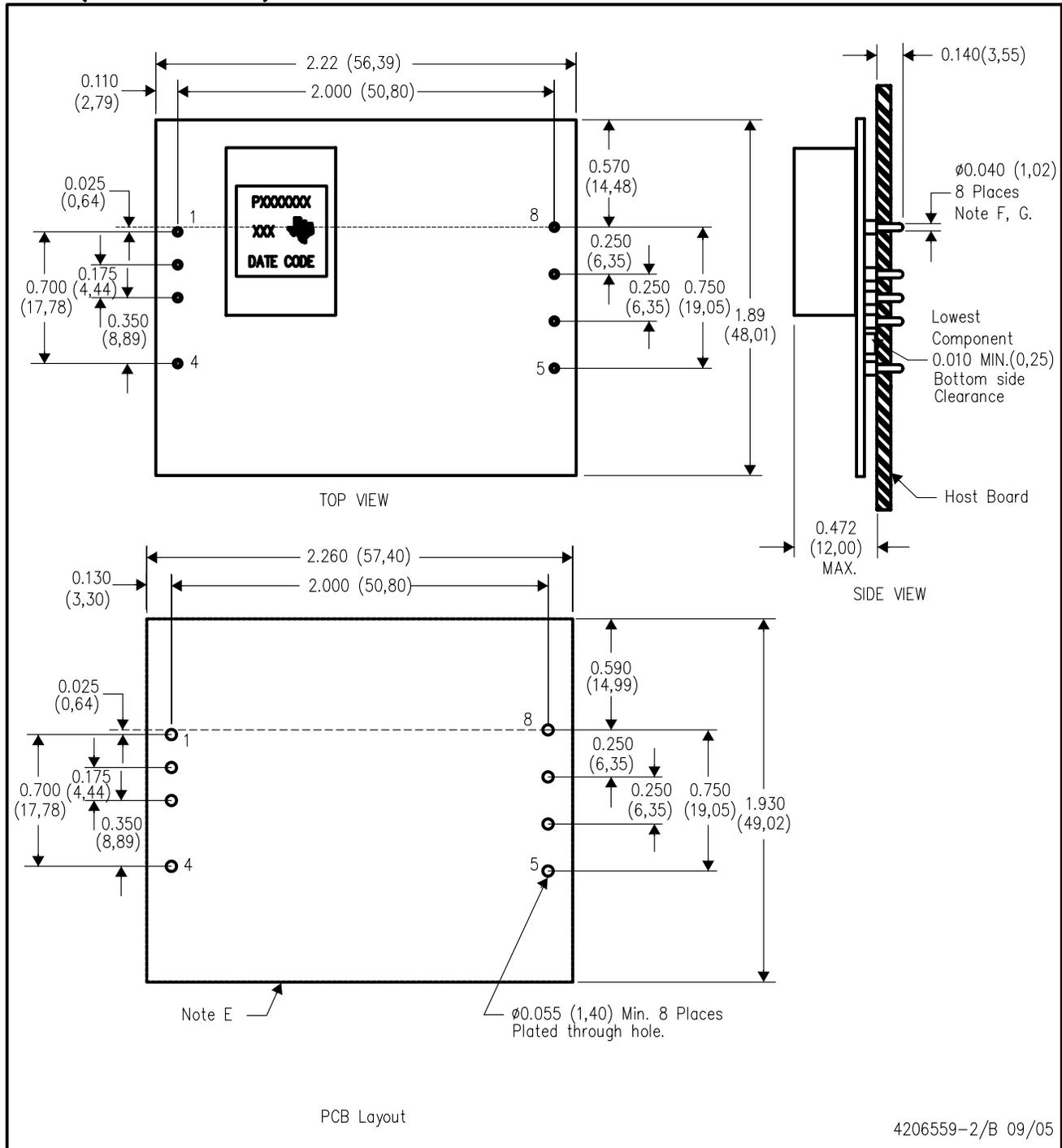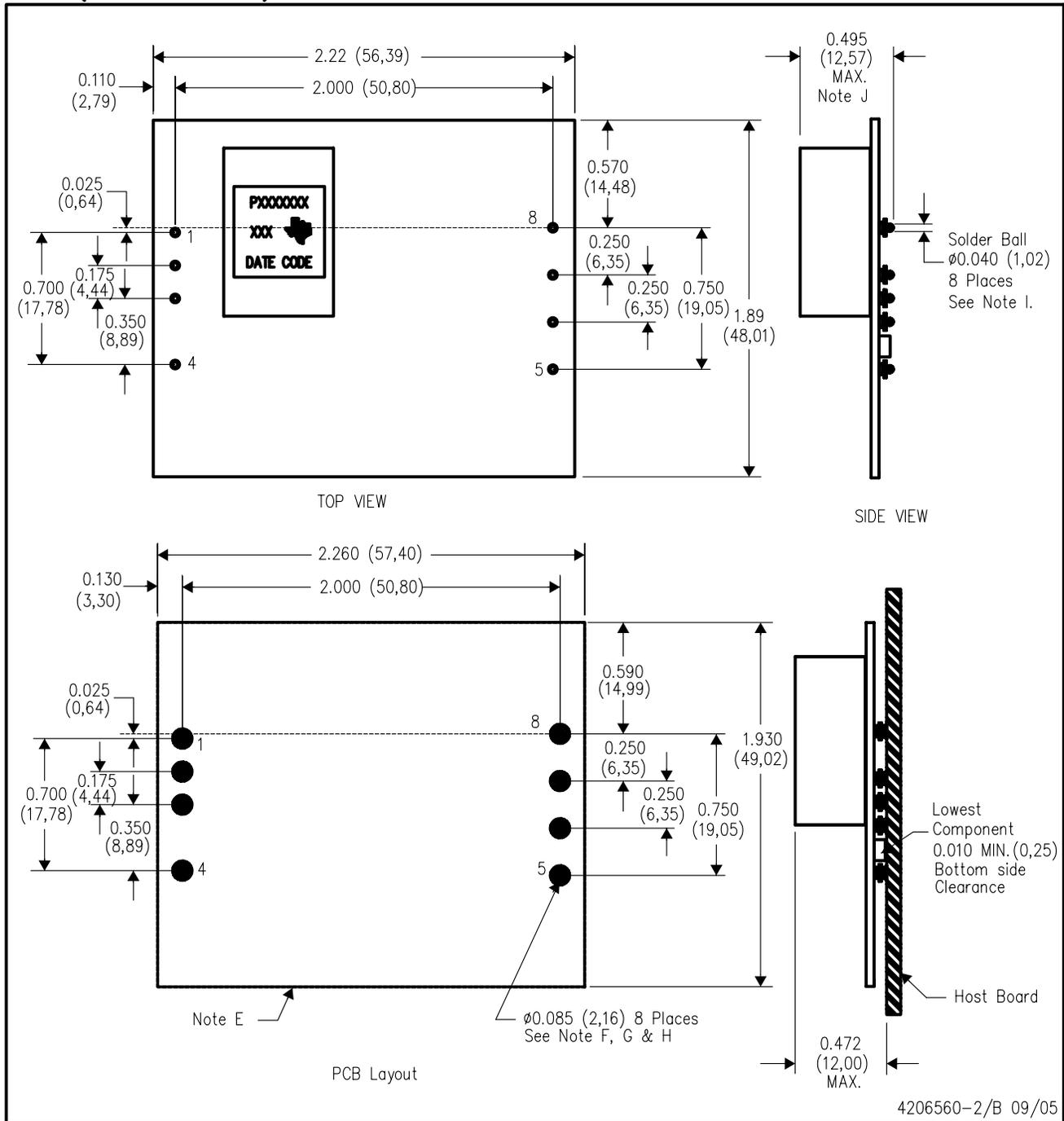
4206559–2/B 09/05

NOTES: A.   All linear dimensions are in inches (mm).
         B.   This drawing is subject to change without notice.
         C.   2 place decimals are ±0.020 (±0,51mm).
         D.   3 place decimals are ±0.010 (±0,25mm).
         E.   Recommended keep out area for user components.

         F.   Pins are 0.040" (1,02) diameter with
              0.070" (1,78) diameter standoff shoulder.
         G.   All pins: Material – Copper Alloy
                        Finish – Tin (100%) over Nickel plate

ERU (R–PDSS–T8)   DOUBLE SIDED MODULE

2.22 (56,39)
2.000 (50,80)
0.110 (2,79)
0.495 (12,57) MAX. Note J

0.025 (0,64)

PXXXXXXX
XXX
DATE CODE

0.570 (14,48)
8
0.250 (6,35)
1
0.250 (6,35) 0.750 (19,05)
0.700 (17,78)
0.175 (4,44)
1.89 (48,01)
0.350 (8,89)
4
5

TOP VIEW

Solder Ball
Ø0.040 (1,02)
8 Places
See Note I.

SIDE VIEW

2.260 (57,40)
2.000 (50,80)
0.130 (3,30)

0.025 (0,64)

0.590 (14,99)
8
0.250 (6,35)
1
0.250 (6,35)
0.700 (17,78)
0.175 (4,44)
1.930 (49,02)
0.750 (19,05)
0.350 (8,89)
4
5

Note E
Ø0.085 (2,16) 8 Places
See Note F, G & H

PCB Layout

Lowest Component
0.010 MIN. (0,25)
Bottom side Clearance

Host Board

0.472 (12,00) MAX.

4206560–2/B 09/05

NOTES: A. All linear dimensions are in inches (mm).
        B. This drawing is subject to change without notice.
        C. 2 place decimals are ±0.020 (±0,51mm).
        D. 3 place decimals are ±0.010 (±0,25mm).
        E. Recommended keep out area for user components.
        F. Power pin connection should utilize four or more vias
            to the interior power plane of 0.025 (0,63) I.D. per input,
            ground and output pin (or the electrical equivalent).

        G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
            Paste screen thickness: 0.006 (0,15).
        H. Pad type: Solder mask defined.
        I. All pins: Material − Copper Alloy
                     Finish − Tin (100%) over Nickel plate
                     Solder Ball − See product data sheet.
        J. Dimension prior to reflow solder.

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Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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Logic	logic.ti.com	Security	www.ti.com/security
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Wireless Connectivity	www.ti.com/wirelessconnectivity		