bq2502

Integrated Backup Unit

Features

- Power monitoring, backup supply, and switching for 3V battery-backup applications
- Write-protect control
- Input decoder for control of up to 2 banks of SRAM
- 3-volt backup power output
- Internal 130mAh lithium-coin cell
- Reset output for system power-on reset
- Less than 10ns chip-enable propagation delay
- 5% or 10% supply operation

General Description

The CMOS bq2502 Integrated Backup Unit provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

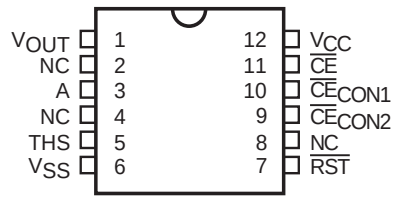
Power for the external SRAMs is switched from the V_{CC} supply to the internal battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the internal lithium supply to the V_{CC} supply.

The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

The internal lithium cell is initially electrically isolated, protecting the battery from accidental discharge. Connection to the battery is made only after the first application of V_{CC}.

Pin Connections



12-Pin 600-mil DIP Module

PN250201.eps

Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	chip-enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip-enable outputs
A	Bank select input
NC	No connect
V_{CC}	5-volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip-enable output pins from the bq2502. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip-enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip-enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold-select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V_{OUT}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{OUT} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µs maximum), the two chip-enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

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As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

The reset output ($\overline{RST}$) goes active within t_R (150µs maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup, as shown in Figure 1.

The internal lithium cell is capable of supplying 3V on V_{OUT} for an extended period. The cumulative length of time that the external SRAMs retain data in the absence of power is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data- retention currents for two external SRAMs are 1µA per SRAM at room temperature, nonvolatility is calculated to be for more than 7 years. If only one external SRAM is used, the data-retention time increases to more than 13 years.

The bq2502 battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq2502 provides SRAMs drawing 2µA total data-retention current with more than 10 years of nonvolatility.

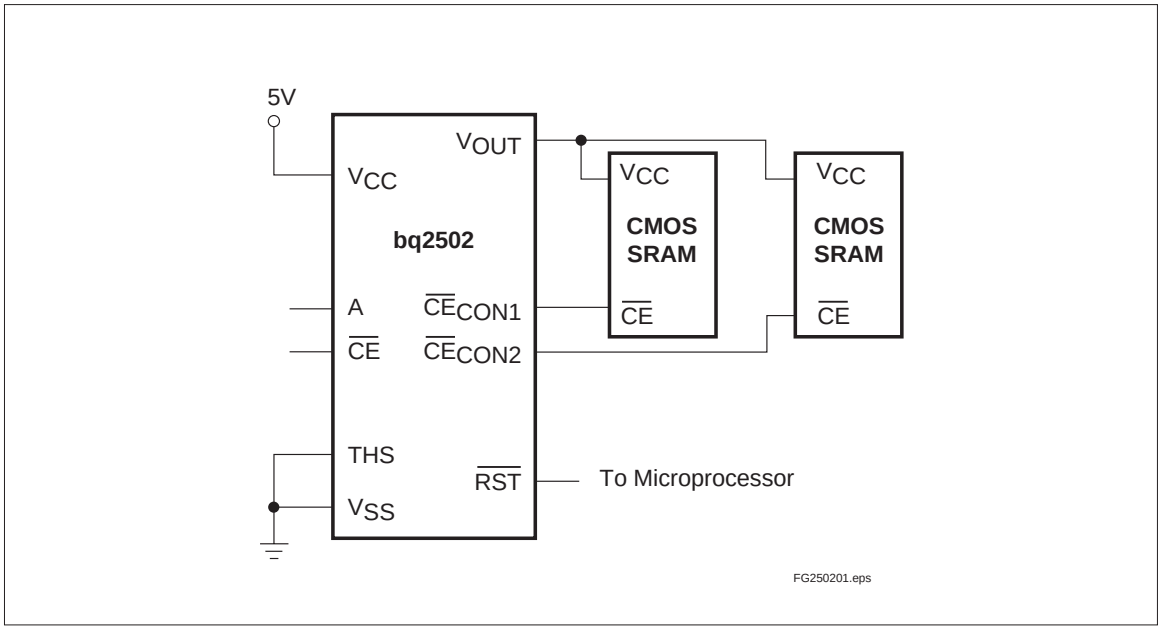

Figure 1. Hardware Hookup (5% Supply Operation)

As shipped from Benchmarq, the internal lithium cell is electrically isolated from V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$. Self-discharge in this condition is less than 0.5% per year at 20°C.

Note: Following the first application of V_{CC}, this isolation is broken, and the backup cell provides power to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ for the external SRAM.

Caution:

Take care to avoid inadvertent discharge through V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ after battery isolation has been broken.

This isolation can be reestablished by applying a valid isolation signal to the bq2502. See Figure 2. This signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power--down. Between these two points in time, $\overline{CE}$ must be brought to (0.48 to 0.52) * V_{CC} and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds 0.54*V_{CC} at any point between V_{CC} crossing V_{PFD} and V_{SO}.

The battery is connected to V_{OUT} immediately on subsequent application and removal of V_{CC}.

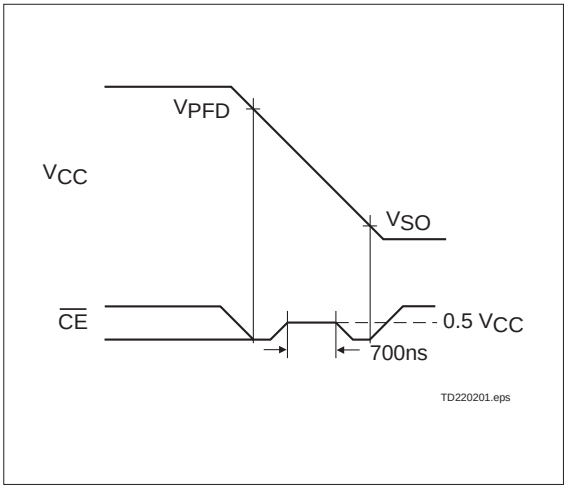

Figure 2. Battery Isolation Signal

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to +7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to +7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to 70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{OUT}
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BAT}.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAhr	Refer to graphs in Typical Battery Characteristics section.
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0mA
V_{OHB}	V_{OH}, backup supply	V_{BAT} - 0.3	-	-	V	$V_{BAT} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0mA
V_{BAT}	Internal battery voltage	-	2.9	-	V	Refer to graphs in Typical Battery Characteristics section.
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{OUT}
V_{SO}	Supply switch-over voltage	-	2.9	-	V	
I_{CCDR}	Data-retention mode current from internal battery	-	-	100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, and $\overline{RST}$.
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BAT}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BAT}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage from internal battery	V_{BAT} - 0.2	-	-	V	$V_{CC} < V_{BAT}$, I_{OUT} = 100µA, from internal battery
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC}$ - 0.3V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BAT}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3

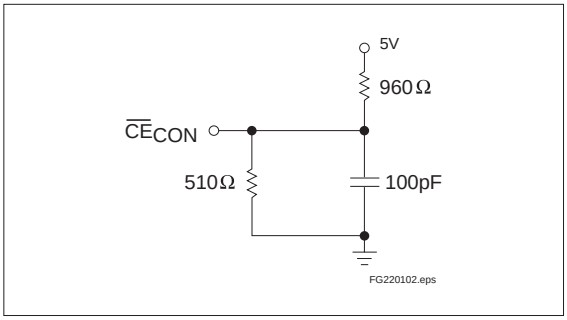

Figure 3. Output Load

Power-Fail Control (T_A = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

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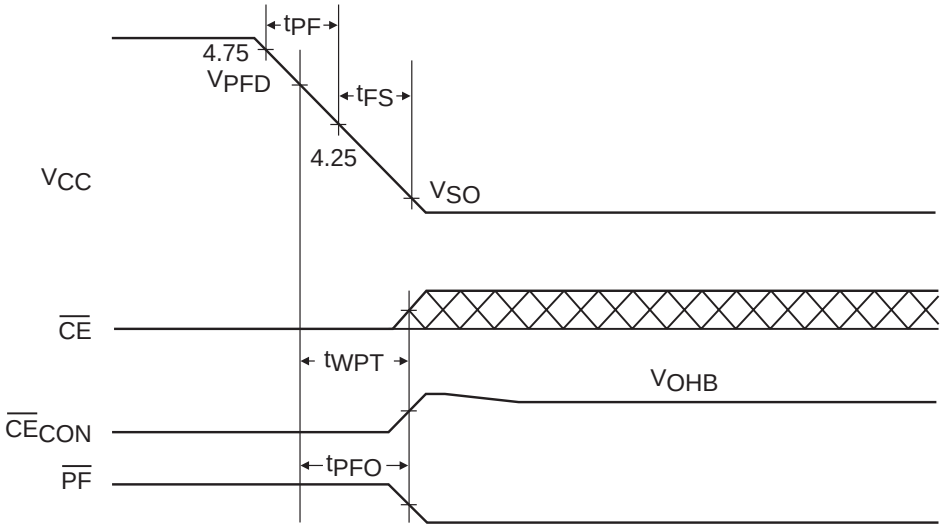
Power-Down Timing



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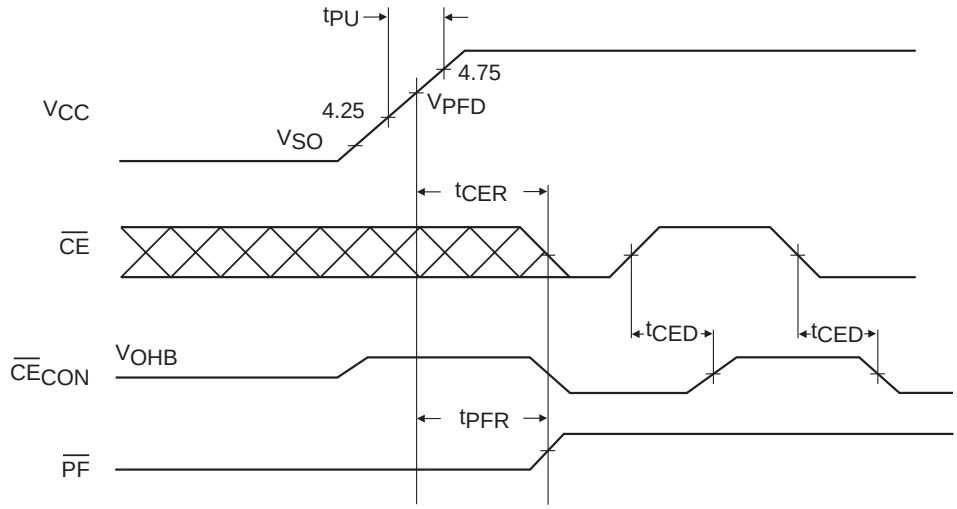
Power-Up Timing



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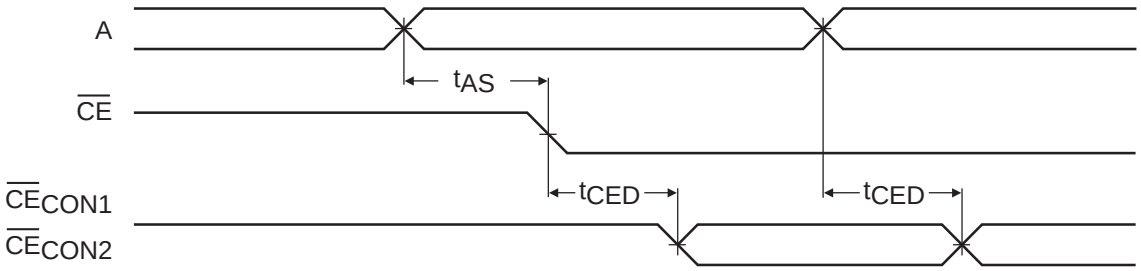
Address-Decode Timing



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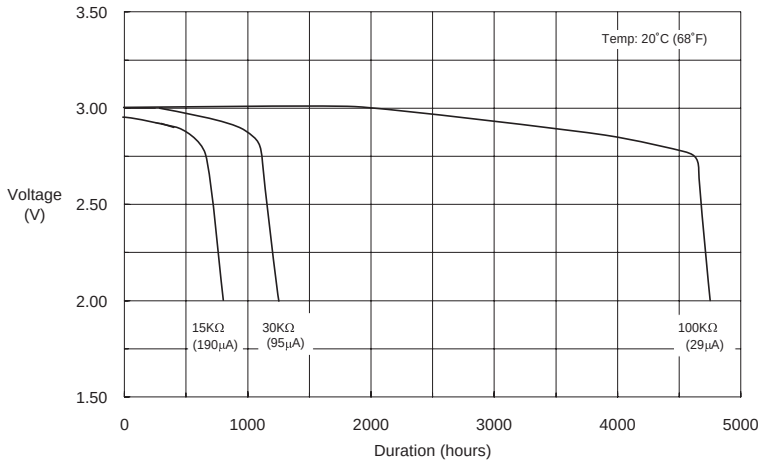
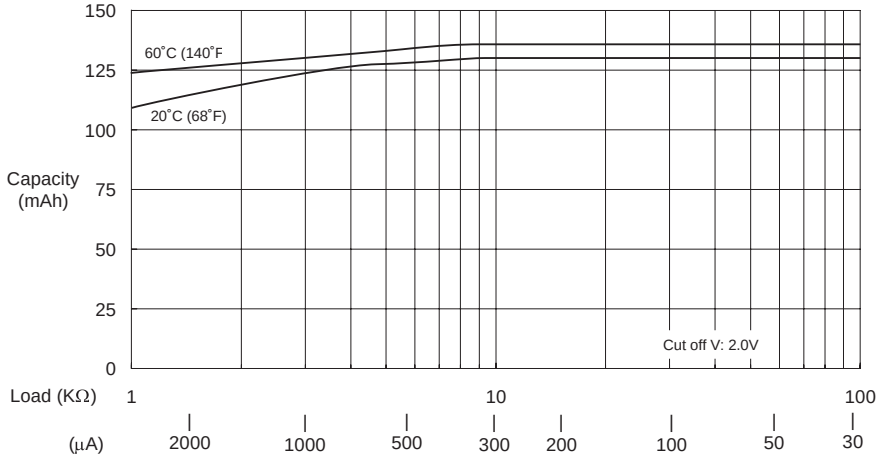
Typical Battery Characteristics (source = Panasonic)

CR1632 Load Characteristics



CR1632 Capacity vs. Load Resistance



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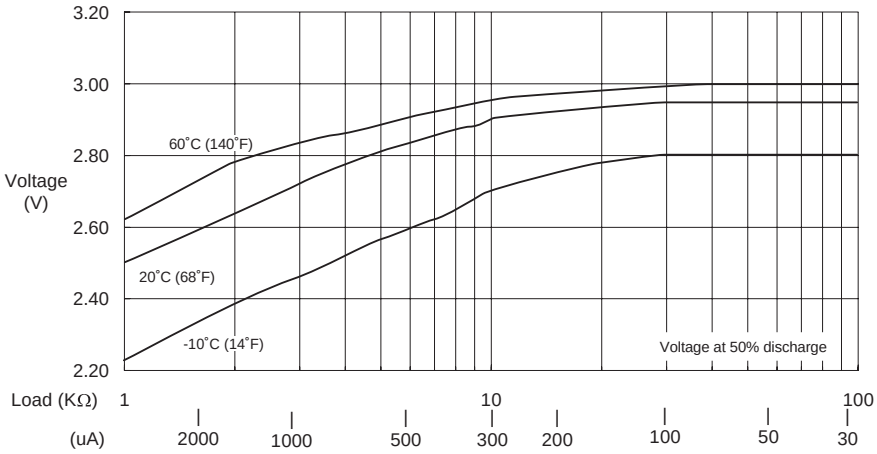
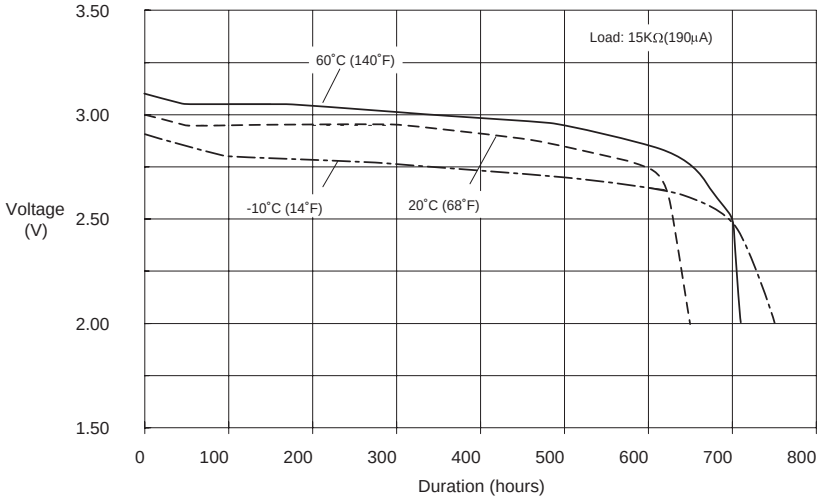
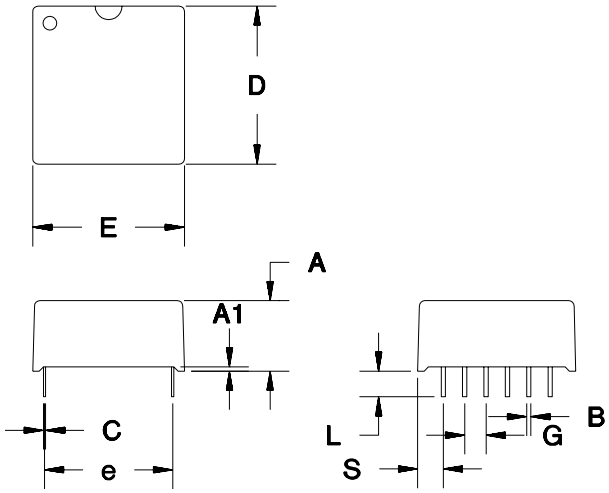
CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics



12-Pin Module



12-Pin Module (MA)

Dimension	Minimum	Maximum
A	0.365	0.375
A1	0.015	-
B	0.017	0.023
C	0.008	0.013
D	0.710	0.740
E	0.710	0.740
e	0.590	0.630
G	0.090	0.110
L	0.120	0.150
S	0.105	0.130

All dimensions are in inches.

Ordering Information

bq2502

Package Option:
MA = 12-pin DIP module

Device:
bq2502 Integrated Backup Unit

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