DUAL 4-A PEAK HIGH-SPEED LOW-SIDE POWER MOSFET DRIVERS

Check for Samples: UCC27323-Q1, UCC27324-Q1, UCC27325-Q1

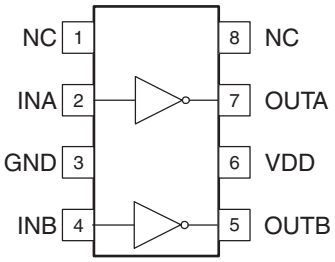
FEATURES

- **Qualified for Automotive Applications**
- **Industry-Standard Pinout**
- **High Current Drive Capability of ±4 A at the Miller Plateau Region**
- **Efficient Constant Current Sourcing Even at Low Supply Voltages**
- **TTL-/CMOS-Compatible Inputs Independent of Supply Voltage**
- **20-ns Typical Rise and 15-ns Typical Fall Times with 1.8-nF Load**
- **Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising**
- **Supply Voltage of 4 V to 15 V**
- **Supply Current of 0.3 mA**
- **Dual Outputs Can Be Paralleled for Higher Drive Current**
- **Available in Thermally Enhanced MSOP PowerPAD™ Package with 4.7°C/W θ_{JC}**
- **Rated From –40°C to 125°C**
- **TrueDrive™ Output Architecture Using Bipolar and CMOS Transistors in Parallel**

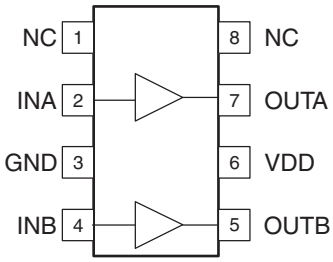
APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**
- **Class D Switching Amplifiers**

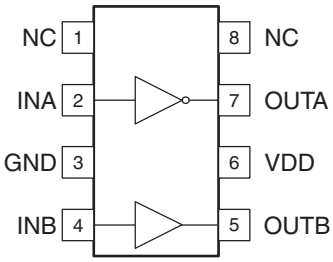
UCC27323
(DUAL INVERTING)
D, DGN, OR P PACKAGE
(TOP VIEW)



UCC27324
(DUAL NONINVERTING)
D, DGN, OR P PACKAGE
(TOP VIEW)



UCC27325
(ONE INVERTING, ONE NONINVERTING)
D, DGN, OR P PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The UCC27323/UCC27324/UCC27325 high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered — dual inverting, dual noninverting, and one inverting and one noninverting driver. The thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. The drivers are also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages.

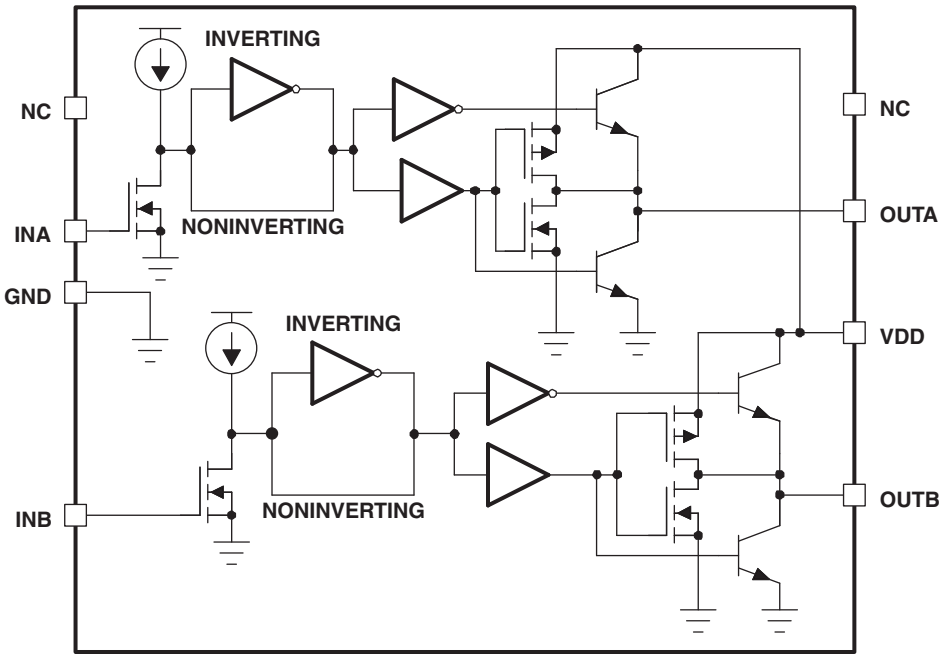
Using a design that inherently minimizes shoot-through current, these drivers deliver 4 A of current where it is needed most, at the Miller plateau region during the MOSFET switching transition. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

ORDERING INFORMATION(1)

$T_A = T_J$	OUTPUT CONFIGURATION	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Dual inverting	PowerPAD – DGN	Reel of 2000	UCC27323QDGNRQ1	PREVIEW
		PDIP – P	Tube of 1000	UCC27323QPQ1	PREVIEW
		SOIC – D	Reel of 2500	UCC27323QDRQ1	PREVIEW
	Dual noninverting	PowerPAD – DGN	Reel of 2000	UCC27324QDGNRQ1	PREVIEW
		PDIP – P	Tube of 1000	UCC27324QPQ1	PREVIEW
		SOIC – D	Reel of 2500	UCC27324QDRQ1	27324Q
	One inverting, One noninverting	PowerPAD – DGN	Reel of 2000	UCC27325QDGNRQ1	PREVIEW
		PDIP – P	Tube of 1000	UCC27325QPQ1	PREVIEW
		SOIC – D	Reel of 2500	UCC27325QDRQ1	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	NC		No connection. Should be grounded.
2	INA	I	Input A. Input signal of the A driver. Has logic-compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
3	GND		Common ground. Should be connected very closely to the source of the power MOSFET that the driver is driving.
4	INB	I	Input B. Input signal of the A driver. Has logic-compatible threshold and hysteresis. If not used, this input should be tied to either V_{DD} or GND. It should not be left floating.
5	OUTB	O	Driver output B. The output stage can provide 4-A drive current to the gate of a power MOSFET.
6	VDD	I	Supply. Supply voltage and the power input connection for this device.
7	OUTA	O	Driver output A. The output stage can provide 4-A drive current to the gate of a power MOSFET.
8	NC		No connection. Should be grounded.

Table 1. FUNCTION TABLE

INPUTS		UCC27323 OUTPUTS		UCC27324 OUTPUTS		UCC27325 OUTPUTS	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	H	H	L	L	H	L
L	H	H	L	L	H	H	H
H	L	L	H	H	L	L	L
H	H	L	L	H	H	L	H

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 16 V
I_O	Output current (OUTA, OUTB)	DC, I_{OUT_DC}	0.3 A
		Pulsed (0.5 µs), I_{OUT_PULSED}	4.5 A
P_D	Power dissipation at T_A = 25°C	DGN package	3 W
		D package	650 mW
		P package	350 mW
T_J	Junction operating temperature		–55°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C
T_{lead}	Lead temperature	Soldering, 10 s	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

POWER DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING (1) T_A = 70°C (mW)	DERATING FACTOR(1) T_A > 70°C (mW/°C)
D (SOIC-8)	42	84 to 160(2)	344 to 655(2)	6.25 to 11.9(2)
P (PDIP-8)	49	110	500	9
DGN (MSOP-8 PowerPAD)(3)	4.7	50 to 59(2)	1370(4)	17.1(4)

(1) 125°C operating junction temperature is used for power rating calculations.
(2) The range of values indicates the effect of the PC board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the PC board where possible to spread the heat away form the device more effectively. For information on the PowerPAD package, see the technical brief, *PowerPad™ Thermally Enhanced Package*, Texas Instruments literature number SLMA002 and the application brief, *PowerPad™ Made Easy*, Texas Instruments literature number SLMA004.
(3) The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.
(4) 150°C operating junction temperature is used for power rating calculations.

OVERALL ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 15 V, T_A = –40°C to 125°C (unless otherwise noted), T_A = T_J

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Static operating current	UCC27323	INA = 0 V	INB = 0 V		300	450	µA
				INB = HIGH		300	450	
			INA = HIGH	INB = 0 V		300	450	
				INB = HIGH		300	450	
		UCC27324	INA = 0 V	INB = 0 V		2	80	
				INB = HIGH		300	450	
			INA = HIGH	INB = 0 V		300	450	
				INB = HIGH		600	800	
		UCC27325	INA = 0 V	INB = 0 V		150	300	
				INB = HIGH		450	600	
			INA = HIGH	INB = 0 V		150	300	
				INB = HIGH		450	600	

INPUT (INA, INB) ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logic 1 input threshold		2			V
V_{IL}	Logic 0 input threshold				1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}	–10	0	10	µA

OUTPUT (OUTA, OUTB) ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
	Output current(1) (2)	V_{DD} = 14 V			4		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA			300	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA			22	45	mV
	Output resistance high(3)	I_{OUT} = –10 mA, V_{DD} = 14 V	25°C	25	30	35	Ω
			Full range	18		43	
	Output resistance low(3)	I_{OUT} = 10 mA, V_{DD} = 14 V	25°C	1.9	2.2	2.5	Ω
			Full range	0.9		4	
	Latch-up protection(1)			500			mA

(1) Specified by design
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

SWITCHING CHARACTERISTICS

V_{CC} = 4.5 V to 15 V, T_A = –40°C to 125°C (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		20	40	ns
t_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF		15	40	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF		25	40	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF		35	50	ns

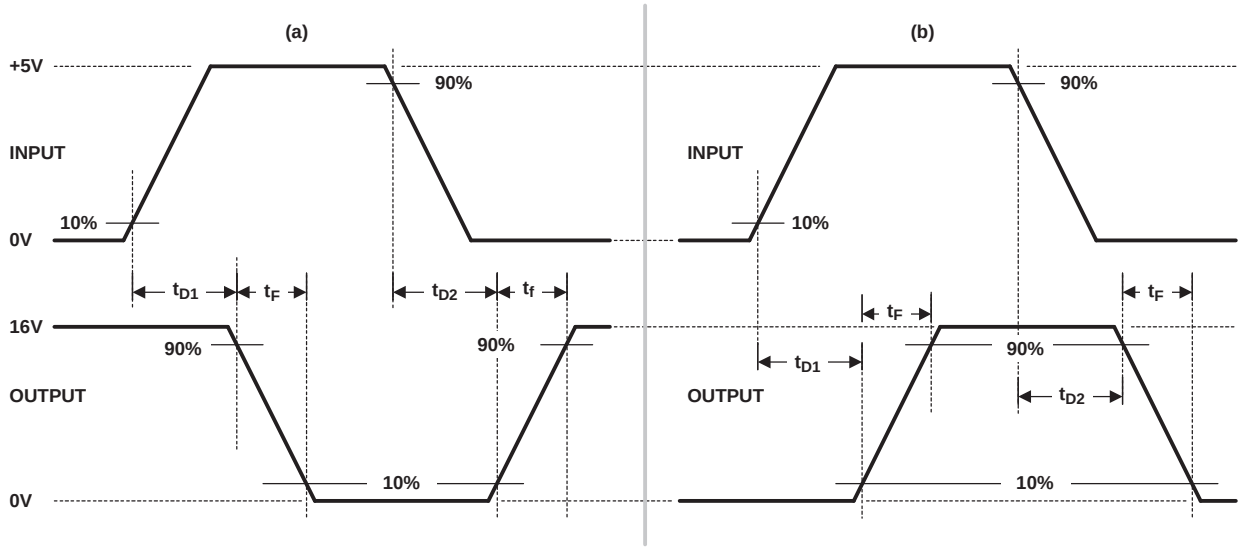


Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

APPLICATION INFORMATION

General Information

High-frequency power supplies often require high-speed high-current drivers such as those available in the UCC2732x family. A leading application is the need to provide a high-power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver is used to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices, which can present an extremely large load to the control circuitry.

Drivers are used when it is not feasible to have the primary PWM regulator directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are intended to drive only the high-impedance input to a driver such as the UCC2732x. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltage, yet it is equally compatable with 0 V to V_{DD} signals.

The inputs of UCC2732x family of drivers are designed to withstand 500-mA reverse current without damage to the device or logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor also may help remove power dissipation from the device package, as discussed in the *Thermal Considerations* section.

Output Stage

Inverting outputs of the UCC27323 and OUTA of the UCC27325 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27324 and OUTB of the UCC27325 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both V_{DD} and GND. The pullup/pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot, due to the body diode of the external MOSFET. This means that, in many cases, external Schottky-clamp diodes are not required.

The UCC27323 family delivers a 4-A gate drive when it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains. A unique bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2732x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver.[1]

Two circuits are used to test the current capabilities of the UCC27323 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 2 is used to verify the current sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27323 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

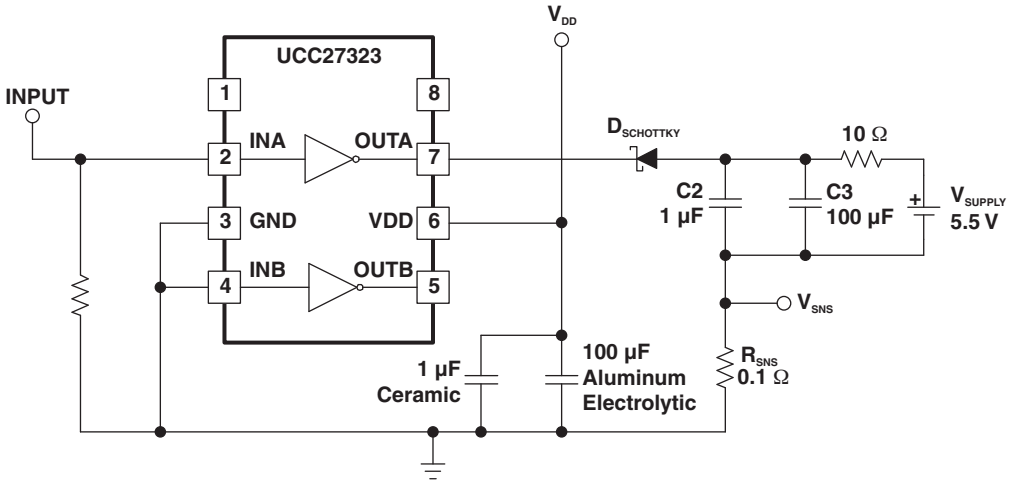


Figure 2.

The circuit in Figure 3 is used to test the current source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC27323 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

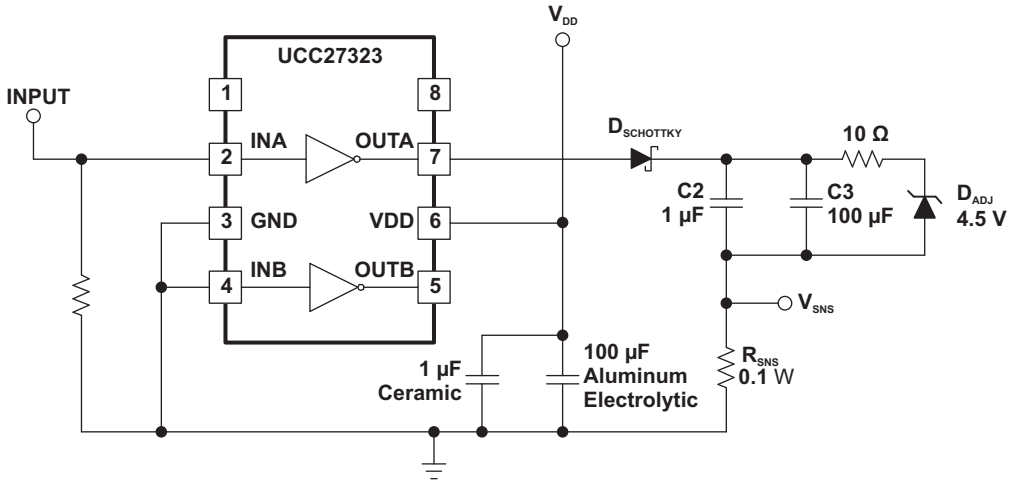


Figure 3.

It should be noted that the current-sink capability is slightly stronger than the current source capability at lower V_{DD}. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 4.

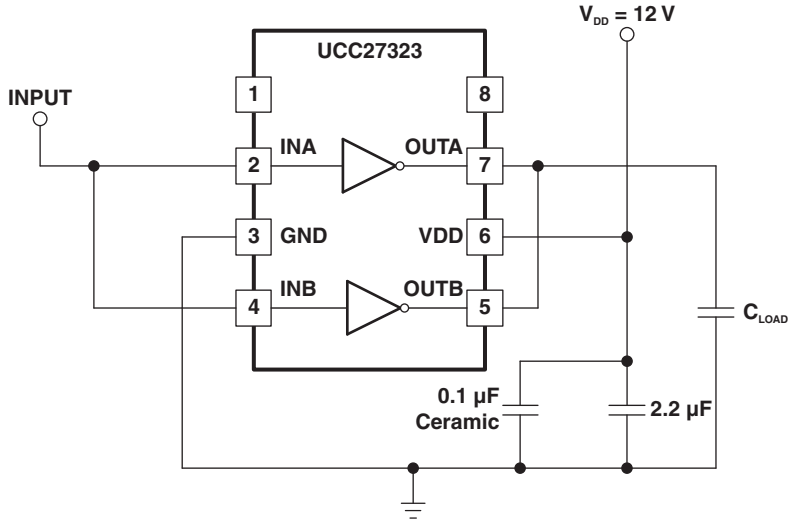


Figure 4.

Operational Waveforms and Circuit Layout

Figure 5 shows the circuit performance achievable with a single driver (half of the 8-pin device) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Sink and source currents of the driver are dependent upon the VDD value and the output capacitive load. The larger the VDD value the higher the current capability, and the larger the capacitive load the higher the current sink/source capability. Trace resistance and inductance, including wires and cables for testing, slows down the rise and fall times of the outputs which reduces the current capabilities of the driver. To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive output load value in order to swap out the effect of the inductance values.

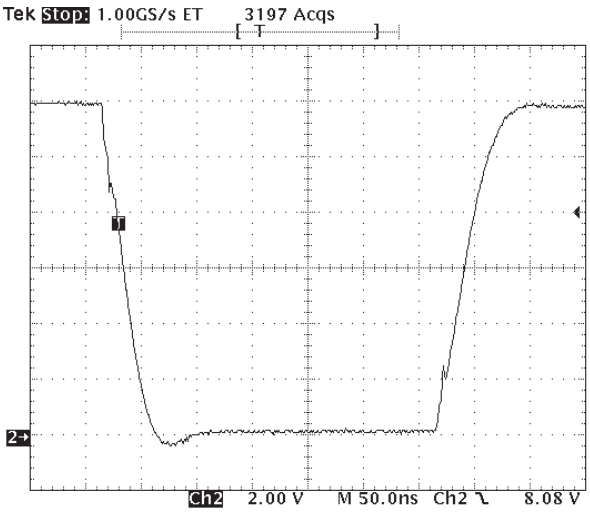


Figure 5.

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high Δi/Δt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver as close as possible to the leads. The driver layout has ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections also should be made with a small enclosed loop area to minimize the inductance.

V_{DD}

Although quiescent V_{DD} current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$I_{OUT} = Q_g \times f$

Where f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-μF ceramic capacitor should be located closest to the V_{DD} to ground connection. In addition, a larger capacitor (such as 1-μF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC2732x drivers are capable of delivering 4 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to quickly turn on the device. Then, to turn off the device, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion, because it is the most common type of switching device used in high-frequency power-conversion equipment.

References 1 and 2 discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 includes information on the previous generation of bipolar gate drivers.

When a driver is tested with a discrete capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = ½CV^2$

Where C is the load capacitor and V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by:

$P = 2 \times ½CV^2f$

Where f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this equates to a current of:

$I = P / V = 0.432\ W / 12\ V = 0.036\ A$

The actual current measured from the supply was 0.037 A, which is very close to the predicted value. But, the I_{DD} current that is due to the internal consumption should be considered. With no load, the current draw is 0.0027 A. Under this condition, the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high-frequency switching spikes and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to the expected value.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Q_g = CeffV to provide the following equation for power:

$P = C \times V^2 \times f = Q_g \times f$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2732x family of drivers is available in three different packages to cover a range of application requirements.

As shown in Power Dissipation Ratings, the SOIC-8 (D) and PDIP-8 (P) packages have power ratings of approximately 0.5 W at T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12-V V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD™ package (DGN) significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 2, the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the package, reducing the θ_{JC} to 4.75°C/W. Data is presented in Reference 2 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 3. This allows a significant improvement in heatsink capability over that available in the D or P packages and is shown to more than double the power capability of the D and P packages.

NOTE

The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

References

1. Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, Laszlo Balogh (SLUP133)
2. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Bill Andreycak (SLUA105)
3. *PowerPad Thermally Enhanced Package* (SLMA002)
4. *PowerPAD Made Easy* (SLMA004)

REVISION HISTORY

Changes from Original (March, 2008) to Revision A **Page**

- Added an extra table note in Power Dissipation Ratings table for the DGN package specifying that T_J = 150°C. 4
- Added $T_A = T_J$ to header of Overall Electrical Characteristics table. 4
- Changed direction of SCHOTTKY Diode and changed 10 W to 10 Ω in Figure 3. 7
- Added an extra paragraph before Figure 5. 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC27324QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

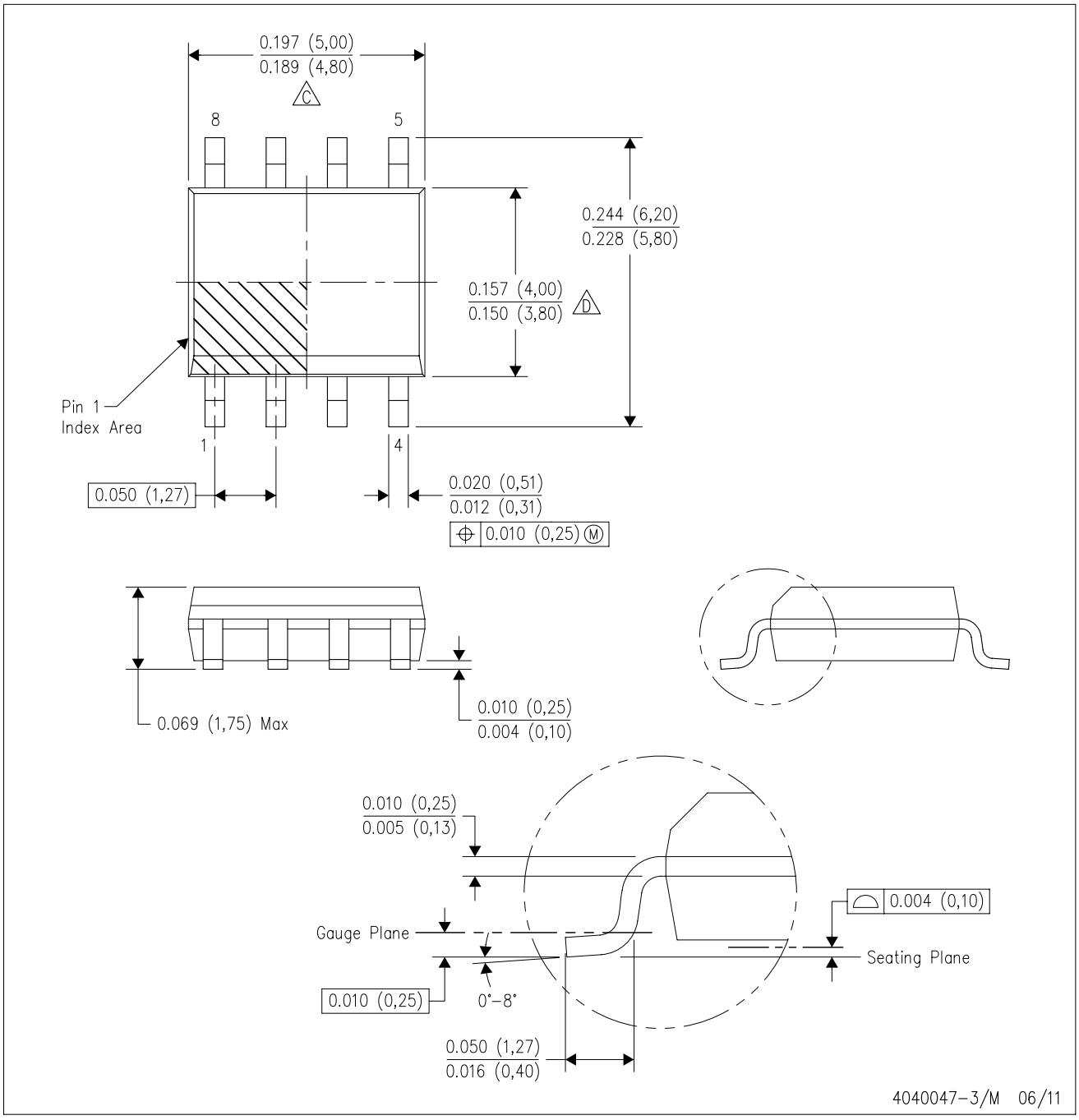
OTHER QUALIFIED VERSIONS OF UCC27324-Q1 :

- Catalog: UCC27324

NOTE: Qualified Version Definitions:

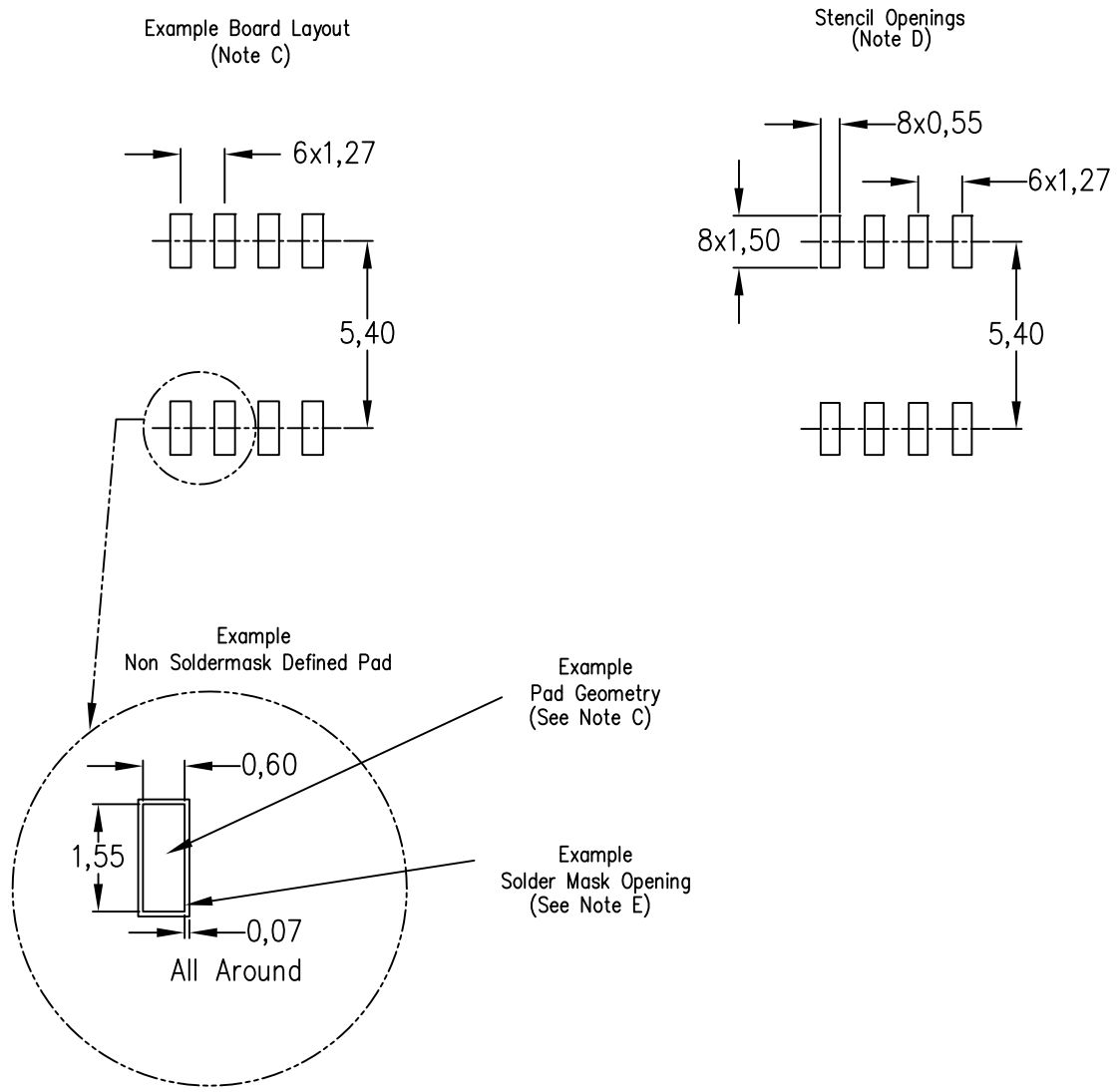
- Catalog - TI's standard catalog product

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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