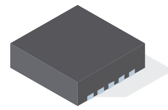


1-A, SINGLE-CHIP, LI-ION AND LI-POL CHARGER IC

Check for Samples: bq24080, bq24081

FEATURES

- **Integrated Power FET and Current Sensor for Up to 1-A Charge Applications From AC Adapter**
- **Precharge Conditioning With Safety Timer**
- **Charge and Power-Good Status Output**
- **Automatic Sleep Mode for Low Power Consumption**
- **Integrated Charge-Current Monitor**
- **Fixed 7-Hour Fast Charge Safety Timer**
- **Ideal for Low-Dropout Charger Designs for Single-Cell Li-Ion or Li-Pol Packs in Space-Limited Portable Applications**
- **Small 3-mm × 3-mm SON Package**

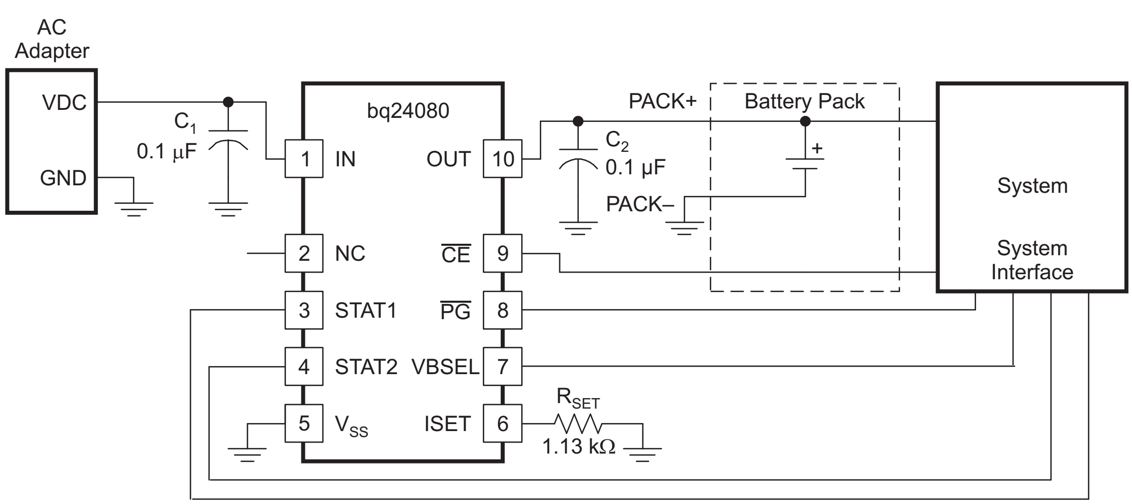
APPLICATIONS

- **PDAs, MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Smartphones**

DESCRIPTION

The bq24080 and bq24081 are highly integrated and flexible Li-Ion linear charge devices targeted at space-limited charger applications. They offer an integrated power FET and current sensor, high-accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device. An external resistor sets the magnitude of the charge current.

The device charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination. The device automatically restarts the charge if the battery voltage falls below an internal threshold. The device automatically enters sleep mode when the ac adapter is removed.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	CHARGE REGULATION VOLTAGE (V)	FUNCTIONS	FAST-CHARGE TIMER (HOURS)	PART NUMBER(1) (2)	MARKINGS
–40°C to 125°C	4.2	$\overline{CE}$ and $\overline{PG}$	7	bq24080DRCR	BRO
				bq24080DRCT	
–40°C to 125°C	4.2	$\overline{TE}$ and TS	7	bq24081DRCR	BRP
				bq24081DRCT	

(1) The DRC package is available taped and reeled only in quantities of 3,000 devices per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C
DRC(1)	46.87 °C/W	4.95 °C/W	1.5 W	0.021 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2- × 3-via matrix.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			bq24080, bq24081	UNIT
V_I	Input voltage(2)	IN, $\overline{CE}$, ISET, OUT, $\overline{PG}$, STAT1, STAT2, $\overline{TE}$, TS	–0.3 to 7	V
	Output sink/source current	STAT1, STAT2, $\overline{PG}$	15	mA
	Output current	OUT	1.5	A
T_A	Operating free-air temperature range		–40 to 125	°C
T_J	Junction temperature range			°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	6.5	V
T_J	Operating junction temperature range	0	125	°C

ELECTRICAL CHARACTERISTICS

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
$I_{CC(VCC)}$	V_{CC} current	$V_{CC} > V_{CC(min)}$		1.2	2	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT pin, $V_{CC} < V_{(SLP)}$		2	5	μA
$I_{CC(STBY)}$	Standby current	$\overline{CE}$ = High, 0°C ≤ T_J ≤ 85°C			150	μA
$I_{IB(OUT)}$	Input current on OUT pin	Charge DONE, $V_{CC} > V_{CC(MIN)}$		1	5	μA
VOLTAGE REGULATION $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$, $I_{(TERM)} < I_{O(OUT)} \le 1$ A						
$V_{O(REG)}$	Output voltage			4.2		V
	Voltage regulation accuracy	T_A = 25°C	−0.35%		0.35%	
			−1%		1%	
$V_{(DO)}$	Dropout voltage ($V_{(IN)} - V_{(OUT)}$)	$V_{O(OUT)} = V_{O(REG)}$, $I_{O(OUT)}$ = 1 A $V_{O(REG)} + V_{(DO)}) \le V_{CC}$		350	500	mV
CURRENT REGULATION						
$I_{O(OUT)}$	Output current range (1)	$V_{I(OUT)} > V_{(LOWV)}$, $V_{I(IN)} - V_{I(OUT)} > V_{(DO)}$, $V_{CC} \ge 4.5$ V	20		1000	mA
$V_{(SET)}$	Output current set voltage	Voltage on ISET pin, $V_{CC} \ge 4.5$ V, $V_I \ge 4.5$ V, $V_{I(OUT)} > V_{(LOWV)}$, $V_I - V_{I(OUT)} > V_{(DO)}$	2.463	2.5	2.538	V
$K_{(SET)}$	Output current set factor	50 mA ≤ $I_{O(OUT)}$ ≤ 1 A	307	322	337	
		10 mA ≤ $I_{O(OUT)}$ < 50 mA	296	320	346	
		1 mA ≤ $I_{O(OUT)}$ < 10 mA	246	320	416	
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	Voltage on OUT pin	2.8	3	3.2	V
	Deglitch time for fast-charge to precharge transition	$V_{CC(MIN)} \ge 4.5$ V, t_{FALL} = 100 ns, 10-mV overdrive, $V_{I(OUT)}$ decreasing below threshold	250	375	500	ms
$I_{O(PRECHG)}$	Precharge range (2)	0 V < $V_{I(OUT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	2		100	mA
$V_{(PRECHG)}$	Precharge set voltage	Voltage on ISET pin, $V_{O(REG)}$ = 4.2 V, 0 V < $V_{I(OUT)} > V_{(LOWV)}$, $t < t_{(PRECHG)}$	240	255	270	mV
TERMINATION DETECTION						
$I_{(TERM)}$	Charge termination detection range (3)	$V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TRMDET)}$	2		100	mA
$V_{(TERM)}$	Charge termination detection set voltage	Voltage on ISET pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TRMDET)}$	235	250	265	mV
t_{TRMDET}	Deglitch time for termination detection	$V_{CC(MIN)} \ge 4.5$ V, t_{FALL} = 100 ns charging current decreasing below 10-mV overdrive	250	375	500	ms

(1) See Equation 2 in the *Function Description* section.
(2) See Equation 1 in the *Function Description* section.
(3) See Equation 4 in the *Function Description* section.

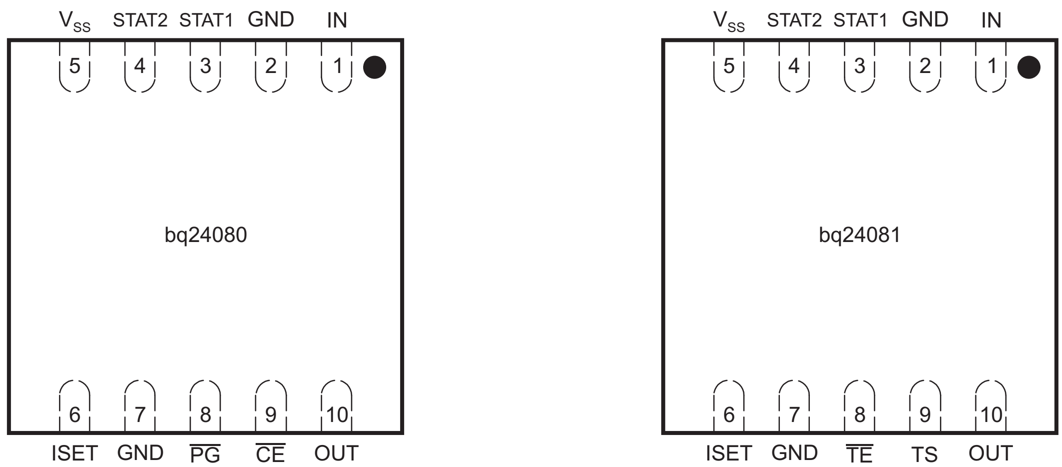
ELECTRICAL CHARACTERISTICS (continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold		$V_{O(REG)}$ – 0.115	$V_{O(REG)}$ − 0.10	$V_{O(REG)}$ − 0.085	V
$t_{(DEGL)}$	Deglitch time for recharge detect	$V_{CC(MIN)}$ ≥ 4.5 V, t_{FALL} = 100 ns decreasing below or increasing above threshold, 10-mV overdrive	250	375	500	ms
STAT1, STAT2, and $\overline{PG}$ OUTPUTS						
V_{OL}	Low-level output saturation voltage	I_O = 5 mA			0.25	V
$\overline{CE}$ and $\overline{TE}$ INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current		–1			μA
I_{IH}	High-level input current				1	μA
TIMERS						
$t_{(PRECHG)}$	Precharge time		1,584	1,800	2,016	s
$t_{(CHG)}$	Charge time		22,176	25,200	28,224	s
$I_{(FAULT)}$	Timer fault recovery current			200		μA
SLEEP COMPARATOR						
$V_{(SLP)}$	Sleep-mode entry threshold voltage	2.3 V ≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$			V_{CC} ≤ $V_{I(OUT)}$ + 80 mV	V
$V_{(SLPEXIT)}$	Sleep-mode exit threshold voltage	2.3 V ≤ $V_{I(OUT)}$ ≤ $V_{O(REG)}$	V_{CC} ≥ $V_{I(OUT)}$ + 190			V
	Sleep-mode entry deglitch time	$V_{(IN)}$ decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive	250	375	500	ms
THERMAL SHUTDOWN THRESHOLDS						
$T_{(SHTDWN)}$	Thermal trip threshold	T_J increasing		165		°C
	Thermal hysteresis	T_J increasing		15		°C
UNDERVOLTAGE LOCKOUT						
UVLO	Undervoltage lockout	Decreasing V_{CC}	2.4	2.5	2.6	V
	Hysteresis			27		mV
TEMPERATURE SENSE COMPARATOR (bq24081)						
$V_{(TS1)}$	High-voltage threshold		2.475	2.5	2.525	V
$V_{(TS2)}$	Low-voltage threshold		0.485	0.5	0.515	V
$I_{(TS)}$	TS pin current source		96	102	108	μA
$t_{(DEGL)}$	Deglitch time for temperature fault		250	375	500	ms

PIN ASSIGNMENT

DRC PACKAGE
(TOP VIEW)



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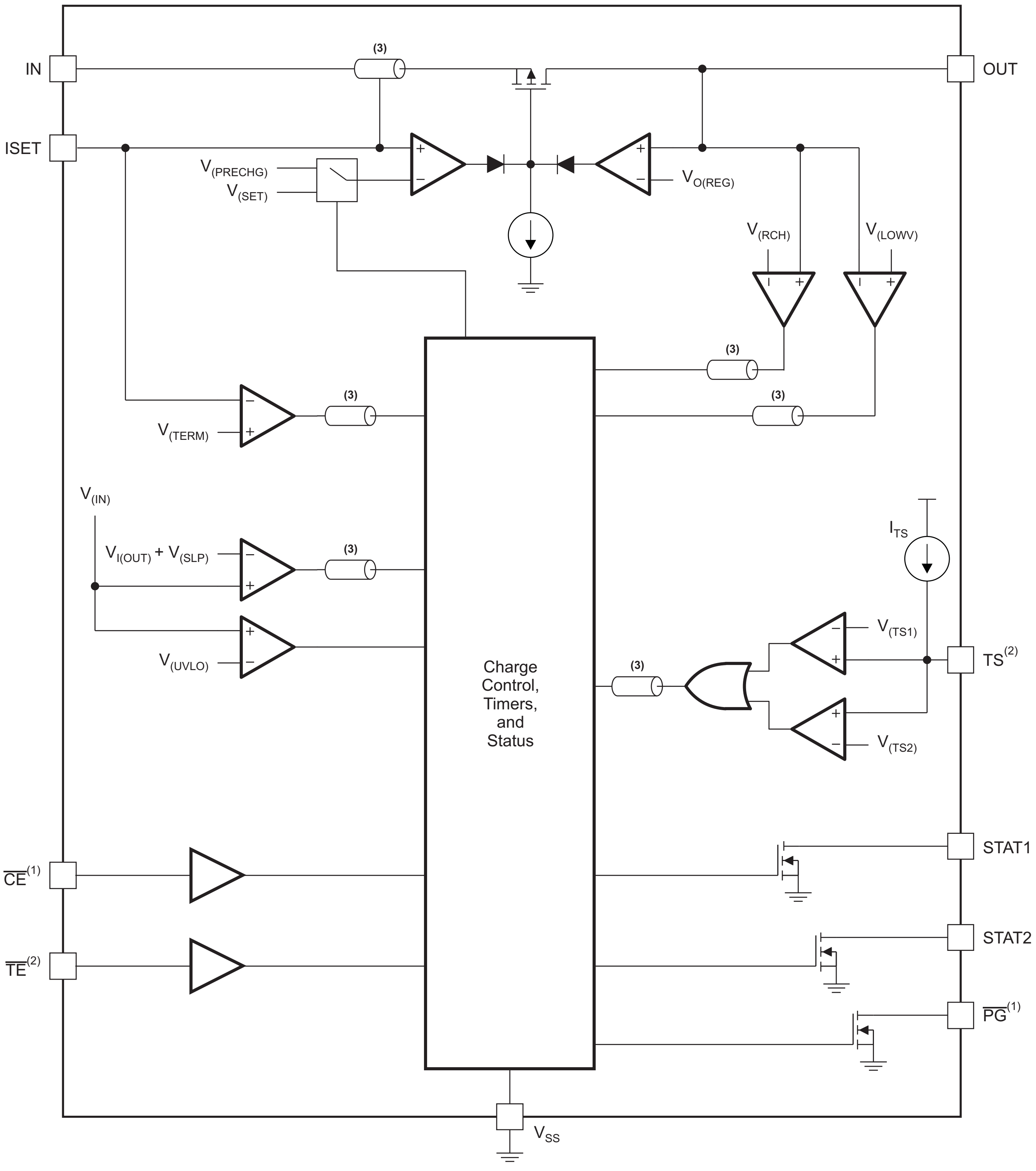
PIN FUNCTIONS

PIN			I/O	DESCRIPTION
NAME	NO.			
	bq24080	bq24081		
$\overline{CE}$	9	–	I	Charge enable input (active-low)
GND	2, 7	2, 7	–	Ground
IN	1	1	I	Adapter dc voltage. Connect minimum 0.1-μF capacitor to V_{SS}.
ISET	6	6	I	Charge current. External resistor to V_{SS} sets precharge and fast-charge current, and also the termination current value. Can be used to monitor the charge current.
OUT	10	10	O	Charge current output. Connect minimum 0.1-μF capacitor to V_{SS}.
$\overline{PG}$	8	–	O	Power-good status output (open-drain)
STAT1	3	3	O	Charge status outputs (open-drain)
STAT2	4	4	O	
$\overline{TE}$	–	8	I	Timer-enable input (active-low)
TS	–	9	I/O	Temperature sense; connect to NTC in battery pack.
V_{SS}	5	5	–	Ground
Thermal pad	–	–	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The exposed thermal pad must be connected to the same potential as the V_{SS} pin on the printed-circuit board. ***Do not use the thermal pad as the primary ground input for the device***. The V_{SS} pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



(1) bq24080 only

(2) bq24081 only

(3) Signal deglitched

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

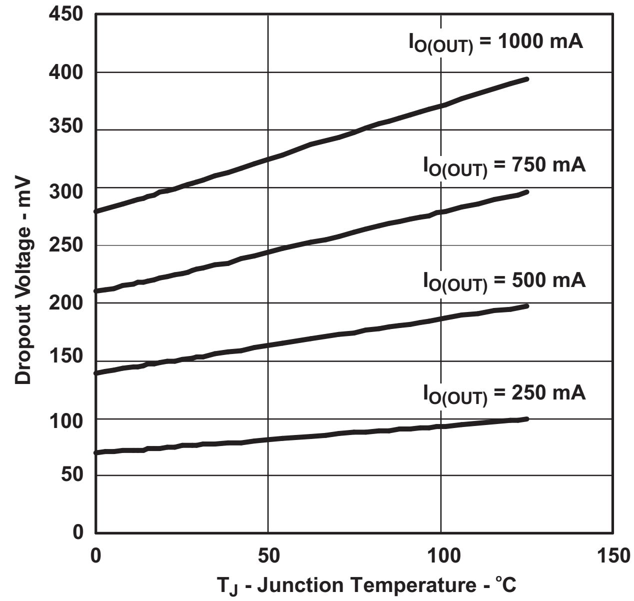


Figure 1.

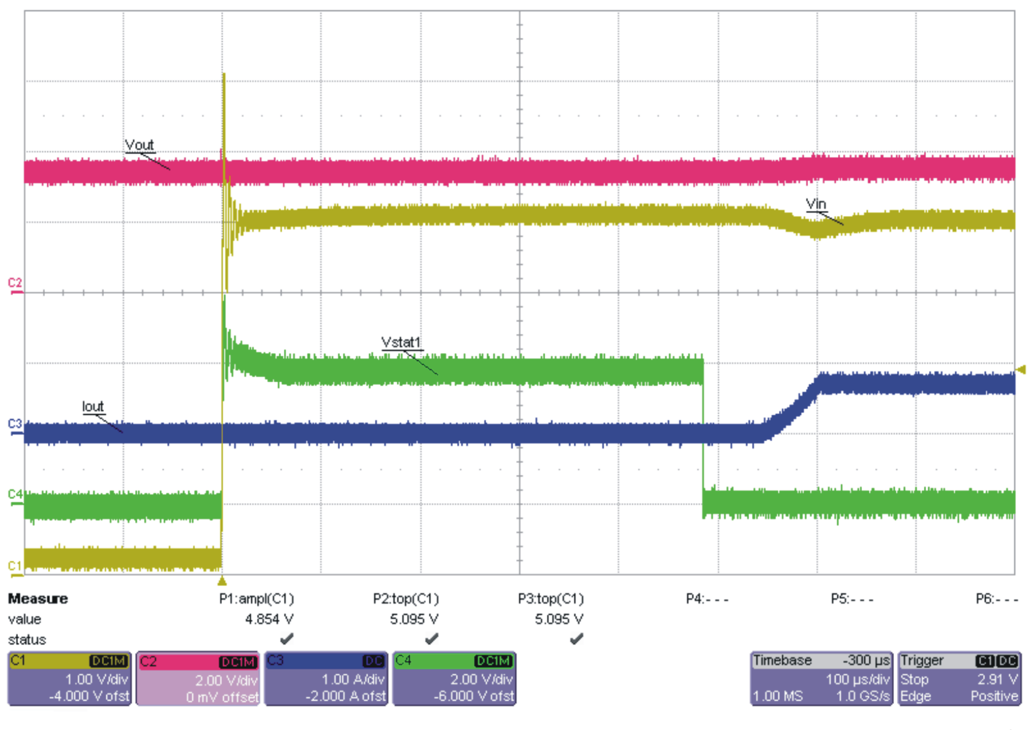


Figure 2. V_{IN} Hot-Plug Power-Up Sequence

TYPICAL CHARACTERISTICS (continued)

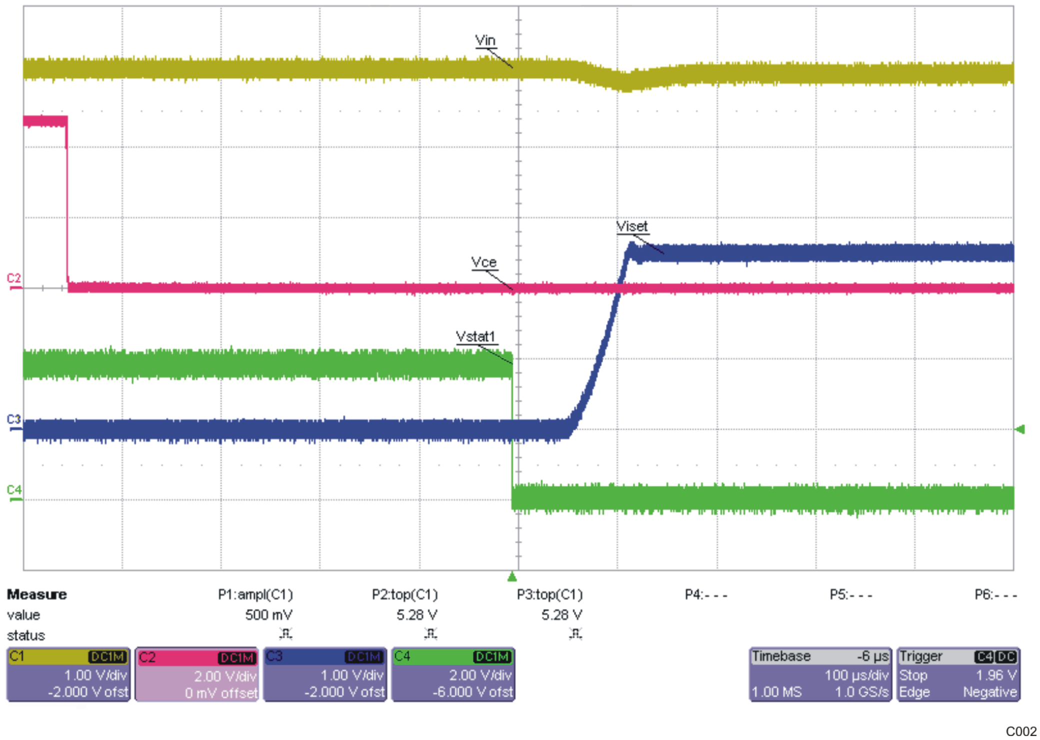


Figure 3. Charge Enable Power-Up Sequence ($\overline{CE}$ = High-to-Low)

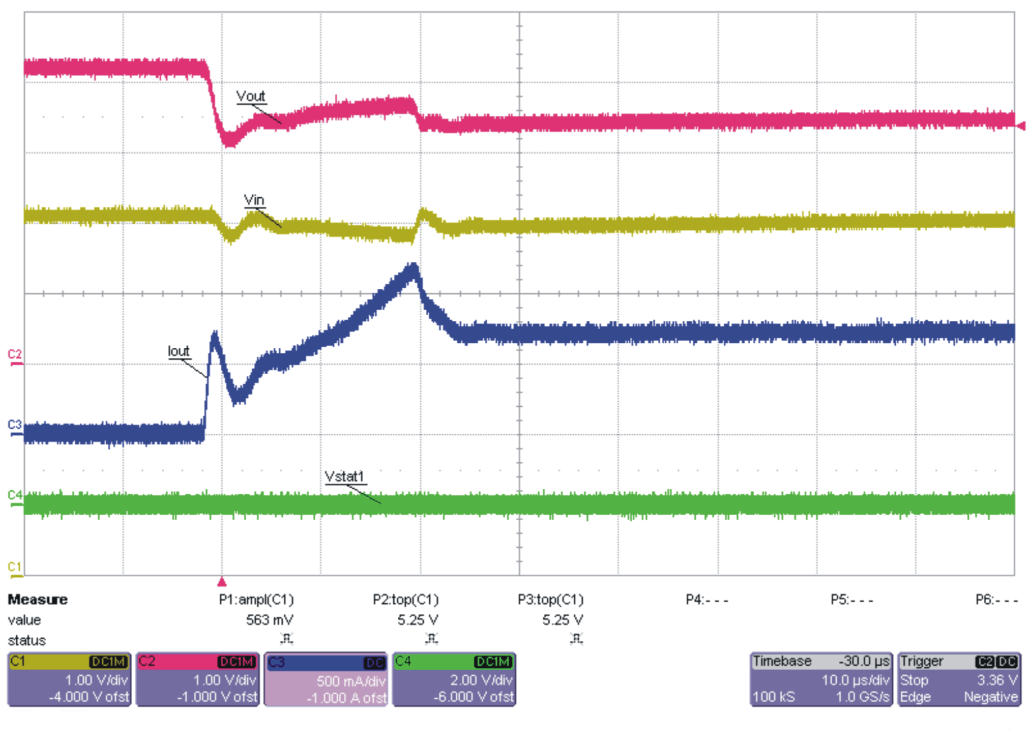
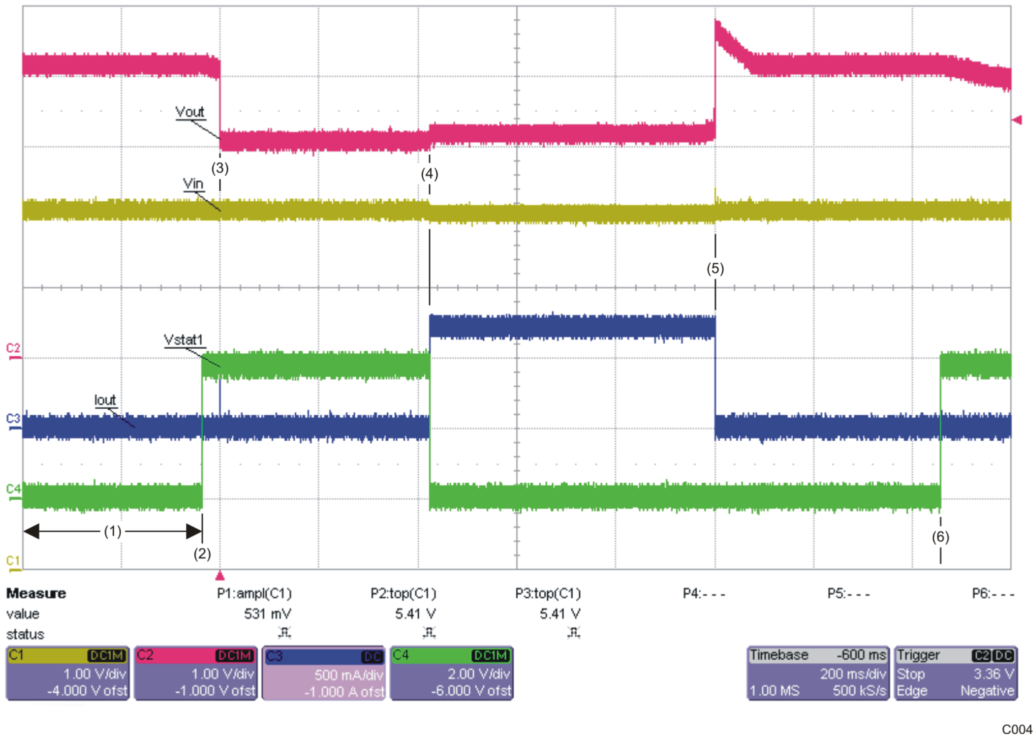


Figure 4. Battery Hot-Plug During Charging Phase

TYPICAL CHARACTERISTICS (continued)



(6) Deglitch timer expires – *charge done* is declared.

Figure 5. Battery Hot-Plug and Removal Power Sequence

FUNCTIONAL DESCRIPTION

The device supports a precision Li-Ion, Li-Pol charging system suitable for single cells. Figure 6 shows a typical charge profile, and Figure 7 shows an operational flow chart.

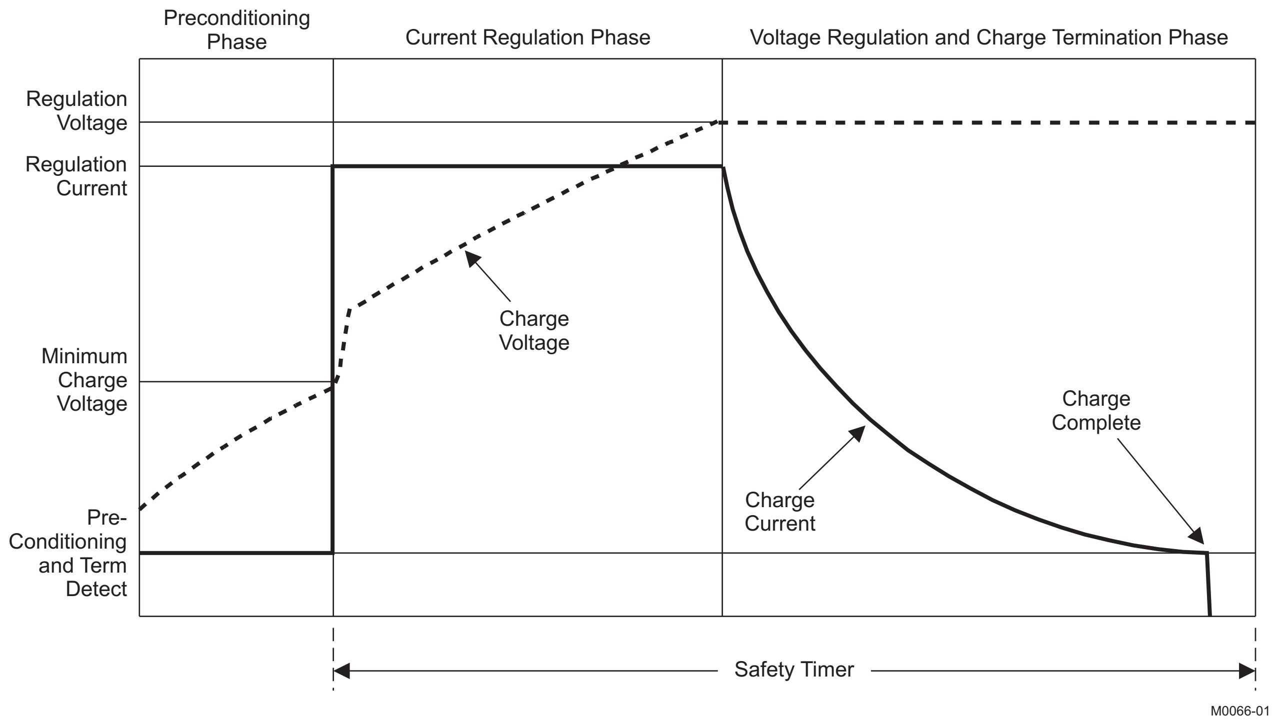


Figure 6. Typical Charging Profile

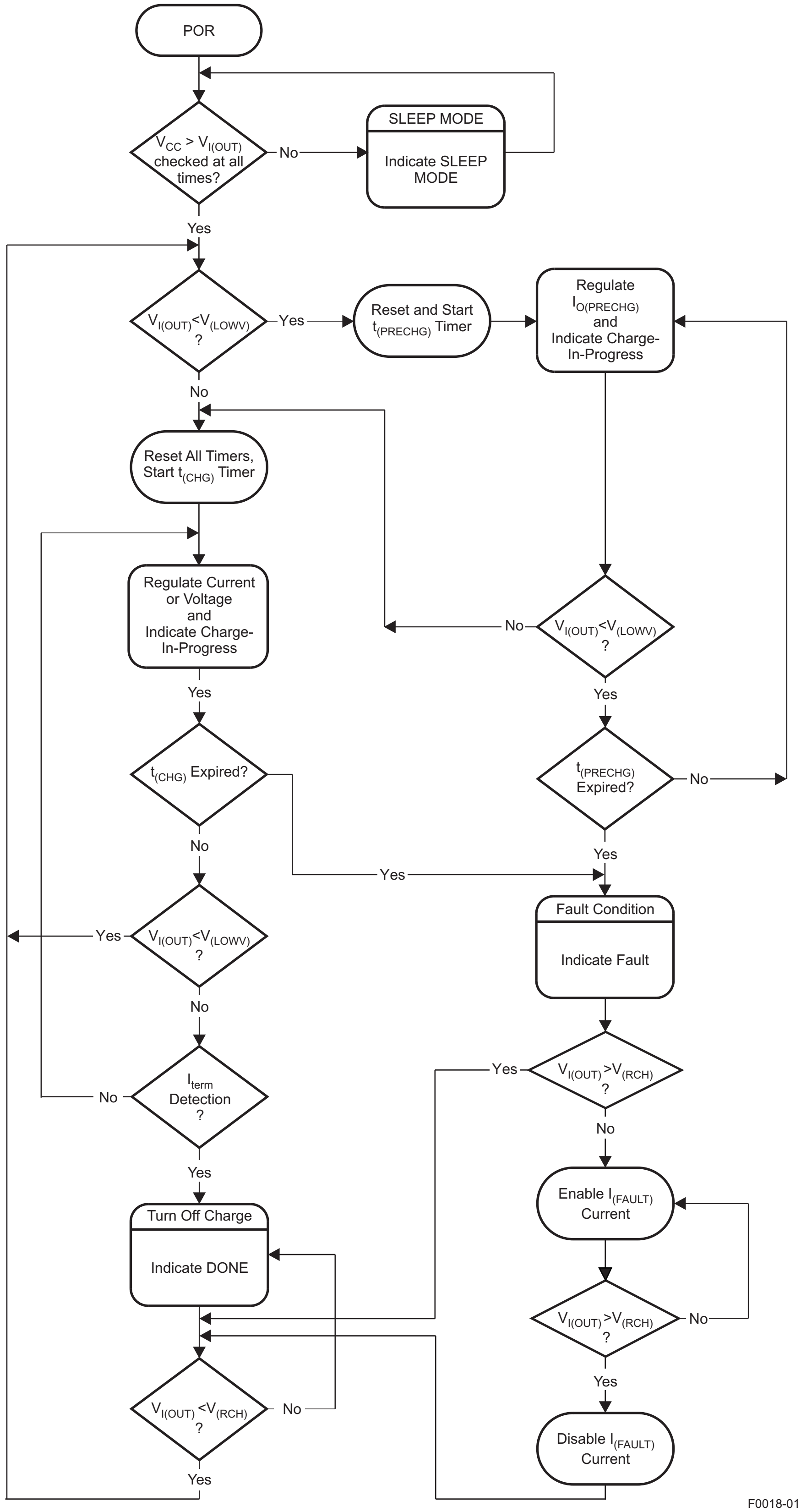


Figure 7. Operational Flow Chart

Battery Preconditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the device applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. Resistor R_{SET}, connected between the ISET and V_{SS}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the *Electrical Characteristics* table.

$$I_{O(PRECHG)} = \frac{K_{(SET)} \times V_{(PRECHG)}}{R_{SET}} \quad (1)$$

The device activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If the $V_{(LOWV)}$ threshold is not reached within the timer period, the device turns off the charger and enunciates FAULT on the STATx pins. See the *Timer Fault Recovery* section for additional details.

Battery Fast-Charge Constant Current

The device offers on-chip current regulation with programmable set point. Resistor R_{SET}, connected between the ISET and V_{SS}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}} \quad (2)$$

Charge-Current Monitor

When the charge function is enabled internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor R_{ISET} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V(ISET) = I(OUT) \times \frac{R_{ISET}}{K_{(SET)}} \quad (3)$$

Battery Fast-Charge Voltage Regulation

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The device monitors the battery-pack voltage between the OUT and V_{SS} pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the device also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the charger is turned off and FAULT is set on the STATx pins. See the *Timer Fault and Recovery* section for additional details.

Charge Termination Detection and Recharge

The device monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, charge is terminated. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(TERM)} = \frac{K_{(SET)} \times V_{(TERM)}}{R_{SET}} \quad (4)$$

After charge termination, the device restarts the charge once the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

The device monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected, the charge is terminated immediately.

Resistor R_{SET}, connected between the ISET and V_{SS}, determines the current level at the termination threshold.

Sleep Mode

The device enters the low-power sleep mode if the input power (IN) is removed from the circuit. This feature prevents draining the battery during the absence of input supply.

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that *OFF* indicates the open-drain transistor is turned off.

Table 1. Status Pin Summary

CHANGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature)	OFF	OFF
Timer fault		
Sleep mode		

$\overline{\text{PG}}$ Output (bq24080)

The open-drain power-good ($\overline{\text{PG}}$) output pulls low when a valid input voltage is present. This output is turned off (high-impedance) in sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

Charge-Enabled ($\overline{\text{CE}}$) Input (bq24080)

The $\overline{\text{CE}}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions.

Timer Enabled ($\overline{\text{TE}}$) Input (bq24081)

The $\overline{\text{TE}}$ digital input is used to disable or enable the fast-charge timer. A low-level signal on this pin enables the fast-charge timer, and a high-level signal disables this feature.

TEMPERATURE QUALIFICATION (bq24081)

The bq24081 continuously monitors battery temperature by measuring the voltage between the TS and V_{SS} pins. An internal current source provides the bias for common 10-kΩ negative-temperature-coefficient thermistors (NTC) (see the functional block diagram). The device compares the voltage on the TS pin with the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed. If a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected, the device immediately suspends the charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns within the normal range.

The allowed temperature range with a 103AT-type thermistor is 0°C to 45°C. However, the user may modify these thresholds by adding external resistors (see Figure 8 and Figure 9

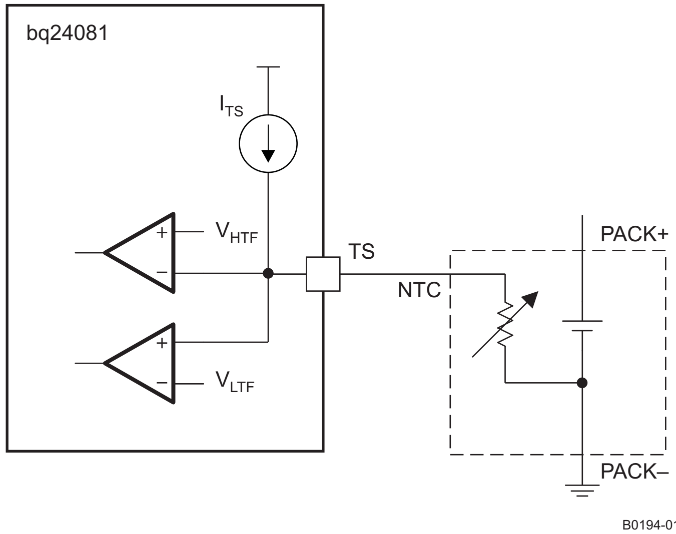


Figure 8. Default Temperature Thresholds

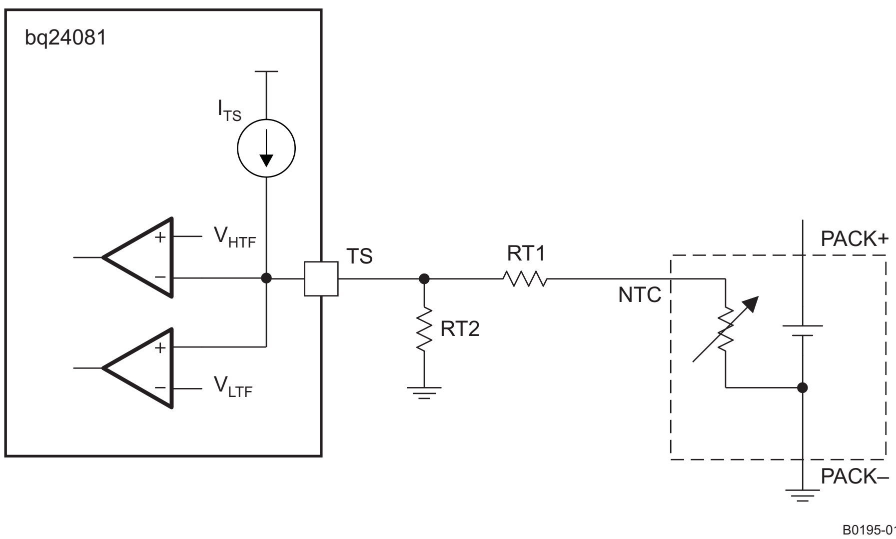


Figure 9. Temperature Thresholds Modified by External Resistors

Timer Fault and Recovery

As shown in Figure 7, the device provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition Number 1

OUT pin voltage is above the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs.

Recovery method: the device waits for the OUT pin voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the OUT pin voltage falls below the recharge threshold, the device clears the fault and starts a new charge cycle. A POR, $\overline{TE}$, or $\overline{CE}$ toggle also clears the fault.

Condition number 2

OUT pin voltage is below the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: Under this scenario, the device applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the OUT pin voltage goes above the recharge threshold, then the device disables the $I_{(FAULT)}$ current and executes the recovery method described for condition number 1. Once the OUT pin voltage falls below the recharge threshold, the bq24080 clears the fault and starts a new charge cycle. A POR, $\overline{TE}$, or $\overline{CE}$ toggle also clears the fault.

APPLICATION INFORMATION

bq24080/1 CHARGER DESIGN EXAMPLE

Requirements

- Supply voltage = 5 V
- Fast-charge current of approximately 750 mA
- Battery-Temperature sense (bq24081): default setting = –2°C to 44.5°C

Calculations

Program the charge current for 750 mA:

$R_{ISET} = [V_{(SET)} \times K_{(SET)} / I_{(OUT)}]$

From electrical characteristics table, $V_{(SET)}$ = 2.5 V.

From electrical characteristics table, $K_{(SET)}$ = 322.

R_{ISET} = [2.5 V × 322 / 0.75 A] = 1.073 kΩ

Selecting the closest standard value, use a 1.07-kΩ resistor connected between ISET (pin 6) and ground.

Battery Temperature Sense (bq24081):

Use a Semitec 103AT-4 NTC thermistor connected between TS (pin 9) and ground.

$R_{THERM\text{-}cold} = [V_{(TS1)} / I_{(TS)}]$ = 2.5V / 100 µA = 25 kΩ

$R_{THERM\text{-}hot} = [V_{(TS2)} / I_{(TS)}]$ = 0.5V / 100 µA = 5 kΩ

Look up the corresponding temperature value in the manufacturer's resistance-temperature table for the thermistor selected. For a 103AT-4 Semitec thermistor:

5 kΩ = 44.5°C

25 kΩ = 2°C

STAT Pins (All Devices) and PG Pin (bq24080):

Status pins Monitored by Processor:

Select a pullup resistor that can source more than the input bias (leakage) current of both the processor and status pins and still provide a logic high. $R_{PULLUP} \leq [V_{(cc\text{-}pullup)} - V_{(logic\ hi\text{-}min)} / (I_{(\mu P\text{-}monitor)} + I_{(STAT\text{-}OpenDrain)})]$ = (3.3 V – 1.9 V) / (1 µA + 1 µA) ≤ 700 kΩ; Connect a 100-kΩ pullup between each status pin and the V_{CC} of the processor. Connect each status pin to a µP monitor pin.

Status viewed by LED:

Select an LED with a current rating less than 10 mA and select a resistor to place in series with the LED to limit the current to the desired current value (brightness). $R_{LED} = [(V_{(IN)} - V_{(LED\text{-}on)}) / I_{(LED)}]$ = (5 V – 2 V) / 1.5 mA = 2 kΩ. Place an LED and resistor in series between the input and each status pin.

Selecting Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. A 0.1-µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works well. In some applications, it may be necessary to protect against a hot plug input voltage overshoot. This is done in three ways:

1. The best way is to add an input zener, 6.2 V, between the IN pin and V_{SS}.
2. A low-power zener is adequate for the single event transient. Increasing the input capacitance lowers the characteristic impedance which makes the input resistance move effective at damping the overshoot, but risks damaging the input contacts by the high inrush current.
3. Placing a resistor in series with the input dampens the overshoot, but causes excess power dissipation.

The device only requires a small capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the OUT and GND pad is typically sufficient.

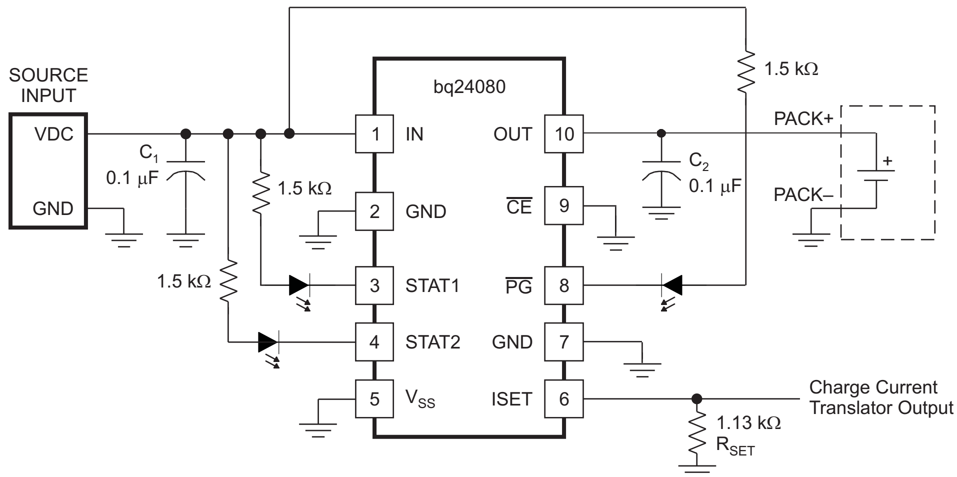


Figure 10. Typical Application Circuit

Thermal Considerations

The bq24080 and bq24081 are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed-circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number SLUA271).

The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for $R_{\theta JA}$ is:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \quad (5)$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of $R_{\theta JA}$ include:

- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested
- Use multiple 10–13 mil vias in the PowerPAD™ to copper ground plane.
- Avoid cutting the ground plane with a signal trace near the power IC.
- The PCB must be sized to have adequate surface area for heat dissipation.
- FR4 (figerglass) thickness should be minimized.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal Power FET. It can be calculated from the following equation:

$$P = (V_{(IN)} - V_{(OUT)}) \times I_{O(OUT)} \quad (6)$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 6.

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to $V_{(IN)}$ and the output filter capacitors from OUT to V_{SS} should be placed as close as possible to the device, with short trace runs to both signal and V_{SS} pins. The V_{SS} pin should have short trace runs to the GND pin.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small-signal ground path and the power ground path.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The device is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24080DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24080DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24080DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24080DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24081DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24081DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24081DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24081DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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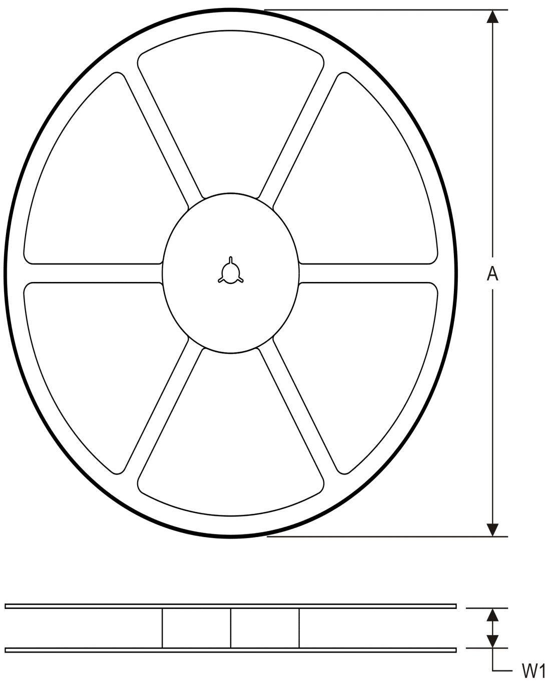
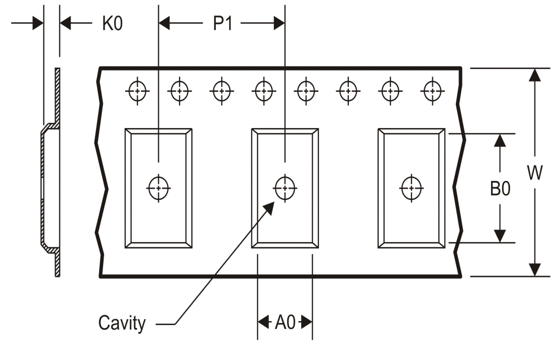
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



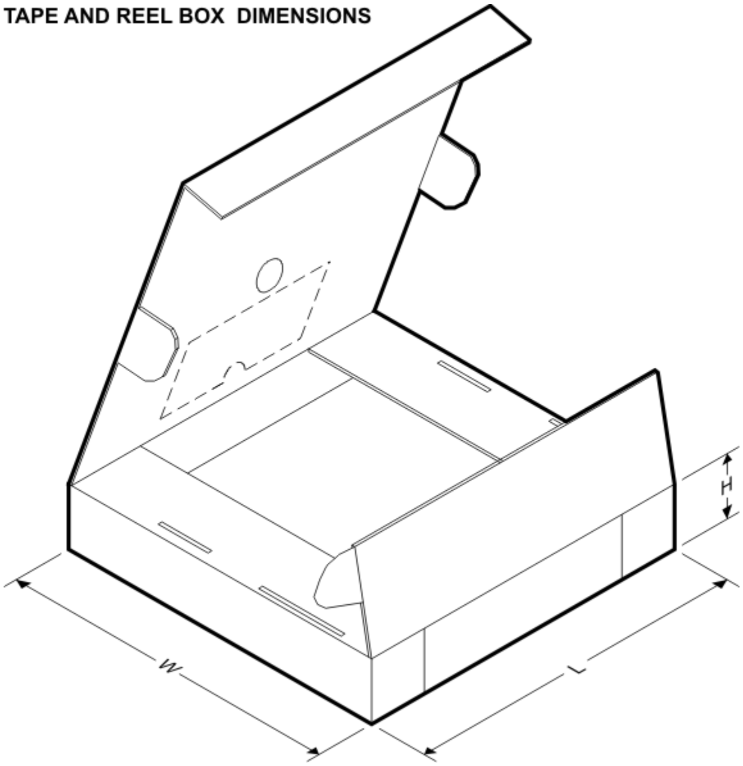
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24080DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
BQ24080DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24080DRCT	SON	DRC	10	250	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
BQ24080DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24081DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24081DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

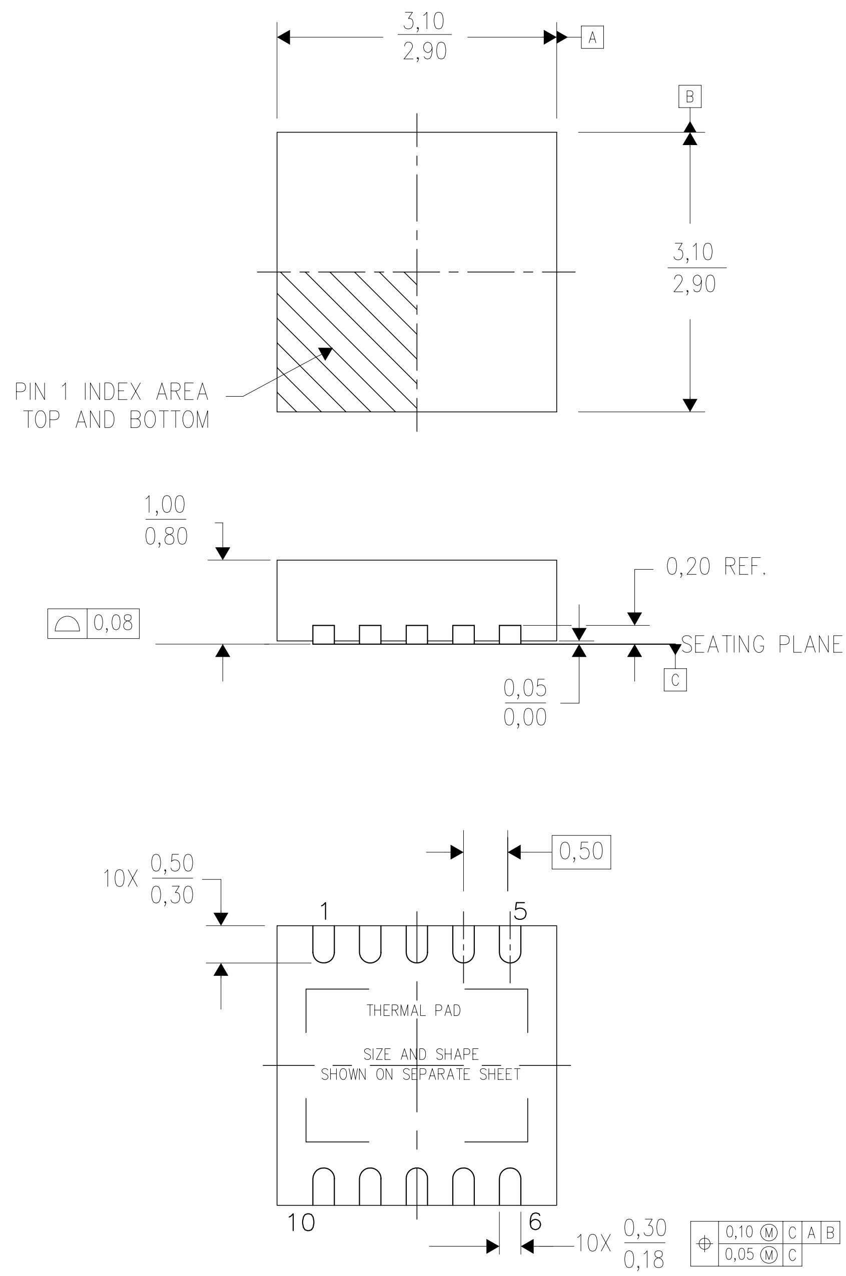
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24080DRCR	SON	DRC	10	3000	370.0	355.0	55.0
BQ24080DRCR	SON	DRC	10	3000	367.0	367.0	35.0
BQ24080DRCT	SON	DRC	10	250	195.0	200.0	45.0
BQ24080DRCT	SON	DRC	10	250	210.0	185.0	35.0
BQ24081DRCR	SON	DRC	10	3000	367.0	367.0	35.0
BQ24081DRCT	SON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

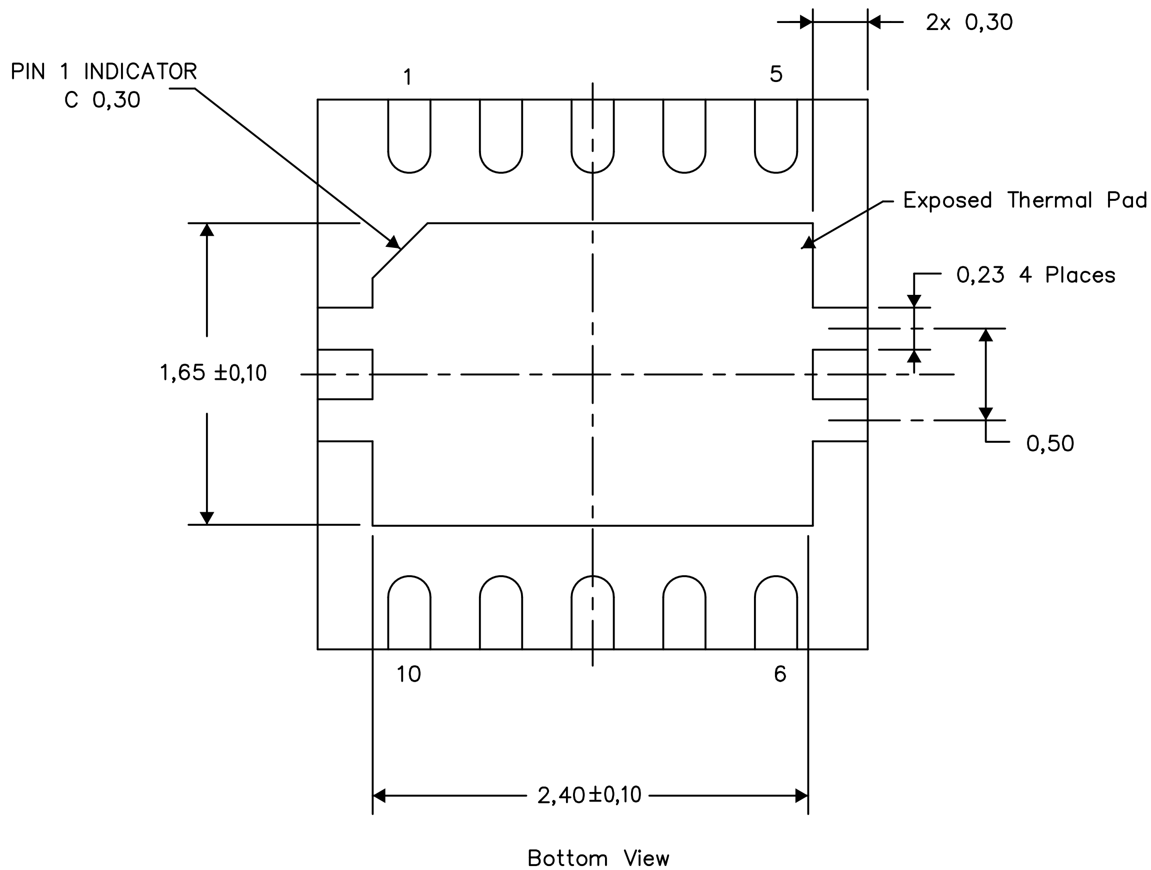
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

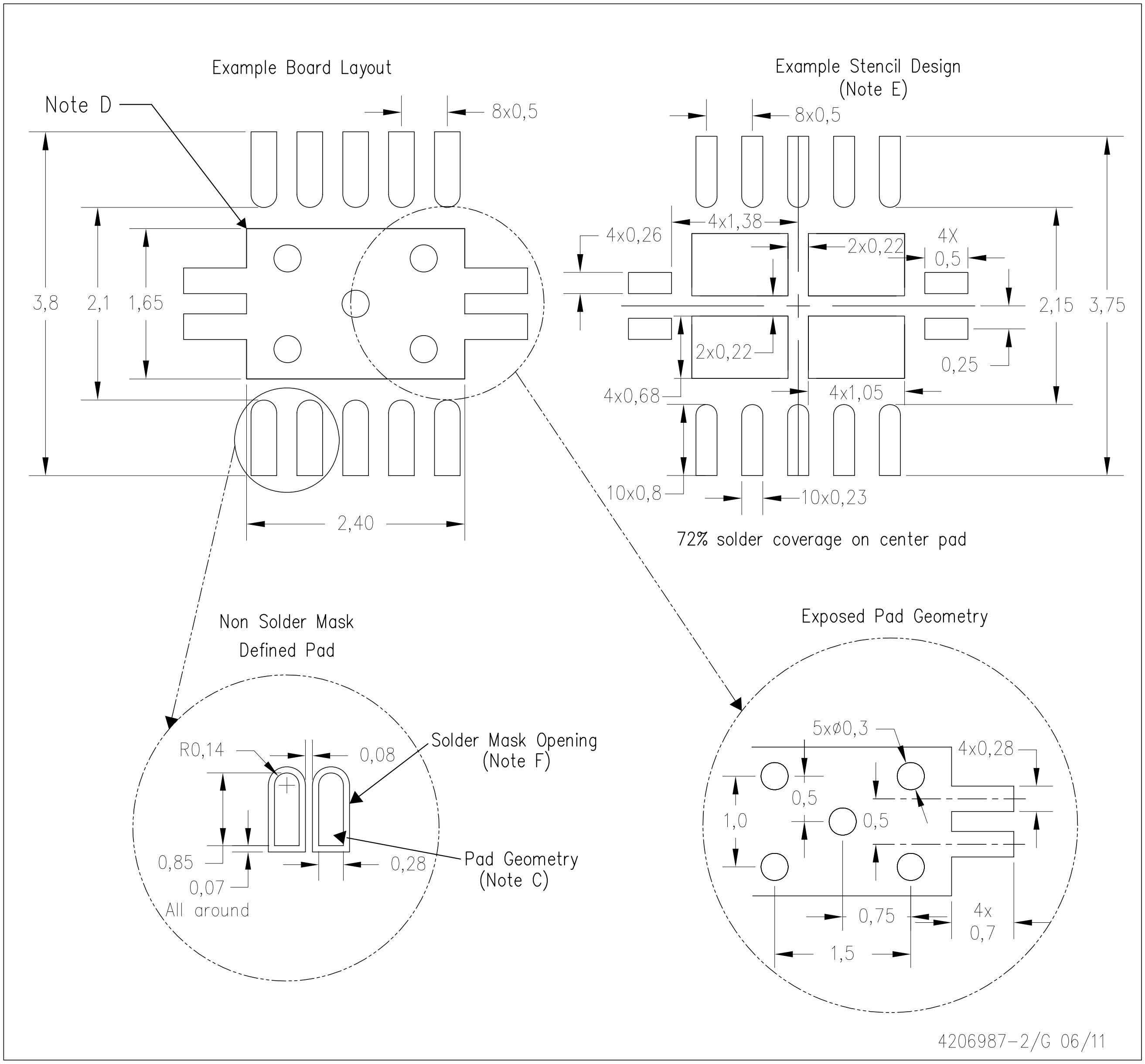


Exposed Thermal Pad Dimensions

4206565–3/N 07/12

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.