HIGH POWER WHITE LED DRIVER
2-MHz SYNCHRONOUS BOOST CONVERTER WITH STANDARD LOGIC INTERFACE

FEATURES

- Four Operational Modes
  - Torch and Flash up to I_{LED} = 700 mA
  - Voltage-Regulated Boost Converter: 5.0 V
  - Shutdown: 0.3 μA (typ)
- Total Solution Circuit Area < 25 mm^2
- Up to 96% Efficiency
- Integrated LED Turn-On Safety Timer
- Zero Latency TX-Masking Input
- Integrated Low Light Dimming Mode
- LED Disconnect During Shutdown
- Open/Shorted LED Protection
- Over-Temperature Protection
- Available in a 12-Pin NanoFree™ (CSP) and 10-Pin QFN Packaging

APPLICATIONS

- Camera White LED Torch/Flash for Cell Phones, Smart-Phones and PDAs
- General Lighting Applications
- Audio Amplifier Power Supply

DESCRIPTION

The TPS6105x device uses a high-frequency synchronous-boost topology with constant current sink to drive single white LEDs. The device uses an inductive fixed-frequency PWM control scheme using small external components, minimizing input ripple current.

The 2-MHz switching frequency allows the use of small and low-profile 2.2-μH inductors. To optimize overall efficiency, the device operates with only a 250-mV LED feedback voltage.

The TPS6105x device not only operates as a regulated current source, but also as a standard voltage-boost regulator. This additional operating mode can be useful to supply other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

The LED current or the desired output voltage can be programmed via two logic signals (MODE0/1). To simplify flash synchronization with the camera module, the device offers a trigger pin (FLASH_SYNC) for fast LED turn-on time.

When the TPS6105x is not in use, it can be put into shutdown mode, reducing the input current to 0.3 μA (typ). During shutdown, the LED pin is high impedance to avoid leakage current through the LED.

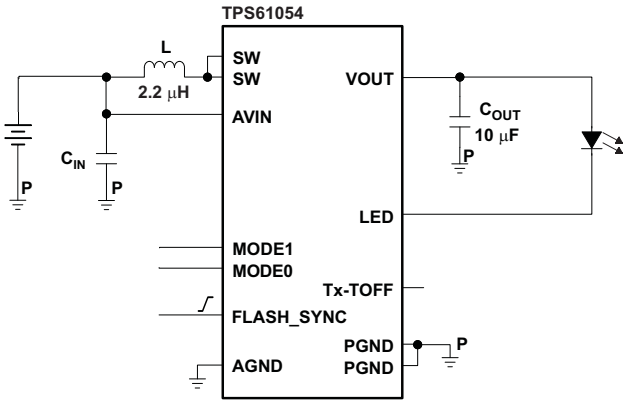

Figure 1. Typical Application

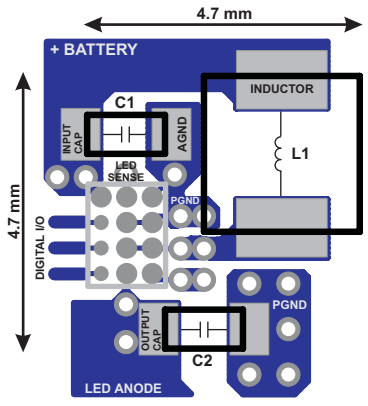

Figure 2. Typical PC-Board Layout

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PART NUMBER(1)(2)	TORCH CURRENT(3)	FLASH CURRENT(3)	SAFETY TIMER MAXIMUM DURATION	CURRENT LIMIT	PACKAGE MARKING	PACKAGE
TPS61054DRC	75 mA	700 mA	820 ms	1500 mA (ILIM = 01)	BRX	QFN-10
TPS61055DRC	75 mA	500 mA	820 ms	1000 mA (ILIM = 00)	BRY	QFN-10

(1) All devices are specified for operation in the commercial temperature range, –40°C to 85°C.
(2) The YZG package is available in tape and reel. Add R suffix (TPS6105xYZGR, TPS6105xDRCR) to order quantities of 3000 parts. Add T suffix (TPS6105xYZGT, TPS6105xDRCT) to order quantities of 250 parts.
(3) For customized current settings, please contact the factory.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		TPS6105X	UNIT
	Voltage range on AVIN, VOUT, SW, LED (2)	–0.3 to 7	V
	Voltage range on MODE0, MODE1, FLASH_SYNC, Tx-TOFF (2)	–0.3 to 7	V
T_A	Operating ambient temperature range (3)	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	150	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD rating(4)	Human body model	2	kV
	Charge device model	1	kV
	Machine model	200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.
(4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE(1) (2)		POWER RATING T_A = 25°C	DERATING FACTOR ABOVE(1) (2) T_A = 25°C
YZG	θ_{JA} = 89°C/W	θ_{JB} = 35°C/W	1.1 W	12 mW/°C
DRC	θ_{JA} = 49°C/W	θ_{JC} = 3.2°C/W	2.4 W	20 mW/°C

(1) Measured with high-K board.
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/ \theta_{JA}$.

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temp. of –40°C ≤ T_J ≤ 125°C. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6.0	V
	Minimum input voltage for start-up	MODE0 = 1, MODE1 = 1, R_L = 10 Ω			2.5	V
I_Q	Operating quiescent current into AVIN	MODE0 = 1, MODE1 = 1		8.5		mA
I_{SD}	Shutdown current into AVIN	MODE0 = 0, MODE1 = 0, –40°C ≤ T_J ≤ 85°C		0.3	3.0	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage range	Current regulator mode	V_{IN}		5.5	V
		Voltage regulator mode		5.0		
OVP	OVP Output overvoltage protection	V_{OUT} rising	5.7	6.0	6.25	V
	Output overvoltage protection hysterisis			0.15		V
D	Minimum duty cycle			7.5%		
	LED current accuracy(1)	0.25 V ≤ V_{LED} ≤ 2.0 V, I_{LED} = I_{TORCH}, T_J = 50°C	–15%		15%	
		0.25 V ≤ V_{LED} ≤ 2.0 V, I_{LED} = I_{FLASH}, T_J = 50°C	–12%		12%	
	LED current temperature coefficient			0.08		%/°C
	DC output voltage accuracy	2.5 V ≤ V_{IN} ≤ 0.9 V_{OUT}, PWM operation	–3%		3%	
V_{LED}	LED sense voltage	Boost Mode		250		mV
	LED input leakage current	V_{LED} = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET on-resistance	V_{OUT} = V_{GS} = 3.6 V		80		mΩ
	Rectifier MOSFET on-resistance			80		
$I_{lkg(SW)}$	Switch MOSFET leakage	V_{DS} = 6.0 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
	Rectifier MOSFET leakage			0.1	1	
I_{lim}	Switch current limit	2.5 V ≤ V_{IN} ≤ 6.0 V, ILIM = 00	850	1000	1150	mA
		2.5 V ≤ V_{IN} ≤ 6.0 V, ILIM = 01 (1)	1275	1500	1725	
	Thermal shutdown (1)		140	160		°C
	Thermal shutdown hysteresis (1)			20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency		1.8	2.0	2.2	MHz
MODE0, MODE1, Tx-TOFF, FLASH_SYNC						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$I_{(LKG)}$	Logic input leakage current	Input connected to V_{IN} or GND, –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
	Tx-TOFF pull-down resistance	Tx-TOFF ≤ 0.4 V		400		kΩ
	FLASH_SYNC pull-down resistance	FLASH_SYNC ≤ 0.4 V		400		kΩ
TIMING						
	Start-up time	From shutdown into flash mode I_{LED} = 700 mA		1.2		ms
		From shutdown into voltage mode MODE0 = 1, MODE1 = 1, I_{OUT} = 0 mA		650		µs
	LED current settling time(2) triggered by rising edge on FLASH_SYNC	MODE0 = 0, MODE1 = 1, I_{LED} = from 75mA to 700 mA		160		µs
	LED current settling time(2) triggered by rising edge on Tx-TOFF	MODE0 = 0, MODE1 = 1, I_{LED} = 700 mA to 75 mA		20		µs

(1) Assured by design. Not tested in production.
(2) Settling time to ±15% of the target value

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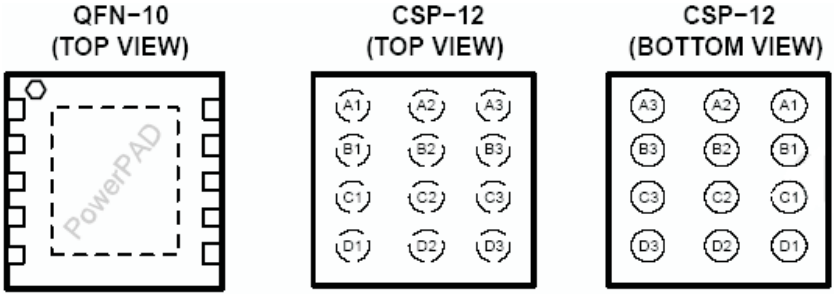
DEVICE INFORMATION

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO. (QFN)	NO. (CSP)		
AVIN	5	D3	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
VOUT	9	A2	O	Boost converter output.
LED	6	D2	I	LED return input. This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. The regulation operates with typically 250 mV dropout voltage. Connect to the cathode of the LED.
FLASH_SYNC	10	A1	I	Flash strobe pulse synchronization input. FLASH_SYNC = LOW (GND): The device is operating and regulating the LED current to the torch current level (TC). FLASH_SYNC = HIGH (VIN): The device is operating and regulating the LED current to the flash current level (FC).
MODE0 MODE1	2 1	B3 A3	I I	Mode selection inputs. These pins must not be left floating and must be terminated. MODE0 = 0, MODE1 = 0: Device in shutdown mode MODE0 = 1, MODE1 = 0: Device in torch only mode MODE0 = 0, MODE1 = 1: Device in torch and flash mode MODE0 = 1, MODE1 = 1: Device in constant voltage regulation mode
Tx-TOFF	3	C3	I	RF PA synchronization input. Tx-TOFF = LOW : The device is operating normally. Tx-TOFF = HIGH : The device is forced into torch mode.
SW	8	B1, B2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
PGND	7	C1, C2		Power ground. Connect to AGND underneath IC.
AGND	4	D1		Analog ground.
PowerPAD™		N/A		Internally connected to PGND.

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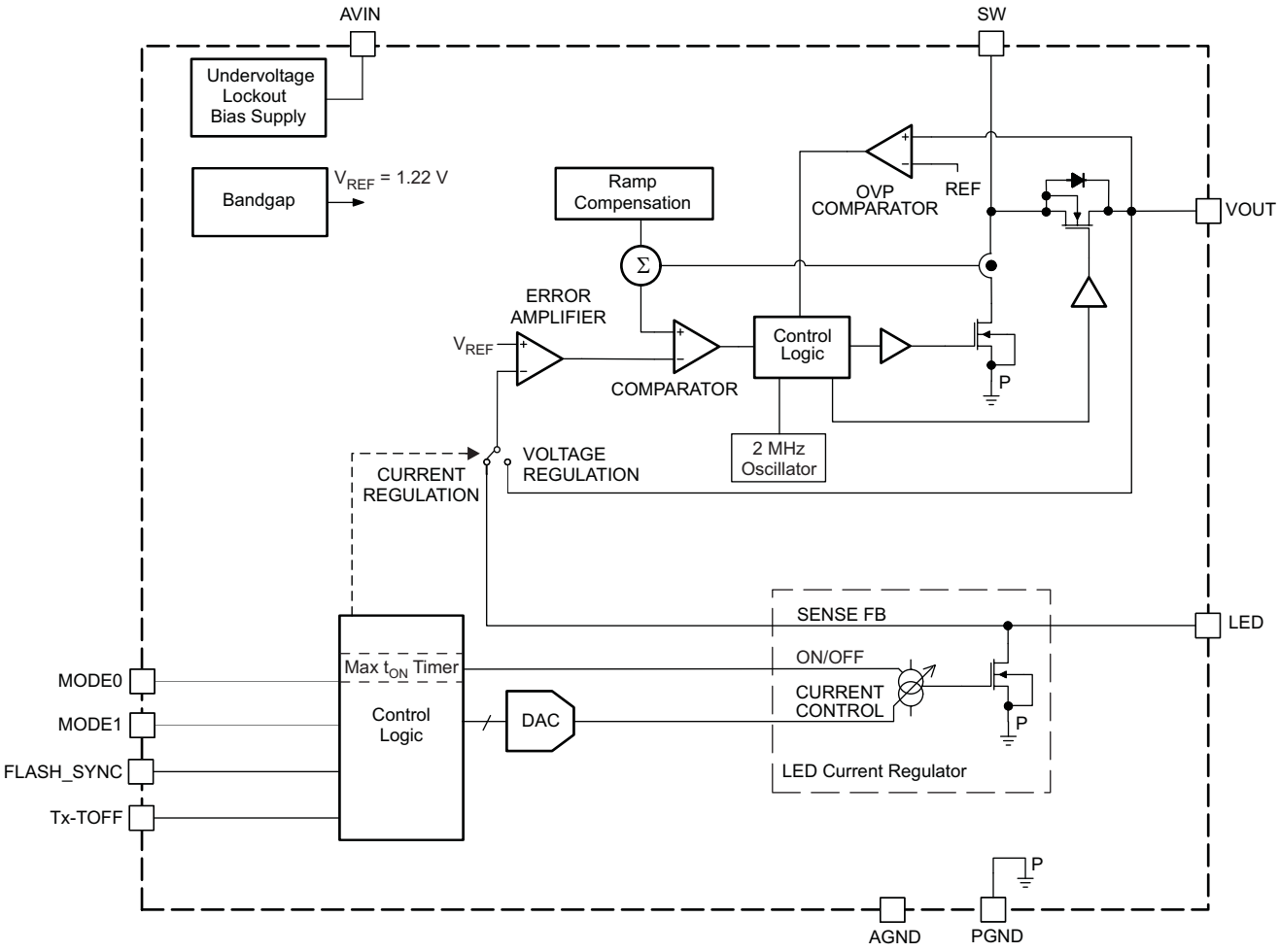
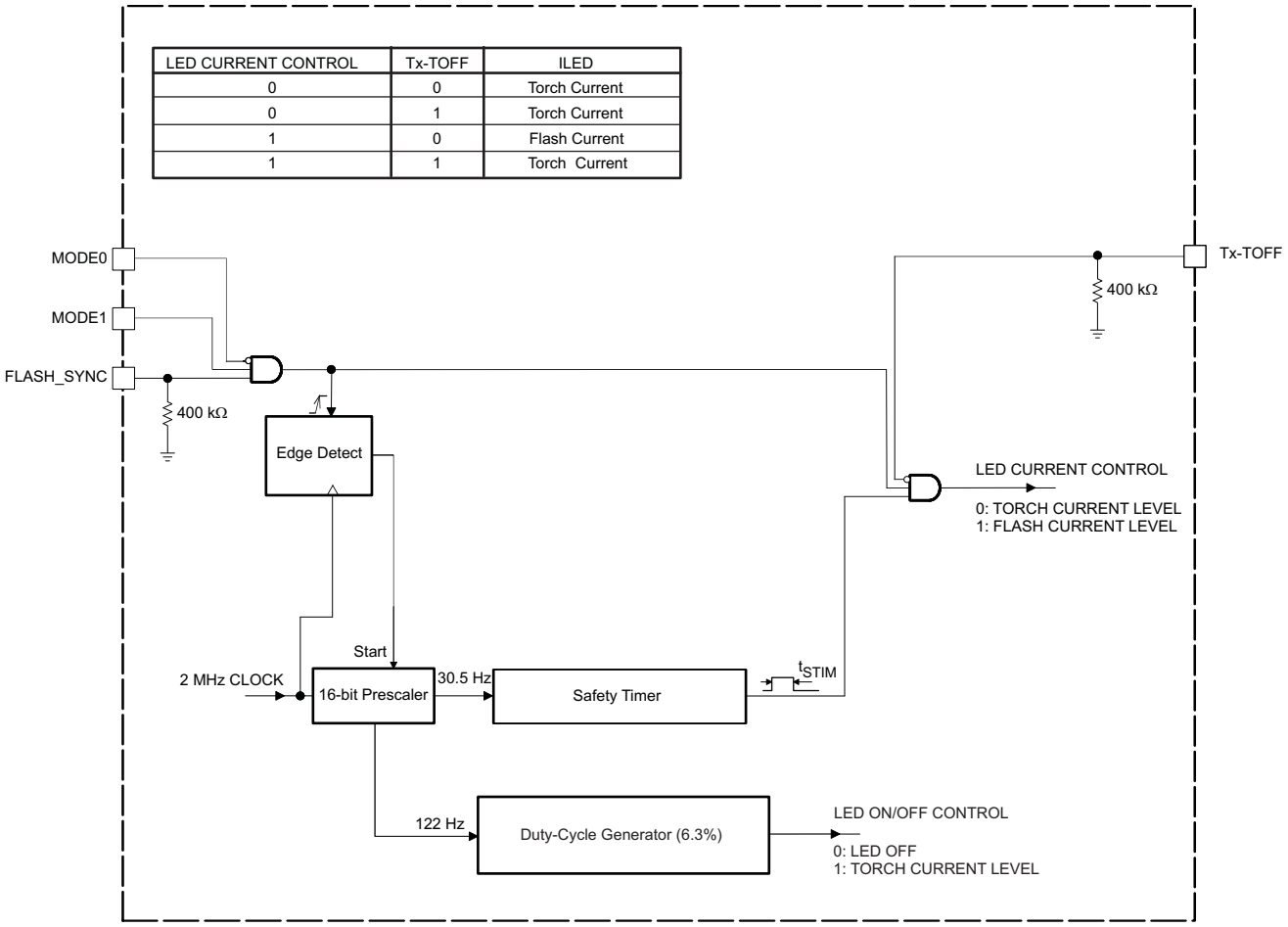
FUNCTIONAL BLOCK DIAGRAM

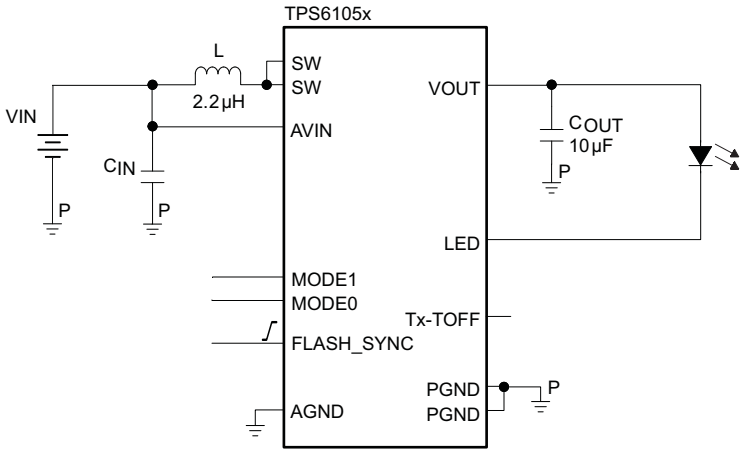


TIMER BLOCK DIAGRAM

LED CURRENT CONTROL	Tx-TOFF	ILED
0	0	Torch Current
0	1	Torch Current
1	0	Flash Current
1	1	Torch Current



PARAMETER MEASUREMENT INFORMATION



List Of Components:
- L = Wuerth Elektronik WE-PD S Series
- C_{IN} = C_{OUT} = TDK C1605X5R0J106MT

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TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

		FIGURE
LED Power Efficiency	vs. Input Voltage	Figure 3, Figure 4
DC Input Current	vs. Input Voltage	Figure 5
LED Current	vs. LED Pin Headroom Voltage	Figure 6
Voltage Mode Efficiency	vs. Output Current	Figure 7
DC Output Voltage	vs. Load Current	Figure 8
DC Output Voltage	vs. Input Voltage	Figure 9
Quiescent Current	vs. Input Voltage	Figure 10
Shutdown Current	vs. Input Voltage	Figure 11
Junction Temperature	vs. GPIO Voltage	Figure 12
PWM Operation		Figure 13
Down-Mode Operation		Figure 14
Voltage Mode Load Transient Response		Figure 15
Down-Mode Line Transient Response		Figure 16
Duty Cycle Jitter		Figure 17
Input Ripple Voltage		Figure 18
Low-Light Dimming Mode Operation		Figure 19
Torch/Flash Sequence		Figure 20
TX-Masking Operation		Figure 21, Figure 22, Figure 23
Start-up Into Flash Operation		Figure 24

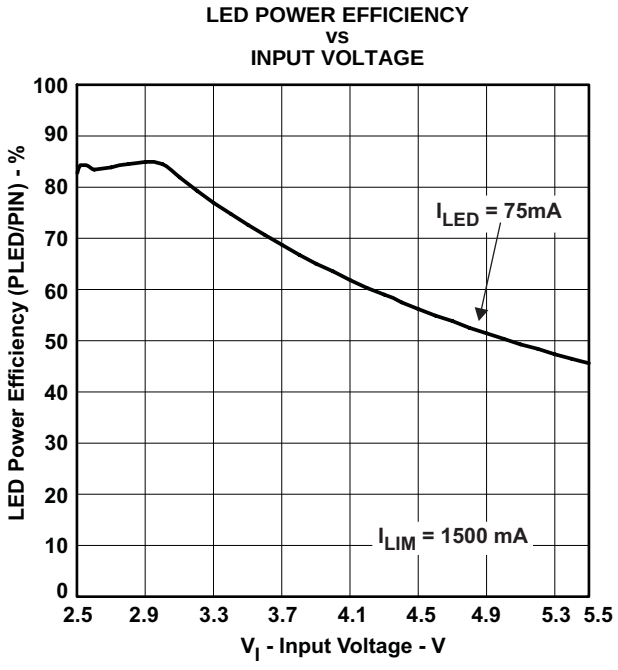
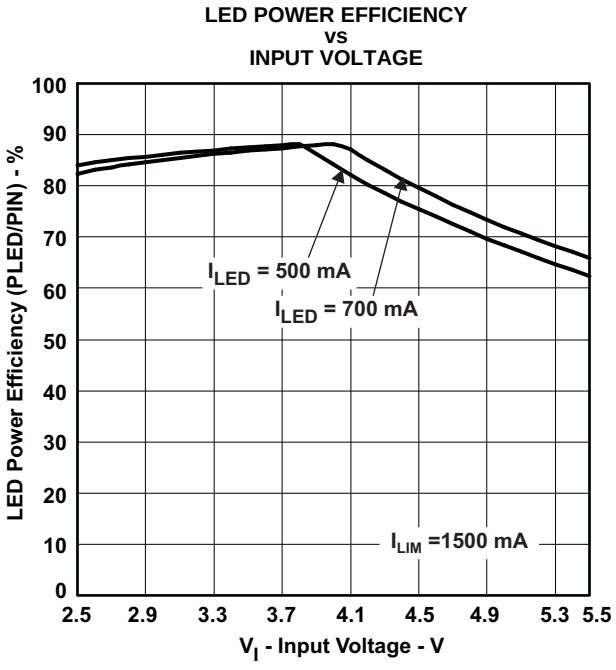


Figure 3.



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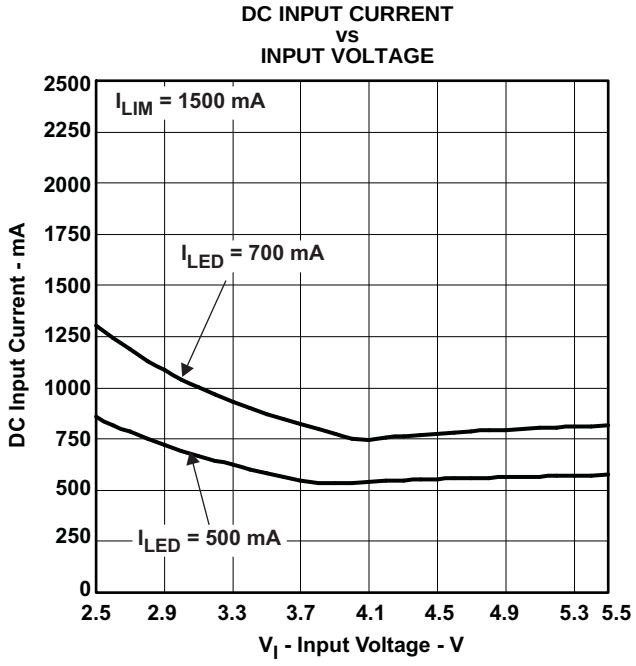

Figure 5.

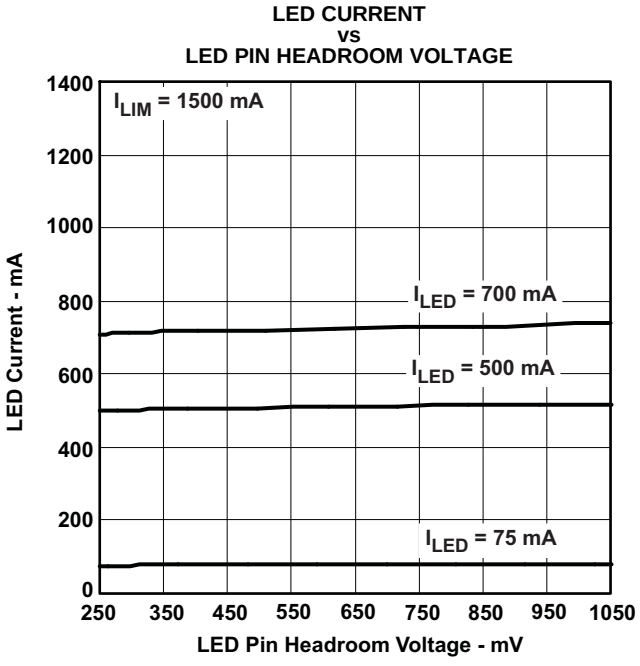

Figure 6.

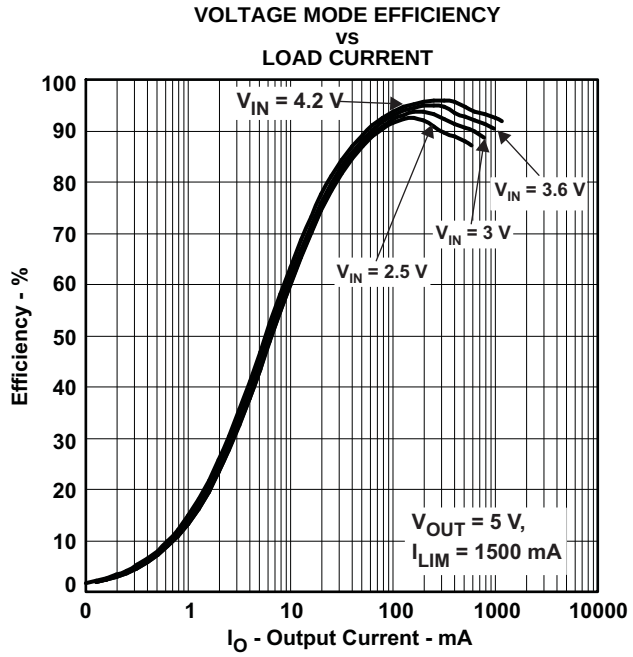

Figure 7.

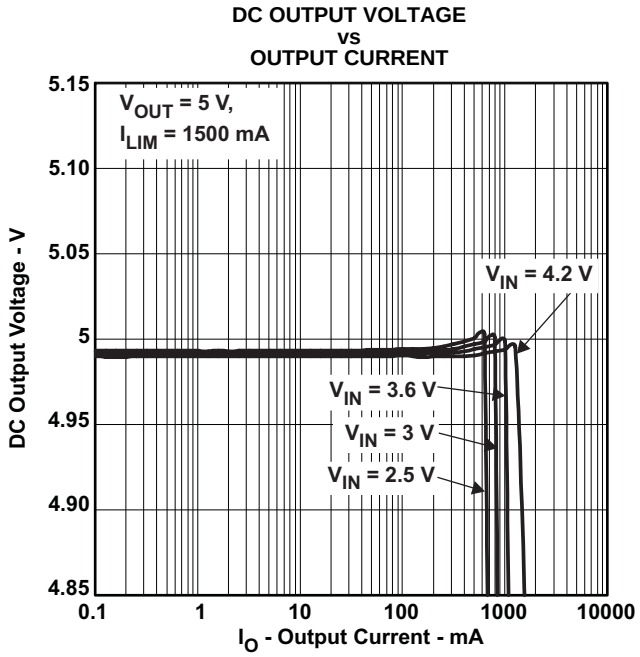

Figure 8.

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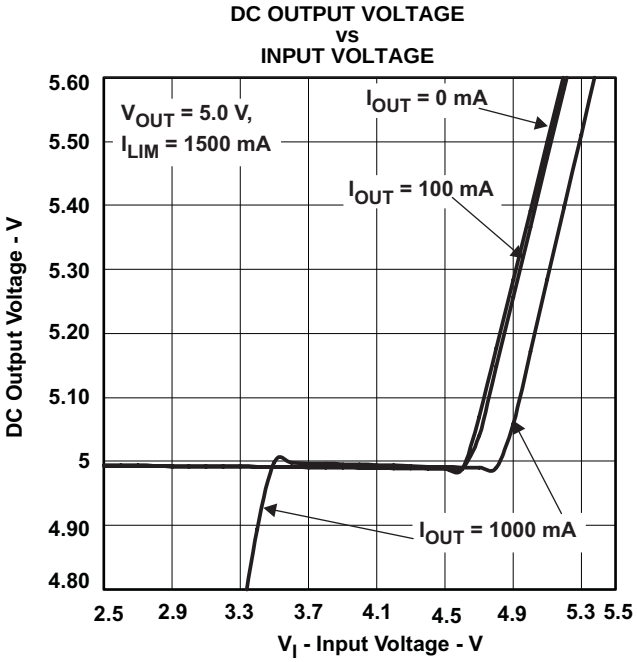


Figure 9.

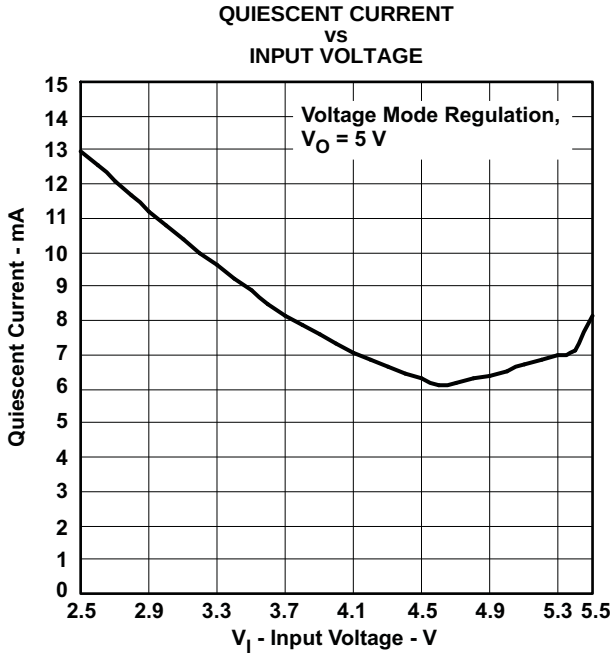
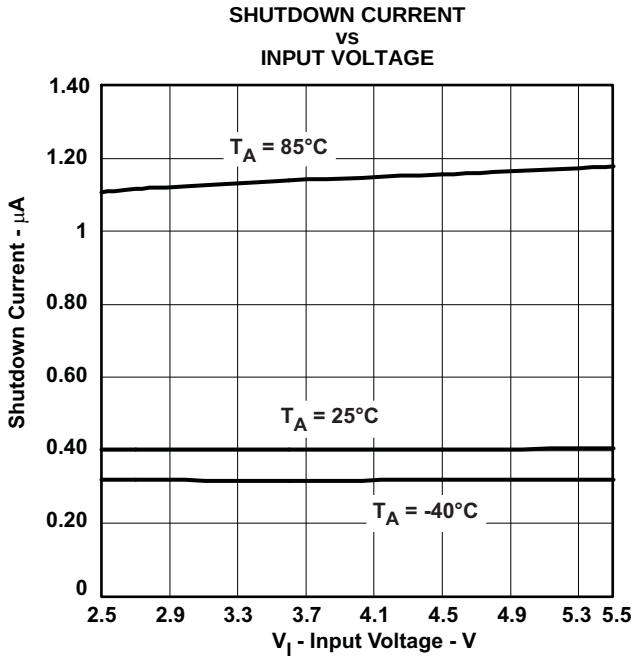


Figure 10.



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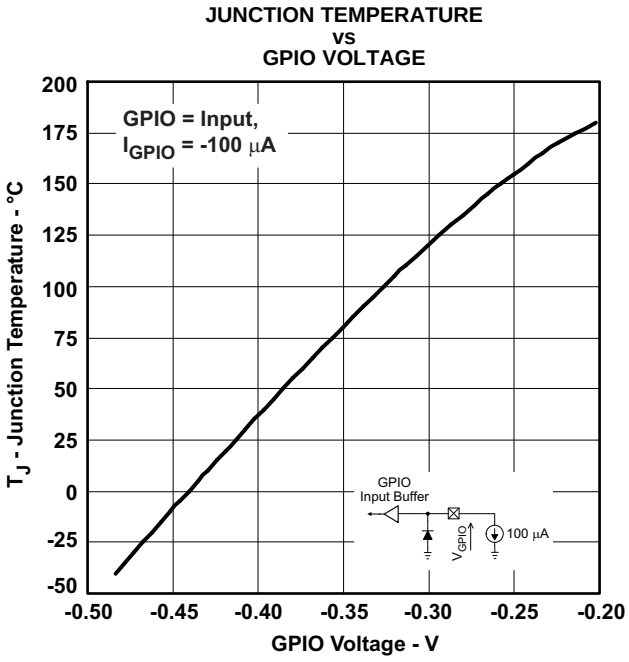
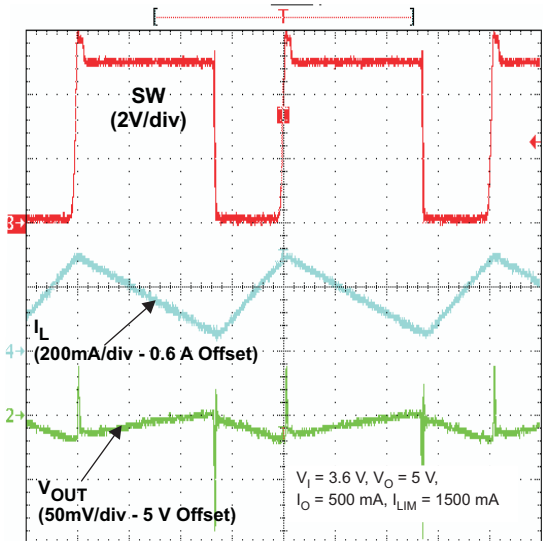


Figure 12.

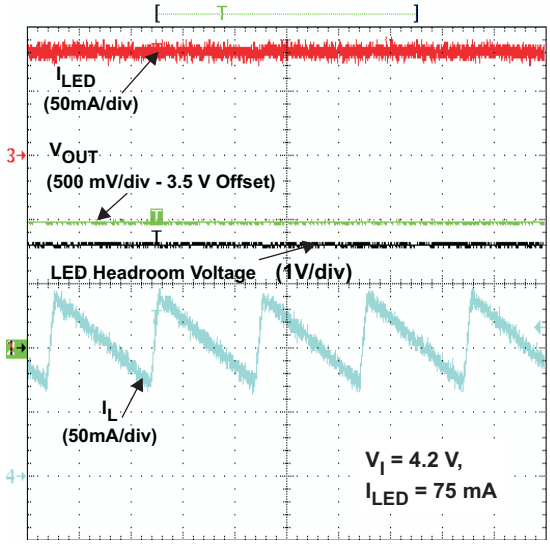
PWM OPERATION



t - Time = 125 ns/div

Figure 13.

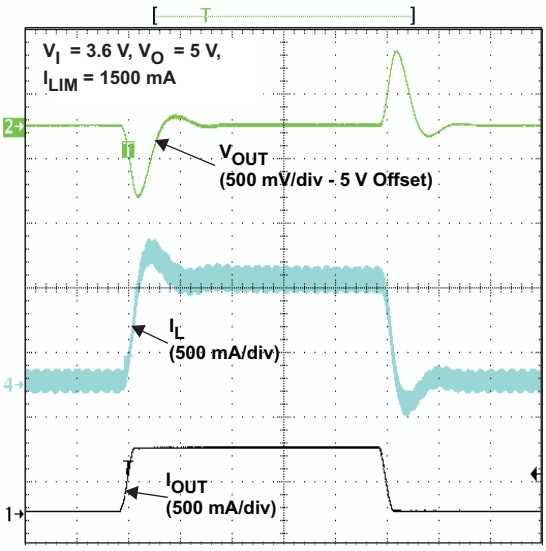
DOWN-MODE OPERATION



t - Time = 250 ns/div

Figure 14.

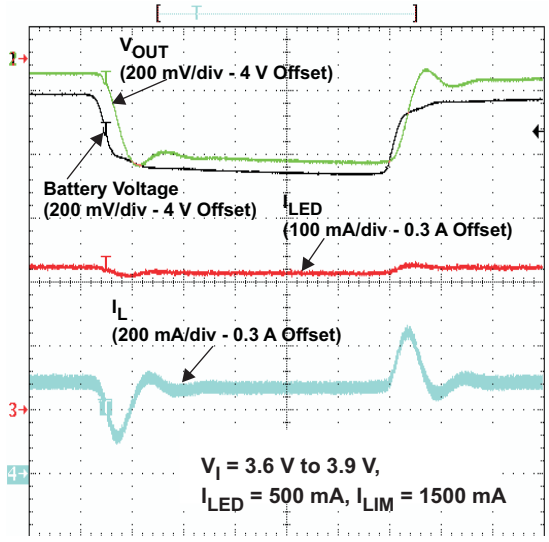
VOLTAGE MODE LOAD TRANSIENT RESPONSE



t - Time = 50 μs/div

Figure 15.

DOWN-MODE LINE TRANSIENT RESPONSE



t - Time = 20 μs/div

Figure 16.

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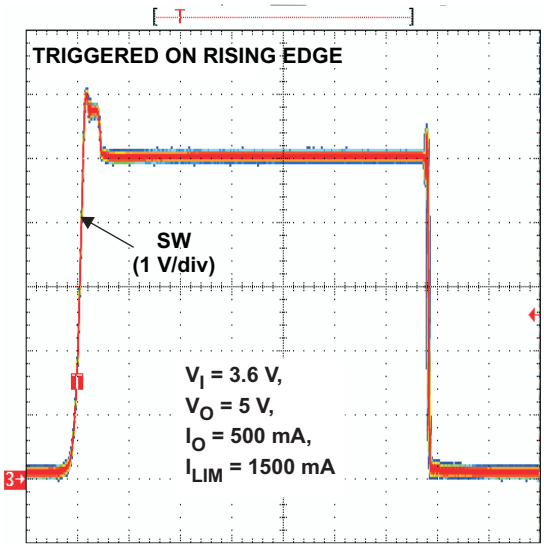
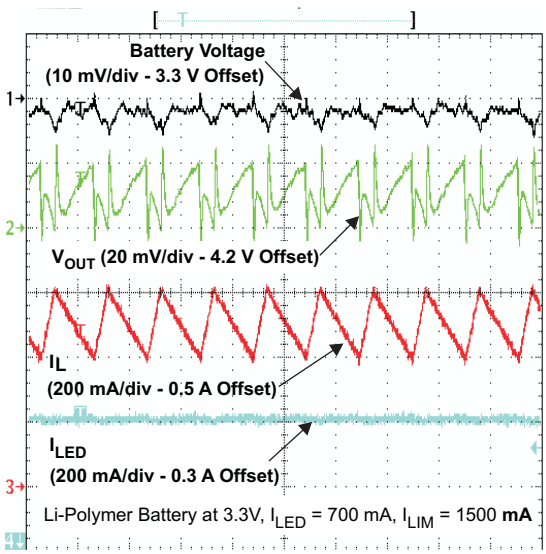
DUTY CYCLE JITTER



t - Time = 50 ns/div

Figure 17.

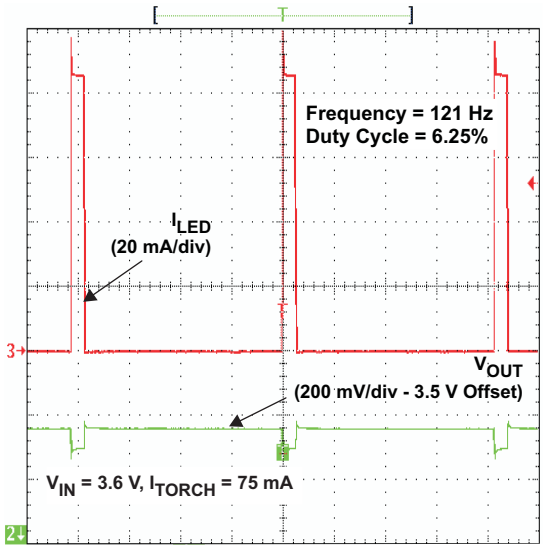
INPUT RIPPLE VOLTAGE



t - Time = 500 ns/div

Figure 18.

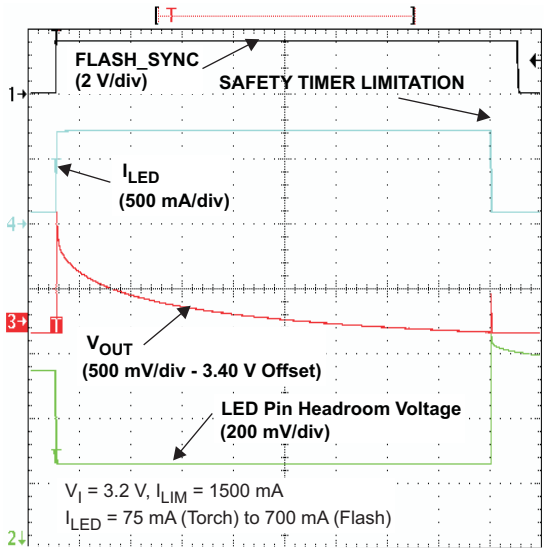
LOW-LIGHT DIMMING MODE OPERATION



t - Time = 2 ms/div

Figure 19.

TORCH/FLASH SEQUENCE



t - Time = 100 ms/div

Figure 20.

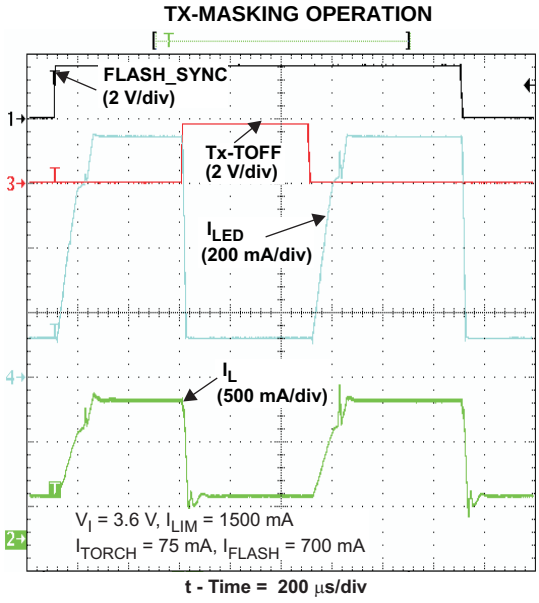


Figure 21.

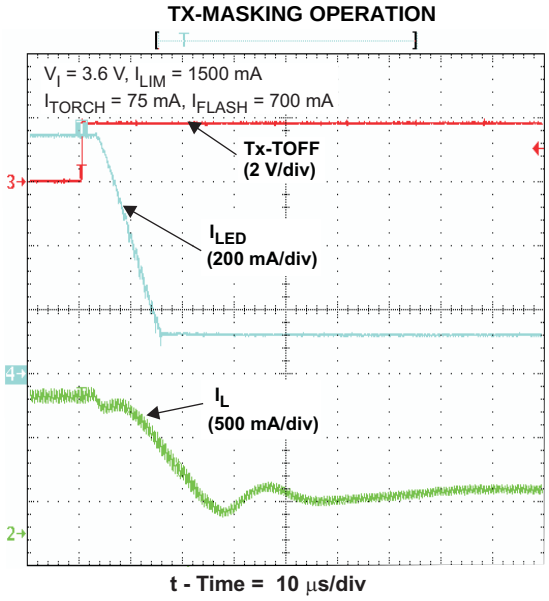


Figure 22.

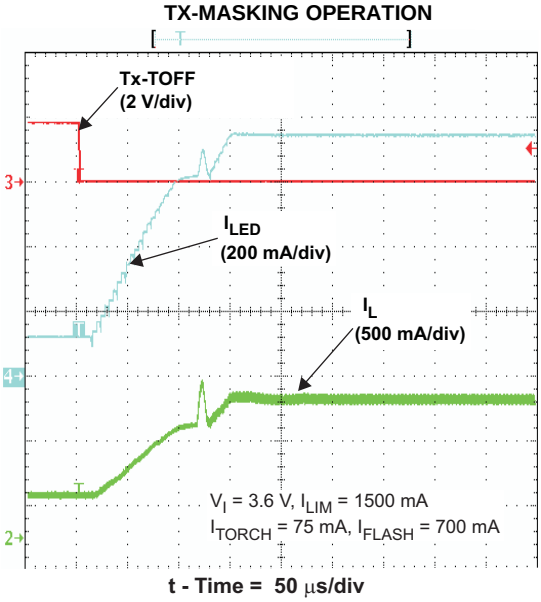


Figure 23.

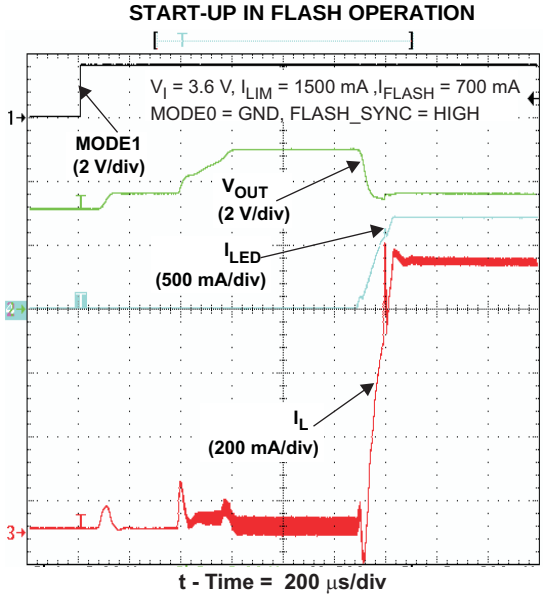


Figure 24.

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DETAILED DESCRIPTION

OPERATION

The TPS6105x family employs a 2-MHz constant-frequency, current-mode PWM converter to generate the output voltage required to drive high-power LEDs. The device integrates a power stage based on an NMOS switch and a synchronous NMOS rectifier. The device also implements a linear low-side current regulator to control the LED current when the battery voltage is higher than the diode forward voltage.

In boost mode, the duty cycle of the converter is set by the error amplifier and the saw-tooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation at duty cycles larger than 50%. The converter is a fully-integrated synchronous-boost converter, always operating in continuous-conduction mode. This allows low-noise operation, and avoids ringing on the switch pin, which would be seen on a converter when entering discontinuous-conduction mode.

The TPS6105x device not only operates as a regulated current source but also as a standard voltage-boost regulator. This additional operating mode can be useful to properly synchronize the converter when supplying other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

The mode of operation (shutdown, torch and flash modes, constant voltage regulation) selection is done via the MODE0/1 control inputs.

Table 2. TPS6105x Operating Modes

MODE1	MODE0	OPERATING MODES
0	0	Power stage is in shutdown. The output is either connected directly to the battery via the rectifier's body diode.
0	1	LED is turned-on for torch light operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
1	0	LED is turned-on for flashlight operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
1	1	LED is turned-off and the converter is operating in voltage regulation mode (VM). The output voltage is regulated to 5.0V.

To simplify flash synchronization with the camera module, the device offers a FLASH_SYNC strobe input pin to switch (with zero latency) the LED current from flash to torch light. The LED is driven at the flashlight current level when a logic high signal is applied to the FLASH_SYNC pin.

The maximum duration of the flash pulse can be limited by means of an internal safety timer (820ms). The safety timer starts on the rising edge of the FLASH_SYNC signal and stops either on its falling edge or after a timeout whatever occurs first.

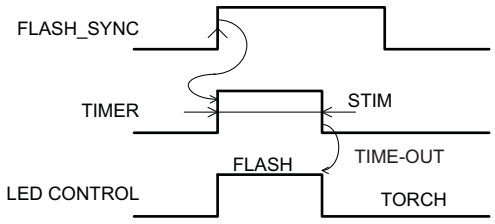

Figure 25. Level Sensitive Safety Timer (Timeout)

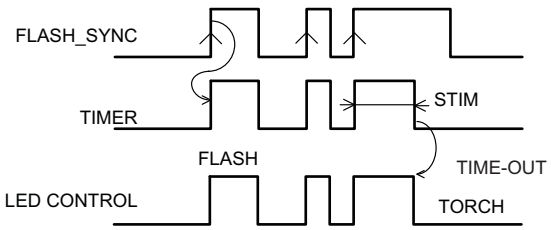

Figure 26. Level Sensitive Safety Timer (Normal Operation + Timeout)

EFFICIENCY

The sense voltage has a direct effect on the converter's efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage, the higher the efficiency will be.

When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED pin of the low-side current regulator is typically 250 mV, which contributes to high power-conversion efficiency.

When running in the linear down-converter mode ($V_{F(LED)} < V_{IN}$), the low-side current regulator drops the voltage difference between the input voltage and the LED forward voltage. Depending on the input voltage and the LED forward voltage characteristic, the converter displays efficiency of approximately 80% to 90%.

FLASH BLANKING

The TPS6105x device also integrates a Tx-TOFF input that can be used as flash masking input. This blanking function turns the LED from flash to torch light, thereby reducing almost instantaneously the peak current loading from the battery. This function has no influence on the safety timer duration.

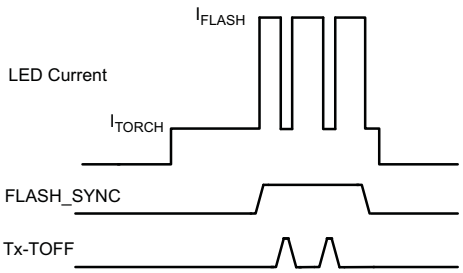

Figure 27. Synchronized Flash With Blanking Periods (MODE0 = 0, MODE1 = 1)

LOW LIGHT DIMMING MODE

The TPS6105x device features white LED drive capability at very low light intensity. To generate a reduced LED average current, the device employs a 122 Hz fixed frequency PWM modulation scheme. Operation is understood best by referring to the timer block diagram.

The torch current is modulated with a 6.3% duty cycle. The low light dimming mode can only be activated in the torch only mode (MODE1 = 0, MODE0 = 1) together with a logic level high applied to the FLASH_SYNC input.

Figure 28. PWM Dimming Principle

White-LED blinking can be achieved by turning on/off periodically the LED dimmer via the (DIM) bit, see Figure 29.

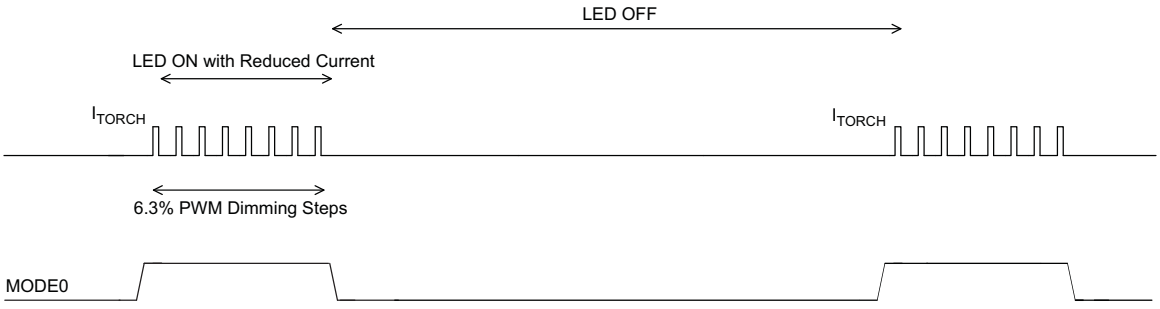

Figure 29. White LED Blinking Control (MODE1 = 0, FLASH_SYNC = 1)

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SOFT-START

Since the output capacitor always remains biased to the input voltage, the TPS6105x can immediately start switching once it has been enabled. The device starts-up by smoothly ramping up it's internal reference voltage, thus limiting the inrush current.

SHUTDOWN

In shutdown mode, the regulator stops switching and the LED pin is high impedance thus eliminating any DC conduction path. The internal switch and rectifier MOSFET are turned off. VOUT is one body-diode drop below the input voltage and the device consumes only a shutdown current of 0.3 μA (typ). The output capacitor remains biased to the input voltage.

LED FAILURE MODES

If the LED fails as a short circuit, the low-side current regulator limits the maximum output current.

If the LED fails as an open circuit, the control loop initially attempts to regulate off of its low-side current regulator feedback signal. This drives VOUT higher. Because the open-circuited LED will never accept its programmed current, VOUT must be voltage-limited by means of a secondary control loop. In this failure mode, the TPS6105x limits VOUT to 6.0 V (typ.).

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the *boost* power stage and the low-side current regulator are turned off. To resume operation, the device needs to be cycled through a shutdown phase (MODE0 = 0, MODE1 = 0).

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APPLICATION INFORMATION

INDUCTOR SELECTION

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS6105x device integrates a current limit protection circuitry. The peak current of the NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor (e.g. 1000 mA or 1500 mA).

In order to optimize solution size the TPS6105x device has been designed to operate with inductance values between a minimum of 1.3 µH and maximum of 2.9 µH. In typical high-current white LED applications a 2.2 µH inductance is recommended.

To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using Equation 1 and Equation 2:

$$I_L \approx I_{OUT} = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (1)$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \text{ with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

with:

f = switching frequency (2 MHz)
L = inductance value (2.2 µH)
η = estimated efficiency (85%)

For example, for an output current of 500 mA at 5 V, the TPS6105x device needs to be set for a 1000 mA current limit operation together with an inductor supporting this peak current.

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 3. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS	I_{LIM} SETTINGS
TDK	VLF3010AT	2,6 mm × 2,8 mm × 1,0 mm max. height	1000 mA (typ.)
TAIYO YUDEN	NR3010	3,0 mm × 3,0 mm × 1,0 mm max. height	
FDK	MIPSA2520	2,5 mm × 2,0 mm × 1,2 mm max. height	
TDK	VLF3014AT	2,6 mm × 2,8 mm × 1,4 mm max. height	1500 mA (typ.)
COILCRAFT	LPS3015	3,0 mm × 3,0 mm × 1,5 mm max. height	
MURATA	LQH3NP	3,0 mm × 3,0 mm × 1,5 mm max. height	
TOKO	FDSE0312	3,0 mm × 3,0 mm × 1,2 mm max. height	

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CAPACITOR SELECTION

Input Capacitor

For good input voltage filtering low ESR ceramic capacitors are recommended. A 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor should be placed as close as possible to the input pin of the converter.

Output Capacitor

The primary parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 3:

$$C_{min} \approx \frac{I_{OUT} \times \left(V_{OUT} - V_{IN}\right)}{f \times \Delta V \times V_{OUT}} \quad (3)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10mV, a minimum capacitance of 10 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 4:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the high current white LED application, a minimum of 3 µF effective output capacitance is usually required when operating with 2.2 µH (typ) inductors. For solution size reasons, this is usually one or more X5R/X7R ceramic capacitors. For stable operation of the internally compensated control loop, a maximum of 50 µF effective output capacitance is tolerable.

Depending on the material, size and margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. It is therefore always recommended to check that the selected capacitors are showing enough effective capacitance under real operating conditions.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The next step in regulation loop evaluation is to perform a load transient test. Output voltage settling time after the load transient event is a good estimate of the control loop bandwidth. The amount of overshoot and subsequent oscillations (ringing) indicates the stability of the control loop. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, output current range, and temperature range.

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LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6105x is 150°C.

The maximum power dissipation gets especially critical when the device operates in the linear down mode at high LED current. For single pulse power thermal analysis (e.g., flash strobe), the allowable power dissipation for the device is given by Figure 30.

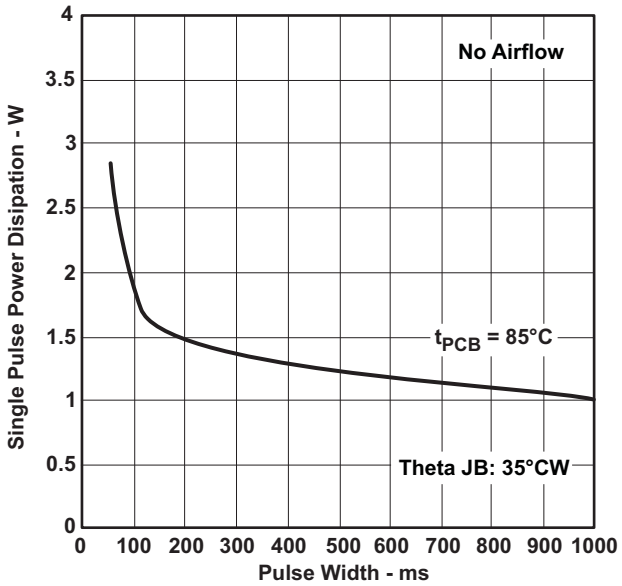

Figure 30. Single Pulse Power Capability (CSP Package)

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TYPICAL APPLICATIONS

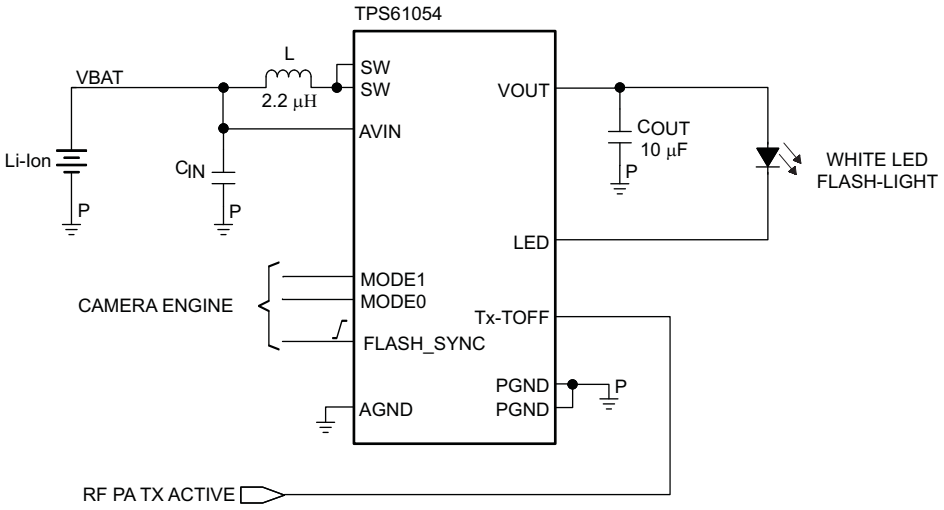


Figure 31. High Power White LED Solution Featuring No-Latency Turn-Down via PA TX Signal

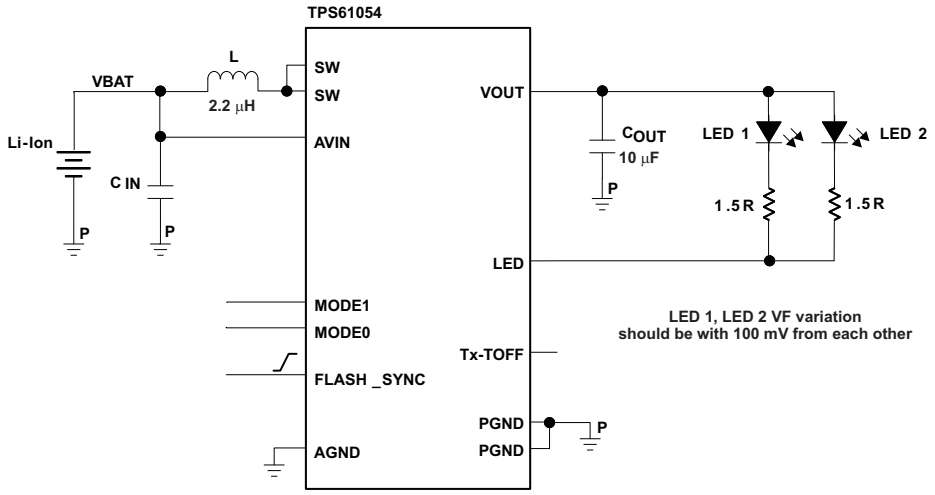
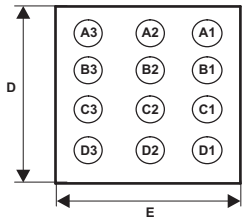


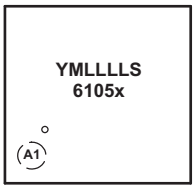
Figure 32. 2 × 350 mA Dual LED Camera Flash

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Code:

- Y — 2 digit date code
- LLLL - lot trace code
- S - assembly site code

PACKAGE DIMENSIONS

The dimensions for the YZG package are shown in Table 4. See the package drawing at the end of this data sheet.

Table 4. YZG Package Dimensions

Packaged Devices	D	E
TPS6105xYZG	1.96 ±0.05 mm	1.46 ±0.05 mm

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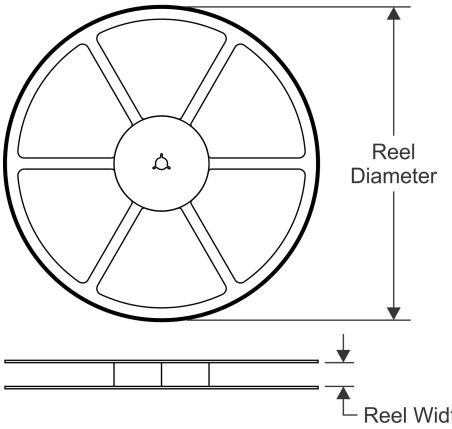
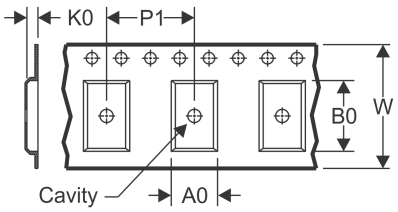
TAPE AND REEL INFORMATION

REEL DIMENSIONS

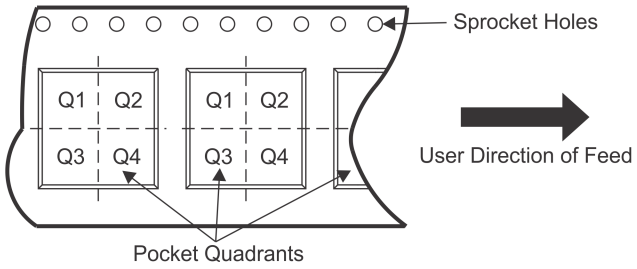


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

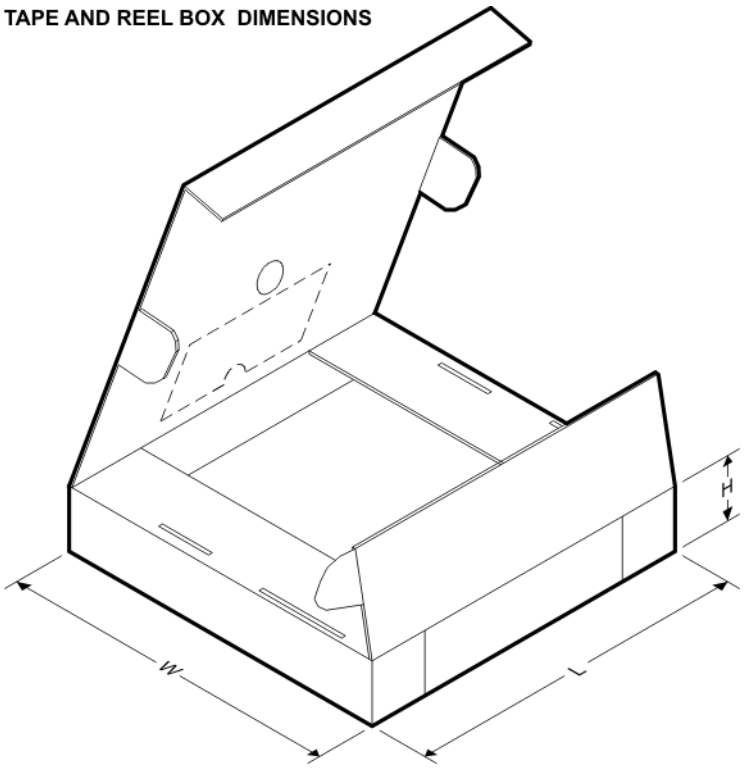
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61054DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61054DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61054YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61054YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61054YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61054YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61055DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61055DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61055YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61055YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61055YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61055YZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1

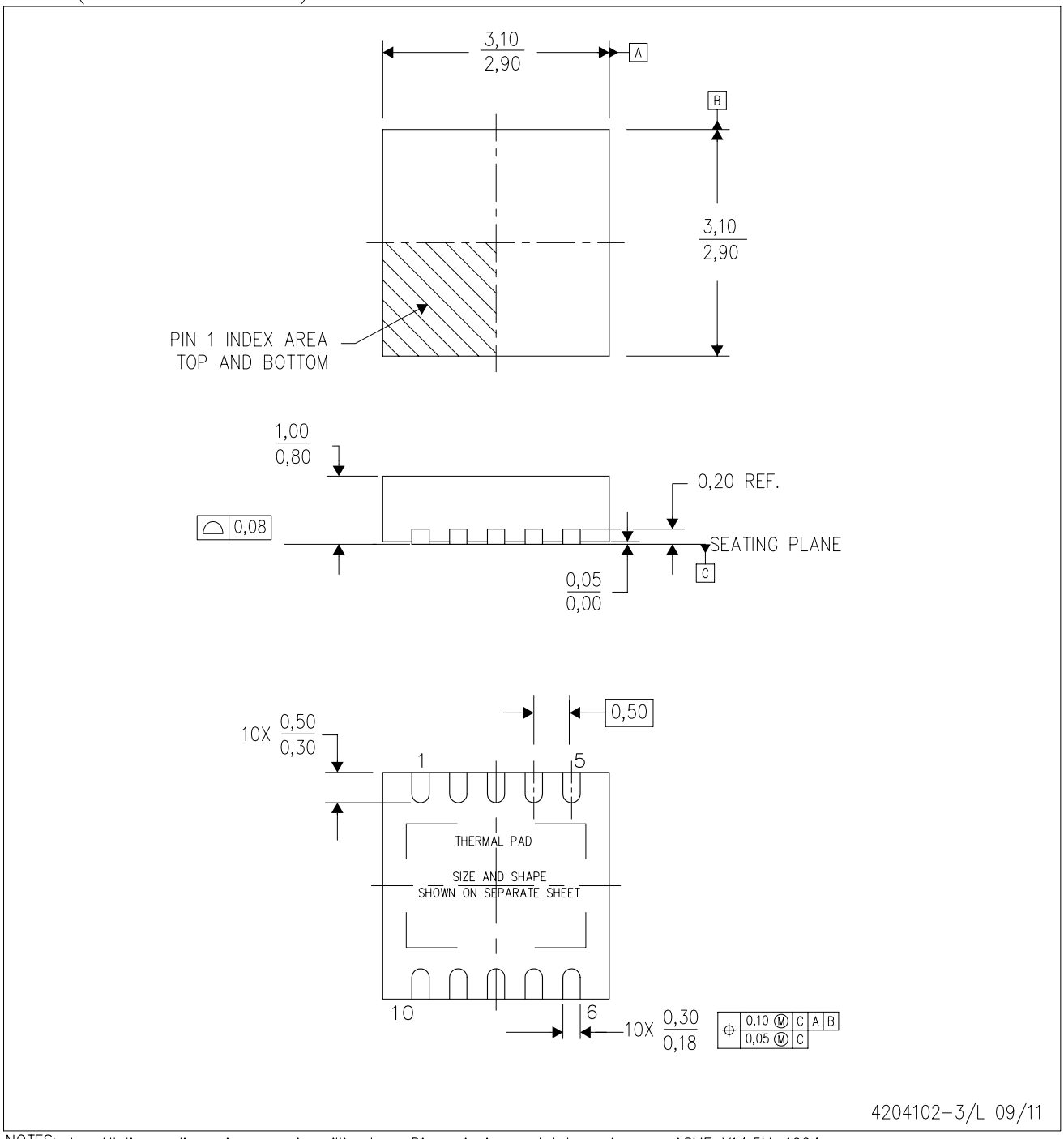
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61054DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS61054DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS61054YZGR	DSBGA	YZG	12	3000	210.0	185.0	35.0
TPS61054YZGR	DSBGA	YZG	12	3000	220.0	220.0	34.0
TPS61054YZGT	DSBGA	YZG	12	250	220.0	220.0	34.0
TPS61054YZGT	DSBGA	YZG	12	250	210.0	185.0	35.0
TPS61055DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS61055DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS61055YZGR	DSBGA	YZG	12	3000	220.0	220.0	34.0
TPS61055YZGR	DSBGA	YZG	12	3000	210.0	185.0	35.0
TPS61055YZGT	DSBGA	YZG	12	250	220.0	220.0	34.0
TPS61055YZGT	DSBGA	YZG	12	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

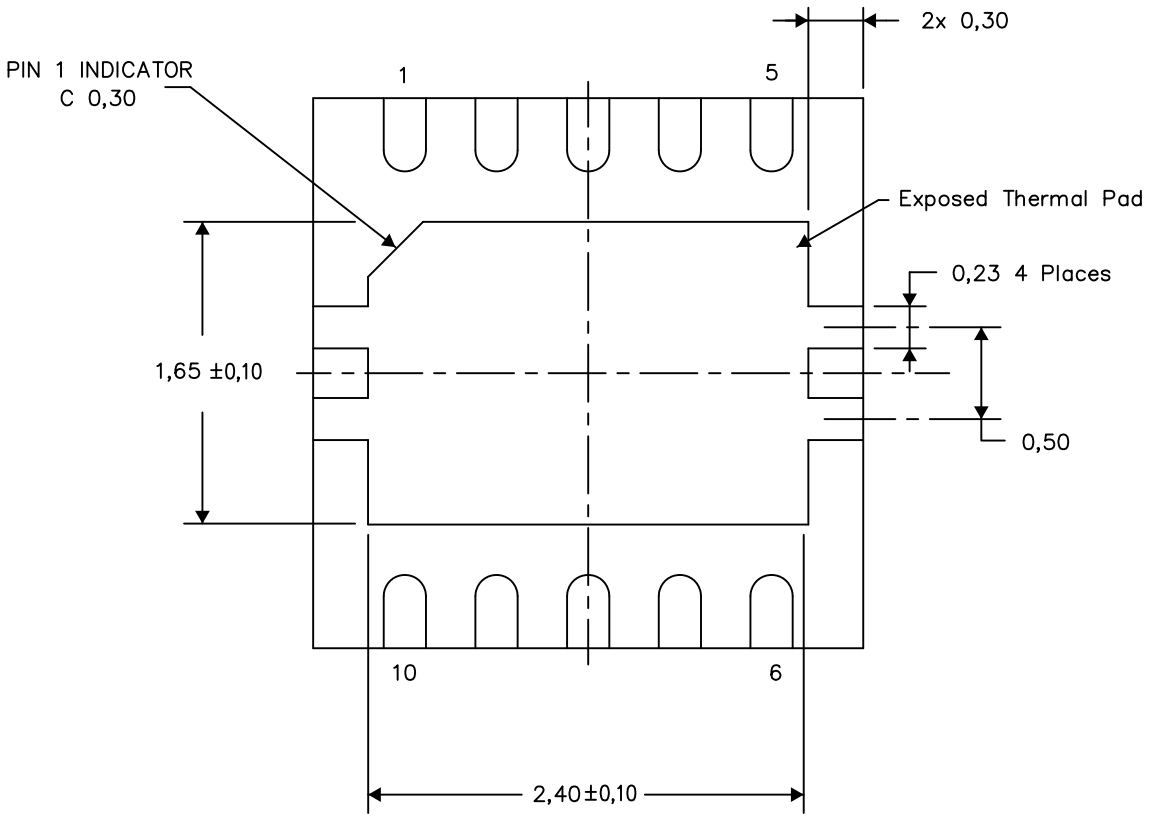
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



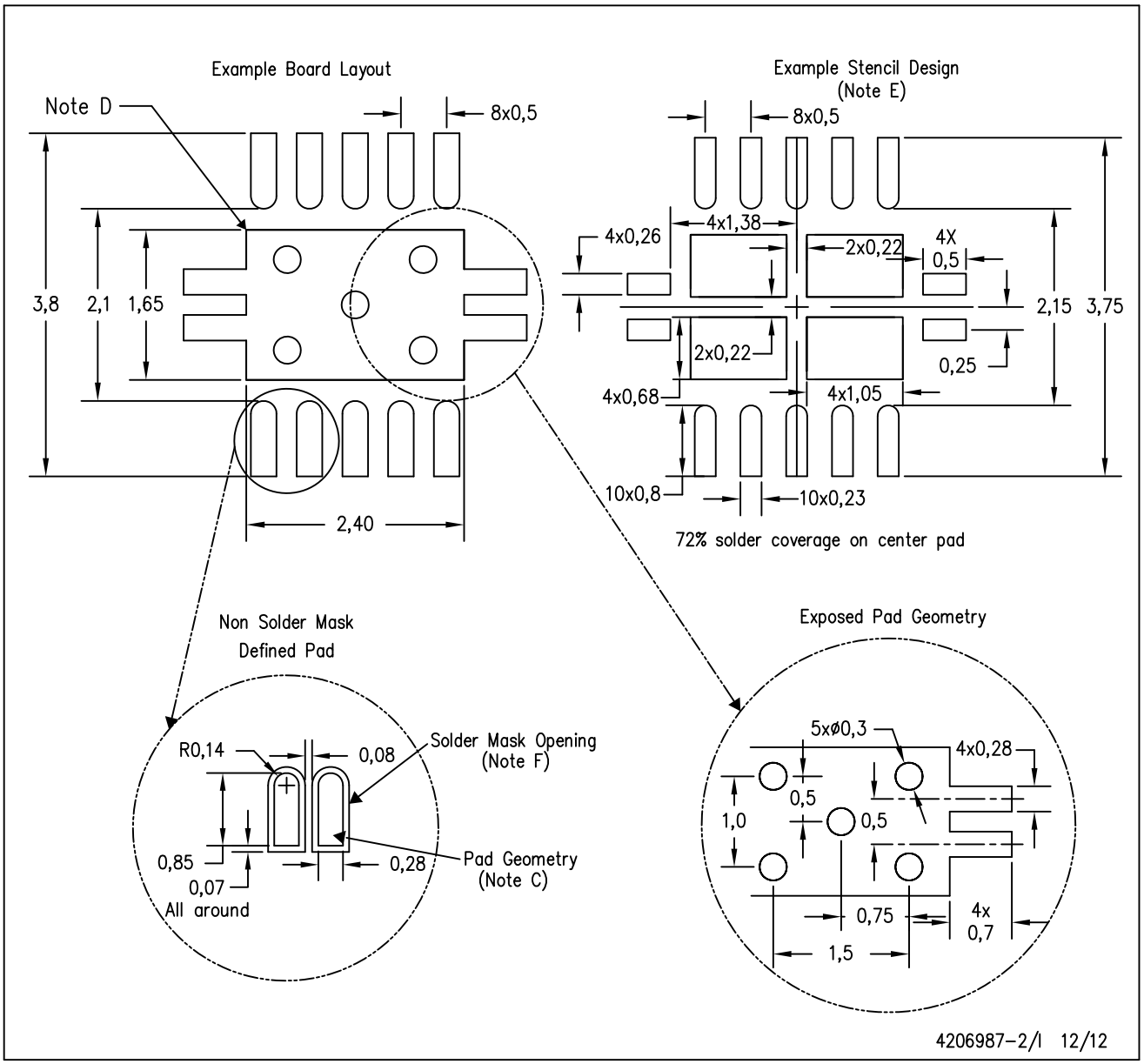
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Q 12/12

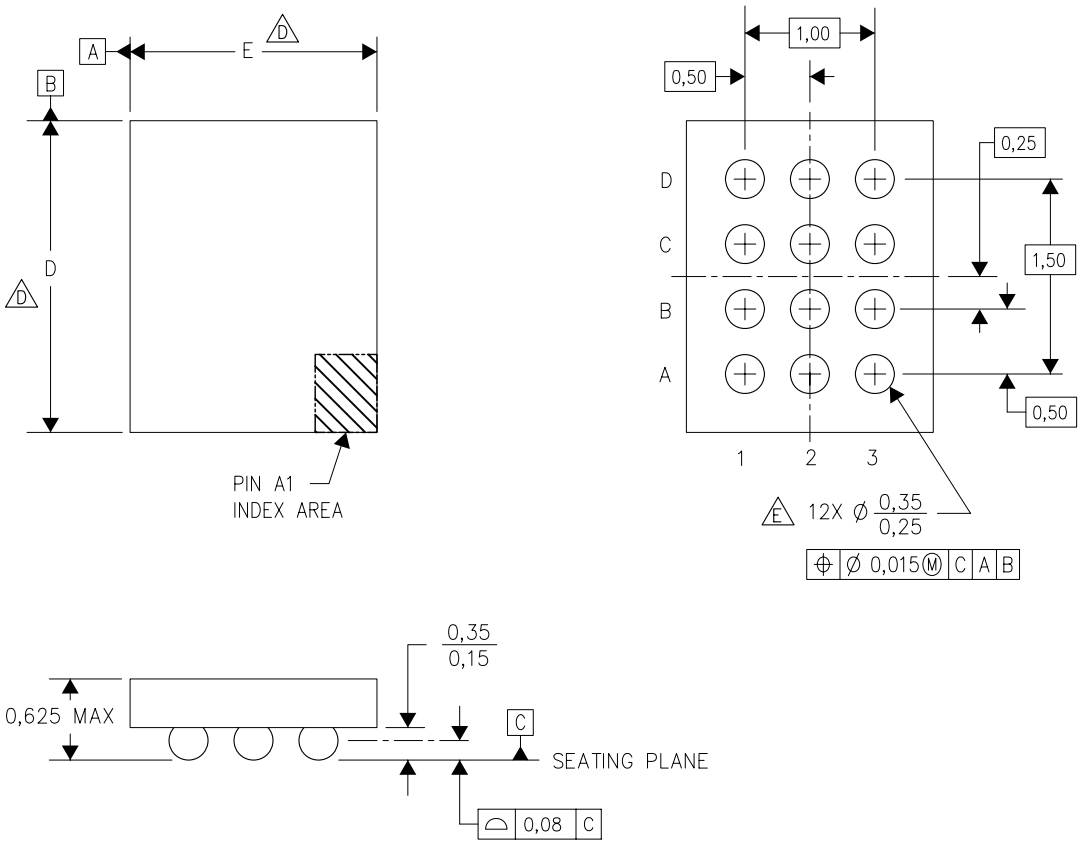
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



4205059/D 06/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZG package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 1.44 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 3 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEG (Drawing #4204182) for tin–lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

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