USB-FRIENDLY LITHIUM-ION BATTERY CHARGER AND POWER-PATH MANAGEMENT IC

Check for Samples: bq24230, bq24232

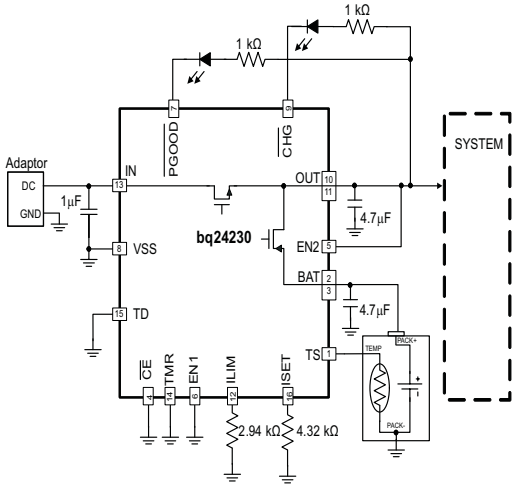
FEATURES

- **Fully Compliant USB Charger**
  - **Selectable 100-mA and 500-mA Maximum Input Current**
  - **100-mA Maximum Current Limit Ensures Compliance to USB-IF Standard**
  - **Input-based Dynamic Power Management (V_{IN}-DPM) for Protection Against Poor USB Sources**
- **28-V Input Rating With Overvoltage Protection**
- **Integrated Dynamic Power-Path Management (DPPM) Function Simultaneously and Independently Powers the System and Charges the Battery**
- **Supports up to 500-mA Charge Current With Current Monitoring Output (ISET)**
- **Programmable Input Current Limit up to 500 mA for Wall Adapters**
- **Programmable Termination Current (bq24232)**
- **Programmable Precharge and Fast-Charge Safety Timers**
- **Reverse Current, Short-Circuit, and Thermal Protection**
- **NTC Thermistor Input**
- **Proprietary Start-Up Sequence Limits Inrush Current**
- **Status Indication – Charging/Done, Power Good**
- **Small 3 mm × 3 mm 16-Lead QFN Package**

APPLICATIONS

- **Bluetooth™ Devices**
- **Low-Power Handheld Devices**

TYPICAL APPLICATION CIRCUIT



DESCRIPTION

The bq2423x series of devices are highly integrated Li-ion linear chargers and system power-path management devices targeted at space-limited portable applications. The devices operate from either a USB port or ac adapter and support charge currents between 25 mA and 500 mA. The high-input-voltage range with input overvoltage protection supports low-cost, unregulated adapters. The USB input current limit accuracy and start-up sequence allow the bq2423x to meet USB-IF inrush current specification. Additionally, the input dynamic power management (V_{IN}-DPM) prevents the charger from crashing poorly designed or incorrectly configured USB sources.

The bq2423x features dynamic power-path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold, thus supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents, enabling the use of a smaller adapter.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has high-accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

ORDERING INFORMATION

PART NUMBER (1) (2)	V_{OVP}	$V_{OUT(REG)}$	V_{DPM}	OPTIONAL FUNCTION	MARKING
bq24230RGTR	6.6 V	4.4 V	$V_{O(REG)}$ – 100 mV	TD	CGN
bq24230RGTT	6.6 V	4.4 V	$V_{O(REG)}$ – 100 mV	TD	CGN
bq24232RGTR	10.5 V	4.4 V	$V_{O(REG)}$ – 100 mV	ITERM	NXK
bq24232RGTT	10.5 V	4.4 V	$V_{O(REG)}$ – 100 mV	ITERM	NXK

(1) The RGT package is available in the following options:
R - taped and reeled in quantities of 3000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS (1)

over the 0°C to 125°C operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_I	Input voltage	IN (with respect to VSS)	–0.3 to 28	V
		OUT (with respect to VSS)	–0.3 to 7	V
		BAT (with respect to VSS)	–0.3 to 5	V
		EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, TMR, TD, ITERM (with respect to VSS)	–0.3 to 7	V
I_I	Input current	IN	600	mA
I_O	Output current (continuous)	OUT	1700	mA
		BAT (Discharge mode)	1700	mA
	Output sink current	$\overline{CHG}$, $\overline{PGOOD}$	15	mA
T_J	Junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS (1)

PACKAGE (2)	$R_{\theta JA}$	$R_{\theta JC}$	POWER RATING	
			$T_A \le 25°C$	$T_A = 85°C$
RGT (1)	39.47 °C/W	2.4 °C/W	2.3 W	225 mW

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	IN voltage range		4.35	26	V
	IN operating voltage range	'230	4.35	6.4	V
		'232	4.35	10.2	
I_{IN}	Input current, IN pin			500	mA
I_{OUT}	Current, OUT pin			1500	mA
I_{BAT}	Current, BAT pin (discharging)			1500	mA
I_{CHG}	Current, BAT pin (charging)			500	mA
T_J	Junction temperature		–40	125	°C
R_{ILIM}	Maximum input current programming resistor		3.1	7.8	kΩ
R_{ISET}	Fast-charge current programming resistor		1.8	36	kΩ
R_{TMR}	Timer programming resistor		18	72	kΩ
R_{ITERM}	Termination programming resistor	'232	0	15	kΩ

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lockout	V_{IN}: 0 V → 4 V	3.2	3.3	3.4	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	V_{IN}: 4 V → 0 V	200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ V_{BAT} = 3.6 V, VIN: 3.5 V → 4 V	55	80	130	mV
$V_{hys(INDT)}$	Hysteresis on $V_{IN(DT)}$	VBAT = 3.6 V, V_{IN}: 4 V → 3.5 V	20			mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V 1-µs rise time to $\overline{PGOOD}$ = LO		2		ms
V_{OVP}	Input overvoltage protection threshold	('230) V_{IN}: 5 V → 7 V	6.4	6.6	6.8	V
		('232) V_{IN}: 5 V → 11 V	10.2	10.5	10.8	
$V_{hys(OVP)}$	Hysteresis on OVP	('230) V_{IN}: 7 V → 5V		110		mV
		('232) V_{IN}: 11 V → 5 V		175		
$t_{DGL(OVP)}$	Input overvoltage blanking time			50		µs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V 1 µs fall time to $\overline{PGOOD}$ = LO		2		ms
ILIM, TEST ISET SHORT CIRCUIT						
I_{SC}	Current source	V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$		1.3		mA
V_{SC}		V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$		520		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, input power not detected, no load on OUT pin			6.5	µA
$I_{IN(STDBY)}$	Standby current into IN pin	EN1= HI, EN2=HI, V_{IN} = 6 V, T_J=85°C			50	µA
		EN1= HI, EN2=HI, V_{IN} = 10 V, T_J=85°C			200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6 V, no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)			1.5	mA
POWER PATH						
$V_{DO(IN-OUT)}$	$V_{IN} – V_{OUT}$	V_{IN} = 4.3 V, I_{IN} = 500 mA, V_{BAT} = 4.2 V		150.0	237.5	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} – V_{OUT}$	I_{OUT} = 500 mA, V_{IN} = 0 V, V_{BAT} > 3 V			62.5	mV
$V_{O(REG)}$	OUT pin voltage regulation	$V_{IN} > V_{OUT} + V_{DO\ (IN-OUT)}$	4.3	4.4	4.5	V
I_{IN}max	Maximum input current	EN1 = LO, EN2 = LO	90	95	100	mA
		EN1 = HI, EN2 = LO	450	475	500	
		EN2 = HI, EN1 = LO		K_{ILIM}/R_{ILIM}		A
K_{ILIM}	Maximum input current factor	I_{LIM} = 200mA to 500mA	1380	1530	1680	AΩ
I_{IN}max	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 3.1 kΩ to 7.8 kΩ	200		500	mA

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN-DPM}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.50	4.63	V
V_{DPPM}	Output voltage threshold when charging current is reduced		$V_{O(REG)}$ – 180 mV	$V_{O(REG)}$ – 100 mV	$V_{O(REG)}$ – 30 mV	V
V_{BSUP1}	Enter battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 10 Ω →2 Ω		$V_{OUT} \le V_{BAT}$ –40 mV		V
V_{BSUP2}	Exit battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 2 Ω →10 Ω		$V_{OUT} \ge V_{BAT}$–20 mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode V_{BAT} – V_{OUT} > $V_{O(SC2)}$ indicates short circuit	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
BATTERY CHARGER						
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection	V_{BAT} = 1.5 V	4	7.5	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage		4.16	4.20	4.23	V
V_{LOWV}	Precharge to fast-charge transition threshold	V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$	2.9	3	3.1	ms
$t_{DGL1(LOWV)}$	Deglitch time on precharge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to precharge transition			25		ms
I_{CHG}	Battery fast-charge current range	$V_{BAT(REG)}$ > V_{BAT} > V_{LOWV}, V_{IN} = 5 V, $\overline{CE}$ = LO, EN1 = LO, EN2 = HI	25		500	mA
	Battery fast-charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, V_{BAT} > V_{LOWV}, V_{IN} = 5 V, I_{IN}max > I_{CHG}, no load on OUT pin, thermal loop and DPM loop not active		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast-charge current factor	25 mA ≥ I_{CHG}≥ 500 mA	797	870	975	AΩ
I_{PRECHG}	Precharge current	2.5 mA ≥ I_{PRECHG}≥ 30 mA	70	88	106	AΩ
I_{TERM}	Termination comparator threshold for termination detection	$\overline{CE}$ = LO, (EN1,EN2) ≠ (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.09*I_{CHG}	0.1*I_{CHG}	0.11*I_{CHG}	A
		$\overline{CE}$ = LO, (EN1,EN2) = (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.027*I_{CHG}	0.033*I_{CHG}	0.040*I_{CHG}	
I_{TERM}	Termination current threshold factor (bq24232)	I_{TERM} = 0% to 50% of I_{CHG}		K_{ITERM}*R_{ITERM}/R_{ISET}		A
$I_{BIAS(ITERM)}$	Current for external termination-setting resistor		72	75	78	µA
K_{ITERM}	K factor for termination detection threshold (externally set) (bq24232)	$\overline{CE}$ = LO, (EN1,EN2) ≠ (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.024	0.030	0.036	A
		$\overline{CE}$ = LO, (EN1,EN2) = (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.009	0.010	0.011	
$I_{BIAS(ITERM)}$	Current for external termination_setting resistor (bq24232)		72	75	78	µA
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
V_{RCH}	Recharge detection threshold	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	$V_{O(REG)}$ –140 mV	$V_{O(REG)}$ –100 mV	$V_{O(REG)}$ –60 mV	V

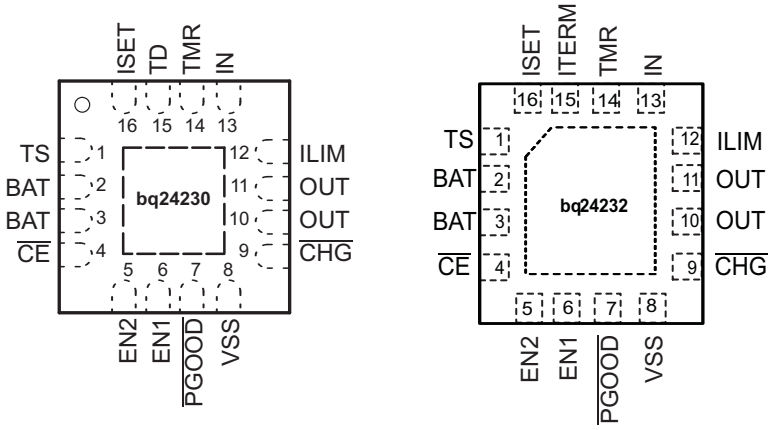
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turnoff	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1-µs fall time		20		ms
$I_{BAT(DET)}$	Sink current for battery detection	V_{BAT}=2.5 V	5	7.5	10	mA
t_{DET}	Battery detection timer	BAT high or low		250		ms
BATTERY CHARGING TIMERS						
t_{PRECHG}	Precharge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Precharge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		R_{TMR} × K_{TMR}		s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		10×RTMR ×K_{TMR}		s
K_{TMR}	Timer factor		30	40	50	s/kΩ
BATTERY-PACK NTC MONITOR(1)						
I_{NTC}	NTC bias current	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	72	75	78	µA
V_{HOT}	High-temperature trip point	Battery charging, V_{TS} Falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, V_{TS} Rising from V_{HOT}		30		mV
V_{COLD}	Low-temperature trip point	Battery charging, V_{TS} Rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, V_{TS} Falling from V_{COLD}		300		mV
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	Battery charging, V_{TS} Falling		50		ms
$V_{DIS(TS)}$	TS function disable threshold	TS unconnected		V_{IN}-200 mV		V
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, TD						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6.0	V
I_{IL}	Input sink current	V_{IL} = 0 V			1	µA
I_{IH}	Input source current	V_{IH} = 1.4 V			10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

RGT PACKAGE
(Top View)



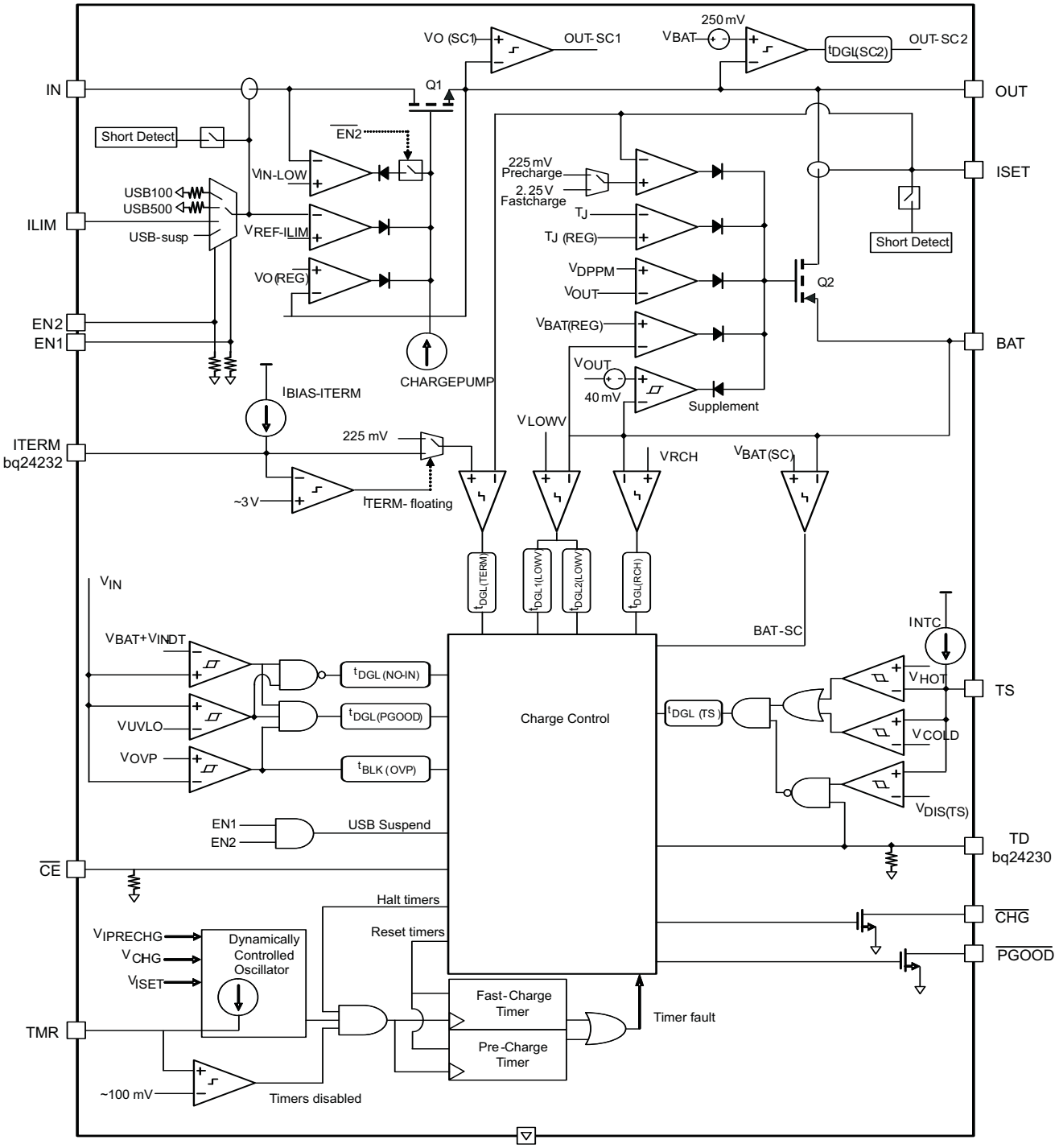
TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NUMBER			
	'230	'232		
TS	1	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10-kΩ NTC thermistor. For applications that do not utilize the TS function, connect a 10-kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS.
BAT	2,3	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
$\overline{CE}$	4	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to place the battery charger in standby mode. In standby mode, OUT is active and battery supplement mode is still available. Connect $\overline{CE}$ to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with ~285 kΩ. Do not leave $\overline{CE}$ unconnected to ensure proper operation.
EN2	5	5	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See Table 2 for the description of the operation states. EN1 and EN2 are internally pulled down with ~285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN1	6	6	I	
$\overline{PGOOD}$	7	7	O	Open-drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 1-kΩ – 100-kΩ resistor, or use with an LED for visual indication.
VSS	8	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{CHG}$	9	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high impedance when charging is complete and when charger is disabled.
OUT	10,11	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to V_{BAT}. Connect OUT to the system load. Bypass OUT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
ILIM	12	12	I	Adjustable Current Limit Programming Input. Connect a 3.1-kΩ to 7.8-kΩ resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current.
IN	13	13	I	Input Power Connection. Connect IN to the connected to external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.6 V. The input can accept voltages up to 26 V without damage but operation is suspended. Connect bypass capacitor 1 μF to 10 μF to VSS.
TMR	14	14	I	Timer Programming Input. TMR controls the precharge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18-kΩ to 72-kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the 5-hour fast charge and 30-minute precharge default timer values.
TD	15	-	I	Termination Dsable Input. Connect TD high to disable charger termination. Connect TD to VSS to enable charger termination. TD is checked during start-up only and cannot be changed during operation. See the TD section in this data sheet for a description of the behavior when termination is disabled. TD is internally pulled down to VSS with ~285 kΩ. Do not leave TD unconnected to ensure proper operation.
ITERM	-	15	I	Termination Current Programming Input. Connect a 0-Ω to 15-kΩ resistor from ITERM to VSS to program the termination current. Leave ITERM unconnected to set the termination current to the internal default 10% threshold.
ISET	16	16	I/O	Fast-Charge Current Programming Input. Connect a 3-kΩ to 36-kΩ resistor from ISET to VSS to program the fast-charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. See the CHARGE CURRENT TRANSLATOR section for more details.
Thermal Pad			–	An internal electrical connection exists between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

Table 1. EN1/EN2 Settings

EN2	EN1	Maximum input current into IN pin
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

SIMPLIFIED BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Typical Application Circuit, EN1=0, EN2=1, T_A=25°C, unless otherwise noted.

ADAPTER PLUG-IN WITH BATTERY CONNECTED
R_{LOAD} = 25Ω

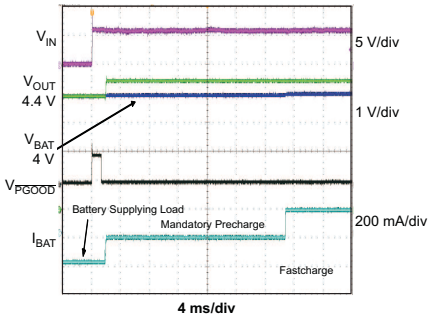


Figure 1.

BATTERY DETECTION -- INSERTION

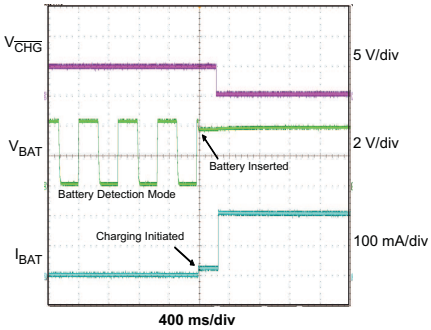


Figure 2.

BATTERY DETECTION -- REMOVAL

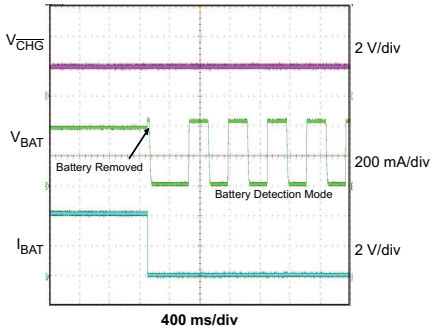


Figure 3.

ENTERING AND EXITING DPPM MODE
R_{LOAD} = 25Ω to 9Ω

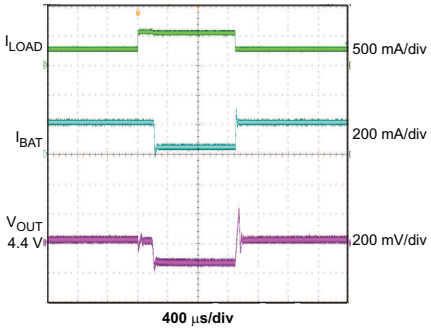


Figure 4.

ENTERING AND EXITING BATTERY SUPPLEMENT MODE
R_{LOAD} = 25Ω to 4.5Ω

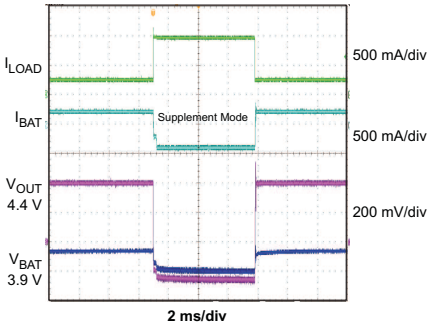


Figure 5.

CHARGER ON/OFF USING $\overline{CE}$

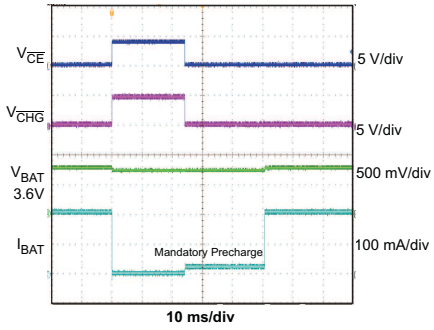


Figure 6.

OVP FAULT
V_{IN} = 6V to 15V
R_{LOAD} = 25Ω

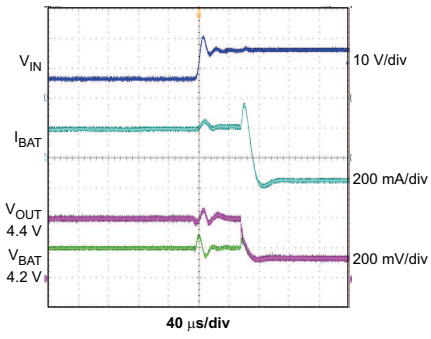


Figure 7.

THERMAL REGULATION

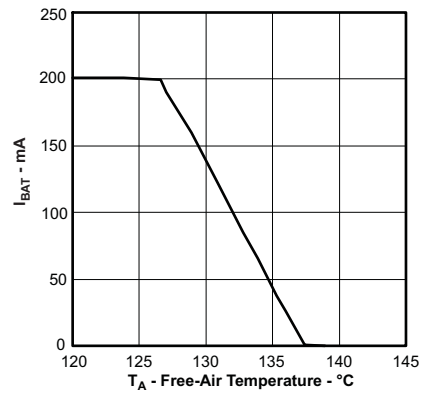


Figure 8.

DROPOUT VOLTAGE vs TEMPERATURE

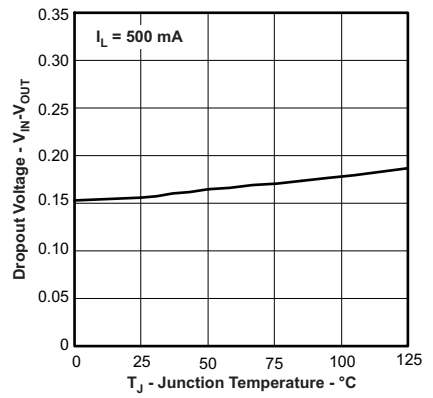


Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical Application Circuit, EN1=0, EN2=1, T_A=25°C, unless otherwise noted.

DROPOUT VOLTAGE vs TEMPERATURE

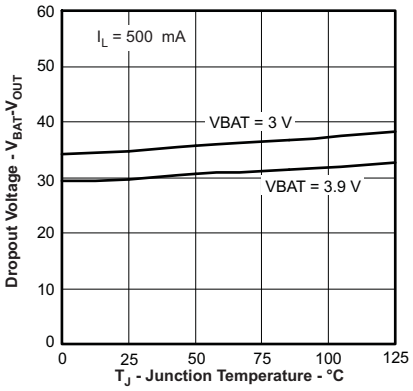


Figure 10.

OUTPUT REGULATION VOLTAGE vs TEMPERATURE

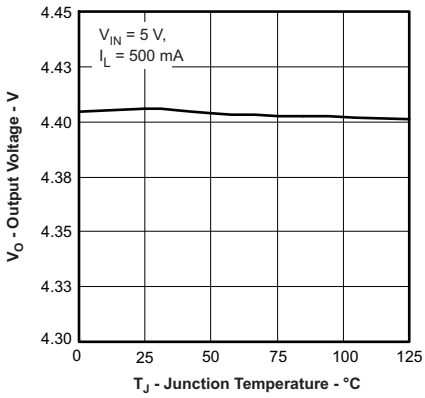


Figure 11.

BATTERY REGULATION VOLTAGE vs TEMPERATURE

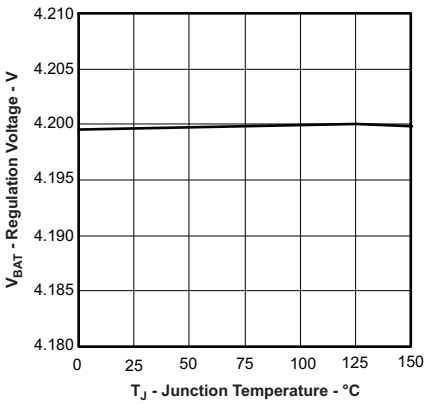


Figure 12.

OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE bq24230

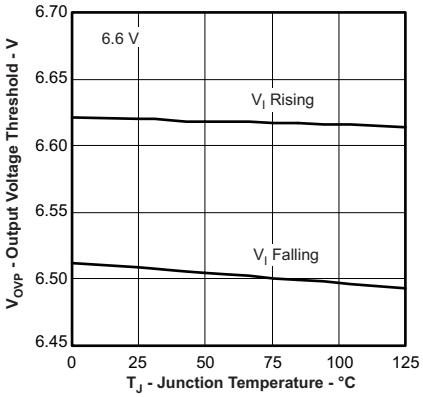


Figure 13.

OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE bq24232

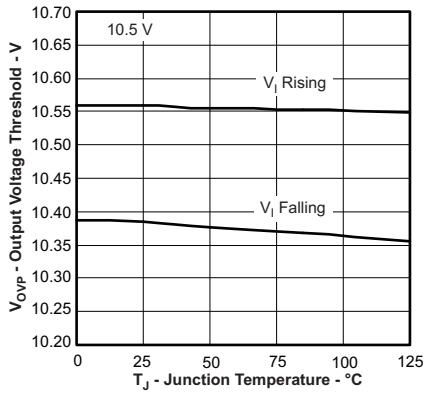


Figure 14.

INPUT CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

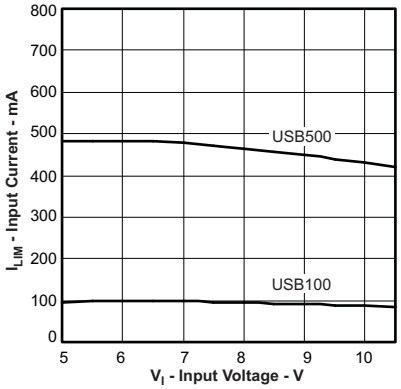


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical Application Circuit, EN1=0, EN2=1, T_A=25°C, unless otherwise noted.

FAST-CHARGE CURRENT vs BATTERY VOLTAGE

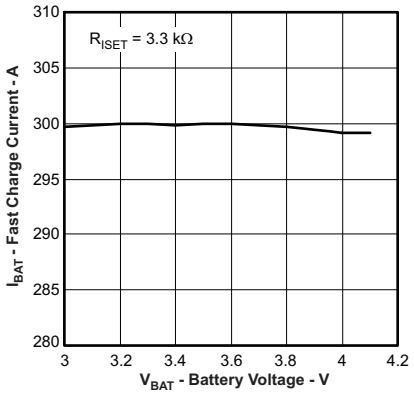


Figure 16.

PRECHARGE CURRENT vs BATTERY VOLTAGE

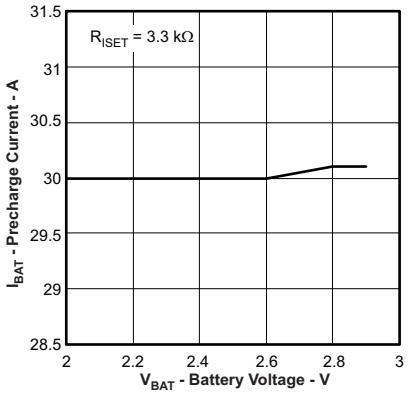


Figure 17.

APPLICATION CIRCUITS

V_{IN} = V_{UVLO} to V_{OVP} , $I_{FASTCHG}$ = 200 mA, $I_{IN(MAX)}$ = 500 mA, Battery Temperature Charge Range 0°C to 50°C, 6.25-hour Fast Charge Safety Timer.

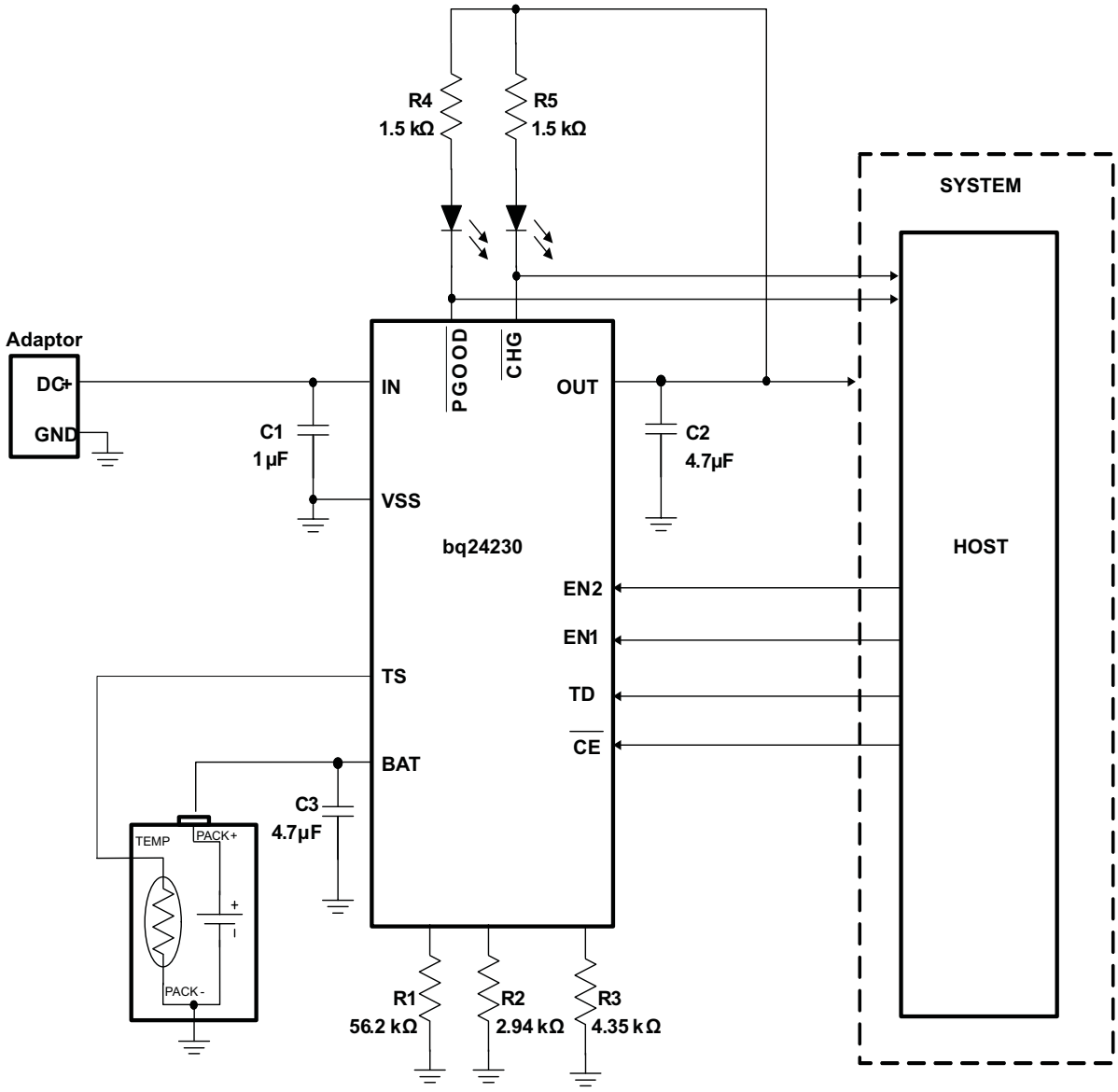


Figure 18. Using the bq24230 in a Host Controlled Charger Application

V_{IN} = V_{UVLO} to V_{OVP} , $I_{FASTCHG}$ = 200 mA, $I_{IN(MAX)}$ = 500 mA, 25-mA Termination Current, ISET mode (EN1=0, EN2=1), Battery Temperature Charge Range 0°C to 50°C, 6.25-hour Fast Charge Safety Timer.

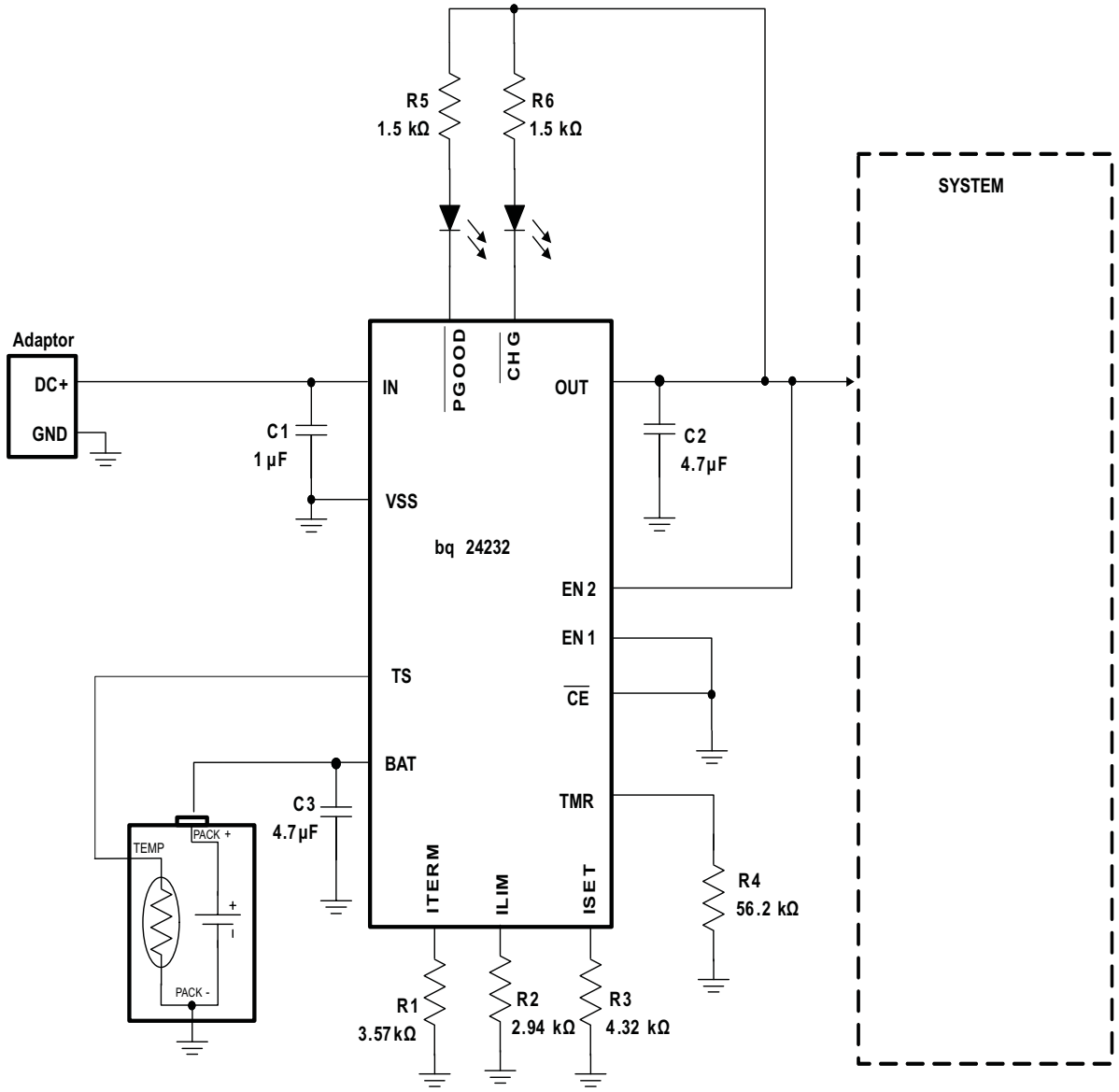


Figure 19. Using the bq24232 in a Stand-Alone Charger Application

EXPLANATION OF DEGLITCH TIMES AND COMPARATOR HYSTERESIS

Figures not to scale

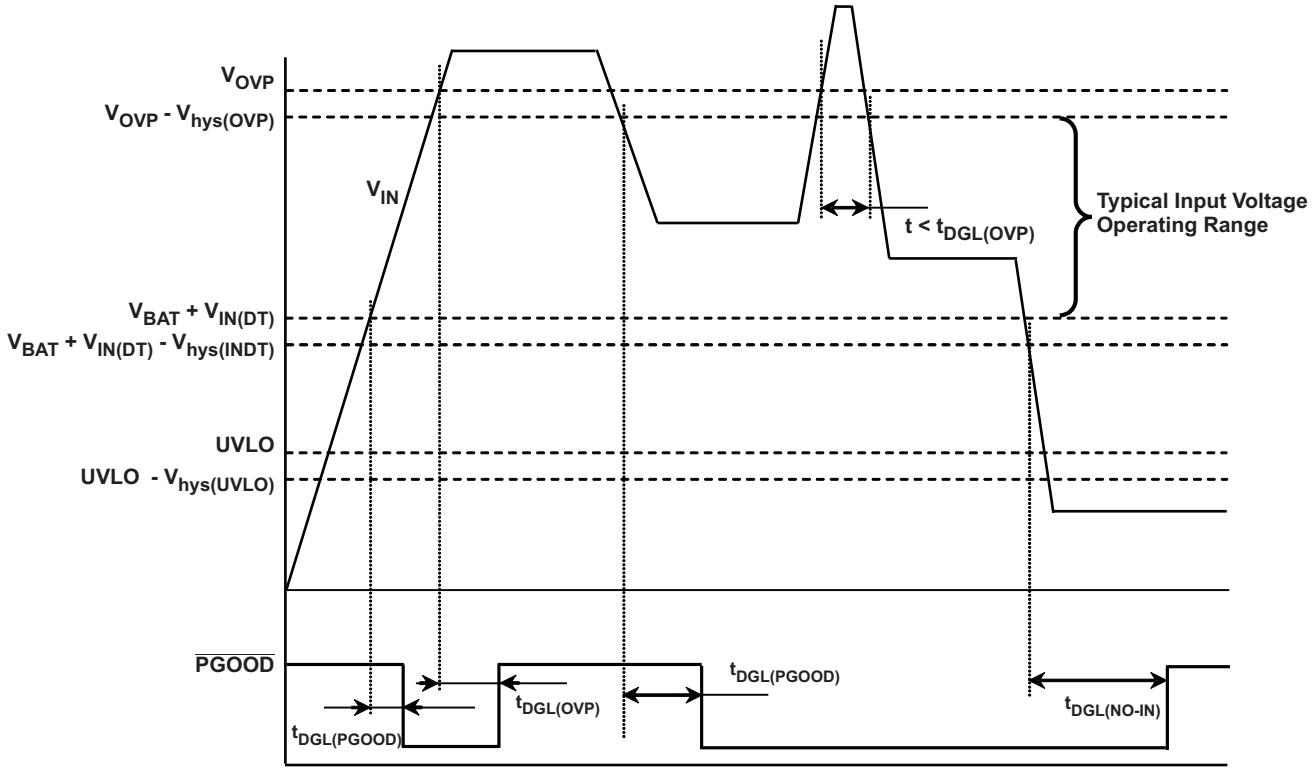


Figure 20. Power Up, Power Down

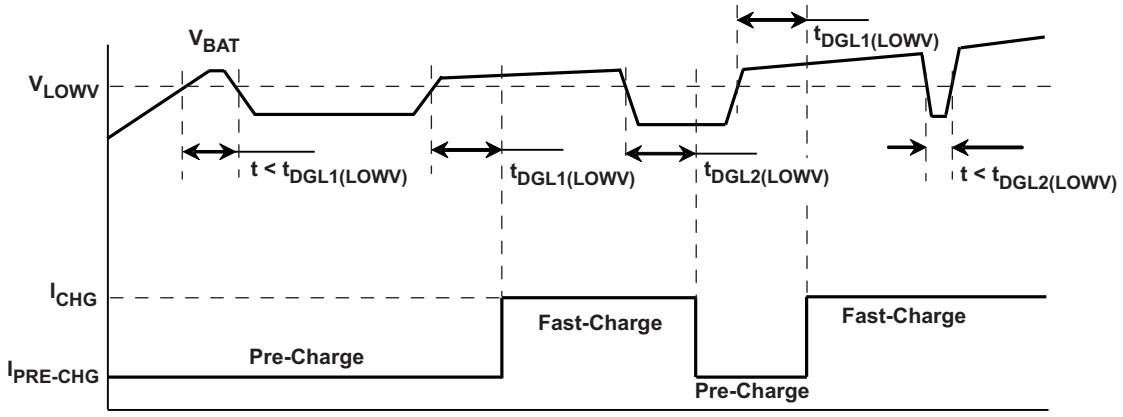


Figure 21. Pre- to Fast-Charge, Fast- to Precharge Transition – $t_{DGL1(LOWV)}$, $t_{DGL2(LOWV)}$

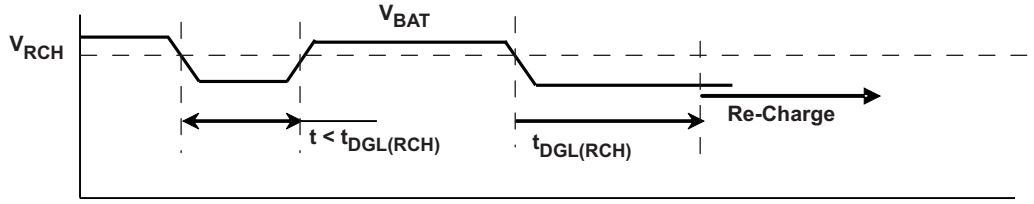


Figure 22. Recharge – $t_{DGL(RCH)}$

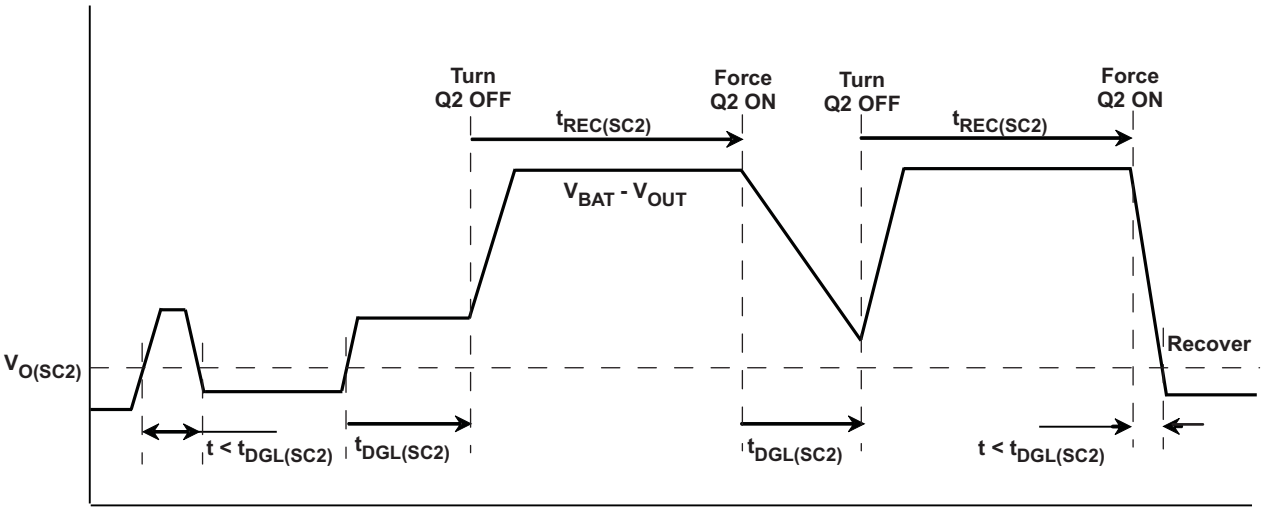


Figure 23. OUT Short-Circuit – Supplement Mode

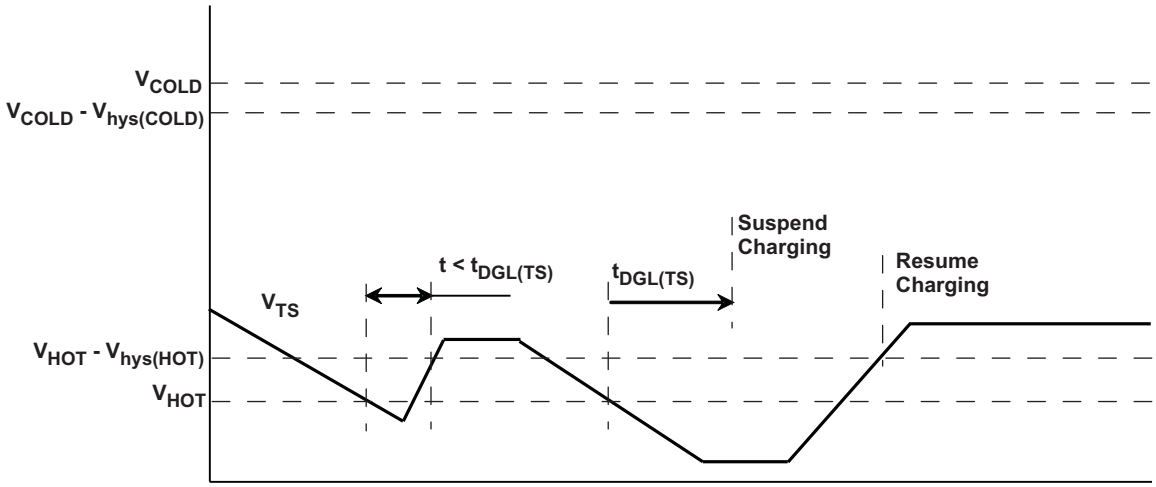


Figure 24. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing

DETAILED FUNCTIONAL DESCRIPTION

The bq2423x devices are integrated Li-ion linear chargers and system power-path management devices targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. It also allows instant system turnon even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power-path management (DPPM), which shares the source current between the system and battery charging and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN}-DPM) circuit reduces the input current limit if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

UNDERVOLTAGE LOCKOUT

The bq2423x family remains in power-down mode when the input voltage at the IN pin is below the undervoltage lockout (UVLO) threshold.

During the power-down mode, the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During power-down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

POWER ON

When V_{IN} exceeds the UVLO threshold, the bq2423x powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs ($\overline{CE}$, EN1, and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, $\overline{PGOOD}$ is low to indicate that the valid power status and the $\overline{CE}$, EN1, and EN2 inputs are read. The device enters standby mode whenever (EN1, EN2) = (1, 1) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON. (If SYSOFF is high, FET Q2 is off). During standby mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO **AND** V_{IN} > V_{BAT} + $V_{IN(DT)}$ **AND** V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)], all internal timers and other circuit blocks are activated. The device checks for short circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100-mA current limit to check for a short circuit at OUT. If V_{OUT} rises above V_{SC}, the FET Q1 switches to the current-limit threshold set by EN1, EN2, and R_{ILIM} and the device enters normal operation where the system is powered by the input source (Q1 is on), and the device continuously monitors the status of $\overline{CE}$, EN1, and EN2 as well as the input voltage conditions.

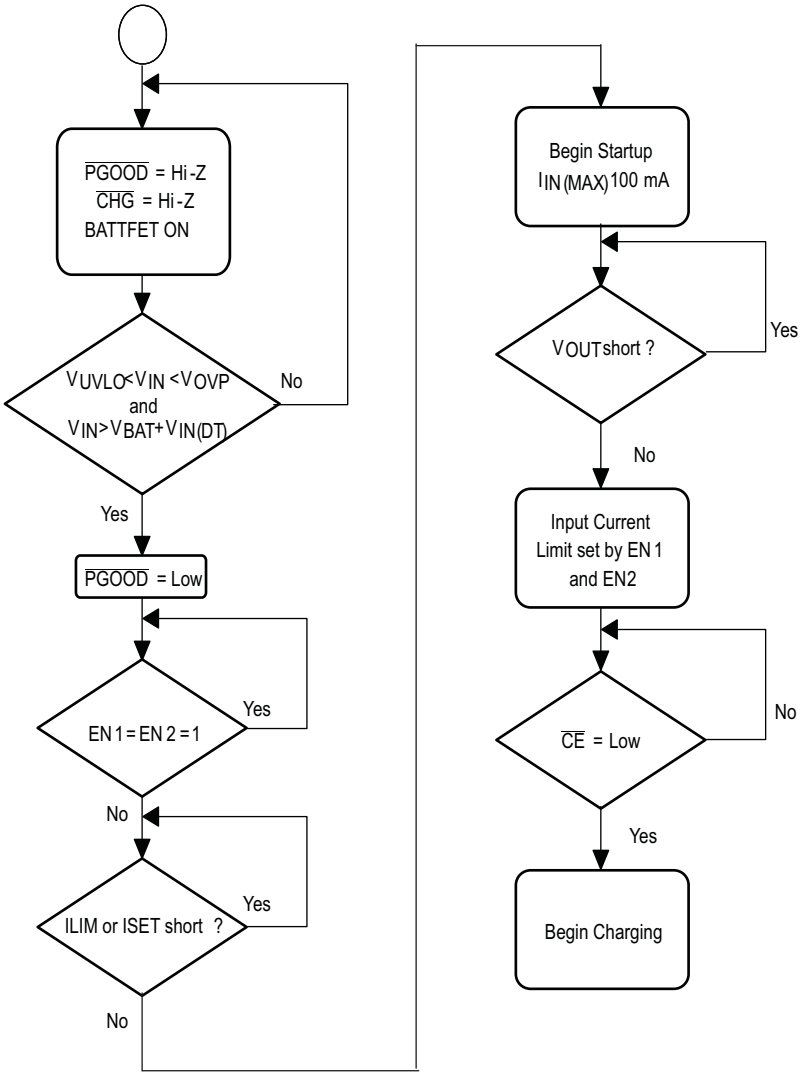


Figure 25. Start-up Flow Diagram

POWER-PATH MANAGEMENT

The bq2423x features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

INPUT SOURCE CONNECTED – ADAPTER or USB

With a source connected, the power-path management circuitry of the bq2423x monitors the input current continuously. The OUT output is regulated to a fixed voltage ($V_{O(REG)}$). The current into IN is shared between charging the battery and powering the system load at OUT. The bq2423x has internal selectable current limits of 100 mA (USB100) and 500 mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit.

The bq2423x is USB-IF compliant for the inrush current testing. The USB spec allows up to 10μF to be hard-started, which establishes a 50 μF as the maximum inrush charge value when exceeding 100 mA. The input current limit for the bq2423x prevents the input current from exceeding this limit, even with system capacitances greater than 10 μF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10 μF), as this current is not limited. Figure 26 demonstrates the startup of the bq2423x and compares it to the USB-IF specification.

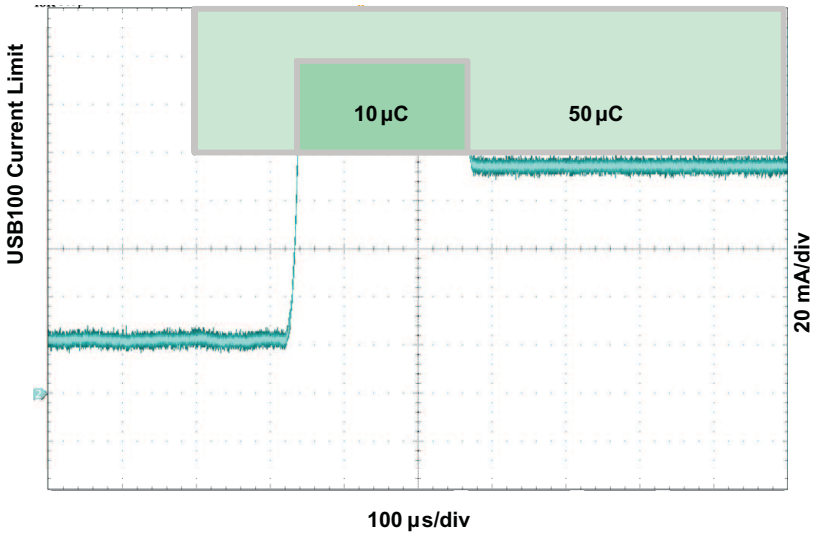


Figure 26. USB-IF Inrush Current Test

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS and is given by the equation:

$$I_{IN\text{-}MAX} = K_{ILIM}/R_{ILIM}$$

The input current limit is adjustable up to 500 mA. The valid resistor range is 3.2 kΩ to 8 kΩ.

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. Figure 27 illustrates examples of the DPPM and supplement modes. These modes are explained in detail in the following sections.

Input DPM Mode, V_{IN}-DPM

The bq2423x uses the V_{IN}-DPM mode for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2=0, EN1=0) or USB500 (EN2=0, EN2=1) modes, the input voltage is monitored. If V_{IN} falls to $V_{IN\text{-}DPM}$, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq2423x from crashing poorly designed or incorrectly configured USB sources.

DPPM Mode

When the sum of the charging and system load currents exceeds the preset maximum input current (programmed with EN1, EN2, and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPPM}, the bq2423x enters DPPM mode. In this mode, the charging current is reduced as the OUT current goes up in order to maintain the system output. Battery termination is disabled while in DPPM mode.

Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the battery voltage by V_{BSUP1}, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the OUT pin rises above the battery voltage by V_{BSUP2}.

During supplement mode, the battery supplement current is not regulated; however, a short-circuit protection circuit is built in. If during battery supplement mode, the voltage at OUT drops 250 mV below the BAT voltage, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short-circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

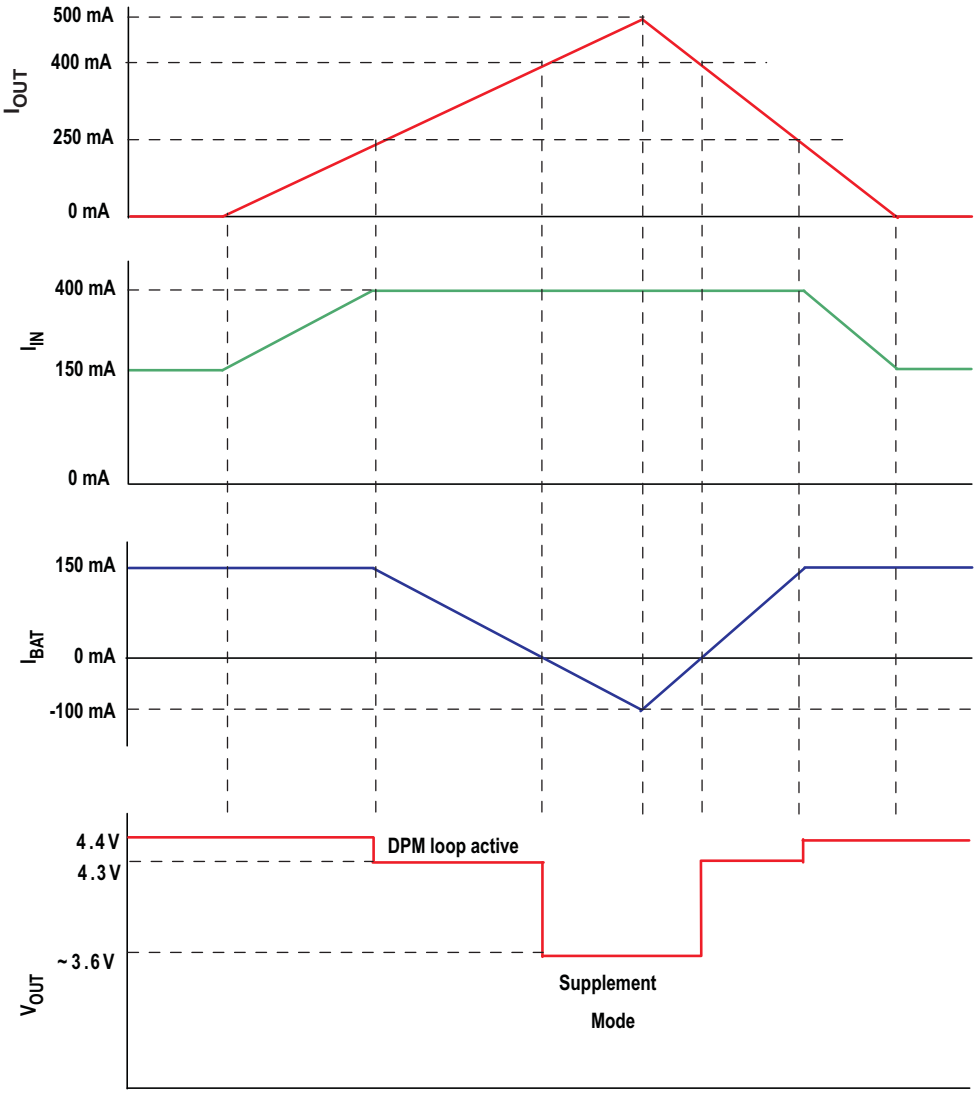


Figure 27. bq2423x DPPM and Battery Supplement Modes (V_{OREG} = 4.4 V, V_{BAT} = 3.6 V, I_{LIM}=400 mA, I_{CHG} = 150 mA)

INPUT SOURCE NOT CONNECTED

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode, the current into OUT is unregulated, similar to *Battery Supplement Mode*; however, the short-circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250 mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short-circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short-circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

BATTERY CHARGING

Set $\overline{CE}$ low to initiate battery charging. First, the device checks for a short circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning precharge, constant-current fast charge (current regulation), and a constant-voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 28 illustrates a normal Li-ion charge cycle using the bq2423x:

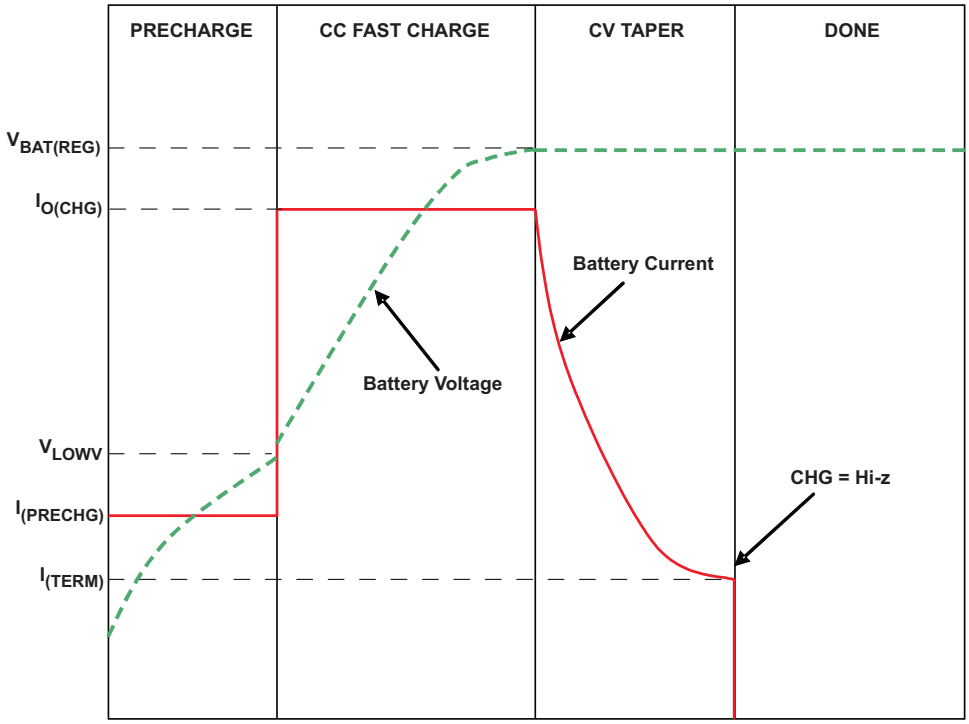


Figure 28.

In the precharge phase, the battery is charged with the precharge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop, or the $V_{IN(LOW)}$ loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation

$$I_{CHG} = K_{ISET}/R_{ISET}$$

The charge current limit is adjustable from 25 mA to 500 mA. The valid resistor range is 1.8 kΩ to 36 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery does not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers are proportionately slowed down.

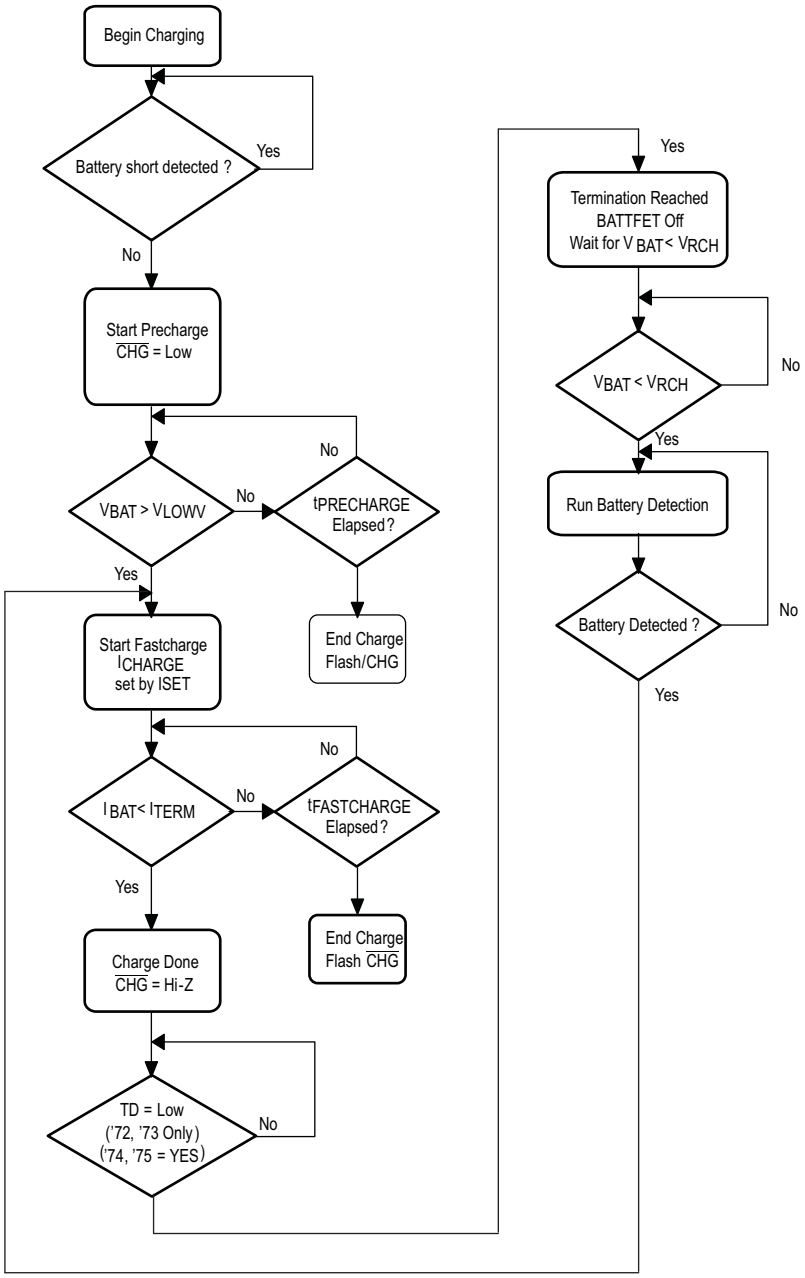


Figure 29. Battery Charging Flow Diagram

CHARGE CURRENT TRANSLATOR

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R_{ISET}, generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET}=(I_{CHARGE} / 400)\times R_{ISET} \quad (1)$$

BATTERY DETECTION AND RECHARGE

The bq2423x automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery detection routine is run. The detection routine first applies $I_{BAT(DET)}$ for t_{DET} to see if V_{BAT} drops below V_{LOWV}. If not, it indicates that the battery is still connected, but has discharged. If $\overline{CE}$ is low, the charger is turned on again to top off the battery. During this recharge cycle, the $\overline{CHG}$ output remains high-impedance as recharge cycles are not indicated by the $\overline{CHG}$ pin. If the BAT voltage falls below V_{LOWV} during the battery detection test, it indicates that the battery has been removed or the protector is open. Next, the precharge current is applied for t_{DET} to close the protector if possible. If the battery voltage does not rise above V_{RCH}, it indicates that the protector is closed, or a battery has been inserted, and a new charge cycle begins. If the voltage rises above V_{RCH}, the battery is determined missing and the detection routine continues. The battery detection runs until a battery is detected.

TERMINATION DISABLE (TD Input, bq24230)

The bq24230 contains a TD input that allows termination to be enabled/disabled. Connect TD to a logic high to disable charge termination. When termination is disabled, the device goes through the precharge, fast-charge, and CV phases, then remains in the CV phase. During the CV phase, the charger maintains the output voltage at BAT equal to $V_{BAT(REG)}$, and charging current does not terminate. BAT sources currents up to I_{CHG} or I_{IN-MAX}, whichever is less. Battery detection is not performed. The $\overline{CHG}$ output is high impedance once the current falls below I_{TERM} and does not go low until the input power or $\overline{CE}$ are toggled. When termination is disabled, the precharge and fast-charge safety timers are also disabled. Battery pack temperature sensing (TS pin functionality) is also disabled if the TD pin is high and the TS pin is unconnected.

ADJUSTABLE TERMINATION THRESHOLD (ITERM Input, bq24232)

The termination current threshold for the bq24232 is user-programmable. Set the termination current by connecting a resistor from ITERM to VSS. For USB100, mode (EN1 = EN2 = VSS), the termination current value is calculated as:

$$I_{TERM} = 0.01 \times R_{ITERM} / R_{ISET}$$

In the other input current limit modes (EN1 ≠ EN2), the termination current value is calculated as:

$$I_{TERM} = 0.03 \times R_{ITERM} / R_{ISET}$$

The termination current is programmable up to 50% of the fast-charge current. The R_{ITERM} resistor must be less than 15 kΩ. Leave ITERM unconnected to select the default internally set termination current.

DYNAMIC CHARGE TIMERS (TMR Input)

The bq2423x devices contain internal safety timers for the precharge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR}$$
$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR}$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation. For the bq24230, the timers are disabled when TD is connected to a high logic level.

During the fast-charge phase, several events increase the timer durations.

1. The system load current activates the DPPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half for two minutes, the timer clock is reduced to half the frequency and the counter counts half as fast resulting in only one minute of counted time.

STATUS INDICATORS ($\overline{PGOOD}$, $\overline{CHG}$)

The bq2423x contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when (V_{BAT} + $V_{IN(DT)}$) < V_{IN} < V_{OVP}. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The $\overline{CHG}$ output signals when a new charge cycle is initiated. After a charge cycle is initiated, $\overline{CHG}$ goes low once the battery is above the short-circuit threshold. $\overline{CHG}$ goes high impedance once the charge current falls below I_{TERM}. $\overline{CHG}$ remains high impedance until the input power is removed and reconnected or the $\overline{CE}$ pin is toggled. It does not signal subsequent recharge cycles.

Table 2. $\overline{PGOOD}$ STATUS INDICATOR

Input State	$\overline{PGOOD}$ Output
V_{IN} < V_{UVLO}	Hi impedance
V_{UVLO} < V_{IN} < $V_{IN(DT)}$ + V_{BAT}	Hi impedance
$V_{IN(DT)}$ + V_{BAT} < V_{IN} < V_{OVP}	Low
V_{IN} > V_{OVP}	Hi impedance

Table 3. $\overline{CHG}$ STATUS INDICATOR

Charge State	$\overline{CHG}$ Output
Charging	Low (first charge cycle)
Charging terminated	Hi impedance until power or $\overline{CE}$ is toggled
Recharging after termination	Hi impedance
Carging suspended by thermal loop	Low (first charge cycle)
Safety timers expired	Flashing at 2Hz
IC disabled or no valid input power	Hi impedance

TIMER FAULT

If the precharge timer expires before the battery voltage reaches V_{LOWV}, the bq2423x indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast-charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition.

THERMAL REGULATION AND THERMAL SHUTDOWN

The bq2423x contain a thermal regulation loop that monitors the die temperature. If the die temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a hiccup mode. Safety timers are slowed proportionally to the charge current in thermal regulation. Battery termination is disabled during thermal regulation and thermal shutdown.

Note that this feature monitors the die temperature of the bq2423x. This is not synonymous with ambient temperature. Self-heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO mode for OUT.

A modified charge cycle with the thermal loop active is shown in Figure 30:

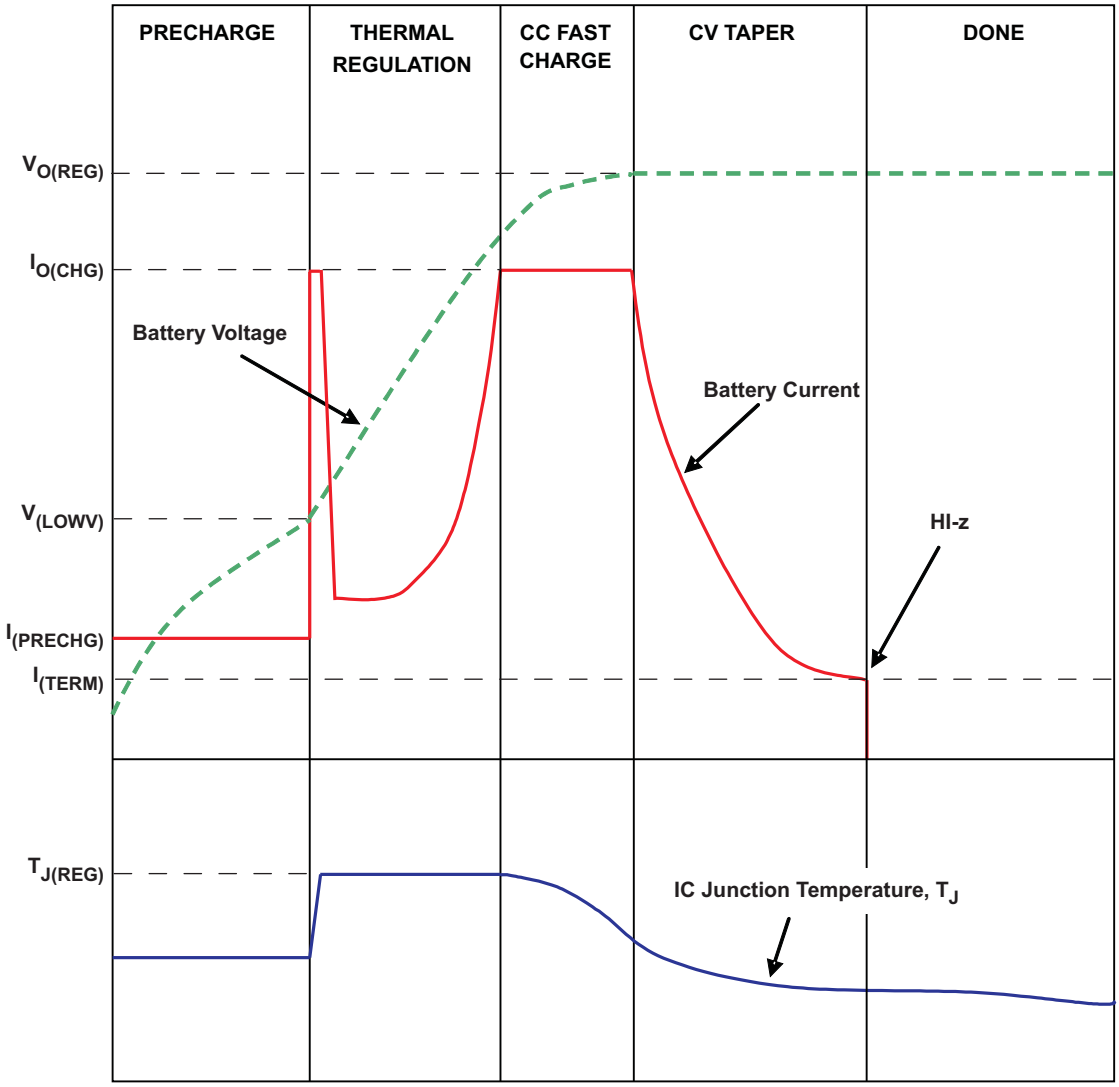


Figure 30.

BATTERY PACK TEMPERATURE MONITORING

The bq2423x features an external battery pack temperature monitoring input. The TS input connects to the NTC resistor in the battery pack to monitor battery temperature and prevent dangerous overtemperature conditions.

During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ pin remains low and continues to indicate *charging*.

For the bq24230, battery pack temperature sensing is disabled when termination is disabled (TD = High) and the voltage at TS is greater than $V_{DIS(TS)}$. The battery pack temperature monitoring is disabled in all devices by connecting a 10-kΩ resistor from TS to VSS.

The allowed temperature range for a 103AT-2 type thermistor is 0°C to 50°C. However, the user can increase the range by adding two external resistors. See Figure 31 for the circuit. The values for Rs and Rp are calculated using the following equations:

$$Rs = \frac{-(R_{TH} + R_{TC}) \pm \sqrt{\left((R_{TH}+R_{TC})^2 - 4\left\{R_{TH} \times R_{TC} + \frac{V_H \times V_C}{(V_H - V_C) \times I_{TS}} \times (R_{TC} - R_{TH})\right\}\right)}}{2} \quad (2)$$

$$Rp = \frac{V_H \times (R_{TH} + R_S)}{I_{TS} \times (R_{TH} + R_S) - V_H} \quad (3)$$

Where:

R_{TH}: Thermistor Hot Trip Value found in thermistor data sheet
R_{TC}: Thermistor Cold Trip Value found in thermistor data sheet
V_H: IC's Hot Trip Threshold = 0.3V nominal
V_C: IC's Cold Trip Threshold = 2.1V nominal
I_{TS}: IC's Output Current Bias = 75µA nominal
NTC Thermsitor Semitec 103AT-4

Rs and Rp 1% values were chosen closest to calculated values

Cold Temp Resistance and Trip Threshold; Ω (°C)	Hot Temp Resistance and Trip Threshold; Ω (°C)	External Bias Resistor, Rs (Ω)	External Bias Resistor, Rp (Ω)
28000 (–0.6)	4000 (51)	0	∞
28480 (–1)	3536 (55)	487	845000
28480 (–1)	3021 (60)	1000	549000
33890 (–5)	4026 (51)	76.8	158000
33890 (–5)	3536 (55)	576	150000
33890 (–5)	3021 (60)	1100	140000

RHOT and RCOLD are the thermistor resistance at the desired hot and cold temperatures, respectively. Note that the temperature window cannot be tightened more than using on the thermistor connected to TS, it can only be extended.

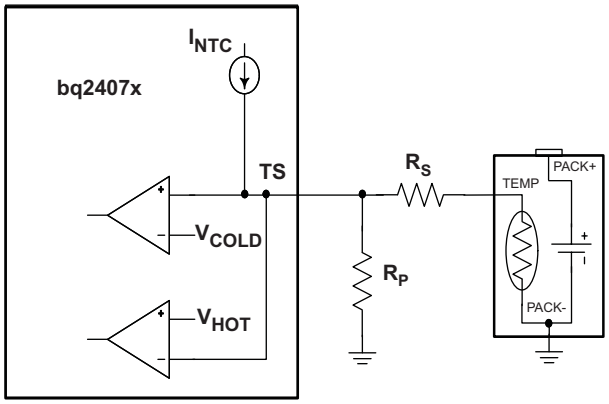


Figure 31. Extended TS Temperature Thresholds

APPLICATIONS INFORMATION

bq24232 CHARGER DESIGN EXAMPLE

See Figure 18 for the Design Example Schematic.

Requirements

- Supply voltage = 5 V
- Fast-charge current of approximately 200 mA; ISET - pin 16
- Input Current Limit =500 mA; ILIM - pin 12
- Termination Current = 25 mA - pin 15
- Safety timer duration, Fast charge = 6.25 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10 kΩ NTC (103AT-2)

Calculations

Program the Fast-Charge Current (ISET):

$R_{ISET} = K_{ISET} / I_{CHG}$
K_{ISET} = 870 AΩ from the electrical characteristics table.
R_{ISET} = 870 AΩ/0.2 A = 4.35kΩ

Select the closest standard value, which for this case is 4.32 kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

Program the Input Current Limit (ILIM)

$R_{ILIM} = K_{ILIM} / I_{I\_MAX}$
K_{ILIM} = 1470 AΩ from the electrical characteristics table.
R_{ISET} = 1470 AΩ / 0.5 A = 2.94 kΩ

Select the closest standard value, which for this case is 2.94 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

Program the Termination Current Threshold (ITERM)

$R_{ITERM} = R_{ISET} \times I_{TERM} / K_{ITERM}$

K_{ITERM} = 0.03 A from electrical characteristics table

R_{ITERM} = 4.32 kΩ × 0.025 A/0.03 A = 3.6 kΩ

Select the closest standard value, which for this case is 3.57 kΩ. Connect this resistor between ITERM (pin 15) and V_{SS}

Program 6.25-Hour Fast-Charge Safety Timer (TMR)

$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$
K_{TMR} = 40 s/kΩ from the electrical characteristics table.
R_{TMR} = (6.25 hr × 3600 s/hr) / (10 × 40 s/kΩ) = 56.25 kΩ

Select the closest standard value, which for this case is 56.2 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

TS Function

Use a 10-kΩ NTC thermistor in the battery pack (103AT). To disable the temperature sense function, use a fixed 10-kΩ resistor between the TS (pin 1) and V_{SS}. Pay close attention to the linearity of the chosen NTC so that it provides the desired hot and cold turnoff thresholds.

$\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$

LED Status: connect a 1.5-kΩ resistor in series with a LED between OUT and $\overline{\text{CHG}}$ and OUT and $\overline{\text{PGOOD}}$.

Processor Monitoring Status: connect a pullup resistor (approximately 100 kΩ) between the processor's power rail and $\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$.

SELECTING IN, OUT, AND BAT PIN CAPACITORS

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output, and battery pins. Using the values shown on the application diagram is recommended. After evaluation of these voltage signals with real system operational conditions, the user can determine if capacitance values can be adjusted toward the minimum recommended values (dc load application) or higher values for fast, high-amplitude, pulsed load applications. ???Note if designed high input voltage sources (bad adapters or wrong adapters), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

THERMAL PACKAGE

The bq2423x is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed-circuit board (PCB). The power pad must be directly connected to the Vss pin. Full PCB design guidelines for this package are provided in the application report entitled: QFN/SON PCB Attachment (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T) / P$$

Where:

T_J = chip junction temperature

T = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

1. Whether the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-ion batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically, after fast charge begins, the pack voltage increases to ~3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is easy to verify, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad must have multiple vias), the charge current and the battery voltage as a function of time. The fast-charge current starts to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} – V_{(BAT)}] \times I_{(BAT)}$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for nontypical situations such as hot environments or higher than normal input source voltage. With that said, the IC still performs as described, if the thermal loop is always active.

Half-Wave Adapters

Some low-cost adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with low-cost adapters under those conditions, the bq2407x family keeps the charger on for at least 20 ms (typical) after the input power puts the part in sleep mode. This feature enables use of external low-cost adapters using 50-Hz networks.

Sleep Mode

After entering sleep mode for >20 ms, the internal FET connection between the IN and OUT pin is disabled and pulling the input to ground does not discharge the battery, other than the leakage on the BAT pin. If the user has a full 1000-mAHr battery and the leakage is 10 μA, then it takes 1000 mAHr/10 μA = 100000 hours (11.4 years) to discharge the battery. The battery's self-discharge is typically 5 times higher.

Layout Tips

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) must be placed as close as possible to the bq2423x, with short trace runs to both IN, OUT, and GND (thermal pad).
- All low-current GND connections must be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into the IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq2423x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed-circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application report entitled: QFN/SON PCB Attachment (SLUA271).

REVISION HISTORY

Changes from Revision B (March 2009) to Revision C	Page
• Changed globally RT1 amd RT2 to Rs and Rp	24
• Added equations 2 and 3, term explanations and resistance table.	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24230RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGN	Samples
BQ24230RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGN	Samples
BQ24230RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGN	Samples
BQ24230RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CGN	Samples
BQ24232RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NXK	Samples
BQ24232RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NXK	Samples
BQ24232RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NXK	Samples
BQ24232RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NXK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

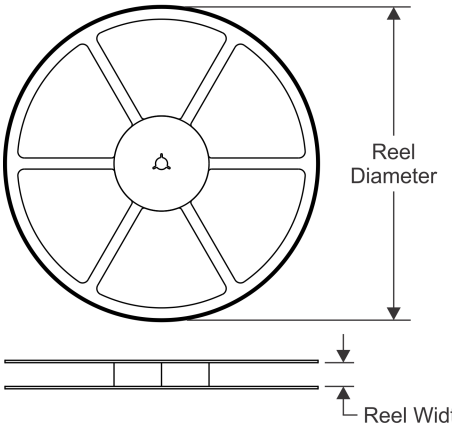
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

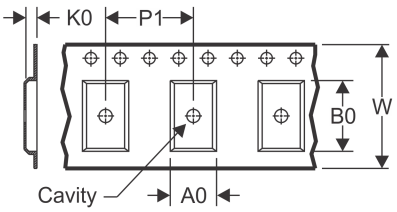
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

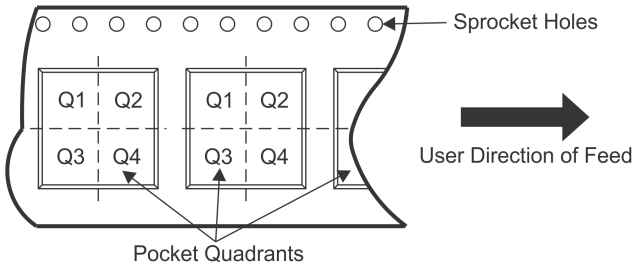


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

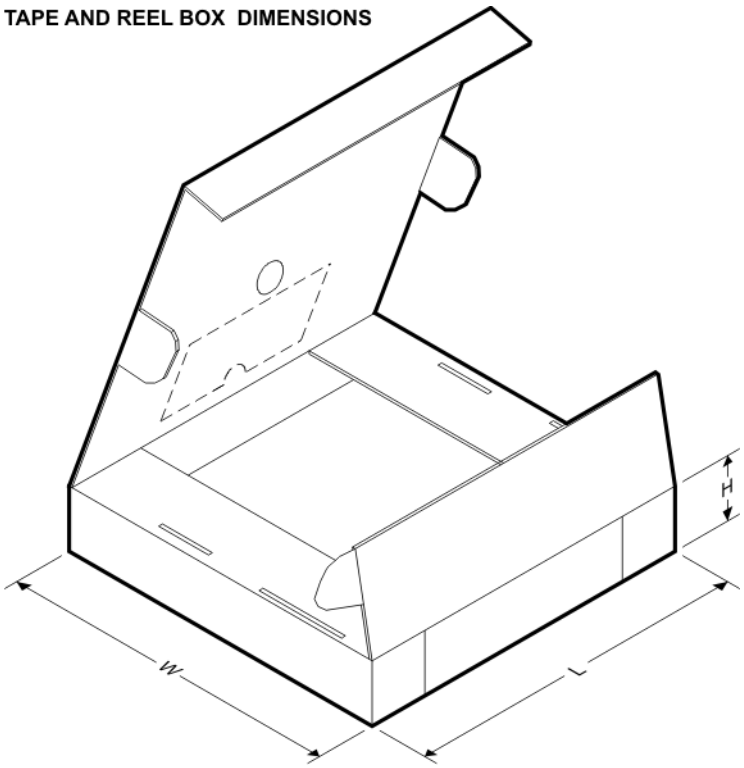
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24230RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24230RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24232RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24232RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24232RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

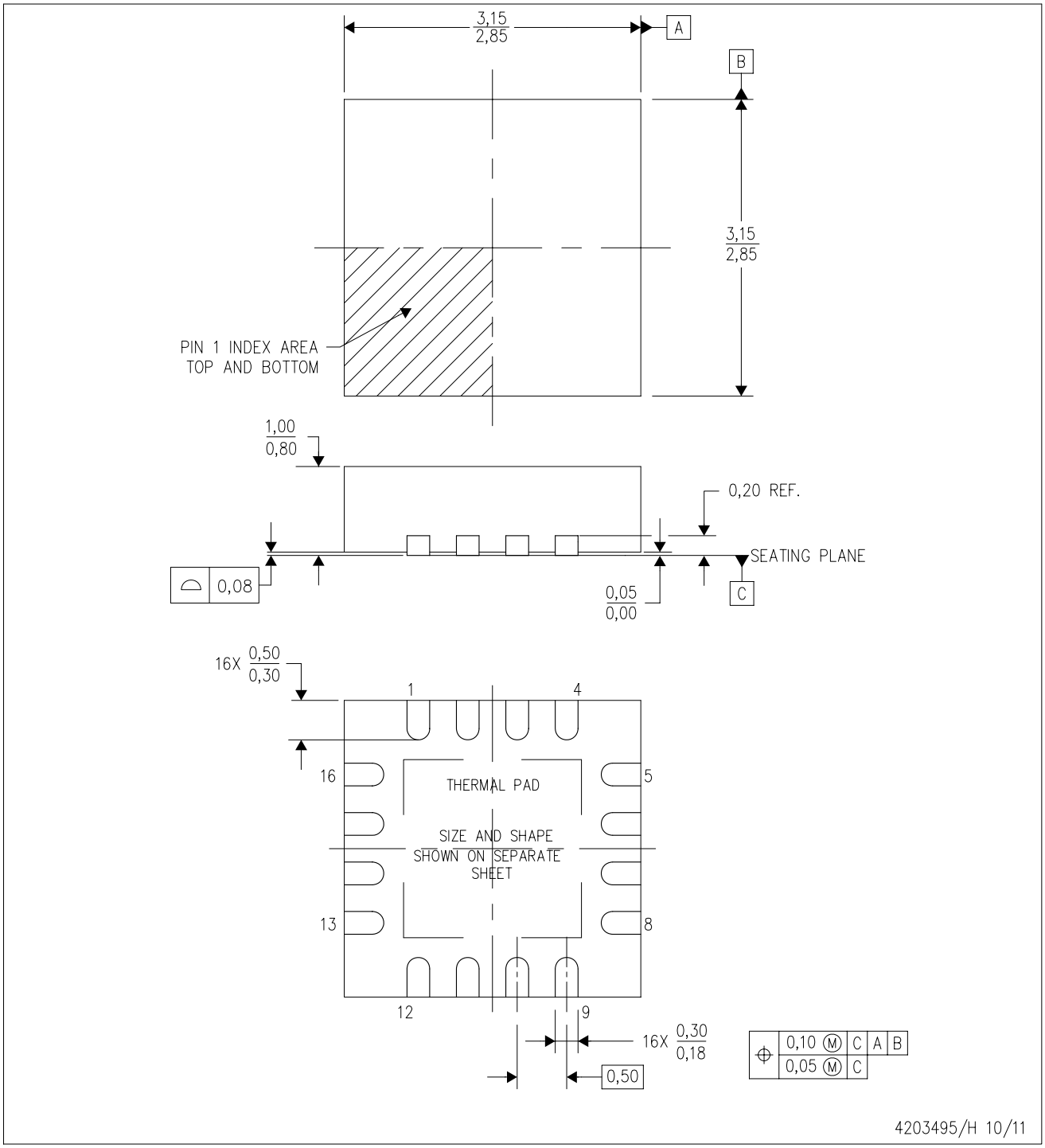
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24230RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24230RGTT	QFN	RGT	16	250	210.0	185.0	35.0
BQ24232RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24232RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24232RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

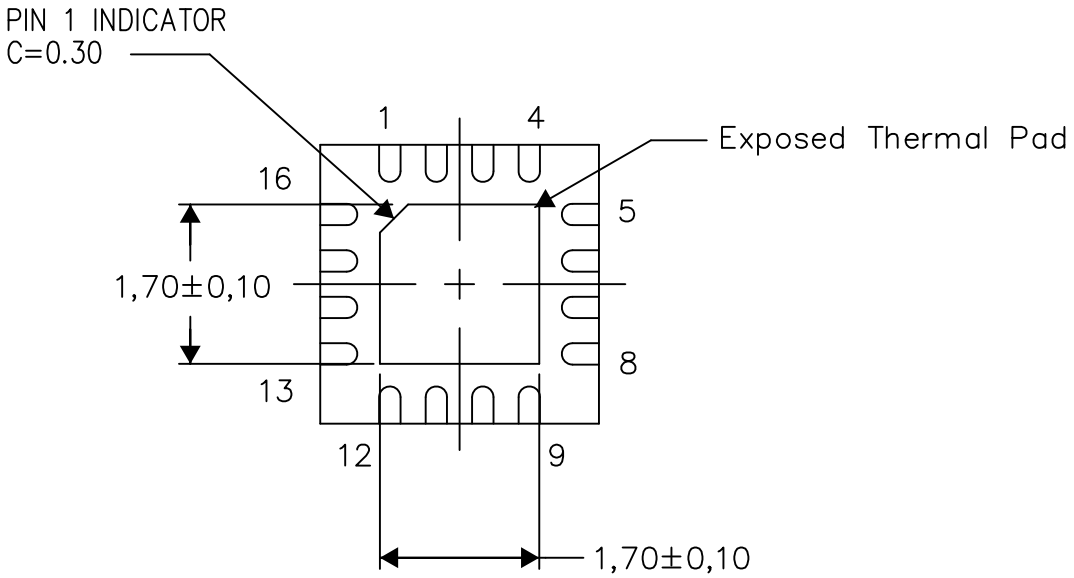
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



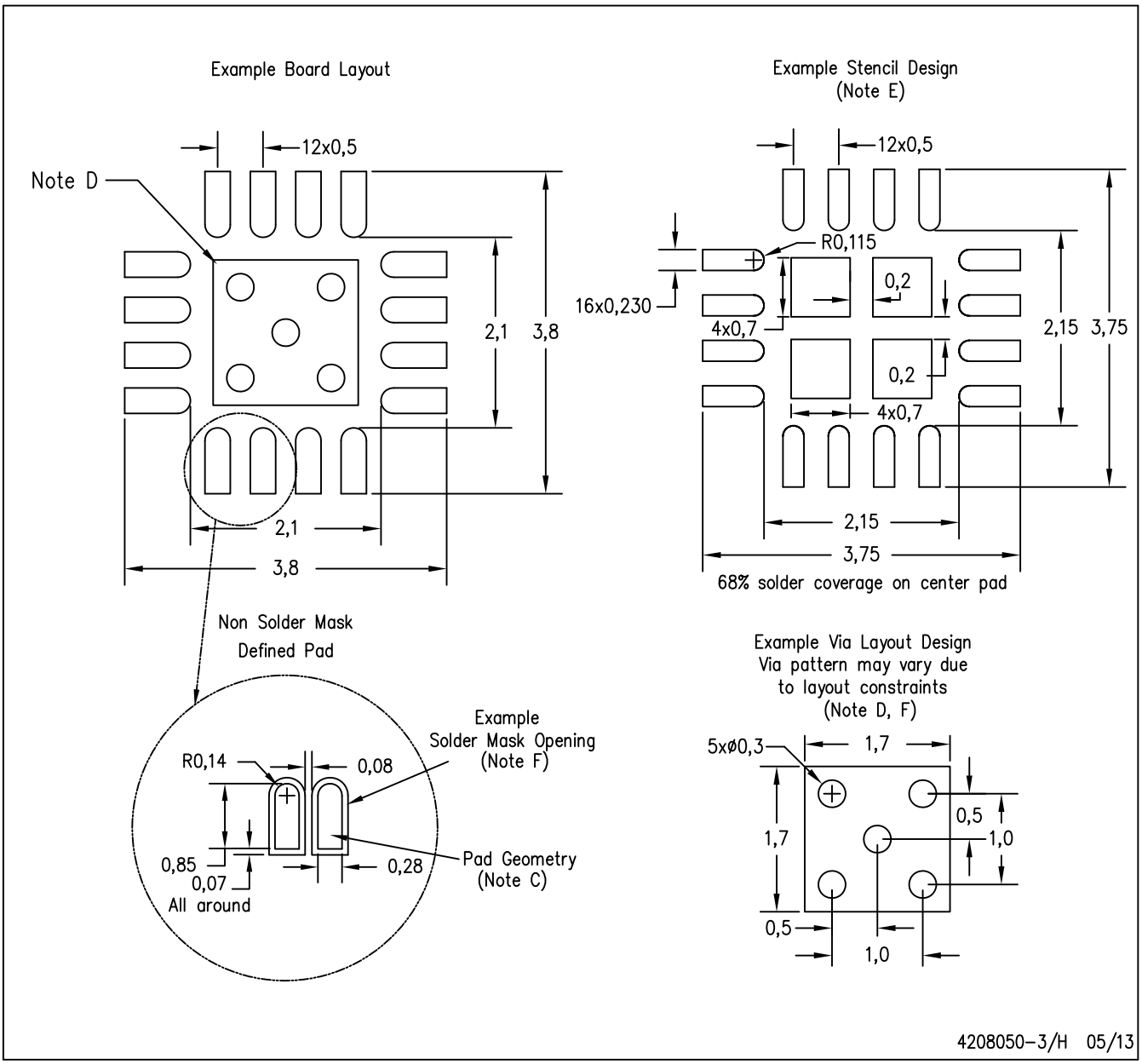
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/T 05/13

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

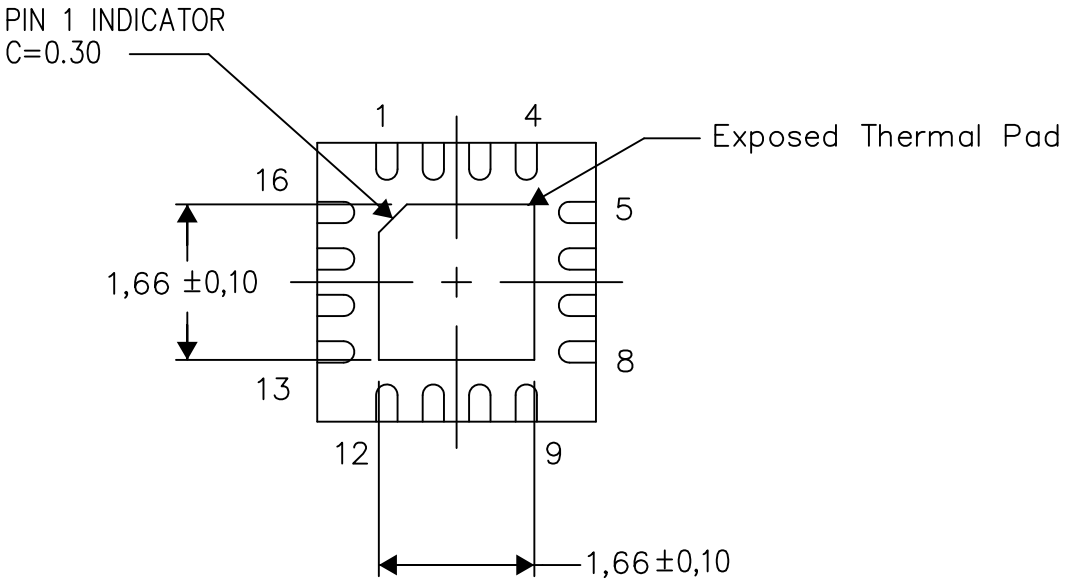
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–9/T 05/13

NOTE: All linear dimensions are in millimeters

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