

# 12-V/3.3-V Hot Swap and ORing Controller with Load Current Monitor for AdvancedMC™

 Check for Samples: [TPS2458](#)

## FEATURES

- ATCA AdvancedMC™ Compliant
- Full Power Control for an AdvancedMC™ Module
- Programmable 12-V Current Limit and Fast Trip
- Optional 12-V ORing Control for MicroTCA™
- Internal 3.3-V Current Limit
- Programmable Shunt Gain
- Interlock Requires 3.3-V Output Prior to 12 V
- 12-V and 3-V Power Good and Fault Outputs
- Load Current Monitor
- 32-Pin PQFN Package

## APPLICATIONS

- ATCA Carrier Boards
- MicroTCA™ Power Modules
- AdvancedMC™ Slots
- Systems Using 12 V and 3.3 V
- Base Stations

## DESCRIPTION

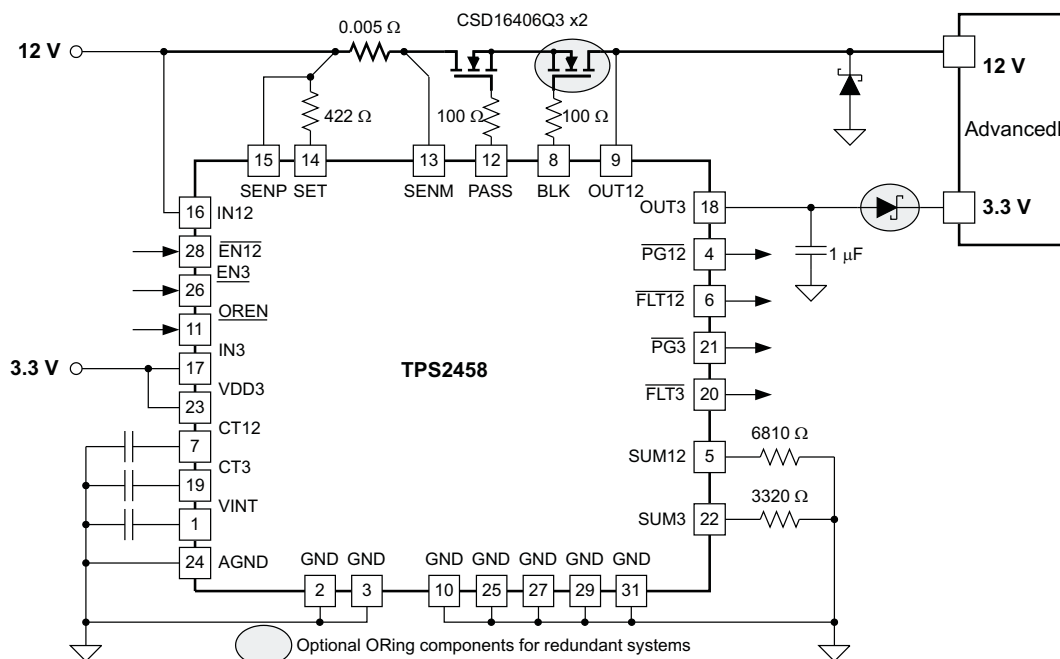
The TPS2458 AdvancedMC™ slot controller is fully compliant with the AdvancedMC™ Standard and provides the required accuracy to meet the demands of an AdvancedMC™ (Advanced Mezzanine Card) module.

The TPS2458 is an extremely flexible solution that protects both the power supply and the load by limiting the maximum current into the load and shutting off in case of a fault. If a severe fault occurs the current shuts off immediately.

Optional ORing support is inherent in the architecture and can be used in MicroTCA™, or other applications requiring ORing support.

The 3.3-V management channel is internal and requires only one external resistor for load monitoring and one external capacitor to set fault time. To comply with the AdvancedMC™ requirements, the 12-V output is disabled unless the 3.3-V Power Good signal is asserted. Load current monitors are provided for both the 12 V and 3.3 V channels. Status outputs include Power Good and Fault indicators for each channel. The TPS2458 is in a 32-pin PQFN package.

## TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**ORDERING INFORMATION**

DEVICE	TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS2458	-40°C to 85°C	QFN32	TPS2458RHB	TPS2458

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
PASS, BLK		-0.3 to 30	V
IN12, OUT12, SENP, SENM, SET, $\overline{\text{EN12}}$ , $\overline{\text{FLT}}_x$ , $\overline{\text{PG}}_x$ , $\overline{\text{OREN}}$		-0.3 to 17	
IN3, OUT3, EN3, VDD, CTx, SUMx		-0.3 to 5	
AGND, GND		-0.3 to 0.3	
ESD	Human Body Model	2	kV
	Charged Device Model	0.5	
$\overline{\text{FLT}}_x$ , $\overline{\text{PG}}_x$		5	mA
SUMx		5	
VINT		-1 to 1	
OUT3		250	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under any conditions beyond those indicated under recommended operating conditions is neither implied nor guaranteed. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

**DISSIPATION RATINGS**

PACKAGE	$\theta_{JA}$ – High-k (°C/W)
QFN32 - RHB	50

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
VIN12	12 V input supply	8.5	12	15	V
VIN3	3.3 V input supply	3	3.3	4	
VVDD3	3.3 V input supply	3	3.3	4	
IOUT3	3.3 V output current			165	mA
ISUMx	Summing pin current		100	1000	$\mu$ A
	PASS pin board leakage current	-1		1	
	VINT bypass capacitance	1	10	250	nF
T <sub>J</sub>	Operating junction temperature range	-40		125	°C

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ENABLE INPUTS</b>					
Threshold voltage, falling edge		1.2	1.3	1.4	V
Hysteresis		20	50	80	mV
Pullup current	$V_{\overline{EN}} = V_{\overline{OREN}} = 0\text{ V}$	5	8	15	$\mu\text{A}$
Input bias current	$V_{\overline{EN12}} = V_{\overline{OREN}} = 17\text{ V}$		6	15	
Input bias current	$V_{\overline{EN3}} = 5\text{ V}$		1	5	$\mu\text{s}$
3.3 V Turn off time	$\overline{EN3}$ deasserts to $V_{VOUT3} < 1.0\text{ V}$ , $C_{OUT} = 0\text{ }\mu\text{F}$			10	
12 V Turn off time	$\overline{EN12}$ deasserts to $V_{VOUT12} < 1.0\text{ V}$ , $C_{OUT} = 0\text{ }\mu\text{F}$ , $C_{QGATE} = 35\text{ nF}$			20	
<b>POWER GOOD OUTPUTS</b>					
Low voltage	Sinking 2 mA		0.14	0.25	V
Leakage current	$V_{\overline{PG}} = 17\text{ V}$			1	mA
Threshold voltage	$\overline{PG12}$ , falling VOUT12	10.2	10.5	10.8	V
	$\overline{PG3}$ , falling VOUT3	2.7	2.8	2.9	
Hysteresis	$\overline{PG12}$ , measured at OUT12		130		mV
	$\overline{PG3}$ , measured at OUT3		50		
Deglintch time	$\overline{PG3}$ falling	50	100	150	$\mu\text{s}$
<b>FAULT OUTPUTS</b>					
Low voltage	Sinking 2 mA		0.14	0.25	V
Leakage current	$\overline{FLT_x} = 17\text{ V}$			1	$\mu\text{A}$
<b>VINT</b>					
Output voltage	$0\text{ V} < I_{VINT} < 50\text{ mA}$	2	2.3	2.8	V
<b>FAULT TIMER</b>					
Sourcing current	$V_{VCT_x} = 0\text{ V}$ , during fault	-7	-10	-13	$\mu\text{A}$
Sinking current	$V_{VCT_x} = 2\text{ V}$	7	10	13	
Upper threshold voltage		1.3	1.35	1.4	V
Lower threshold voltage		0.33	0.35	0.37	
<b>12-V SUMMING NODE</b>					
Input referred offset	$10.8\text{ V} \leq V_{\text{SENEM}} \leq 13.2\text{ V}$ , $V_{\text{SENP}} = (V_{\text{SENEM}} + 50\text{ mV})$ , measure $V_{\text{SET}} - V_{\text{SENEM}}$	-1.5		1.5	mV
Summing threshold	$V_{\text{PASS}} = 15\text{ V}$	0.66	0.675	0.69	V
Leakage current	$V_{\text{SET}} = (V_{\text{SENEM}} - 10\text{ mV})$			1	$\mu\text{A}$
<b>12-V CURRENT LIMIT</b>					
Current limit threshold	$R_{\text{SUM}} = 6.8\text{ k}\Omega$ , $R_{\text{SET}} = 422\text{ }\Omega$ , increase $I_{\text{LOAD}}$ and measure $V_{\text{SENP}} - V_{\text{SENEM}}$ when $V_{\text{PASS}} = 15\text{ V}$	47.5	50	52.5	mV
Sink current in current limit	$I_{\text{PASS}}$ measured at $V_{\text{SUM}} = 1\text{ V}$ and $V_{\text{PASS}} = 12\text{ V}$	20		40	$\mu\text{A}$
Fast trip threshold	Measure $V_{\text{SENP}} - V_{\text{SENEM}}$	80	100	120	mV
Fast turn-off delay	20 mV overdrive, $C_{\text{PASS}} = 0\text{ pF}$ , tp50-50		200	300	ns
Timer start threshold	$V_{\text{PASS}} - V_{\text{IN}}$ when timer starts, while $V_{\text{PASS}}$ falling due to overcurrent	5	6	7	V

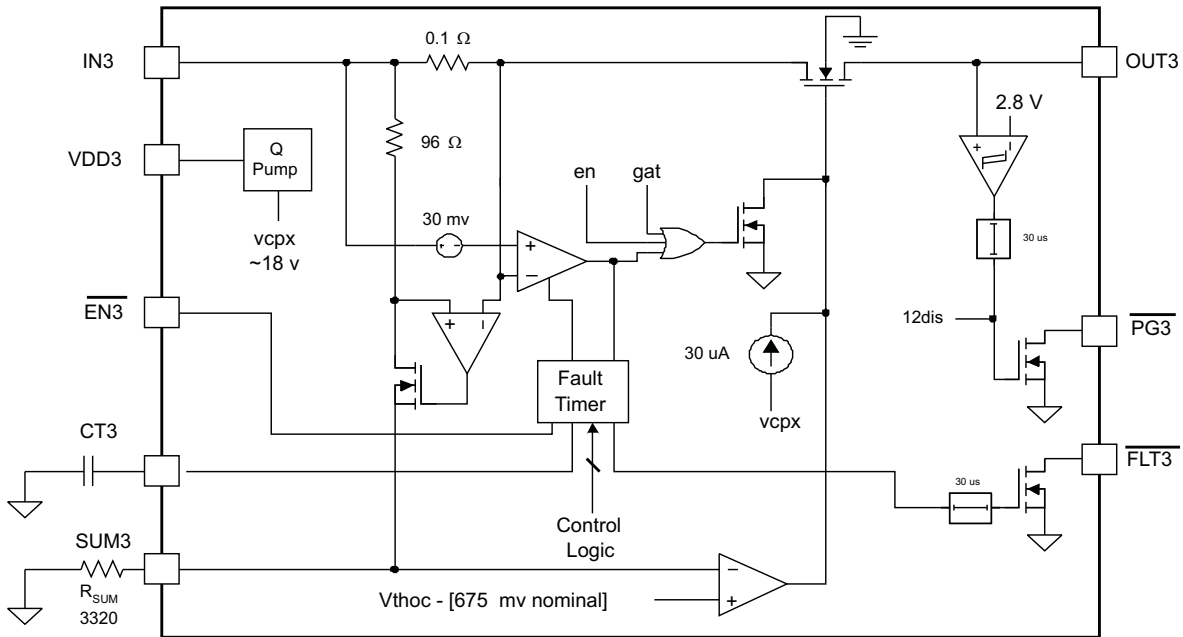
**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

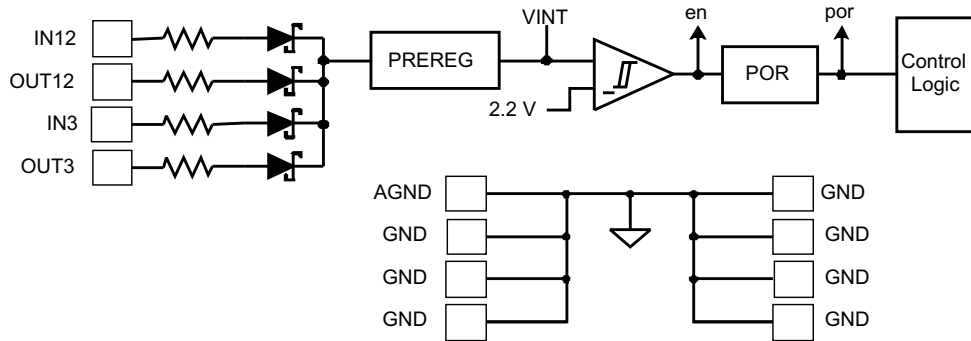
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>12-V UVLO</b>					
UVLO rising	IN12 rising	8.1	8.5	8.9	V
UVLO hysteresis	IN12 falling	0.44	0.5	0.59	
<b>12-V BLOCKING</b>					
Turn-on threshold	Measure $V_{SENP} - V_{VOUT}$	5	10	15	mV
Turn-off threshold	Measure $V_{SENP} - V_{VOUT}$	-6	-3	0	
Turn-off delay	20-mV overdrive, $C_{BLK} = 0$ pF, $t_{P50-50}$		200	300	ns
<b>12-V GATE DRIVERS (PASS, BLK)</b>					
Output voltage	$V_{VIN12} = V_{VOUT12} = 10$ V	21.5	23	24.5	V
Sourcing current	$V_{VIN12} = V_{VOUT12} = 10$ V, $V_{PASS} = V_{BLK} = 17$ V	20	30	40	$\mu$ A
Sinking current	Fast turnoff, $V_{PASS} = V_{BLK} = 14$ V	0.5	1		A
	$4$ V $\leq V_{PASS} = V_{BLK} \leq 25$ V	6	14	25	mA
Pulldown resistance	In OTSD ( at 150°C )	14	20	26	k $\Omega$
Fast turn-off duration		5	10	15	$\mu$ s
Safety gate pulldown	IRF3710, slew S or D 15 V in 1mS			1.25	V
Disable delay	EN12 pin to PASS and BLK, $t_{P50-90}$			1	$\mu$ s
Startup time	IN12 rising to PASS and BLK sourcing			0.25	ms
<b>3.3-V SUMMING NODE</b>					
Summing threshold		655	675	695	mV
<b>3.3-V CURRENT LIMIT</b>					
On-resistance	$I_{OUT3} = 150$ mA		290	500	m $\Omega$
Current limit	$R_{SUM3} = 3.3$ k $\Omega$ , $V_{VOUT3} = 0$ V	170	195	225	mA
Fast trip threshold		240	300	400	
Fast turn-off delay	$I_{OUT3} = 400$ mA, $t_{P50-50}$		750	1300	ns
<b>3.3-V UVLO</b>					
UVLO rising	IN3 rising	2.65	2.75	2.85	V
UVLO hysteresis	IN3 falling	200	240	300	mV
Safety gate pulldown1	Slew IN3x, OUT3x 5 V in 1 ms			15	mA
<b>SUPPLY CURRENTS</b>					
Both channels enabled	$I_{OUT3} = 0$		3.1	4	mA
Both channels disabled			2	2.8	
<b>THERMAL SHUTDOWN</b>					
Whole-chip shutdown temperature	$T_J$ rising, $I_{OUT3} = 0$	140	150		$^{\circ}$ C
3.3-V channel shutdown temperature	$T_J$ rising, $I_{OUT3}$ in current limit	130	140		
Hysteresis	Whole chip or 3.3-V channel		10		



3.3-V Channel Circuitry



Circuitry Common to Both Channels



DEVICE INFORMATION

TPS2458  
(Top View)

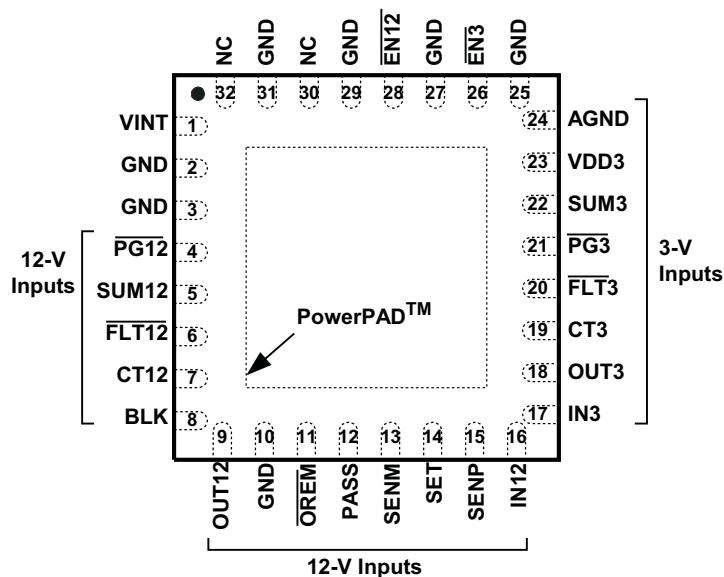


Figure 1.

TERMINAL FUNCTIONS

NAME	NO.	I/O	
AGND	24	—	Analog ground. Ground pin for the analog circuitry inside Bypass capacitor connection point for internal supply the TPS2458.
BLK	8	O	12-V blocking transistor gate drive. Gate drive pin for the 12-V channel BLK FET. This pin sources 30 $\mu$ A to turn the FET on. An internal clam prevents this pin from rising more than 14.5 V above OUT12. Setting the OREN pin high holds the BLK pin low.
CT12	7	I/O	12-V fault timing capacitor. A capacitor from CT12 to GND sets the time the channel can remain in current limit before it shuts down and declares a fault. Current limit causes this pin to source 10 $\mu$ A into the external capacitor (CT). When $V_{CT12}$ reaches 1.35 V, the TPS2458 shuts the channel off by pulling the FET gate low and declares an overcurrent fault by pulling the FLT12 pin low
CT3	19	I/O	3-V fault timing capacitor. A capacitor from CT3 to GND sets the time the channel can remain in current limit before it shuts down and declares a fault. Current limit causes this pin to source 10 $\mu$ A into the external capacitor (CT). When $V_{CT3}$ reaches 1.35 V, the TPS2458 shuts the channel off by pulling the FET gate low and declares an overcurrent fault by pulling the FLT3 pin low.
$\overline{EN12}$	28	I	12-V enable. (active low). Pulling this pin high (or allowing it to float high) turns off the 12-V channel by pulling both BLK and PASS low. An internal 200-k $\Omega$ resistor pulls this pin up to VINT when disconnected.
$\overline{EN3}$	26	I	3-V enable. (active low) Pulling this pin high (or allowing it to float high) turns off the 3-V channel by pulling the gate of the internal pass FET to GND. An internal 200-k $\Omega$ resistor pulls this pin up to VINT when disconnected.
$\overline{FLT12}$	6	O	12-V fault output (active low) Open-drain output indicating that channel 12 has remained in current limit long enough to time out the fault timer and shut the channel down. asserted when 12-V fault timer runs out
$\overline{FLT3}$	20	O	3-V fault output (active low) Open-drain output indicating that channel 3 has remained in current limit long enough to time out the fault timer and shut the channel down. asserted when 3-V fault timer runs out

**TERMINAL FUNCTIONS (continued)**

GND	2	—	Ground connections.
	3		
	10		
	25		
	27		
	29		
	31		
IN3	17	I	3-V input. Supply pin for the 3-V channel internal pass FET.
IN12	16	I	12-V input. Supply pin for 12-V channel internal circuitry.
$\overline{\text{OREN}}$	11	I	12-V blocking transistor enable. (active low). Pulling this pin low allows the 12-V channel ORing function to operate normally. Pulling this pin high (or allowing it to float high) disables the 12-V ORing function by pulling the BLK pin low. An internal 200-k $\Omega$ resistor pulls this pin up to VINT when disconnected.
OUT12	9	I/O	12-V output. Senses the output voltage of the 12-V channel.
OUT3	18	I/O	3-V output. Output of the 3-V channel internal pass FET.
PASS	12	O	12-V pass transistor gate drive. This pin sources 30 $\mu\text{A}$ to turn the FET on. An internal clamp prevents this pin from rising more than 14.5 V above IN12.
$\overline{\text{PG12}}$	4	O	12-V power good output, asserts when $V_{\text{OUT12}} > V_{\overline{\text{PG12}}}$ ( active low) . Open-drain output indicating that channel 12 output voltage has dropped below the PG threshold, which nominally equals 10.5 V.
$\overline{\text{PG3}}$	21	O	3-V power good output, asserts when $V_{\text{OUT3}} > 2.8 \text{ V}$ ( active low) . Open-drain output indicating that channel 3 output voltage has dropped below the PG threshold, which nominally equals 2.85 V.
SENM	13	I	12-V current limit sense. Senses the voltage on the low side of the 12-V channel current sense resistor.
SENP	15	I	12-V input sense. Senses the voltage on the high side of the 12-V channel current sense resistor.
SET	14	I	12-V current limit set. A resistor connected from this pin to SENP sets the current limit level in conjunction with the current sense resistor and the resistor connected to the SUM12 pin, as described in 12-V thresholds, setting current limit and fast overcurrent trip section.
SUM12	5	I/O	12 V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
SUM3	22	I/O	3 V summing node. A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches 675 mV, the current limit amplifier acts to prevent the current from further increasing.
VDD3	23	I	3-V charge pump input
VINT	1	I/O	Bypass capacitor connection point for internal supply. This pin connects to the internal 2.35-V rail. A 0.1- $\mu\text{F}$ capacitor must be connected from this pin to ground. <b>Do not connect other external circuitry to this pin except the address programming pins</b> , as required.



TYPICAL CHARACTERISTICS

3-V INPUT CURRENT  
vs  
JUNCTION TEMPERATURE

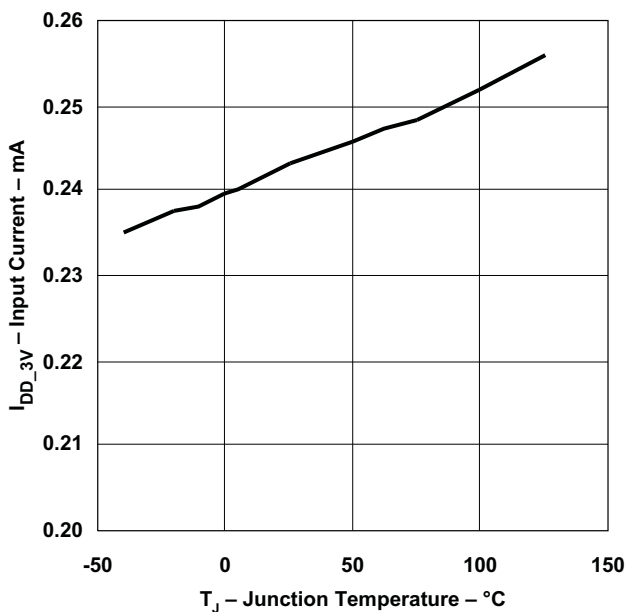


Figure 2.

12-V TURN OFF VOLTAGE THRESHOLD  
vs  
JUNCTION TEMPERATURE

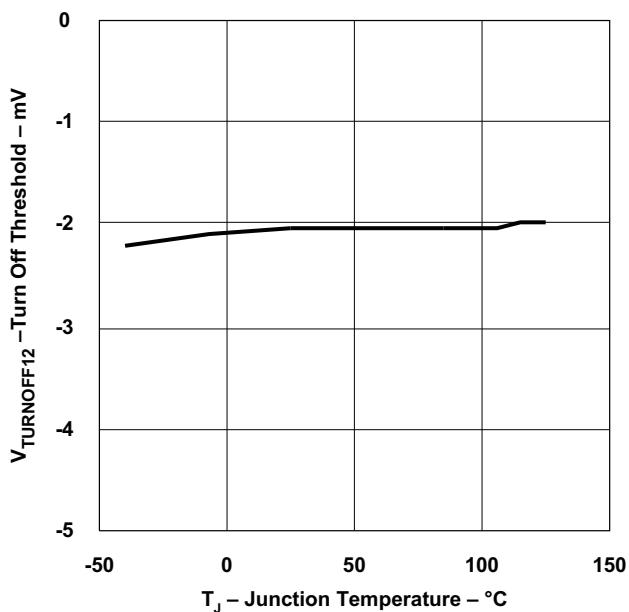


Figure 3.

12-V INPUT CURRENT  
vs  
JUNCTION TEMPERATURE

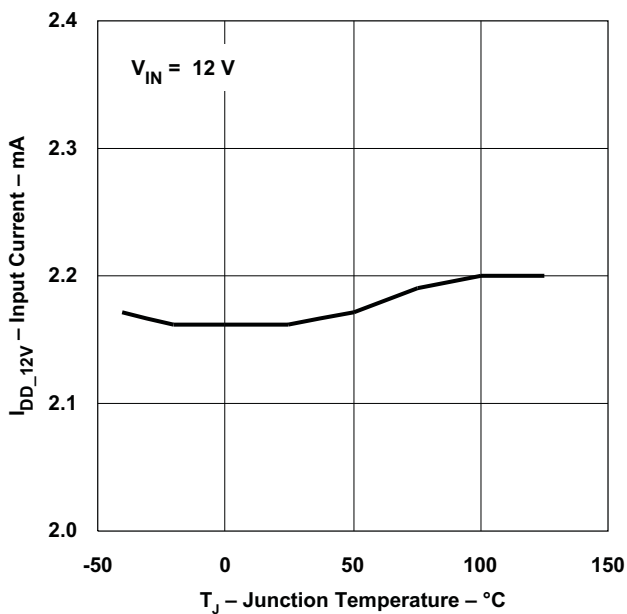


Figure 4.

12-V TURN ON THRESHOLD  
vs  
JUNCTION TEMPERATURE

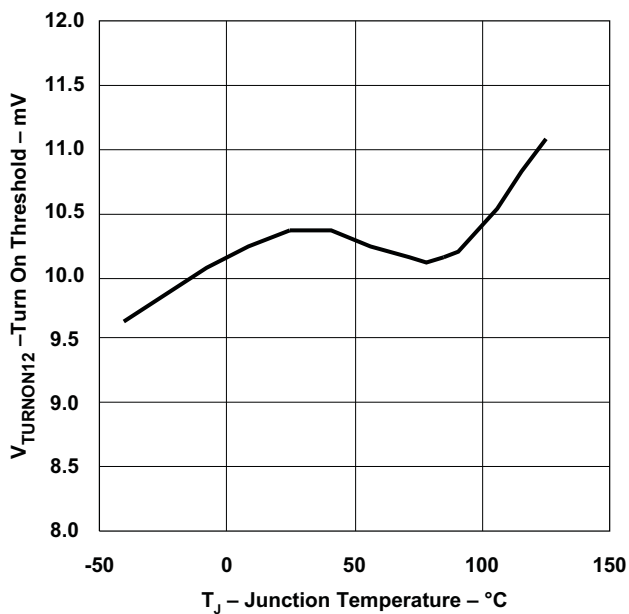


Figure 5.

**TYPICAL CHARACTERISTICS (continued)**

**12-V INPUT CURRENT  
vs  
INPUT VOLTAGE**

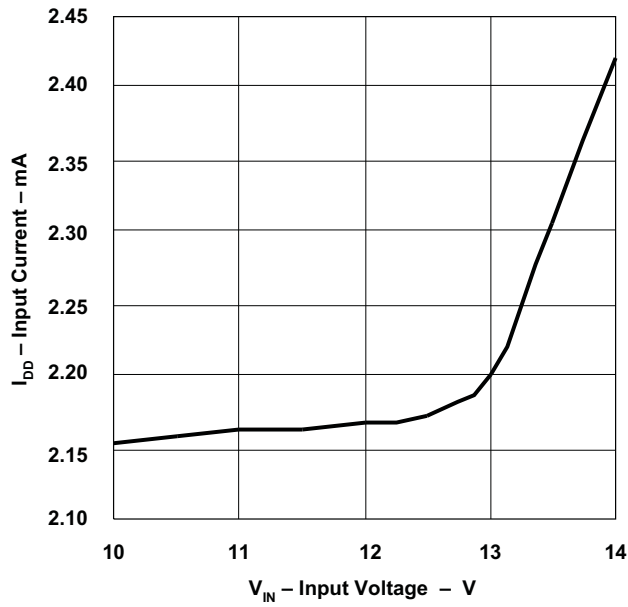


Figure 6.

**12-V CURRENT LIMIT THRESHOLD VOLTAGE  
vs  
JUNCTION TEMPERATURE**

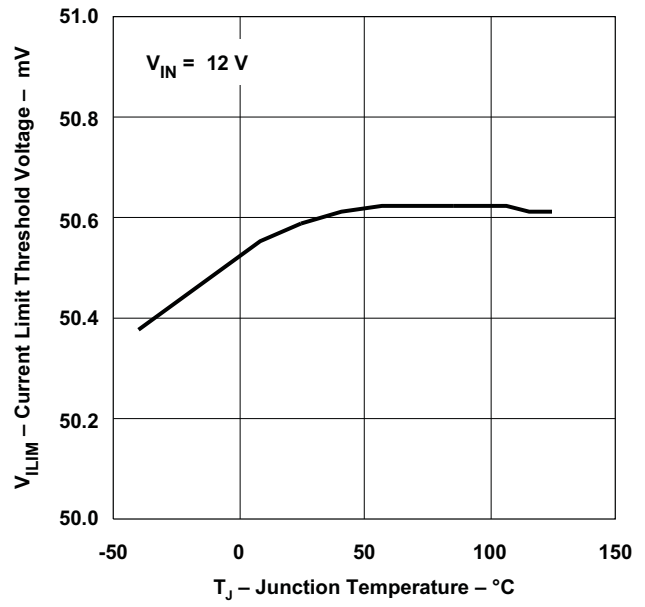


Figure 7.

TYPICAL WAVEFORMS

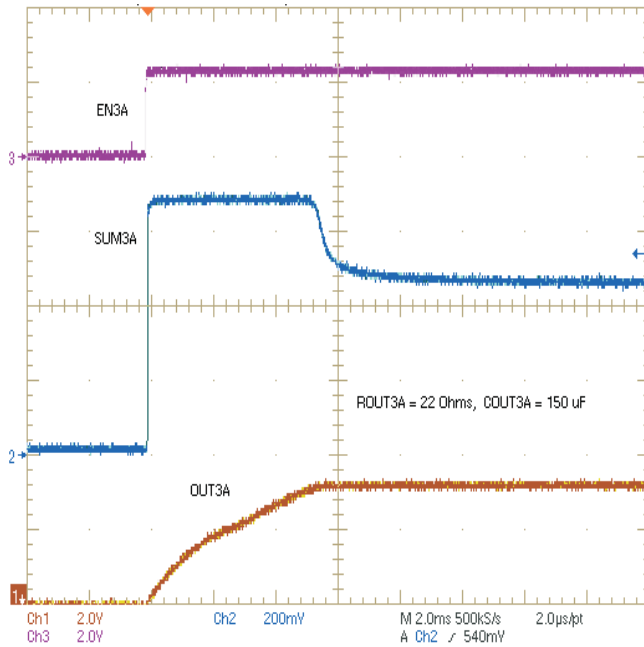


Figure 8. OUT3 Startup Into 22-Ω, (150 mA), 150-μF Load

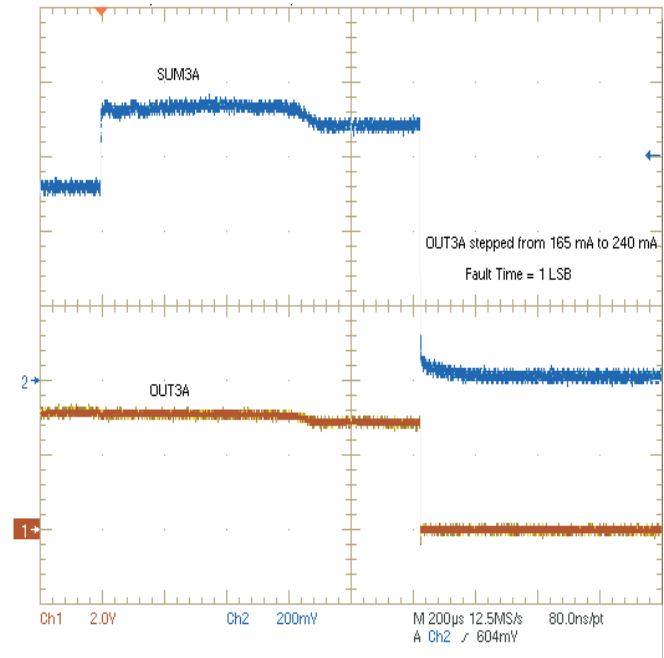


Figure 9. OUT3 Load Stepped from 165 mA to 240 mA

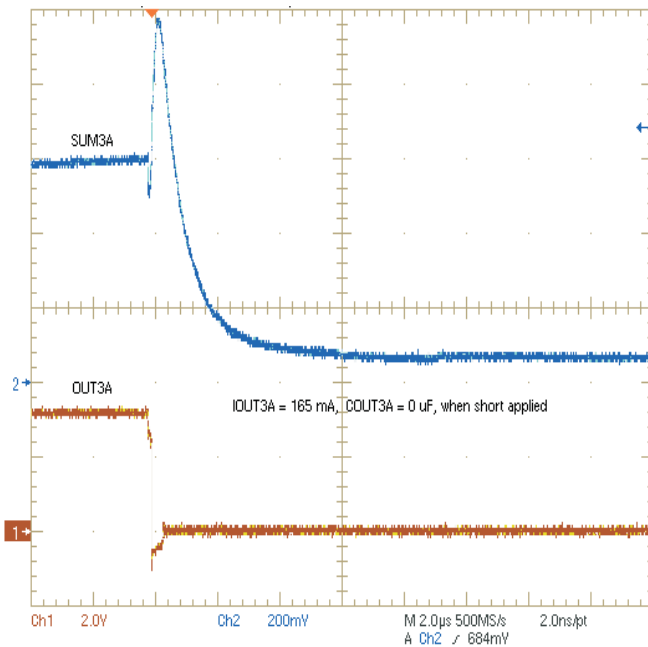


Figure 10. OUT3 Short Circuit Under Full Load, (165 mA), Zoom View

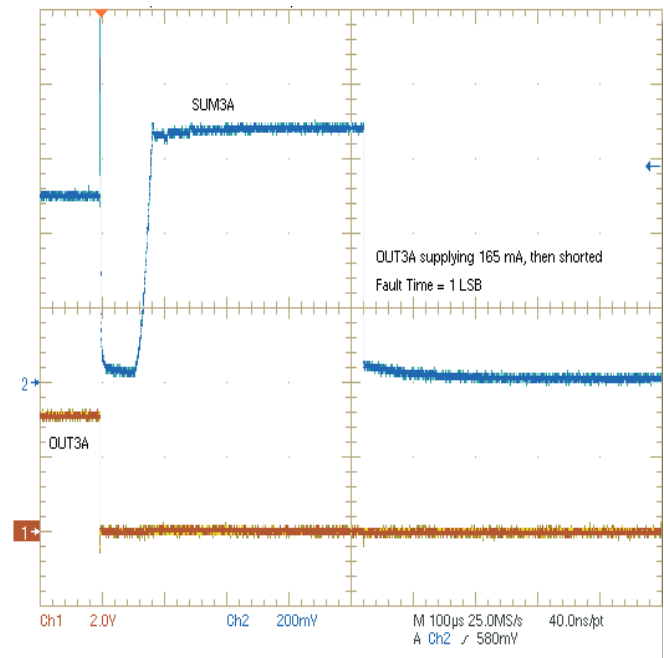


Figure 11. OUT3 Short Circuit Under Full Load, (165 mA), Wide View

TYPICAL WAVEFORMS (continued)

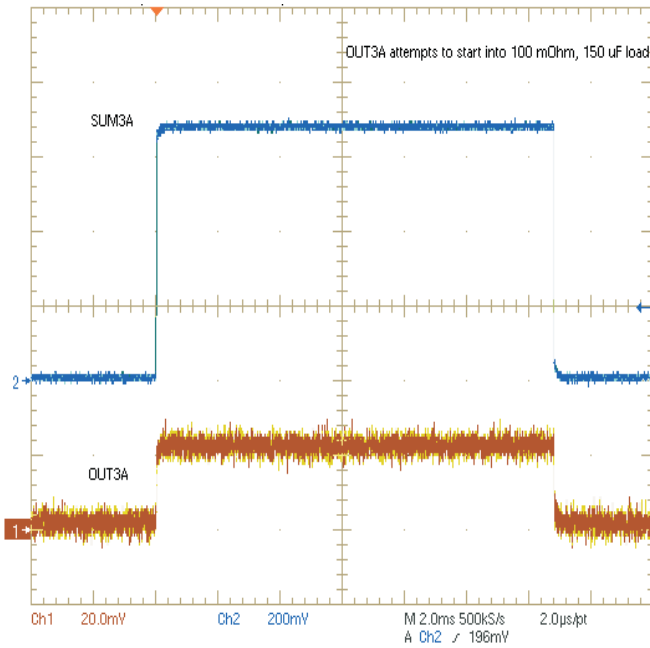


Figure 12. OUT3 Startup Into Short Circuit

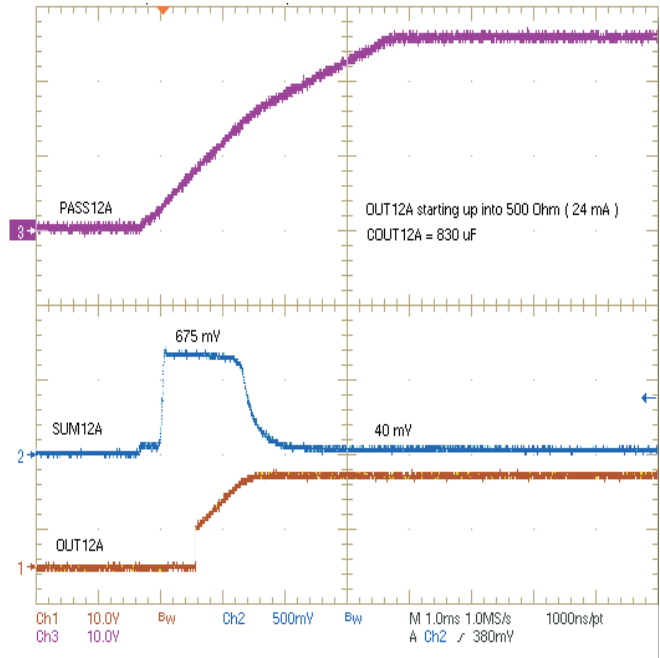


Figure 13. OUT12 Startup Into 500-Ω, 830-μF Load

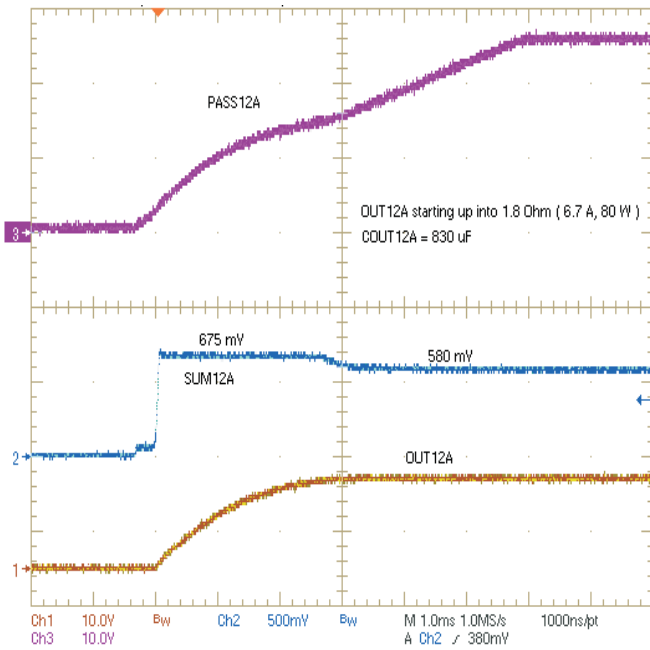


Figure 14. OUT12 Startup Into 80-W, 830-μF Load

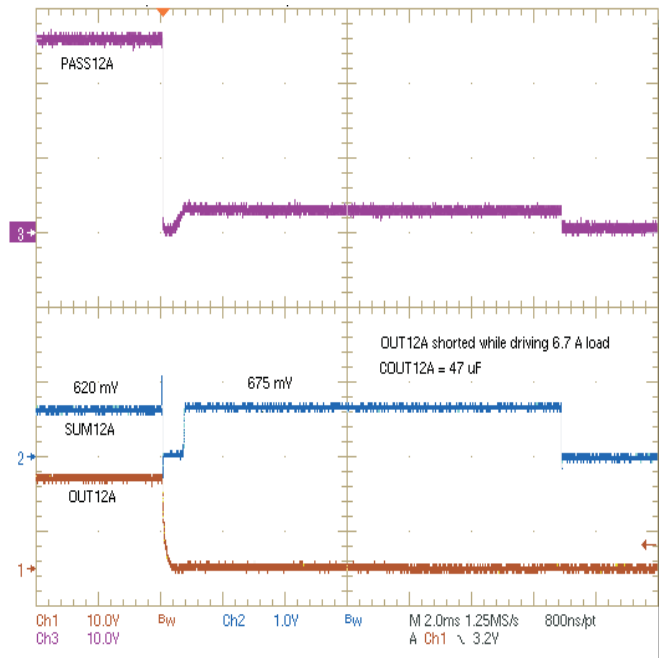


Figure 15. OUT12 Short Circuit Under Full Load, (6.7 A), Wide View

TYPICAL WAVEFORMS (continued)

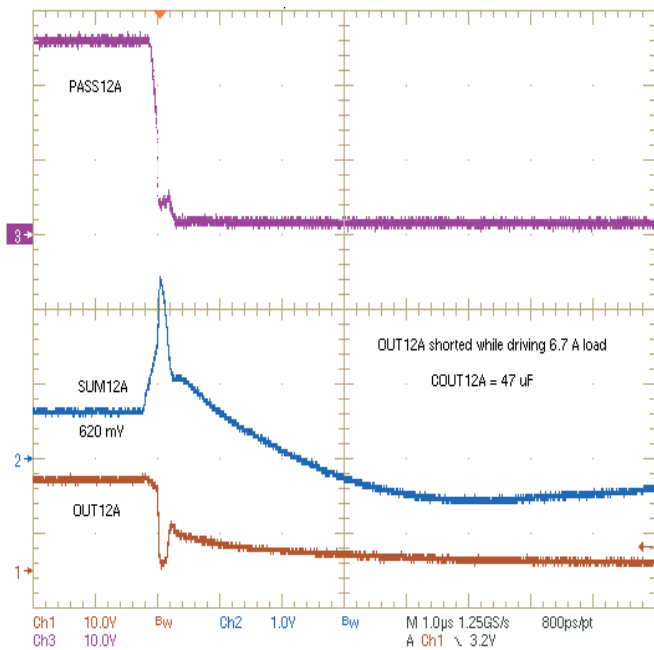


Figure 16. OUT12 Short Circuit Under Full Load, (6.7 A), Zoom View

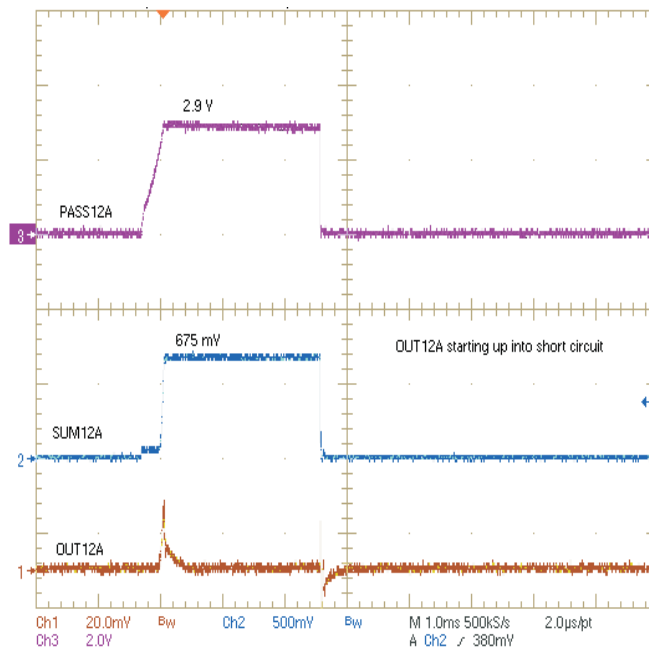


Figure 17. OUT12 Startup Into Short Circuit

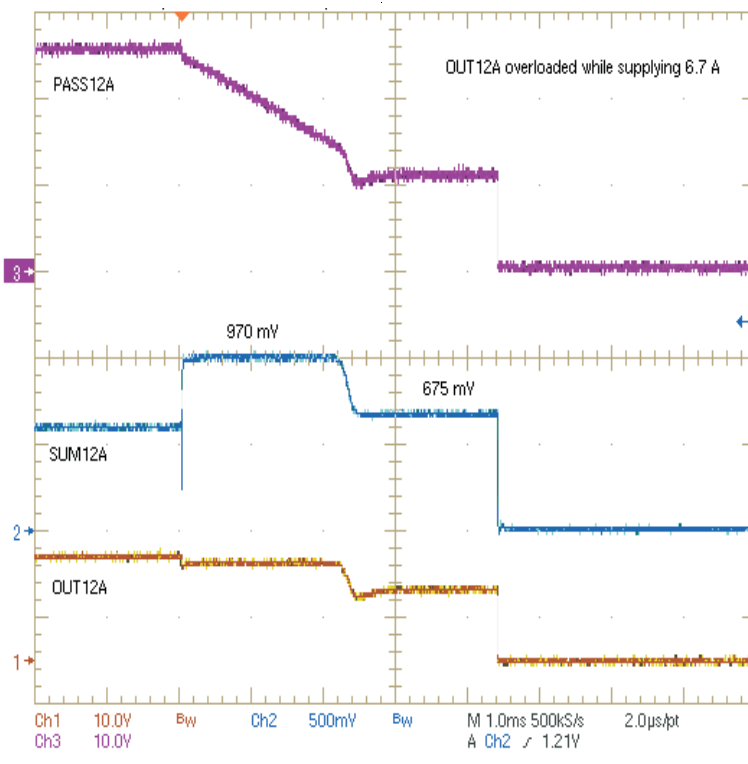


Figure 18. OUT12 Overloaded While Supplying 6.7 A

## APPLICATION INFORMATION

The TPS2458 has been designed to simplify compliance with the PICMG-AMC.R2.0 and PICMG-MTCA.0 specifications. These specifications were developed by the PCI Industrial Computer Manufacturers Group (PICMG). These two specifications are derivations of the PICMG-ATCA (Advanced Telecommunication Computing Architecture) specification originally released in December, 2002.

### PICMG-AMC Highlights

- AMC – Advanced Mezzanine Cards
- Designed to Plug into ATCA Carrier Boards
- AdvancedMC™ Focuses on Low Cost
- 1 to 8 AdvancedMC™ per ATCA Carrier Board
- 3.3-V Management Power – Maximum Current Draw of 150 mA
- 12-V Payload Power – Converted to Required Voltages on AMC
- Maximum 80 W Dissipation per AdvancedMC™
- Hotswap and Current Limiting and must be Present on Carrier Board
- For details, see [www.picmg.org/](http://www.picmg.org/)

### PICMG-MTCA Highlights

- MTCA – MicroTelecommunications Computing Architecture
- Architecture for Using AMCs without an ATCA Carrier Board
- Up to 12 AMCs per System, plus Two MicroTCA Carrier Hub (MCH)s, plus Two Cooling Units (CU)s
- Focuses on Low Cost – Commoditizes the Hardware
- All Functions of ATCA Carrier Board must be Provided
- MicroTCA is also known as MTCA, mTCA,  $\mu$ TCA or uTCA
- For details, see [www.picmg.org/](http://www.picmg.org/)

## Introduction

The TPS2458 has a 12-V power path and a 3.3-V power path. The TPS2458 is in a 32-pin QFN package. The following sections describe the main functions of the TPS2458 and provide guidance for designing systems using this device.

## Control Logic and Power-On Reset

The TPS2458 circuitry draws power from an internal bus fed by a preregulator. A capacitor attached to the VINT pin provides decoupling and output filtering for this preregulator. It can draw power from either of two inputs (IN12 or IN3) or from either of the two outputs (OUT12 or OUT3). This feature allows the internal circuitry to function regardless of which channels receive power, or from what source. The two external FET drive pins (PASS, and BLK) are held low during startup to ensure that the 12-V channel remains off. The internal 3.3-V channel is also held off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset circuit initializes the TPS2458.

## Enable Functions

The TPS2458 provides three external enable pins for the AdvancedMC™ slot. Pulling the  $\overline{\text{EN3}}$  low turns on the 3-V channel. Pulling the  $\overline{\text{EN12}}$  pin low turns on the 12-V channel. If the  $\overline{\text{EN12}}$  pin goes high, the TPS2458 pulls the PASS and BLK pins to ground. Pulling the  $\overline{\text{OREN}}$  pin low turns on the reverse blocking logic in the 12-V channel. If the OREN pin goes high, then the BLK pin remains low. Each of the three enable pins has an internal 200-k $\Omega$  pull-up resistor to VINT.

## Power Good ( $\overline{\text{PG}}$ ) Outputs

The TPS2458 provides two active-low open-drain outputs that reflect the status of the two output voltage rails. The power good output for each channel pulls low whenever the voltage on its OUT pin exceeds the PG threshold. The 3.3-V channel has a nominal threshold of 2.85 V and the 12-V channel has a nominal threshold of 10.5 V.

## Fault ( $\overline{\text{FLT}}$ ) Outputs

The TPS2458 provides two active-low open-drain fault outputs, one for each channel. A fault output pulls low when the channel has remained in current limit long enough to run out the fault timer. A channel experiencing a fault condition automatically shuts down. To clear the fault and re-enable the channel, turn the channel off and back on using the appropriate  $\overline{\text{ENx}}$  pin.

## Current Limit and Fast Trip Thresholds

Both channels monitor current by sensing the voltage across a resistor. The 3.3-V channel uses an internal sense resistor with a nominal value of 290 m $\Omega$ . The 12-V channel uses an external sense resistor that typically lies in the range of 4 m $\Omega$  to 10 m $\Omega$ . Each channel features two distinct thresholds: a current limit threshold and a fast trip threshold.

The current limit threshold sets the regulation point of a feedback loop. If the current flowing through the channel exceeds the current limit threshold, then this feedback loop reduces the gate-to-source voltage imposed on the pass FET. This causes the current flowing through the channel to settle to the value determined by the current limit threshold. For example, when a module first powers up, it draws an inrush current to charge its load capacitance. The current limit feedback loop ensures that this inrush current does not exceed the current limit threshold.

The current limit feedback loop has a finite response time. Serious faults such as shorted loads require a faster response in order to prevent damage to the pass FETs or voltage sags on the supply rails. A comparator monitors the current flowing through the sense resistor, and if it ever exceeds the fast trip threshold it immediately shuts off the channel. Then it will immediately attempt a normal turn on which allows the current limit feedback loop time to respond. The fast trip threshold is normally set 2 to 5 times higher than the current limit.

### 3.3-V Current Limiting

The 3.3-V management power channel includes an internal pass FET and current sense resistor. The on-resistance of the management channel — including pass FET, sense resistor, metallization resistance, and bond wires — typically equals 290 mΩ and never exceeds 500 mΩ. The AdvancedMC™ specification allows a total of 1 Ω between the power source and the load. The TPS2458 never consumes more than half of this budget.

### 3.3-V Fast Trip Function

The 3.3-V fast trip function protects the channel against short-circuit events. If the current through the channel exceeds a nominal value of 300 mA, then the TPS2458 immediately disables the internal pass transistor and then allows it to slowly turn back on into current limiting.

### 3.3-V Current Limit Function

The 3.3-V current limit function internally limits the current to comply with the AdvancedMC™ and MicroTCA™ specifications. External resistor  $R_{SUM3}$  allows the user to adjust the current limit threshold. The nominal current limit threshold  $I_{LIMIT}$  is shown in [Equation 1](#).

$$I_{LIMIT} = \frac{650\text{ V}}{R_{SUM3}} \quad (1)$$

A 3320-Ω resistor gives a nominal current limit of  $I_{LIMIT} = 195\text{ mA}$  which complies with AdvancedMC™ and MicroTCA™ specifications. This resistance corresponds to an EIA 1% value. Alternatively, a 3.3-kΩ resistor also suffices. Whenever the 3.3-V channel enters current limit, its fault timer begins to operate (see *Fault Timer Programming* section).

### 3.3-V Over-Temperature Shutdown

The 3.3-V over-temperature shutdown trips if the 3.3-V channel remains in current limit so long that the die temperature exceeds approximately 140 °C. When this occurs, the chip turns off until the it cools by approximately 10 °C. This feature prevents a prolonged fault on one 3.3-V channel from disabling the other 3.3-V channel, or disabling the 12-V channel.



## 12-V Fast Trip and Current Limiting

Figure 19 shows a simplified block diagram of the circuitry associated with the fast trip and current limit circuitry in the 12-V channel, which requires an external N-channel pass FET and three external resistors. These resistors allow the user to independently set the fast trip threshold and the current limit threshold, as described below.

### 12-V Fast Trip Function

The 12-V fast trip function is designed to protect the channel against short-circuit events. If the voltage across  $R_{SENSE}$  exceeds a nominal threshold of 100 mV, the device will immediately disable the pass transistor and declare a fault condition. The nominal fast trip threshold is shown in Equation 2.

$$I_{FT} = \frac{100\text{mV}}{R_S} \quad (2)$$

### 12-V Current Limit Function

The 12-V current limit function regulates the PASS pin voltage to prevent the current through the channel from exceeding  $I_{LIMIT}$ . The current limit circuitry includes two amplifiers,  $A_1$  and  $A_2$ , as shown in Figure 19. Amplifier  $A_1$  forces the voltage across external resistor  $R_{SET}$  to equal the voltage across external resistor  $R_{SENSE}$ . The current that flows through  $R_{SET}$  also flows through external resistor  $R_{SUM}$ , generating a voltage on the 12SUM pin is shown in Equation 3.

$$V_{12SUM} = \left( \frac{R_{SENSE} \times R_{SUM}}{R_{SET}} \right) \times I_{SENSE} \quad (3)$$

Amplifier  $A_2$  senses the voltage on the 12SUM pin. As long as this voltage is less than the reference voltage on its positive input (nominally 0.675 V), the amplifier sources current to PASS. When the voltage on the 12SUM pin exceeds the reference voltage, amplifier  $A_2$  begins to sink current from the PASS pin. The gate-to-source voltage of pass FET MPASS drops until the voltages on the two inputs of amplifier  $A_2$  balance. The current flowing through the channel then nominally is shown in Equation 4.

$$I_{LIMIT} = \left( \frac{R_{SET}}{R_{SUM} \times R_{SENSE}} \right) \times 0.675\text{V} \quad (4)$$

The recommended value of  $R_{SUM}$  is 6810  $\Omega$ . This resistor should never equal less than 675  $\Omega$  to prevent excessive currents from flowing through the internal circuitry. Using the recommended values of  $R_{SENSE} = 5\text{ m}\Omega$  and  $R_{SUM} = 6810\text{ }\Omega$  gives Equation 5.

$$I_{LIMIT} = \left( \frac{0.0198\text{ A}}{\Omega} \right) \times R_{SET} \quad (5)$$



### Multiswap Operation in Redundant Systems

The TPS2458 features an additional mode of operation called Multiswap redundancy. This technique does not require a microcontroller, making it simpler and faster than the redundancy schemes described in the MicroTCA™ standard. Multiswap is especially attractive for AdvancedMC™ applications that require redundancy but need not comply with the MicroTCA™ power module standard.

In order to implement Multiswap redundancy, connect the SUM pins of the redundant channels together and tie a single  $R_{SUM}$  resistor from this node to ground. The current limit thresholds now apply to the sum of the currents delivered by the redundant supplies. When implementing Multiswap redundancy on 12-V channels, all of the channels must use the same values of resistors for  $R_{SENSE}$  and  $R_{SET}$ .

Figure 20 compares the redundancy technique advocated by the MicroTCA™ specification with Multiswap redundancy. MicroTCA™ redundancy independently limits the current delivered by each power source. The current drawn by the load cannot exceed the sum of the current limits of the individual power sources. Multiswap redundancy limits the current drawn by the load to a fixed value regardless of the number of operational power sources. Removing or inserting power sources within a Multiswap system does not affect the current limit seen by the load.

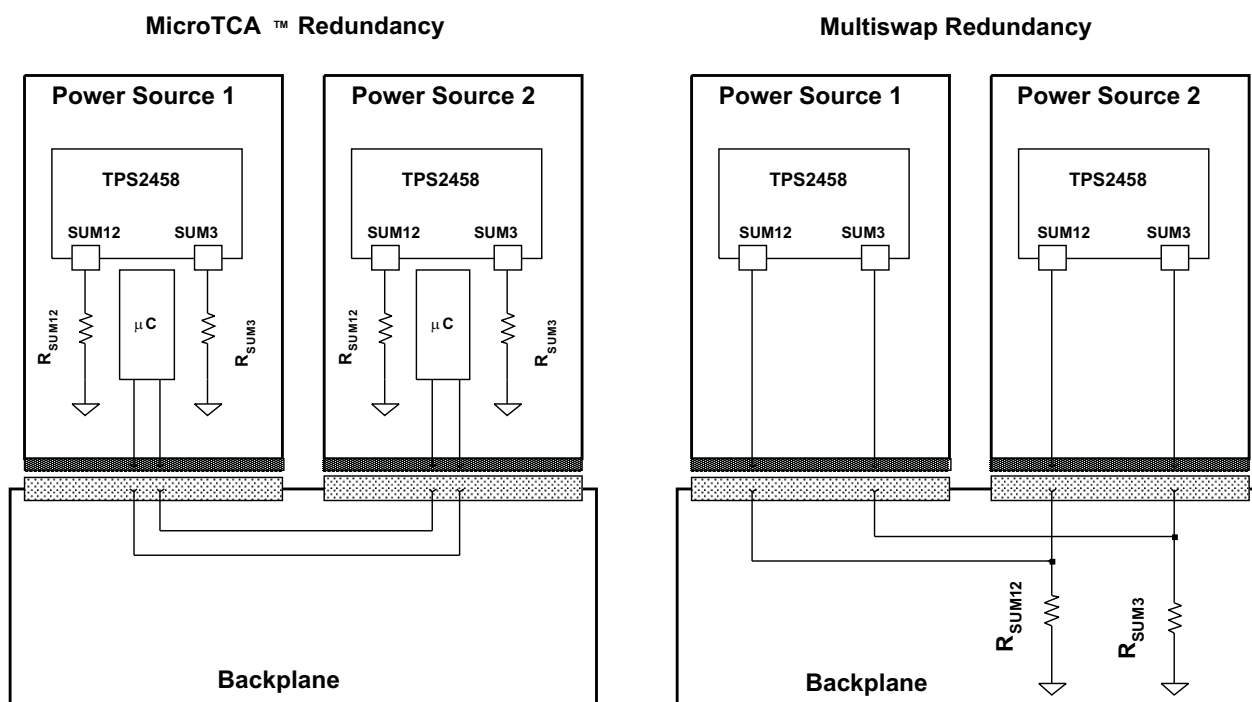


Figure 20. MicroTCA Redundancy vs. Multiswap Redundancy

### 12-V Inrush Slew Rate Control

Although it is possible to slow the gate slew rate it is very unlikely that would be necessary since the TPS2458 limits inrush current at turn on. The limit level is programmed by the user.

As normally configured, the turn-on slew rate of the 12-V channel output voltage  $V_{OUT}$  is shown in Equation 8.

$$\frac{\Delta V_{OUT}}{\Delta t} \cong \frac{I_{SFC}}{C_g} \tag{8}$$

where  $I_{SFC}$  equals the current sourced by the PASS pin (nominally 30  $\mu$ A) and  $C_g$  equals the effective gate capacitance. For purposes of this computation, the effective gate capacitance approximately equals the reverse transfer capacitance,  $C_{rss}$ . To reduce the slew rate, increase  $C_g$  by connecting additional capacitance from PASS to ground. Place a resistor of at least 1000  $\Omega$  in series with the additional capacitance to prevent it from interfering with the fast turn off of the FET.

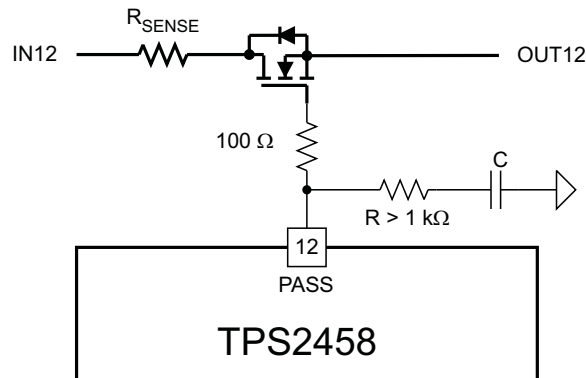


Figure 21. RC Slew Rate Control

### 12-V ORing Operation for Redundant Systems

The 12-V channels use external pass FETs to provide reverse blocking. The TPS2458 pulls the BLK pin high when the input-to-output differential voltage  $V_{IN12}-OUT12$  exceeds a nominal value of 10 mV, and it pulls the pin low when this differential falls below a nominal value of -3 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering (Figure 21).

The source of the blocking FET connects to the source of the pass FET, and the drain of the blocking FET connects to the load. This orients the body diode of the blocking FET such that it conducts forward current and blocks reverse current. The body diode of the blocking FET does not normally conduct current because the FET turns on when the voltage differential across it exceeds 10 mV.

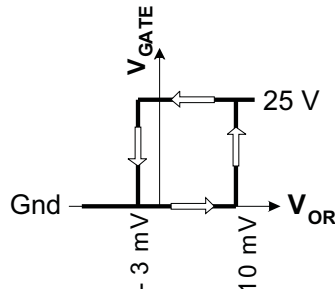
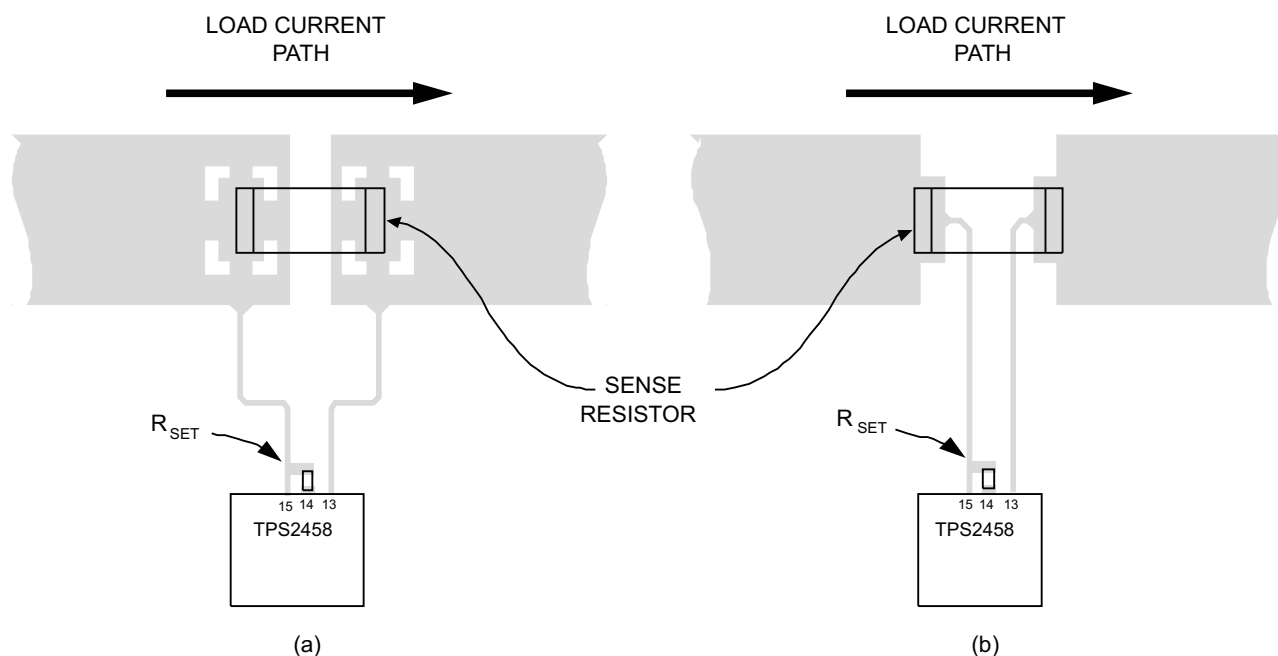


Figure 22. ORing Thresholds

## Layout Considerations

TPS2458 applications require layout attention to ensure proper performance and minimize susceptibility to transients and noise. In general, all runs should be as short as possible but the list below deserves first consideration.

1. Decoupling capacitors on IN12 and IN3 should have minimal length to the pin and to GND.
2. SENM and SENP runs must be short and run side by side to maximize common mode rejection. Kelvin connections should be used at the points of contact with  $R_{SENSE}$ . (Figure 23).
3. SET runs need to be short on both sides of  $R_{SET}$ .
4. These runs should be as short as possible and sized to carry at least 20 A, more if possible.
  - (a) Runs on both side of  $R_{SENSE}$ .
  - (b) Runs from the drains and sources of the external FETs.
5. Runs from the BLK FETs to OUT12 should be as short as possible.
6. Runs connecting to IN3 and OUT3 should be sized for 1 A or more.
7. Connections to GND and SUM pins should be minimized after the runs above have been placed.
8. The device will dissipate low average power so soldering the powerpad to the board is not a requirement. However, doing so will improve thermal performance and reduce susceptibility to noise.



\*ADDITIONAL DETAILS OMITTED FOR CLARITY.

**Figure 23. Recommended  $R_{SENSE}$  Layout**

## Transient Protection

TPS2458 devices in deployed systems are not likely to have long, inductive feeds or long load wires. However, it is always advised that an analysis be performed to determine the need for transient protection. When the TPS2458 interrupts current flow any inductance on the input will tend to cause a positive voltage spike on the input and any inductance on the output will tend to cause a negative voltage spike on the output. The following equations allow the designer to make a reasonably accurate prediction of the voltage spike due to interruptions in current.

$$V_{\text{SPIKE}} = V_{\text{NOM}} + I_{\text{LOAD}} \times \sqrt{L/C}$$

where

- $V_{\text{NOM}}$  is the nominal voltage at terminal being analyzed
- $L$  is the combined inductance of feed to RTN lines.
- $C$  is the capacitance at point of disconnect.
- $I_{\text{LOAD}}$  is the current through terminal at  $T_{\text{DISCONNECT}}$

$$L_{\text{STRAIGHTWIRE}} \cong \left( 0.2 \times \text{length} \times \left( \ln \left( \frac{4 \times \text{length}}{\text{diameter}} \right) - 0.75 \right) \right) \quad (9)$$

This equation can be used to calculate the capacitance required to limit the voltage spike to a desired level above the nominal voltage.

$$C = \frac{L I^2}{(V_{\text{SPIKE}} - V_{\text{NOM}})^2} \quad (10)$$

## REVISION HISTORY

<b>Changes from Revision A (August 2009) to Revision B</b>	<b>Page</b>
• Changed Typical Application Diagram .....	1
• Changed 12-V Channel Circuitry Diagram .....	5
• Changed <a href="#">Figure 19</a> .....	18
• Added <a href="#">Equation 7</a> .....	18
• Changed <a href="#">Figure 21</a> .....	20

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2458RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS2458RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2



TAPE AND REEL BOX DIMENSIONS

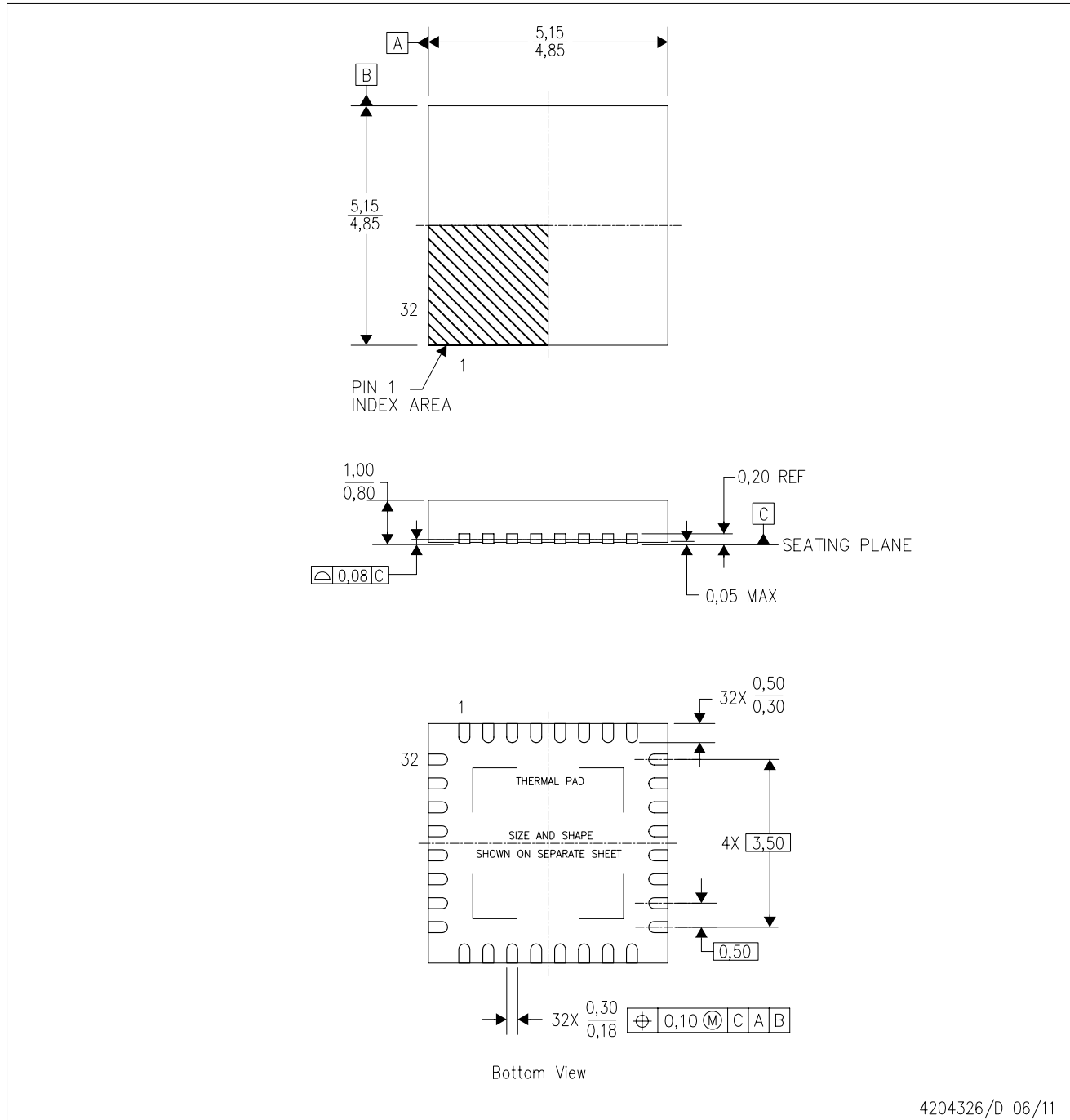


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2458RHBR	QFN	RHB	32	3000	367.0	367.0	35.0
TPS2458RHBT	QFN	RHB	32	250	210.0	185.0	35.0

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RHB (S-PVQFN-N32)

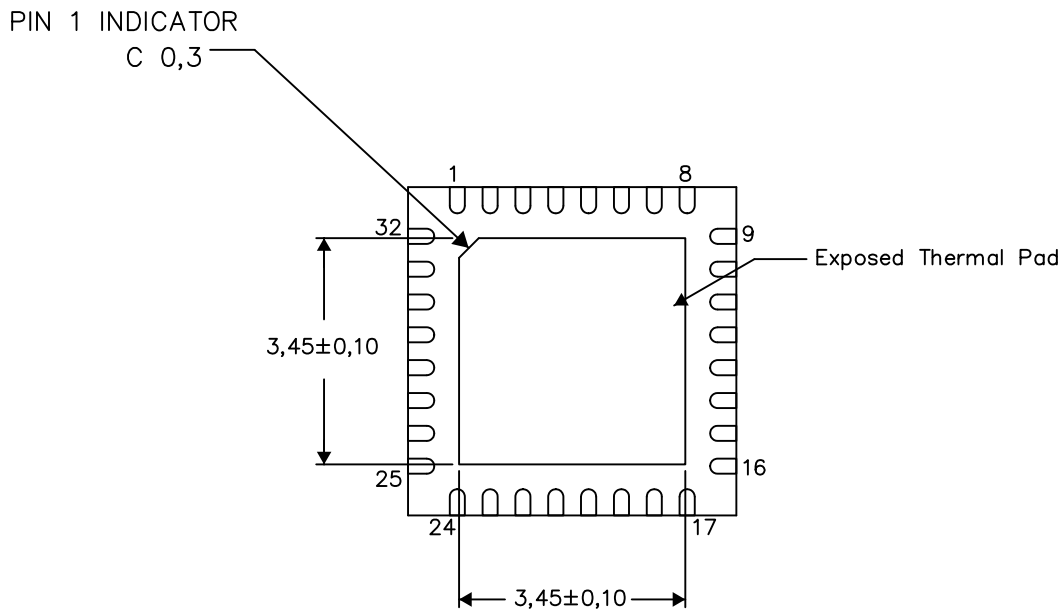
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



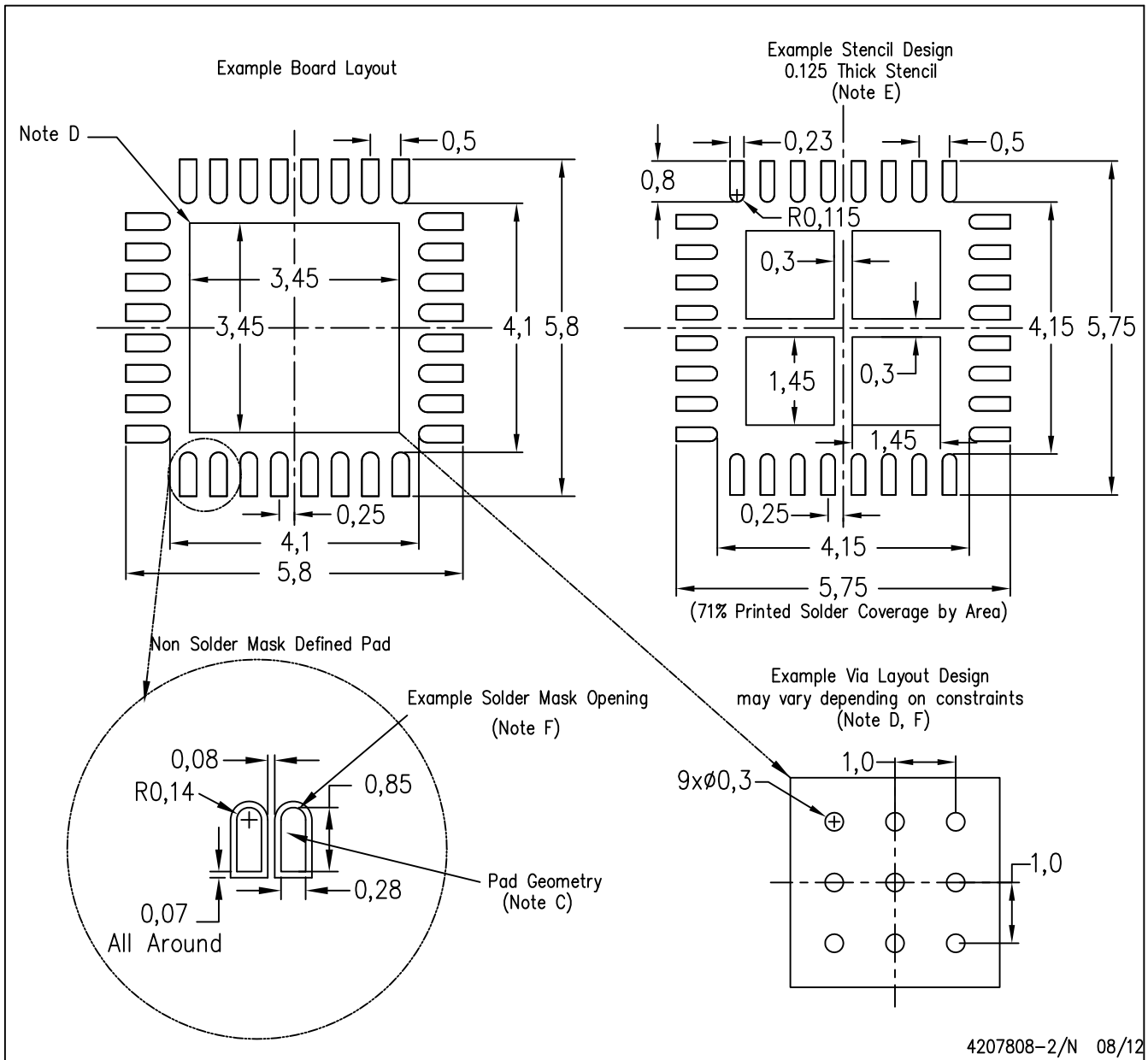
Exposed Thermal Pad Dimensions

4206356-2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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